Simulations for an upgraded Belle II vertex detector

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on behalf of the Belle II Collaboration

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• Presentation of Belle II experiment: why do we consider an upgrade ?

Detailed simulation development: Digitizer

III. Performance results for two new geometries

SuperKEKB collider





- Electron (7 GeV) Positron (4 GeV) collider
- B, charm and τ factory



Today

- Peak luminosity: 2.4.10³⁴ cm⁻² s⁻¹ (WR!)
- Int. luminosity: ~ 90 fb⁻¹ of data collected

Goal

- Peak luminosity: 6.10³⁵ cm⁻² s⁻¹
- Int. luminosity: 50 ab⁻¹

Long shutdown in 2026:

> Opportunity for upgrade of detector





- Average track multiplicity:
 - 11 physics tracks.
- Similar momentum ranges and distributions.
- Low momentum tracks > multiple scattering, curling tracks.



Particle types visible in Tracking Detectors of typical Y(4S) event					
Particle type	Average fraction	alized			
π^{\pm}	72.8%	Vorm			
K^{\pm}	14.9%	2			
e^{\pm}	5.8%				
μ^{\pm}	4.7%				
p^{\pm}	1.8%				





- Sizeable **beam-induced background**.
- Occupancy **dominated** by background

Belle II detector





Challenges addressed by dedicated detectors:

- Central drift chamber CDC
 - Vertex detector VXD:
 - Four double-sided silicon strip detectors SVD
 - Two pixelated vertex detectors PXD

Track finding

Precise vertices measurement

Vertex detector upgrade?



Current occupancy extrapolation at peak luminosity (background hard to extrapolate) close to a limit (above 3-5% occupancy, serious performance degradation) + large uncertainty on background from continuous injection.



• Opportunity to upgrade the vertex detector in 2026:

- Better performances
- Better background handling
- Fully pixelated and fast detector (CMOS technology)

• Goals:

- Use current Belle II software
- Implement new technologies and geometries
- Develop a full simulation
- Show that Belle II can benefit from a fully pixelated vertex detector

CMOS pixel sensors

Requirements for the new detector:

- Same acceptance:
 - Radius: first layer at 1.4 cm last layer at 14 cm
 - Length: from 12 cm to 72 cm
- Reduce occupancy and increase tracking performances:
 - Pitches: 30-40 μm
 - Integration times < 100 ns
 - Material budget: 0.1% to 0.5%
 - Thickness < 50 μm
 - Power dissipation < 200 mW/cm²

- MonoPix-1 / 2: Pitches: 33x33 / 40x36 μm Integration times: 25 ns Thickness: 30 μm
- Match CMOS sensor technology
- MonoPix-1 & 2 good candidates

First task

> Implementation of the hit response in the Belle II software.







Tuning of the digitizer

• When a particle goes through the pixelated layer, it creates charge diffusion inside the depleted width. Those charges are then converted to digits to process them.





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- A few parameters can be adjusted, like the integration time window, the active thickness, the transverse diffusion or the hit threshold.
- Those parameters have been tuned to match a test-beam experiment made at DESY with TJ MonoPix-1 [1] chips, predecessor of TJ MonoPix-2 which is a good candidate for the upgrade.



MonoPix-1 simulation results: clusters





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10



• Three new "VTX" (Vertex) geometries implemented and connected to existing tracking:



Performance





- > Stand-alone figure of merits with background from 2019 predictions
- Occupancy
 - Average VTX layer 1 occupancy: 0.0016%
 > 3 order of magnitude lower than VXD

Tracking efficiency

	Background x 1	Background x 5
Current SVD	0.961	0.907
5 layer	0.984	0.979
7 layer	0.987	0.978

- Better tracking performances at low momentum range
- Very low occupancy in innermost VTX layers
- Robust to the increase of the background



- Opportunity for a VXD upgrade in 2026.
- Digitizer is well tuned to reproduce MonoPix-1 and predicts the MonoPix-2 performances.
- According to MC:
 - Better tracking performances
 - More robust to background
 - Lower occupancy
- Next step: Study the impact of the upgrade on physics channels.

Thank you for your attention

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Background types



Machine background



Luminosity background



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16

Tracking system of Belle II



CDC (Central Drift Chamber)



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17

CMOS pixel sensors



Main features

- Small pixel size possible down to few μm²
- Signal processing on chip → digital output
 - In-pixel amplification → high SNR: "active"
 - No additional FEE readout: "monolithic"
- Sensitive (epi) layer
 - Thin (or thick if bulk)
 - Depleted for fast signal & radiation tolerance
- Operation at room temperature

Industrial technology

- Integrated circuits (chips)
- Lithography feature size < 200 nm
- Reticule limits $\simeq 25x30$ mm2

	Pitch (µm²)	Time resolution (ns)	Sensor thickness (µm)	Comments
DEPFET	50x50	3000	30	Inner layers and disks
Thin strips	50x75	8	140	Outer layers
TSI-180 nm	150x50	25	30	Full volume
TowerJazz 180 nm	30x30	25 - 100	30	Full volume
SOI	35x35	63	75	Full volume





Tuning of the digitizer



When a particle go through the pixelated layer, it creates charge diffusion inside the depleted layer. Those charge are then converted to digits. Based on digitizer of the current Belle II DEPFET layer in the software, Blue parameters are adjustable.

- Check if the particle hit is inside the integration time window T_{int}
- Split the path of the particle in the pixel active thickness E into segments and drift the charges from the center of each segments.
 - The transvers diffusion (coeff. D) follows a gaussian with a width defined as: sigmaDiffus = sqrt (D * e/2)
- Integrate charges per pixel and add the noise to the charge
- Substract hit threshold
 Charge -= chargeThreshold
- Check if Charge still positive
- Amplify and digitize charge
 Charge = Charge / ElectronToToT
- Clipping of the ToT codes
 Charge = Charge % MaxToT
- Store the digit





Conversion factor :

Equation from H. Bichsel, Rev. Mod. Phys. 60 (1988) 663–699, doi:10.1103/RevModPhys.60.663

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 For a normal incidence, we can estimate the conversion factor (c) from the MPV of the cluster charge, which follows :

$$S = \frac{Q(l) - t}{c} = \frac{e (100.6 + 35.35 \ln(e))}{3.6 \times c} - \frac{t}{c}$$
 with $e = 30$ um $t = 500 e^{-1}$

- After a Laudau fit of the cluster charge from the testbeam file, we get $c = 120 e^{-}/ADU$

Diffusion factor :

- For normal incidence, the std deviation of the gaussian diffusion of Q follows :

$$\sigma = \sqrt{\frac{De}{2}}$$

- We get D = 0.6 um

-> Those parameters are then tweaked a bit to try to get the same distributions as Monopix1 testbeam data with D the diffusion factor (CloudSize in the next slide) $\sigma \sim 3um$

Test-beam simulation





VTX Monopix 1 tune

uPitch:	0.004 cm
vPitch :	0.0036 cm
Active Thickness:	0.003 cm

Charge Threshold:	540 e ⁻
Electronic Noise:	20 e ⁻
Electron To ADU:	120
ADC bits:	6 bits
Cloud Size:	8.5e-05 cm

VTX TJ Monopix2:

uPitch:	0.0033 cm
vPitch :	0.0033 cm
Active Thickness:	0.003 cm

Charge Threshold:	150 e ⁻
Electronic Noise:	20 e ⁻
Electron To ADU:	120
ADC bits:	7 bits
Cloud Size:	8.5e-05 cm



DUT pointing resolution $\sigma_u vs \theta$







23





Track definitions

- The reconstructed tracks from pattern recognition (PR) are tagged following the number of hits they share with Monte Carlo tracks (MC)



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Material budget of the VTX





5 layer with discs: angular acceptance







p = 0.300 GeV/c

 Geometry with disk increases acceptance for low momentum tracks at small angles but according to simulations, performances doesn't improve compared to CMOS 5 layers.

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27

5 layer geometry



VTX with 5 pixelated layers

5 layers	1	2	3	4	5
Radius (cm)	1.4	2.2	3.9	8.9	14.0
# ladders	6	10	8	18	26
Sensor type	Α	Α	Α'	A'	Α'
# Sensor rows along z direction	1	1	2	4	6

	Sensor A	Sensor A'	
Width (cm)	2.0	2.0 (*2)	
Height (mm)	0.4	1.0	
Length (cm)	12		
	Sensitive area		
Width (cm)	1.8	1.75 (*2)	
Height (µm)	40	100	
Length (cm)	1	2	
# Pixels U	51	12	
# Pixels V	3584 (256*14)		
Charge Threshold (ENC)	150		
Integration time (ns)	100		







7 layer geometry



VTX with 7 pixelated layers

7 layers	1	2	3	4	5	6	7
Radius (cm)	1.4	2.2	3.5	6.0	9.0	11.5	13.5
# ladders	6	10	14	12	18	22	26
Sensor type	Α	Α	Α	A'	A'	A'	A'
# Sensor rows along z direction	1	1	2	3	4	5	6



	Sensor A	Sensor A'	
Width (cm)	2.0	2.0 (*2)	
Height (mm)	0.4	1.0	
Length (cm)	12		
	Sensiti	ve area	
Width (cm)	1.8	1.75 (*2)	
Height (µm)	40	100	
Length (cm)	1	2	
# Pixels U	51	12	
# Pixels V	3584 (256*14)		
Charge Threshold (ENC)	150		
Integration time (ns)	100		





Standalone performance



• Validation figures for

• CMOS 5 layer

Bkg scale	finding efficiency	fake rate	clone rate
x 1	0.984	0.20	0.022
x 2	0.983	0.42	0.023
x 3	0.982	0.60	0.023
x 5	0.979	0.79	0.023
≥ 10	0.953	0.90	0.018

• CMOS 7 layer

Bkg scale	finding efficiency	fake rate	clone rate
x 1	0.987	0.22	0.034
x 2	0.986	0.44	0.033
x 3	0.985	0.60	0.033
x 5	0.978	0.79	0.034
x 10	0.943	0.90	0.026