The Junction boards and the FADC boards were developed by HEPHY Vienna, and assembled by a company, also in Vienna. They were optically tested at this company, but not electrically, which is why a test system had to be implemented which tests all the on top of the Belle II detector structure. They control the detector, convert the SVD data into digital domain, and perform first data processing using powerful FPGAs. From the FADC boards the data are then sent out to optical converter boards (FTBs) and to the control DAQ system, which further sends the data to servers.

The Silicon Vertex Detector (SVD) of the Belle II experiment at the High Energy Accelerator Research Organization (KEK) in Tsukuba, Japan, consists of 172 double-sided micro strip technology silicon sensors arranged cylindrically in four layers around the interaction point. A total of 1748 readout chips (APV25) process and send the analog signals over 2.5 meter long copper cables to 48 Junction Boards (J Bs) located inside the detector housing which provide an interface for connecting the cables on the inside of the detector with those of the outer world, and to power the detector with radiation-hard and magnetic insensitive DC-DC converters, inside the detector housing (48 LV + 48 HV). From there the analog data are sent over 13 meter long copper cables to 52 A/D Converter boards (FADCs) located in crates on top of the Belle II detector structure. They control the detector, convert the SVD data into digital domain, and perform first data processing using powerful FPGAs. From the FADC boards the data are then sent out to optical converter boards (FTBs) and to the central DAQ system.

The Junction boards and the FADC boards were developed by HEPHY Vienna, and assembled by a company, also in Vienna. They were optically tested at this company, but not electrically, which is why a test system had to be implemented which tests all the components, interconnections and connections on these boards. Including spares there are more than 60 boards each. So this testing had to be designed to be performed at least partially automatically, so that for example some leaning hardware equipment is to be connected to the device under test, a test firmware is flashed onto the board, a button is clicked on the PC, and the test is running. The test procedure is designed to not require much acknowledgment of the detailed internals of the hard- and firmware, so it can be performed also by people who were not involved in the hardware development, by following a well-defined step-by-step instruction manual.

The first tests on all boards are thermal inspection using an infrared camera and power consumption, measured using the internal current monitors of the VME crates. The FADC boards and laboratory power supplies for the junction boards.

For the FADC boards a special test hardware together with firmware for the on-board FPGA and software for the PLC controlling the VME bus has been developed. The “P1” connector and the inner rows of the “P2” connector to the VME bus are tested using VME transfers. The remaining digital pins of the “P2” connector as well as those of the “P3” connector are inter-connected with a special cable, which connects each LVDS input to an LVDS output. Since the amount of outputs does not exactly match the one of the inputs, some test pins on the FADC board are used additionally. The firmware sends 0x1024 packets to one single output at different frequencies up to 40 MHz. Independent counters enumerate the signal changes on all inputs individually at the same time. The results are then read out and interpreted by the software. If the input connected to the active output counted any other number than 1024, or any other output counted anything else but zero, the test has failed, and the faulty line gets reported. The same is then done for all other lines on these two connectors successively, and also for some digital signals of the front connectors like the power-good and enable signals of the DCDC converters on the junction boards. All this digital testing only needs a few seconds per board.

The analog inputs for the detector signals are tested in a different way: The differential input pair of each flash analog digital converter can be switched to one output of two voltage dividers, or to both of them at the same time, using reed relays controlled by I/Os on the FADC board. If any other input counted anything else but zero, the test has failed, and the faulty line gets reported. The same is then done for all other lines on these two connectors successively. The remaining lines on the front connectors are slowly control signal inputs like voltage and temperature monitors. They are simply tested by feeding them with different voltages generated by different voltage dividers also switched by reed relays. They are converted to 24 bit digital data by analog-digital ADCs which the software reads and compares to the nominal values. The I/Os connections are tested using an USB blaster to flash and verify the ECPROMs of the two FPGAs (which additionally is verified by reboots of the procedure), the onboard JTAG Flasher by flashing the Stratix FPGA via the Cyclone FPGA, and the Digital Ethernet by sending and receiving packets to and from a PC.

On these tests some component population errors have been detected, like a few so-called tombstone SMG monitors and capacitors before only one side of the component is soldered properly, one clock distributor IC soldered by 180 degrees, one FPGA with badly soldered BGA connectors, and more. These failures have been successfully repaired, and all boards behaved well afterwards.

The Junction boards and all cables are tested using a commercial cable tester which measures resistances and capacities as well as diode characteristics between any combination of its connectors and so compares the whole board to a stored sample. For the DCDC converters we developed and built a board which measures and displays the voltages. Only a few minor errors have been found, and they have been corrected on-the-fly.

In a second pass each FADC gets connected to a junction board and to a class B LV detector ladder one after the other. The separation of the sensor bias voltage (“HV”) on the FADC boards, the cables and the junction boards are tested using a 200V power supply with current measurement, and all channels of the ladder are read out by the DAQ PC. This procedure (but without the HV power supply) is repeated later for each channel every time before the final detector gets connected to the system.

After all the boards were tested individually twice (once in Vienna, and once at KEK in Japan) using this test procedure, the whole essential system was put together like the assembly in December 2018, in the final detector structure.

In January 2019, Phase 3 operation has started and the SVD system is running stable and reliably.