Switcher and DCD ASIC irradiation studies for the Pixel Detector of the Belle II experiment

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Introduction

It is a fundamental human desire to seek and acquire new knowledge and to describe the world around us. This pursuit began with basic observations of nature, evolved through systematic inquiry and experimentation, and has culminated in the Standard Model (SM) – a remarkably successful framework that describes all currently known fundamental particles and three of the four fundamental forces: the electromagnetic, weak, and strong interactions. The SM has demonstrated its validity by accurately describing a wide range of experimental results and phenomena. Nevertheless, the unification of these forces with gravity remains an unresolved challenge in physics [1].

Due to the significance of the SM, numerous experiments worldwide aim to test its predictions and explore its characteristics. One such characteristics is the violation of CP symmetry in B-meson decays. CP symmetry refers to the combined conservation of charge conjugation (C), which transforms particles into their antiparticles, and parity (P), which inverts spatial coordinates. Within the SM, CP violation is allowed through the presence of a complex phase in the Cabibbo-Kobayashi-Maskawa (CKM) matrix, which governs the mixing and decay of quarks [2].

To validate this phenomenon, the Belle experiment at the KEKB asymmetric-energy e^+e^- collider was designed and successfully confirmed CP violation in a B-meson decay in 2001 [2, 3]. This achievement was recognized with the awarding of the Nobel Prize in Physics to Cabibbo, Kobayashi, and Maskawa in 2008 for their theoretical prediction of the mechanism behind CP violation [4].

After operating KEKB for 11 years, from 1999 to 2010, and reaching all of its technical milestones, an upgrade was undertaken to enable further studies. The new SuperKEKB collider offers a 40-fold increase in luminosity compared to its predecessor [5]. With this increased luminosity, a much larger data sample will be available, unlocking new possibilities for measurements in heavy flavour particle physics. These studies are expected to become a crucial and unique resource for investigating new physics processes, providing complementary insights to the discoveries anticipated at future hadron colliders. To address the significantly increased background levels in this more challenging environment, the Belle detector was upgraded to Belle II. The new design largely follows the architecture of Belle with the addition of a PiXel Detector (PXD) as the innermost layer. Belle II is a multi-layer cylindrical detector system surrounding the SuperKEKB interaction point [6].

The pixel matrix of the PXD is based on DEpleted P-channel Field Effect Transistor (DEPFET) technology and is read out and controlled by three types of Application-Specific Integrated Circuit (ASIC). As the innermost subdetector of Belle II, the PXD is exposed to elevated radiation doses. During operation, an

increase in dark-current noise was observed due to the accumulation of ionizing radiation. This leads to a degradation of the signal-to-noise ratio and therefore the performance of the PXD. The hypothesis arose that this noise increase might originate from irradiation damage in the readout and control ASICs.

Due to the lack of dedicated studies in this field, irradiation campaigns were conducted within the scope of this thesis to investigate the ASICs as a possible source of the observed noise increase. For this purpose, the Drain Current Digitizer (DCD) and the Switcher were individually irradiated using an X-ray tube. The DCD reads the pixel matrix and converts the drain currents into digital values, while the Switcher controls the voltages required for the readout of the DEPFET pixel matrix.

Chapter 1 introduces the SuperKEKB accelerator and provides an overview of the Belle II detector system. Chapter 2 describes the Pixel Detector in detail, including a basic introduction to the DEPFET working principle and a discussion of the irradiation induced noise increase that motivated this thesis. The experimental setup for the irradiation of the ASICs is presented in chapter 3. Chapter 4 elaborates on the conducted measurements and their results. Finally, chapter 5 presents the conclusion.

CHAPTER 1

SuperKEKB and the Belle II Experiment

To explore the processes described by the Standard Model, particle colliders must provide sufficiently high energies to access heavy particles or extremely high luminosities to accumulate the large statistics required for the study of rare phenomena. KEKB, and in particular its upgrade SuperKEKB, belong to the latter category: they operate at a moderate center-of-mass energy of 10.58 GeV at the $\Upsilon(4S)$ resonance, but achieve unprecedented luminosities that enable precision studies of rare processes [5].

The essential counterpart to these accelerators are experiments like Belle II, constructed around the interaction regions, where high energy collisions produce particles that are analyzed. The experiment relies on a series of specialized detectors, each designed to measure specific properties of the particles, enabling detailed investigations of fundamental interactions and processes [2].

1.1 SuperKEKB

SuperKEKB, illustrated in Figure 1.1, is a high-luminosity double-ring e^+e^- collider. It was designed to achieve a 40-fold increase in luminosity compared to its predecessor. This dramatic increase in luminosity is essential for investigating rare processes, such as time-dependent CP violation in B-meson decays. For instance, precise measurements of the CP violating phase $\sin 2\phi_1$ in $b \to c\bar{c}s$ transitions require a large data sample to reduce statistical uncertainties and probe for possible deviations from the Standard Model [5, 7].

The collider operates with asymmetric beam energies, 7 GeV for electrons and 4 GeV for positrons, resulting in a center-of-mass energy of 10.58 GeV that corresponds to the $\Upsilon(4S)$ resonance. This quarkonium state of a bottom quark and an anti-bottom quark decays with a branching fraction of more than 96% into a $B\overline{B}$ pair [8], making SuperKEKB an efficient B-factory. The beam-energy asymmetry provides a Lorentz boost to the B-meson system, which is essential since B-mesons are short-lived and decay close to the interaction region. The boost enables separation of the decay vertices, precise reconstruction of individual events, and the measurement of the decay time difference in a $B\overline{B}$ pair, which is crucial for studies of time-dependent CP violation [9, 10]. SuperKEKB achieves its unprecedented

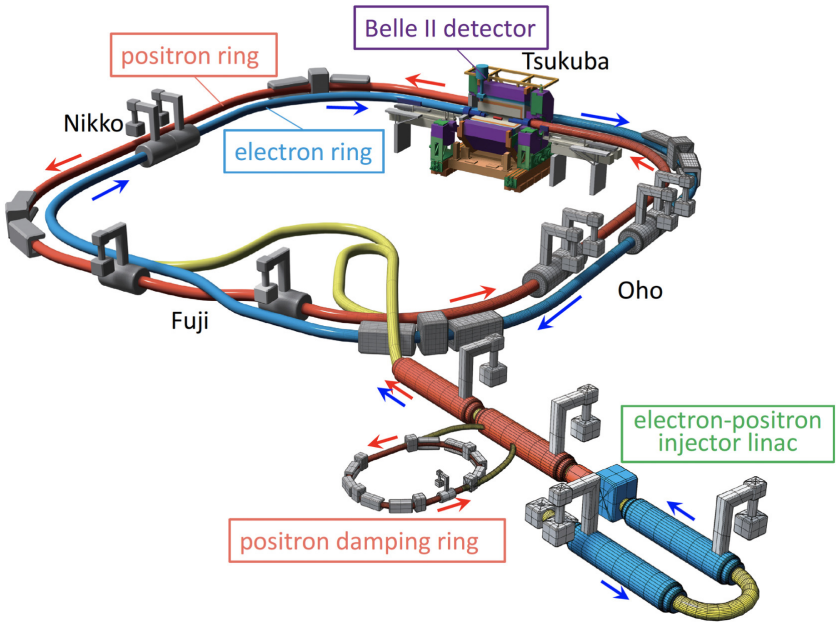


Figure 1.1: Schematic overview of the SuperKEKB accelerator complex, including the Low Energy Ring (LER) for positrons, the High Energy Ring (HER) for electrons, the electron-positron injector linac, and the Belle II detector located at the Tsukuba interaction region. The two storage rings have a circumference of approximately 3 km each [5].

luminosity of $8 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ through two key upgrades: the implementation of the *nano-beam* collision scheme, which reduces the beam sizes at the Interaction Point (IP), and the increase of beam currents to enhance collision rates [5, 11].

1.2 Belle II Experiment

The Belle II experiment is located at the interaction region of the SuperKEKB accelerator and is designed to study the particles produced in e^+e^- collisions with high precision. The multi-layer detector system, illustrated in Figure 1.2, is arranged cylindrically around the IP and consists of several subsystems, each optimized to measure specific properties of the particles. These include tracking trajectories, measuring momenta, reconstructing decay vertices, and identifying particle types.

In the following, the individual subdetectors of Belle II are introduced in sequence, starting from the outermost layers and proceeding inward toward the IP.

The **K_L and μ Detector (KLM)** detector is the outermost subdetector of Belle II, consisting of a barrel section and two endcaps. It is composed of alternating layers of active sensor elements and iron plates. In the barrel region, the sensor layers primarily consist of resistive plate chambers. The innermost two layers of the barrel area and the endcap layers are made of polystyrene scintillator strips with wavelength-shifting fibers. These fibers are read out by silicon photomultipliers. The iron plates serve as return yoke for the solenoid's magnetic field.

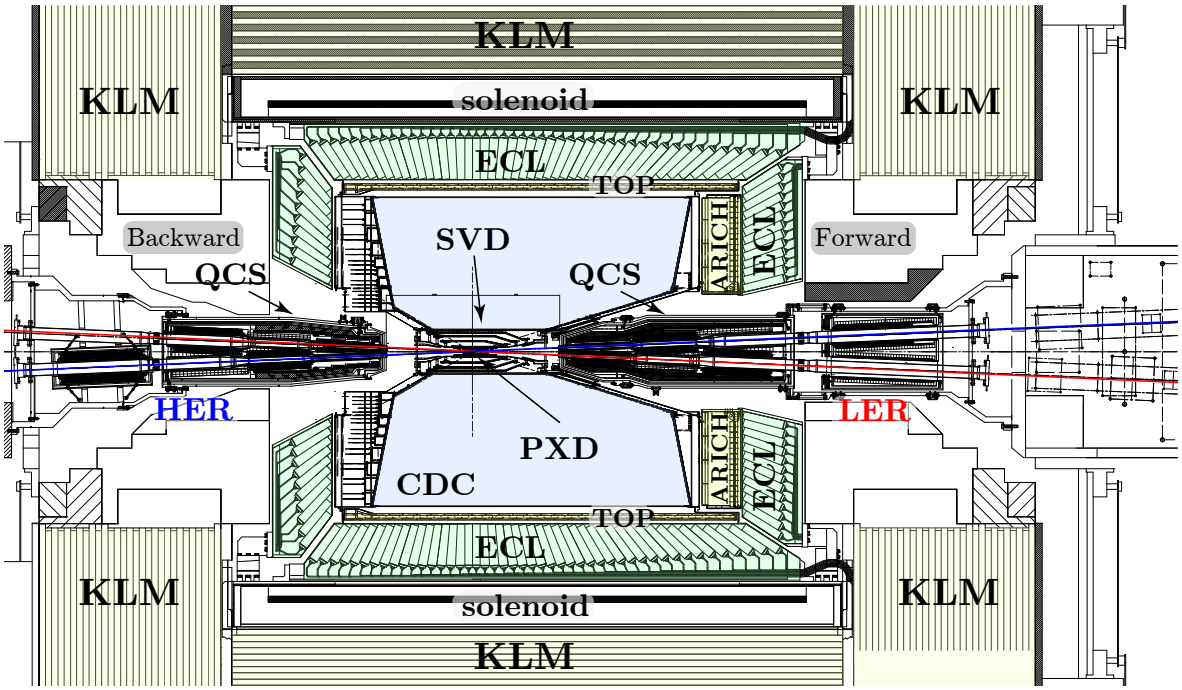


Figure 1.2: Schematic cross section of the Interaction region with the surrounding Belle II detector, showing all major subdetectors from the outermost K_L and μ Detector (KLM) to the innermost VerteX Detector (VXD). Additionally the particle beams (HER: electrons, LER: positrons) and final focus quadruple magnet system (QCS) are indicated [12].

Long-lived neutral kaons traverse the inner subdetectors undetected but cascade into hadronic showers within the iron plates. Muons are identified by correlating KLM hits with tracks reconstructed in the Central Drift Chamber (CDC) [13].

Under the KLM layer is a superconducting **solenoid** that generates a magnetic field of 1.5 T. This field bends the trajectories of charged particles, allowing their momenta to be determined.

Below the solenoid sits the **Electromagnetic Calorimeter (ECL)**, composed of a barrel section and two endcaps. It consists of 8736 thallium-doped cesium iodide (CsI(Tl)) scintillation crystals, pointing towards the IP. The main task of the ECL is the precise energy and position measurement of photons and the identification of particles. Additionally, it is used for luminosity measurement and is part of the triggering system.

In front of the ECL forward endcap sits the newly developed **Aerogel Ring Imaging Cherenkov Detector (ARICH)** detector. It is one of the two subdetectors that make up the particle identification system. It separates kaons from pions up to a momentum of 4 GeV/s and can discriminate pions, muons and electrons below 1 GeV/s.

The second part of the particle identification system is the **Time-of-Propagation (TOP)** detector, located in the barrel region. It consists of long silica bars in which charged particles emit Cherenkov photons.

These photons reflect internally and are detected by micro-channel plate photomultiplier tubes (MCP-PMTs), which provide coarse spatial information (in x and y direction) and precise timing. From this, the time-of-flight and Cherenkov angle are reconstructed, allowing pion-kaon separation [14].

The **Central Drift Chamber (CDC)** is located just inside the particle identification system (ARICH/TOP). It provides spatial and momentum information for charged particles and serves as input to the track trigger. The CDC is a gas-filled chamber (helium-methane mixture) containing 42,240 aluminum field wires and 14,336 gold-plated tungsten sense wires arranged in nine super-layers, each composed of multiple sublayers. These super-layers alternate between axial orientation (wires parallel to the beam pipe) and stereo orientation (wires tilted at a small angle), enabling 3D track reconstruction. A high voltage difference between field and sense wires creates a drift potential. Charged particles ionize the gas and the resulting electron avalanches, proportional to the energy loss, are detected by the sense wires. Combined with the curvature in the magnetic field, this allows reconstruction of the particle's trajectory, momentum, and energy loss. Taking drift times into account, the CDC achieves a spatial resolution of about 120 µm.

The innermost subdetector, the **VerteX Detector (VXD)**, is designed to track ionizing particles close to the interaction region with high spatial resolution, allowing precise reconstruction of the points where these particles originated. The point where a particle is produced or decays into other particles is referred to as its vertex. The VXD consists of two subsystems: the **PiXel Detector (PXD)** at its core, surrounded by the **Silicon Vertex Detector (SVD)**. The SVD is composed of four layers of double-sided silicon strip detector modules. Each module features an n-type silicon bulk with orthogonally oriented p- and n-type strip implants on opposing sides. As ionizing particles traverse the silicon, they generate electron-hole pairs in the bulk. These charge carriers drift to the nearest p- and n-type strips, and the signals from the perpendicular strip pairs allow for precise determination of the particle crossing points. However, the strip-based system cannot cope with the extremely high particle density closest to the IP. Therefore, the two innermost layers of the VXD are pixelated detectors based on DEpleted P-channel Field Effect Transistor (DEPFET) technology, which provide even finer spatial resolution and can handle much higher particle rates. The PXD system is described in further detail in the next chapter (*The PiXel Detector*). [6]

1.3 Backgrounds at Belle II

The high luminosity of Belle II creates a challenging radiation environment around the IP. Two fundamental beam dynamics effects, betatron and synchrotron oscillations, underlie many of the observed background effects. Six dominant beam-induced background sources are continuously present during standard operation: Touschek scattering, beam – gas interactions, radiative Bhabha scattering, synchrotron radiation, two-photon processes, and injection background [12, 15]. Finally, sudden beam loss events can occur, producing abrupt and localized radiation bursts that pose a serious threat to detector integrity and electronics reliability [16].

Betatron oscillations describe the transverse motion of charged particles around the ideal beam trajectory. These oscillations are governed by the focusing instruments of the accelerator, particularly superconducting quadrupole magnets. If the betatron amplitude becomes too large, particles can hit the beam pipe and be lost.

Synchrotron oscillations correspond to the longitudinal oscillations of charged particles within a bunch. Particles with less energy than the nominal bunch energy are located in the tail of the bunch, while those with higher energy are found at the front. Since the bending radius in the dipole magnets depends on particle energy, these deviations can couple to the transverse betatron oscillations and enhance them, potentially leading to particle losses.

Touschek scattering refers to Coulomb interactions between particles within the same bunch. Such interactions produce energy deviations from the nominal beam energy, causing affected particles to deviate from the stable orbit and be lost along the ring. In the nano-beam scheme, the reduced beam size significantly increases the overall Touschek scattering rate. However, horizontal collimators installed near the interaction region effectively suppress the associated losses inside Belle II.

Beam – gas interactions occur when particles in the beam scatter off residual gas molecules inside the vacuum chamber. These elastic or inelastic interactions cause particle losses along the ring, and the resulting background depends on the beam current and the local vacuum quality.

Radiative Bhabha scattering involves the emission of high-energy photons in electron – positron scattering events $e^+e^- \to e^+e^- + \gamma$. Although these photons typically do not traverse the Belle II detector, they strike beam optics magnets downstream, generating neutrons via photo-nuclear reactions. Some neutrons can scatter back into the detector and increase occupancy, particularly in the KLM. To mitigate this effect, additional neutron shielding is installed. Only a small fraction of the scattered electrons and positrons are lost inside the detector itself.

Two-photon processes $\left(e^+e^- \to e^+e^- + \gamma\gamma \to e^+e^- + e^+e^-\right)$ are especially relevant for the innermost subdetectors. Low-momentum e^+e^- pairs are emitted by the beam particles and spiral along the solenoidal magnetic field lines. If their transverse momentum is sufficient, they can leave multiple hits in the vertex detector, particularly in the PXD, while their impact on outer subdetectors remains minor.

Synchrotron Radiation (SR) is emitted when charged particles are deflected by the final focusing magnets near the IP. The dominant source is the HER electron beam due to its higher energy. A distinction is made between upstream SR, which directly reaches the detector, and downstream SR, which scatters back from beam pipe surfaces via Rayleigh or Compton scattering. To suppress this background, the inner beam pipe is coated with a thin gold layer that absorbs low-energy photons and reduces occupancy in the vertex detector.

Injection background arises during top-up injection of new bunches into the storage rings. Newly injected bunches oscillate horizontally around the stored beam, producing elevated background levels near the IP for several milliseconds after each injection. To prevent readout saturation, trigger vetoes are applied, which introduce dead time and reduce the recorded luminosity.

Sudden beam loss events occur when the stored beam is rapidly lost within a few turns, for reasons that are not yet fully understood. Such events have caused severe damage to Belle II components, quenches of QCS magnets, damage to collimator jaws, and unplanned interruptions to SuperKEKB operation [16].

To suppress backgrounds, SuperKEKB employs a multi-layered mitigation strategy. Movable beam collimators in the LER and HER intercept particles with large transverse deviations before they reach the interaction region, protecting Belle II and the QCS magnets from unexpected beam losses. Horizontal collimators primarily stop Touschek-scattered particles, while vertical collimators target beam – gas

scattered particles. Tungsten shields are installed outside the IP beam pipe and around the QCS to intercept beam particles that escape the collimators and are lost inside the detector. In 2024, dust from degraded vacuum sealing materials in coupling sections was identified as a major contributor to sudden beam losses. Removing these materials significantly reduced such events. [12, 15]

CHAPTER 2

The PiXel Detector

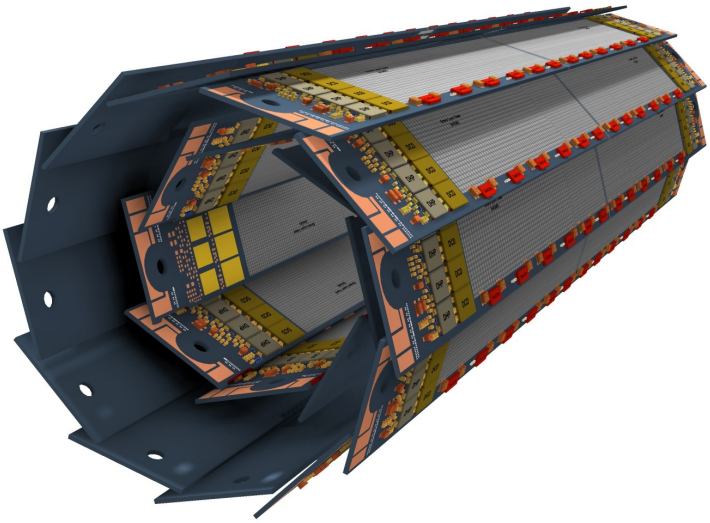


Figure 2.1: Layout of the PXD at Belle II. Two layers with 8 and 12 ladders respectively arranged in a windmill-like pattern at a minimum distance of 7 mm around the interaction point of SuperKEKB. [12]

The luminosity increase at SuperKEKB results in significantly higher particle densities, particularly in the innermost detector layers. This effect is further intensified by the reduced beam pipe diameter, enabled by the nano-beam scheme [5], which allows the first detector layer to be positioned as close as 7 mm from the interaction point. Consequently, a new detector technology, the *PiXel Detector* (PXD), is required, as the *Silicon Vertex Detector* (SVD) alone could not operate reliably under these conditions [6, 9]. The PXD comprises two layers, consisting of 8 and 12 ladders respectively, arranged in a windmill-like pattern to ensure full angular coverage. Each ladder consists of two mirrored modules (forward and backward) glued together back-to-back. The radii were minimized to maximize tracking performance and are positioned at a 7 mm and 11 mm distance from the beam line, as shown in Figure 2.1.

The PXD is based on DEpleted P-channel Field Effect Transistor (DEPFET) technology, chosen for its ability to meet the demanding conditions near the interaction point. Key design goals included high

vertex resolution, high granularity to mitigate pixel occupancy at elevated background levels, and high detection efficiency across the full angular range of $17^\circ < \theta < 150^\circ$. These performance targets had to be achieved while also ensuring sufficient radiation hardness and mechanical stability, as well as a low material budget to reduce multiple scattering and thereby preserve the precision of track reconstruction in the outer detectors. Additionally, low power consumption was critical to avoid the need for bulky cooling infrastructure, while a fast readout system was required to handle high trigger rates and minimize dead time. [6]

2.0.1 PXD modules

Each module, shown in Figure 2.2, contains a DEPFET pixel matrix with 768×250 pixels. The matrix is divided into regions with three different pixel sizes to optimize spatial resolution and coverage: closer to the interaction point a smaller pixel pitch of 50 µm × 55 µm (width × length) is used, while in the outer regions the pixel length increases to 60 µm and 85 µm to accommodate particles incident at shallower angles [12, 17]. Row-control and readout is done by three types of ASICs, as described in section 2.2.

To achieve the required low material budget, the DEPFET matrix is thinned to 75 µm. It is attached to a silicon handle wafer to preserve mechanical stability and simultaneously provides the mounting surface for the control and readout ASICs [18].

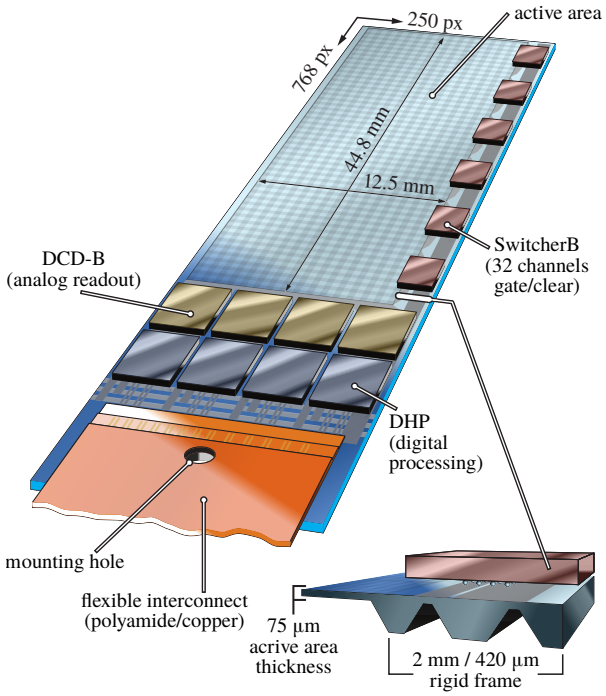


Figure 2.2: The PXD module consists of the DEPFET pixel matrix mounted on a support frame, with control and readout ASICs next to the pixel matrix. Grooves in the support frame minimize the material budget of the detector to reduce multiple scattering [18].

2.1 DEPFET Working Principle

The DEPFET detector technology integrates p-channel Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) into a fully depleted n-doped silicon bulk, which serves as the sensor substrate, as illustrated in Figure 2.3. The bulk is depleted from the backside implant by applying a high voltage via a punch-through mechanism from the front [12]. Beneath the *external gate*, an additional n-doped implant creates a potential minimum for electrons, referred to as the *internal gate*. Thus, electron-hole pairs created by ionizing particles traversing the detector substrate split up. Holes drift to the backside implant, while electrons drift towards the internal gate and are accumulated. The collected charges induce mirror charges in the MOSFET channel and thereby shift the effective gate potential. This modulates the channel conductivity and leads to an increased drain-source current, which constitutes the measurable signal of the DEPFET pixel. Since charge collection and amplification occur in the same device, DEPFET sensors combine a compact design with an intrinsically high signal-to-noise ratio.

The resulting current amplification per collected electron is referred to as the charge gain g_q [19]:

$$g_q = \frac{\partial I_{DS}}{\partial Q_{\text{sig}}} = 750 \frac{\mu\text{A}}{\text{e}^-},$$

where I_{DS} is the source-drain current and Q_{sig} is the signal charge in the internal gate. This gain depends on the MOSFET geometry, specifically the gate length L, gate width W, gate oxide capacitance C_{ox}, hole mobility μ_h, and drain-source current I_{DS} [20]:

$$g_q = \sqrt{\mu_h \frac{1}{L^3 W C_{\text{ox}}} I_{DS}}\,.$$

To remove the collected signal charge and reset the pixel for the next event, an additional strongly n-doped *clear* implant is placed next to the internal gate. When a positive voltage pulse (relative to the source voltage) is applied to the clear implant, electrons in the internal gate drift away into the clear implant. To assist the charge removal, a *clear gate* is located between the internal gate and the clear implant. This clear gate is not directly controlled but is capacitively coupled to the clear implant. To ensure that signal electrons are collected in the internal gate rather than lost to the clear implant, a deep p-well is placed beneath the clear region [12].

2.2 Pixel Layout and Readout Mechanism

For the readout of DEPFET pixels, control and digitizer ASICs are required: the Switchers and the Drain Current Digitizers (DCDs). The Switchers provide multiple channels to supply the gate and clear voltages for controlling the pixel rows, while the DCDs use Analog-to-Digital Converters (ADCs) channels to digitize the drain currents. These ASICs are described in more detail in the next section (Front-end Electronics).

The DEPFET pixel matrix is built from fourfold base units, as illustrated in Figure 2.4(a), with rows oriented vertically and columns horizontally. A double-row pattern is used for the arrangement of pixels,

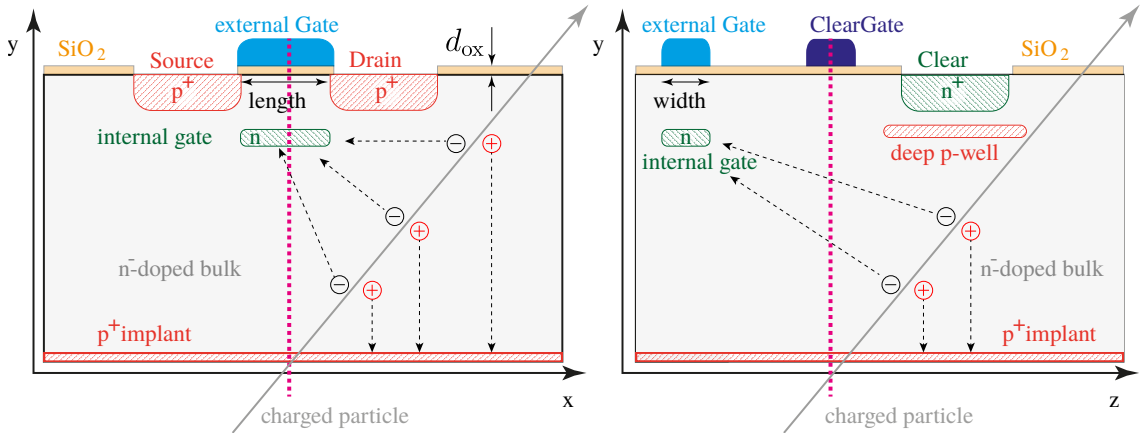


Figure 2.3: Schematic cross-section of a DEPFET pixel from two perspectives. The pink line indicates the *zy*- and *xy*-planes. The pixel integrates a MOSFET with p^+ source and drain implants, and external gate. Additionally, an n-type implant beneath the external gate forms the internal gate, which collects signal electrons. Incident particles generate electron-hole pairs in the bulk. Holes drift to the p^+ backside contact, while electrons accumulate in the internal gate and amplify the source-drain current. A dedicated n^+ clear implant enables removal of accumulated signal electrons, resetting the pixel for the next event. [12]

where every second row is mirrored for a more compact layout. Four pixels share a common gate structure, and two pixels share a common source. Each clear implant is connected to four pixels at once, positioned at the pixel corners and enclosing the internal gate from two sides, which makes the clearing process more reliable. The source implants lie between two adjacent pixels, allowing them to be shared. Clear gates are distributed pairwise across entire rows.

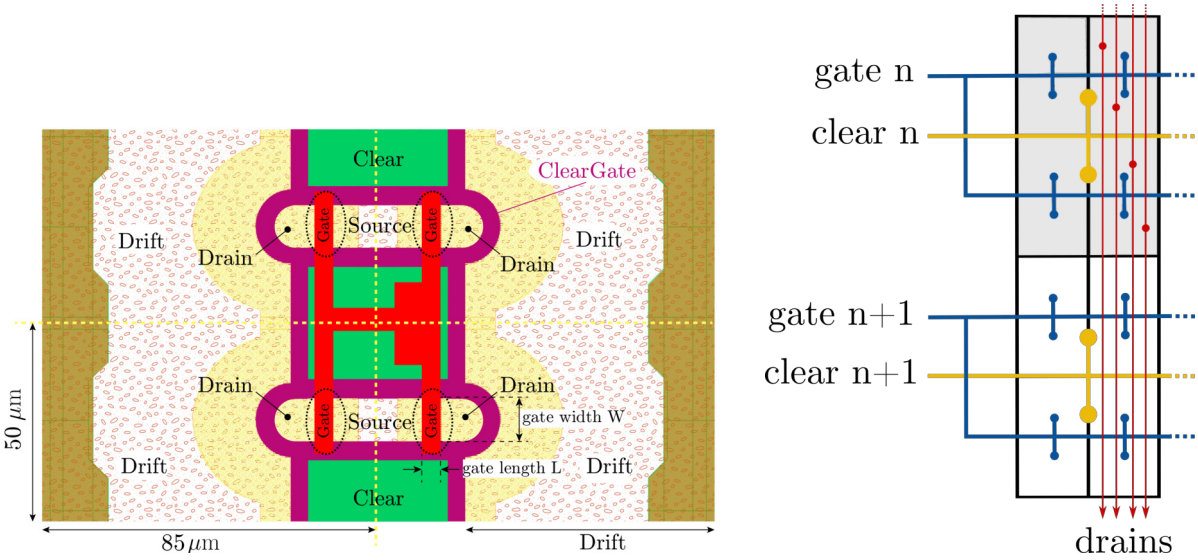
2.2.1 Row-Control

Four pixel rows are controlled together as one unit, forming a row quadruple as illustrated in Figure 2.4. The gate voltage is applied simultaneously to all four pixel rows of such a quadruple, reducing the number of required Switcher channels by a factor of four. Consequently, each pixel column has four separate drain lines, with each line connected to every fourth pixel in a column. Each of these drain lines is digitized by a dedicated DCD channel. The clear implants of two consecutive double-rows are connected to a common clear channel, ensuring simultaneous clearing within the row quadruple.

With this configuration, 192 Switcher gate/clear channel pairs and 1000 ADC channels provided by the DCD are required to control and read out the full matrix of 768×250 pixels.

2.2.2 Readout

The described design is chosen since the PXD operates in rolling shutter mode, where the row quadruples are read out sequentially. Combined with the fourfold readout scheme, this enables a fast readout speed of 50 kHz while keeping the power consumption low, since only 1/192 of the gates are active at once.



(a) Pixel layout of the PXD. The pixels are arranged in a double-row pattern. Four pixels share a common gate, two pixels share a common source, and the clear implants are connected to four pixels at the corners. The dotted yellow lines indicate the pixel boundaries [12].

(b) Row-control and readout scheme. Four pixel rows are controlled together as a row quadruple, and each column has four drain lines, each connected to every fourth row [21].

Figure 2.4: Pixel layout and row-control scheme of the DEPFET pixel matrix.

During each cycle, every row quadruple undergoes three phases, controlled by the gate and clear voltages provided by the Switcher channels [12]:

Integration phase (*gate = off, clear = off*) Lasting about 20 µs, in this phase, signal charge is collected. Electrons generated by traversing ionizing particles drift towards and accumulate in the internal gate.

Sampling phase (*gate = on, clear = off*) The gates of the row quadruple are activated, and the drain currents establish within a few ns. Once saturated, the drain currents are sampled.

Clearing phase (*gate = on, clear = on*) At the end of the sampling phase, the pixels are reset during the clearing phase of about 25 ns. The applied clear voltage removes the collected charge from the internal gate through the clear implant.

The sampling and clearing phases together last about 105 ns and are applied sequentially to all 192 row quadruples. Between these short phases, each row quadruple remains in the integration phase while the others are read out. The resulting drain current for two consecutive row quadruples is shown in Figure 2.5, where the sampling points are marked by red lines.

Pedestal currents The measured drain current is the sum of the signal current induced by the collected charge in the internal gate and the dark current, referred to as the pedestal current or just *pedestals*:

$$I_{\text{drain}} = I_{\text{sig}} + I_{\text{ped}}.$$

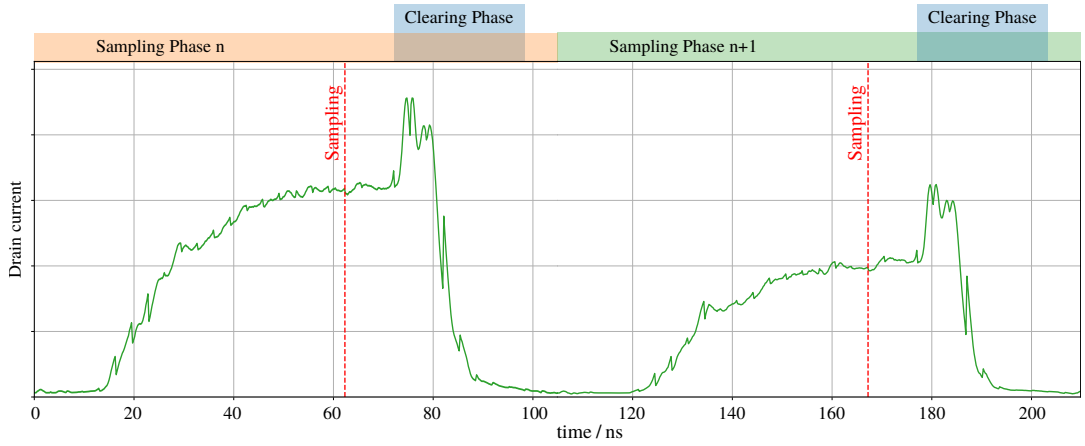


Figure 2.5: Drain current of two consecutive row quadruples during rolling shutter readout. The sampling points are indicated by red lines, while the readout phases are shown as colored blocks at the top.

To extract the true signal, the pedestal current must be subtracted. Many DEPFET systems achieve this by measuring the pedestal current immediately after the clearing phase. In the PXD, however, a *single-sampling* approach is used [18]. Here, pedestal values are determined beforehand by averaging multiple measurements for each pixel. The resulting pedestal map is stored and used during operation to calculate the signal current [12]:

$$I_{\text{sig}} = I_{\text{drain}} - \langle I_{\text{ped}} \rangle .$$

Although this leads to slightly higher noise and more frequent calibrations, it significantly reduces sampling time and enables the fast readout required for the PXD.

2.3 Front-End Electronics (ASICs)

For readout, row-control, and initial data reduction, a set of Application-Specific Integrated Circuit (ASICs) is required. ASICs are integrated circuits designed for a specific application and have a fixed internal structure. Unlike programmable micro controllers, their functionality cannot be modified after fabrication. However, this constraint brings significant advantages. ASICs offer much higher speed at lower power consumption and require less space. These characteristics are crucial for minimizing the material budget in the PXD.

An overview of the ASICs used in the PXD and their functional connections is shown in Figure 2.6, which includes the schematic layout and data/control flow. The working principles of these components are described in the following subsections.

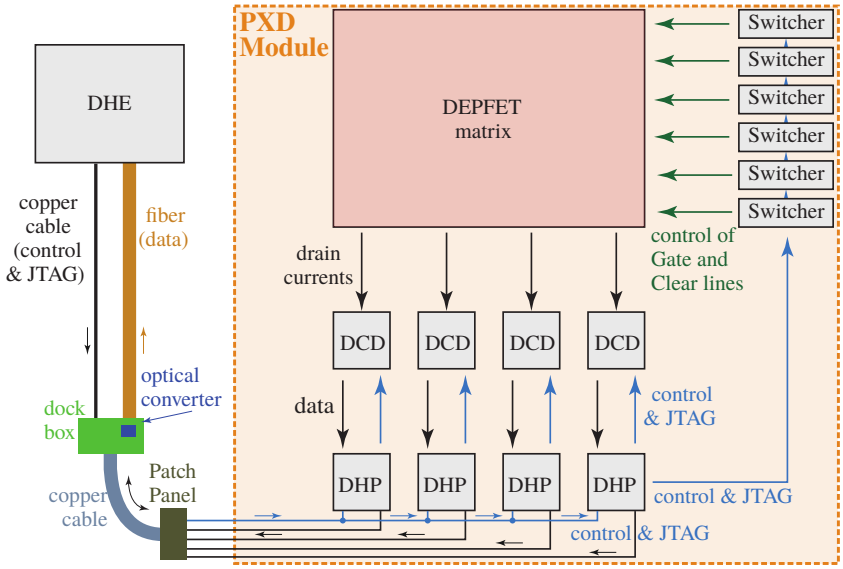


Figure 2.6: Schematic overview of the PXD components. Each module consists of the DEPFET matrix, six Switchers, and four DCD-DHP pairs. Control, Joint Test Action Group (JTAG), and data connections are indicated. The Data Handling Engine (DHE) is not part of the PXD module but belongs to the data acquisition system (DAQ), with data transferred via the patch panel and dockbox [12].

2.3.1 Switcher

The Switcher ASIC provides the gate and clear voltages to steer the DEPFET rows, thereby implementing the rolling-shutter readout of the matrix. Each Switcher provides 32 output channels for gate control and 32 for clear control. Since each Switcher channel controls four physical pixel rows at once, six Switchers are required to address all 192 logical rows and 768 pixel rows in a PXD module. The Switchers are controlled by one of the Data Handling Processors (DHPs) using four digital signals [22].

Switcher Sequence The four digital control signals are defined by the Switcher sequence stored in the memory of the DHP. The sequence is composed of 128-bit memory words, with each word corresponding to one channel. These words are divided into four 32-bit sections, each decoding one of the signals: `SerIn`, `StrC` (Strobe Clear), `StrG` (Strobe Gate), and `CLK` (Clock). Adjusting the pattern of these signals, the Switcher logic supports multiple operating modes [23]. For the PXD, only the mode with non-overlapping gates is used, where at most one gate is active at any given time. In this mode, the gates of two consecutive pixel rows are switched on and off simultaneously. The specific Switcher sequence used in the PXD, including the resulting `GateOn` and `ClearOn` states for the first two channels, is shown in Figure 2.7. Although the `GateOn` signal is logically high during activation, the actual applied gate voltage is negative.

All four control signals are transmitted simultaneously and the next word is sent after every 32 bits. The bits are applied at a rate of 305 MHz, resulting in a total duration of approximately 105 ns per word.

Each readout cycle begins with a `SerIn` pulse, sent by the DHP, which must be logically high during a rising `CLK` edge. It propagates internally through the channels with each `CLK` signal and defines the active output channel. However, two clock cycles delayed. Therefore, to start the readout with the first pixel row,

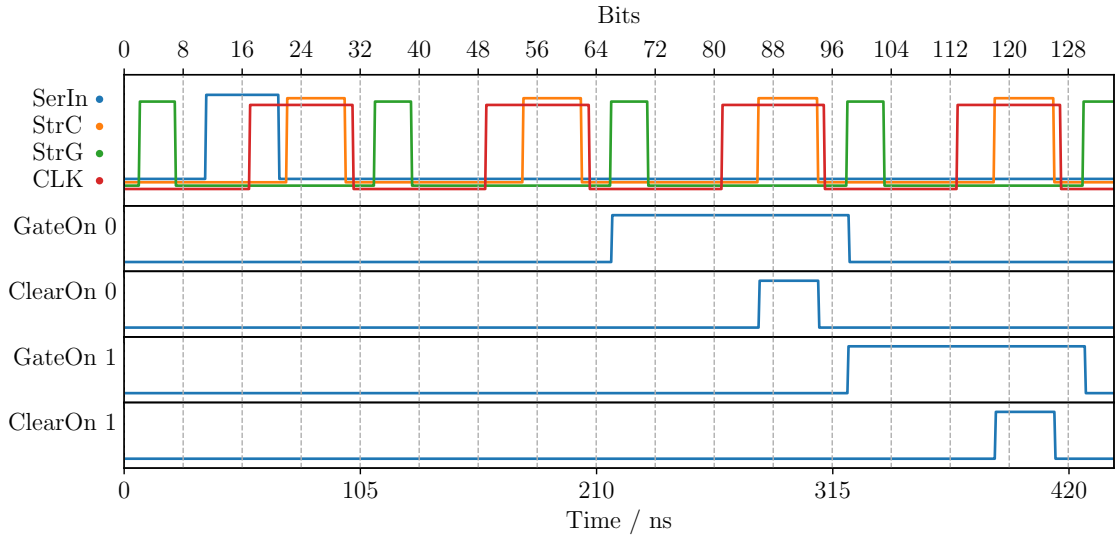


Figure 2.7: PXD Switcher Sequence and output of the first two channels. In color: Digital steering signals (Switcher sequence). Below: `GateOn` and `ClearOn` states for the first two rows. Two consecutive gates are activated and deactivated simultaneously. This switching occurs after the leading row is cleared. Gates are toggled by the rising edge of `StrG`. However, this must be after the falling edge of the `CLK` signal. The `ClearOn` signal is active when `CLK`, `StrC`, and `GateOn` are all high. The `SerIn` signal starts each cycle and must be transmitted two channels before the first gate.

`SerIn` must be set in the word corresponding to the second-to-last channel. To support daisy-chaining, each Switcher provides a `SerOut` output, which serves as the `SerIn` input for the next device.

The `StrG` signal activates the gate of the currently active channel, as defined by `SerIn`. `GateOn` state becomes logically high when `StrG` rises, and returns to low at a subsequent `StrG` pulse during a low `CLK` phase. In nominal operation, this leads to a sequential activation and deactivation of consecutive gates essential for the rolling shutter readout. If, however, `StrG` and `CLK` overlap, the `GateOn`-high states of consecutive channels overlap, resulting in a temporarily summed drain current from adjacent rows.

The `StrC` signal controls the clear pulse of the currently active gate channel. The `ClearOn` state is set to high only when `StrC`, `CLK`, and `GateOn` of the corresponding channel are simultaneously high.

Figure 2.8 shows the Switcher sequence in detail. The `StrG` signal is delayed by three bits relative to `CLK` to avoid overlap of active gates. Before the gate is deactivated by a second `StrG` pulse, the corresponding row is cleared via the `StrC` signal, which is synchronized with the `CLK` signal to activate `ClearOn`.

This timing sequence ensures that the sampling of the drain current occurs immediately before the clearing pulse. Since the sampling moment is fixed, the Switcher sequence is optimized to allow the drain current to settle as much as possible before being sampled, as shown in Figure 2.5.

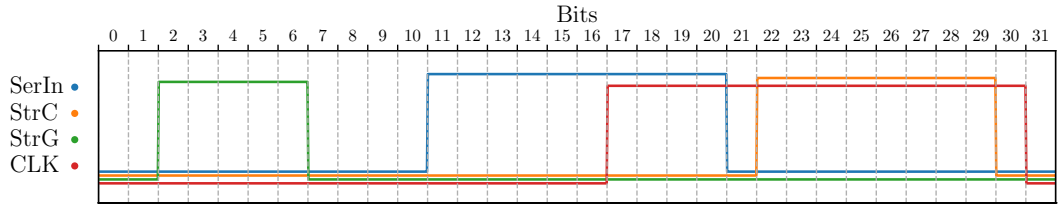


Figure 2.8: 128-bit Switcher memory word used in the PXD. The `SerIn` signal is transmitted only once per readout cycle. `StrG` is delayed relative to `CLK` to avoid overlapping gate activation. The `StrC` signal is within the bounds of the `CLK` signal, to enable a clear channel.

New Switcher Version

In the PXD at Belle II, SwitcherB18V2.1 is installed. However, a new version, SwitcherB18V2.3, is available and was used for the scope of this work. This version integrates additional over voltage protection to mitigate voltage spikes observed during beam loss events. The protection consists of RC clamp circuits to suppress fast transients and sensor-diode circuits to collect excess charge and stabilize internal voltages. In combination with the standard on-chip protection elements, these measures improve the robustness of the driver stages under sudden radiation-induced disturbances [24].

2.3.2 Drain Current Digitizer – DCD

The Drain Current Digitizers (DCDs) are responsible for digitizing the analog drain currents produced by the pixel matrix. The DCDs assign 8-bit digital values to the incoming currents, enabling precise signal processing and readout.

Each DCD provides 256 analog channels (see Figure 2.9). The pixel matrix has 250 columns with four drain lines each, requiring 1000 channels in total. Therefore, four DCDs, each using 250 of their channels, are employed so that every drain line is connected to an individual analog channel for parallel digitization.

The most important circuits of the analog channels are detailed below [25].

Receiver (Amplifier)

The receiver is a resistive current receiver and amplifies the incoming DEPFET current. The main component is a transimpedance amplifier. The ADC input current calculates to

$$I_{\mathrm{ADC}} = G \times \left(I_{\mathrm{in}} - I_{\mathrm{SubIn}} + I_{\mathrm{AddIn}} + I_{\mathrm{DAC}}\right) + I_{\mathrm{SubOut}} - I_{\mathrm{AddOut}} - I_{\mathrm{offset}}\,,$$

where G is the gain and can be adjusted by setting a registry, that adjusts the resistor parallel to the amplifier. The formula takes all other current sources besides the input current into account. These currents sources are SubIn, AddIn, SubOut and AddOut that allow for current subtraction and addition before and after the receiver. The offset current is defined as $I_{\mathrm{offset}} = (V_{\mathrm{in}} - V_{\mathrm{ADCin}})/R_s$, where V_{ADCin} is the constant input potential of the ADC and R_s the resistance between amplifier and ADC [25].

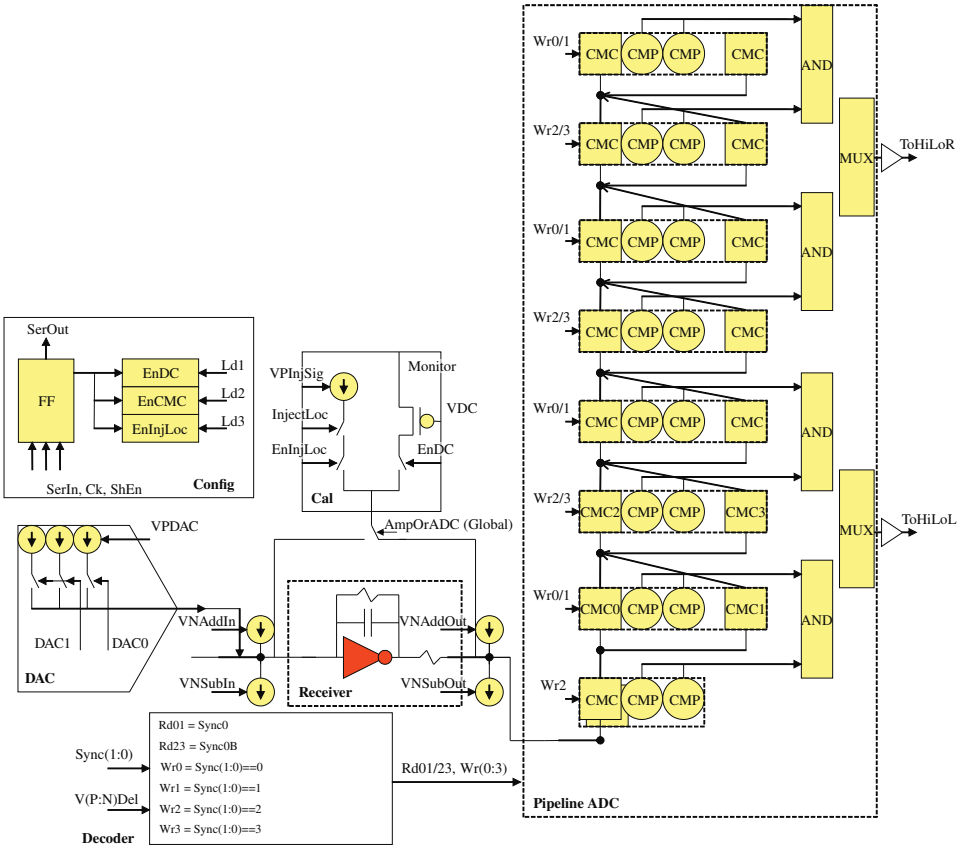


Figure 2.9: Block diagram of a DCD analog channel. Each channel compromises the following main circuits: (resistive current) Receiver – amplifies the incoming current; 8-bit current-mode pipeline ADC; 2-bit Digital-to-Analog Converter (DAC) for pedestal correction; Decoder – generates the control signals for the ADC; Config – configuration register [25]

Pipeline ADC

The ADC in each analog channel of the DCD performs an 8-bit current-mode conversion using the Redundant Signed-Digit (RSD) algorithm, implemented in a pipeline structure with 8 stages. Each stage encodes the input current into an RSD digit $\{-1, 0, +1\}$, represented by a pair of bits $(\mathtt{h_i}, \mathtt{l_i})$, by comparing the input current with positive and negative thresholds. Depending on the comparison result, a reference current is either added, subtracted, or left unchanged.

- Input current above positive threshold: output code $\mathtt{10} \rightarrow +1$, subtract reference current
- Input current below negative threshold: output code $\mathtt{01} \rightarrow -1$, add reference current
- Input current between thresholds: output code $\mathtt{00} \rightarrow 0$, no correction applied

The current transfer behavior according to this algorithm is visualized in Figure 2.10.

The resulting current is multiplied by two and passed to the next stage.

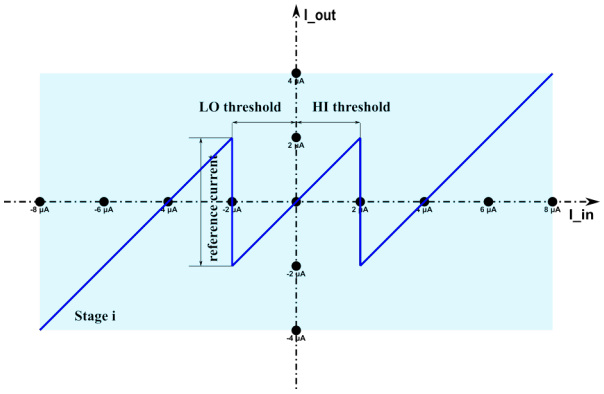


Figure 2.10: Current transfer between stages according to the Redundant Signed-Digit (RSD) algorithm [26].

The redundancy in the RSD algorithm allows for tolerance against comparator offsets: deviations up to half the threshold do not affect the final result. After 8 stages, the bit pairs $(\mathtt{h_i}, \mathtt{l_i})$ are decoded into a signed 8-bit number [25]:

$$D = \sum_{i=0}^{7} 2^i \cdot (\mathtt{h_i} - \mathtt{l_i}) \,.$$

Each stage consists of the following components:

- Two **Current Memory Cells (CMCs)** to store the signal and residue currents
- Two **comparators** for threshold decision making, connected to the first CMC

The pipeline structure enables high sampling rates, as each stage is used only once per conversion cycle. Once the current is passed to the next stage, the previous stage is immediately ready to process the next current sample. Each stage executes a sequence of four steps to generate one bit pair for the RSD algorithm. For even-numbered stages, the sequence is as follows:

Step 1: The currents from the previous stage are written into the first memory cell (active steering signals: `Wr0, Rd23`). The comparators connected to this cell are in reset state.

Step 2: The currents from the previous stage are written into the second memory cell (`Wr1, Rd23`). The comparators are now in compare state.

Step 3: The comparators latch the decision. Currents from both memory cells are read, summed, and written to the first cell of the next stage (`Rd01, Wr2`) . Depending on the comparator results, the reference current gets added or subtracted from the current read from the memory cells.

Step 4: Repetition of Step 3, but the currents are written to the second memory cell of the next stage (`Rd01`, `Wr3`).

When properly calibrated, the output current from both memory cells is half the full-scale signal range, which is 4 times the reference current R (output current = $\pm 2R$). Therefore, summing the two is equivalent to multiplying the current by two.

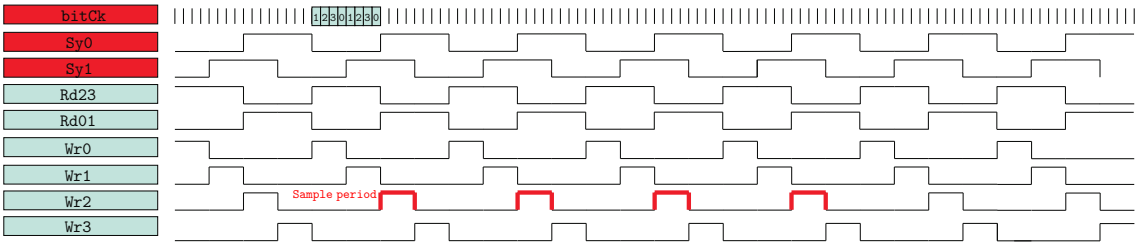


Figure 2.11: Timing diagram of the ADC steering signals, generated by the decoder from two synchronization signals `Sy0` and `Sy1` [25].

Odd-numbered stages follow the same steps but are time shifted by two steps, as they use `Wr2` and `Wr3` instead of `Wr0` and `Wr1`. This timing offset can be seen in Figure 2.11. In the first pipeline stage, both memory cells are written simultaneously. This doubles the dynamic range and halves the time that the current gets sampled in.

The finally resulting high/low bit pairs of the comparators get compressed by the `AND` and multiplexer logic and sent to the digital readout block. A discrete 8-bit output code is calculated by discarding the Least Significant Bit (LSB) [25].

This ADC design ensures high-speed digitization, low noise, and resilience against analog imperfections. The pipeline structure overlaps sampling and conversion, enabling a high sample rate.

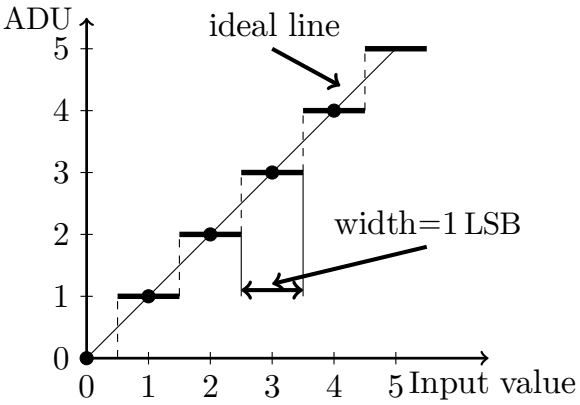
Pedestal Correction DAC

Since pedestals and signal are measured simultaneously, it is essential to compensate for the pixel specific pedestal variation. This ensures that the limited dynamic range of the ADC is not exceeded. To achieve this, each channel is equipped with a programmable 2-bit DAC, which subtracts a fixed current from the signal prior to digitization.

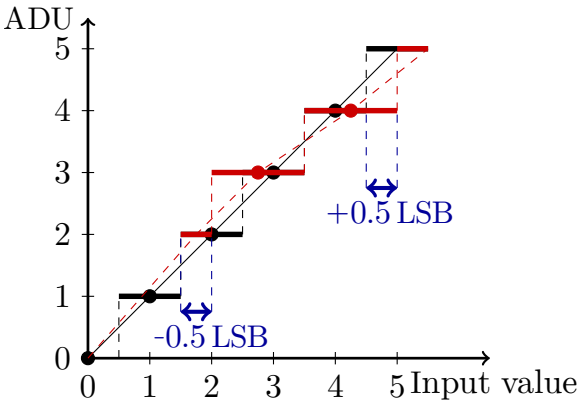
Transfer Curve

The transfer curve represents the translation between input current and digital output value. The ideal ADC with infinite resolution has a linear transfer curve. A real ADC however has a limited resolution and the transfer curve goes up in steps (see Figure 2.12(a)). The step width is called the Least Significant Bit (LSB) and is defined as:

$$LSB = \frac{\text{dynamic range}}{\text{\# steps}}$$



(a) Ideal transfer curve. The ideal line passes through the midpoint of the individual output codes. The output values are given in Arbitrary Digital Unit (ADU).



(b) Differential Non-Linearity (DNL). Positive values correspond to widened steps, negative values to narrowed steps. The black line indicates the ideal reference.

Figure 2.12: Illustration of ADC transfer curve characteristics: (a) transfer curve and (b) differential non-linearity [12].

In practice, the transfer curve can have several types of deviations from the ideal behavior:

Differential Non-Linearity (DNL) The differential non-linearity qualifies the deviation of the ideal step width (LSB), as shown in 2.12(b). It can be positive or negative, depending on whether the step width is larger or smaller than the LSB, respectively. A DNL of zero implies perfect step size.

Special cases include:

- *Wide code*: DNL = +1, the step width is twice the ideal.
- *Missing code*: DNL = −1, the corresponding output code is skipped entirely.

Offset error The offset error is the deviation of the zero output code from the ideal origin along the input axis.

Gain error The gain error refers to the deviation of the slope of the actual transfer curve from the ideal slope.

Integral Non-Linearity (INL) After correcting for offset and gain errors, the integral non-linearity describes the remaining deviation from a straight line connecting the first and last output codes. It can also be interpreted as the cumulative integral of the DNL across all steps.

To optimize the ADC performance, the DCD ASIC has several configurable reference voltages and currents. For the calibration, ADC transfer curves are recorded for various DCD configurations by applying a known current to the ADCs. The resulting transfer curves are then evaluated by performing some tests to improve on the errors listed above, as well as some other defects like limited range and noise. The final configuration chosen for PXD operation corresponds to the setup that yields the highest number of well-performing ADC channels. Additional details on ADC tuning and evaluation can be found in section 4.1.3.

2.3.3 Data Handling Processor – DHP

Each PXD module integrates four Data Handling Processors (DHPs), with each DHP placed behind one of the DCDs, forming a so-called ASIC pair. Each DHP is dedicated to the readout and control of its corresponding DCD and performs initial data processing to reduce the data rate. To ensure synchronization of the DEPFET matrix control with the DCD readout, the DHPs also generate the four digital steering signals required by the Switcher ASICs. The Switcher sequence is stored in a dedicated, writable memory within the DHPs. Only the DHP located closest to the Switchers transmits the steering signals (see Figure 2.6).

The DHP stores a pixel offset map and transmits the corresponding offset values to the DCD, which applies them for analog pedestal correction via the 2-bit DACs in the ADC channels before sampling. For data reduction, the DHP performs *zero-suppression* to distinguish real hits from noise. First, pedestals stored in a pedestal map in the DHP's memory are subtracted from the sampled data. The result is then compared to a configurable threshold, and only hits that exceed this threshold are further processed. This reduces the data rate from the DCD (20 Gbit/s) to a level that can be handled by the high-speed link (1.6 Gbit/s) to the DAQ [27].

Alternatively, data can be transmitted without pedestal subtraction and zero-suppression. However, due to the lack of data compression, the resulting data rate is significantly higher and limits the maximum achievable trigger frequency.

2.4 Module Operation System

For the operation of PXD custom power supplies and a data acquisition system are necessary.

Each PXD module needs its own Power Supply (PS), which provides the 23 different voltages required to operate the DEPFET pixel matrix and the ASICs: 10 voltages for the Switcher ASICs, 4 for the DCDs, 2 for the DHPs, and the remaining 7 for the DEPFET matrix itself. The *PXD PS* must also fulfill several important requirements such as low noise, post-regulation after sensing to compensate for voltage drops over the 15 m long cables to the modules, adjustable current limitation, control of dependencies between some voltages, precise power-up and power-down sequences, fine tuning of voltages, and more. Therefore, a custom PS was designed for the PXD [28]. Table 2.1 summarizes the most important voltages and their functions.

2.4.1 Data Acquisition System

The PXD data acquisition system (DAQ) is implemented by the Data Handling Hybrid (DHH) [29]. Each PXD module connects to a Data Handling Engine (DHE), an FPGA[1]-based module that receives zero-suppressed data over the high-speed links from the DHPs. The DHE is also responsible for slow control via JTAG[2], cluster reconstruction, and local buffering. Groups of five DHEs transmit their

[1] Field-Programmable Gate Array

[2] Joint Test Action Group: Industry standard interface for serial communication to configure, test, and debug integrated circuits.

Table 2.1: Key supply voltages for the Switcher, DCD, and DEPFET matrix, with their functions and typical values [17].

Block	**Voltage**	**Purpose**
Switcher	DVDD (1.8 V)	Digital supply
	RefIn (−5.3 V)	Reference input
	Gate-on (−2.3 V)	Gate-on supply
	Gate-off (5 V)	Gate-off supply
	Clear-on (19 V)	Clear-off supply
	Clear-off (3 V)	Clear-on supply
DCD	AVDD (1.8 V)	Analog supply
	DVDD (1.8 V)	Digital supply
	RefIn (725 mV)	Reference input
	AmpLow (300 mV)	Current sink
Matrix	HV *high voltage* (−66 V)	Bulk depletion
	Source (6 V)	Source supply

processed data to a Data Handling Concentrator (DHC) via 6.5 Gbit/s links. The DHC builds sub-events based on trigger numbers and forwards the data to the Online Selection Nodes (OnSeN) system [29]. Additionally, it receives the global clock, trigger signals, and slow control communication from the global Belle II trigger and timing system and transmits it via the Data Handling Insulator (DHI) to the module. The DHI galvanically isolates the five electrical channels to the detector [30]. For the full PXD system, eight DHHs are used. In test environments, a single DHE can operate independently using dedicated firmware that generates clock and control signals and streams data directly to the LocalDAQ [31].

The OnSeN system receives data from the eight DHCs and reduces the data by a factor of about ten. It defines Region Of Interest (ROI) from tracks reconstructed in surrounding detectors, most importantly the DCD. Only hits within ROIs are retained, significantly suppressing noise and background before passing the data on to the Belle II event builder [32].

2.4.2 Total Ionizing Dose (TID) Damage

The radiation environment at BelleII leads to long-term degradation of detector components through the accumulation of Total Ionizing Dose (TID). This form of damage is caused by the ionization of insulating materials, primarily silicon dioxide layers. Unlike Non-Ionizing Energy Loss (NIEL), which creates displacement damage in the silicon bulk, TID primarily affects surface and interface regions at the Si–SiO_2 boundary [33]. For the PXD, it has been shown that NIEL is negligible [34].

As energetic particles traverse oxide layers, electron-hole pairs are generated. Most electrons are removed by internal fields, whereas holes can be trapped in the oxide or at the Si–SiO_2 interface. The resulting positive oxide charge together with interface states modifies local electric fields and band bending and drives drifts in device parameters such as threshold voltage and leakage current..

In DEPFET sensors, which rely on field-effect modulation in a fully depleted bulk, these surface-related effects reduce breakdown margins, increase surface leakage, and alter field uniformity. A negative shift of the DEPFET threshold voltage due to positive oxide charge is typically observed and is compensated in operation; its magnitude depends on the dielectric stack and processing conditions.

For the front-end electronics used with the PXD, which are based on metal oxide semiconductor (MOS) transistors, TID similarly induces threshold shifts and excess leakage that can perturb analog biasing and timing, thereby affecting noise and stability of the readout chain.

TID-induced oxide-trapped charge partially relaxes after irradiation at room temperature via tunnel-related processes, with elevated temperature accelerating recovery. Bias conditions during and after irradiation influence the net effect. Interface traps, in contrast, anneal only weakly at room temperature and therefore contribute more persistently to long-term parameter drift.

2.4.3 Pedestal Noise Degradation in PXD

During data taking in Phase 3 of the Belle II experiment (2019–2022), an increase in pedestal noise was observed in the PXD modules, which correlated with the accumulated TID [35]. Detailed analysis revealed that not only the total dose but also the rate of TID accumulation had a measurable impact on the pedestal evolution. Figure 2.14 illustrates this correlation.

In Phase 3, the PXD was only partially installed, with a fully populated inner layer and only two ladders in the outer layer. Radiation monitoring data from this period [35] indicate that TID was not uniformly distributed across the detector volume. In particular, modules facing away from the accelerator ring experienced higher TID levels compared to their inward-facing counterparts. This radial asymmetry in TID exposure is illustrated in Figure 2.13, which shows the deposited TID across all modules of the inner layer.

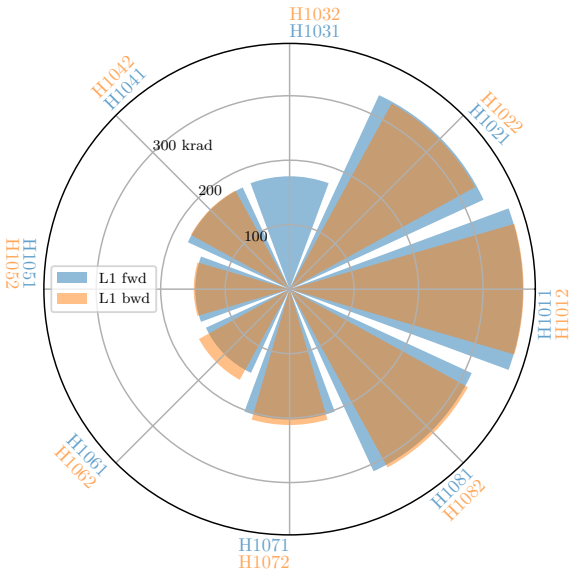
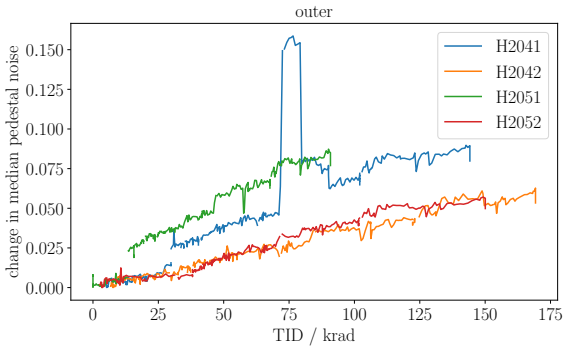
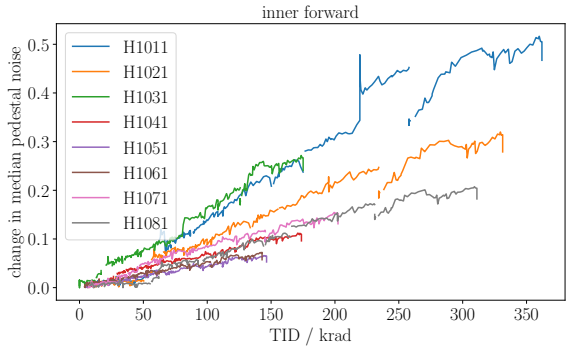


Figure 2.13: Radial TID distribution across forward (fwd) and backward (bwd) modules in the inner PXD layer. Modules facing outward relative to the accelerator ring (right side) accumulated about twice the TID dose of inward-facing modules. Based on data from [35].



(a) Median pedestal noise increase vs. TID in outer layer forward and backward modules.



(b) Median pedestal noise increase vs. TID for inner layer forward modules. The behavior of backward-facing modules is nearly identical; therefore, the corresponding plot is omitted here.

Figure 2.14: Correlation between pedestal noise increase and accumulated TID. Forward- and outward-facing modules with higher TID show a steeper increase. Adapted from [35].

The impact of this asymmetric dose deposition is reflected in the pedestal noise evolution. Figure 2.14 shows the pedestal noise increase in outer-layer modules and the forward facing modules in the inner layer. A rise in median noise is observed as a function of TID. Modules which received a higher TID due to higher dose rate, exhibited a steeper noise increase.

Since pedestal noise directly affects the signal-to-noise ratio and thus the performance of the PXD, the observed correlation with TID demands thorough investigation. The search for the origin of this degradation motivated the design and execution of two dedicated irradiation campaigns. In these studies, the control and readout ASICs, Switcher and DCD, were irradiated separately under controlled conditions to identify their individual contributions to the observed noise increase. This thesis presents the methodology, execution, and results of these irradiation campaigns, which are discussed in detail in the following chapters.

CHAPTER 3

Experimental Setup

This chapter outlines the experimental setup employed to irradiate DCD and Switcher ASICs under controlled conditions.

In the laboratory, a simplified version of the full Belle II PXD module is commonly employed, referred to as *Hybrid5*. It comprises a smaller DEPFET matrix and a single set of front-end ASICs. For readout and control, a standalone DHE is used, which transmits data directly to a local data acquisition system, thereby eliminating the need for the intermediate DHH and DHC components required in the full-scale Belle II PXD setup.

This simplified setup is advantageous in experimental environments, especially when individual components must be irradiated and accommodated inside radiation-shielded enclosures.

A photograph of the complete lab setup is shown in Figure 3.1. One primary power supply is dedicated to the PXD PS and its cooling fan. The other powers the DHE carrier board, which interfaces the DHE with the control PC and also includes a fan for thermal management.

Power delivery from the PXD PS to the Hybrid5 is achieved in two stages. In the first stage, power is transmitted over two 15 m long cables identical to those deployed in the Belle II detector. These cables connect to a *power breakout board*, serving as a substitute for the *dock box* in the full system. In the second stage, a *Glenair* cable merges both lines and connects the breakout board directly to the Hybrid5. This cable consists of individual copper cables each for an individual voltage, e.g. Source, DCD-RefIn, Gate-On.

The DHE is linked to the Hybrid5 using two *InfiniBand* cables: one for the high-speed data stream and one for the JTAG-based slow control.

Communication between the DHE, PXD PS, and the control PC is managed via independent network interfaces. The DHE requires two separate Ethernet connections: one for high-speed data transfer and one for slow control. Consequently, the PC must provide at least four network interfaces: two for the DHE, one for the PXD PS, and one for external laboratory network access. All components are controlled via an EPICS (Experimental Physics and Industrial Control System) based framework.

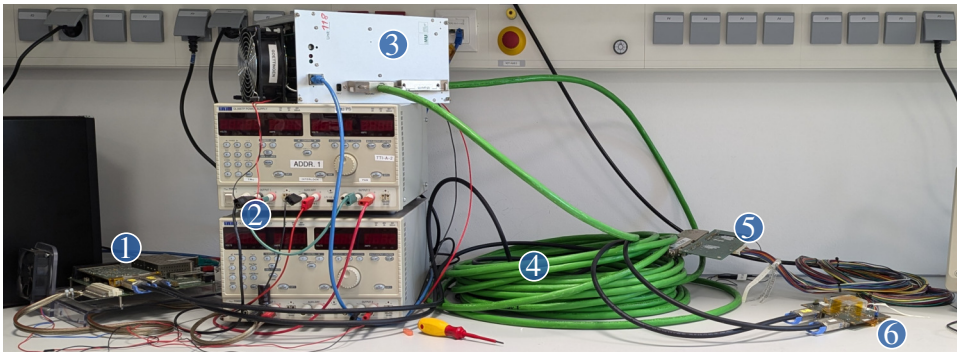


Figure 3.1: Photograph of the Hybrid5 lab setup showing: ① DHE, ② two bench power supplies, ③ PXD Power Supply, ④ power cables (15 m), ⑤ Power Breakout Board, ⑥ Hybrid5 module.

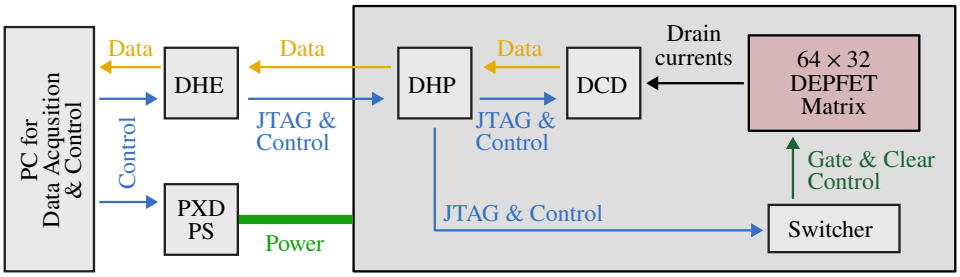


Figure 3.2: Block diagram of the Hybrid5 lab setup, illustrating control and data flow directions.

3.1 Hybrid5

A photograph of a Hybrid5 module is shown in Figure 3.3. It typically includes a 64×32 DEPFET pixel matrix, although versions with larger matrices exist for the smallest available pixel size of 55 µm. These matrices were fabricated on the same wafers as the full-scale PXD DEPFET sensors for Belle II.

The matrix is controlled by a single Switcher ASIC that applies gate and clear voltages to the pixel rows. Signal readout is performed by a DCD-DHP ASIC pair. These ASICs, along with the DEPFET matrix, are mounted on individual surfboards and glued onto the Hybrid5 circuit board. Electrical connections are established by open wire bonds, as shown in Figure 3.4.

Due to the reduced matrix dimensions, only 128 of the 256 DCD channels are utilized, corresponding to the 32-column matrix width. Similarly, only 16 of the 32 Switcher channels are used to control the 64-row matrix. This configuration preserves the fourfold readout scheme of PXD. The Hybrid5 employed for this work utilizes a DEPFET matrix with 55 µm pixels providing enough pixels such that 20 Switcher channels are connected to the sensor. Often, adjusted Switcher sequences are used for the Hybrid5s. They are either adjusted for 16 or 32 Switcher channels depending on which Switcher channels are connected to the matrix. However, for the scope of this work the same Switcher sequence as for a full scale PXD module with 192 Switcher channels was employed, in order to ensure better comparability to the conditions of the Belle II experiment.

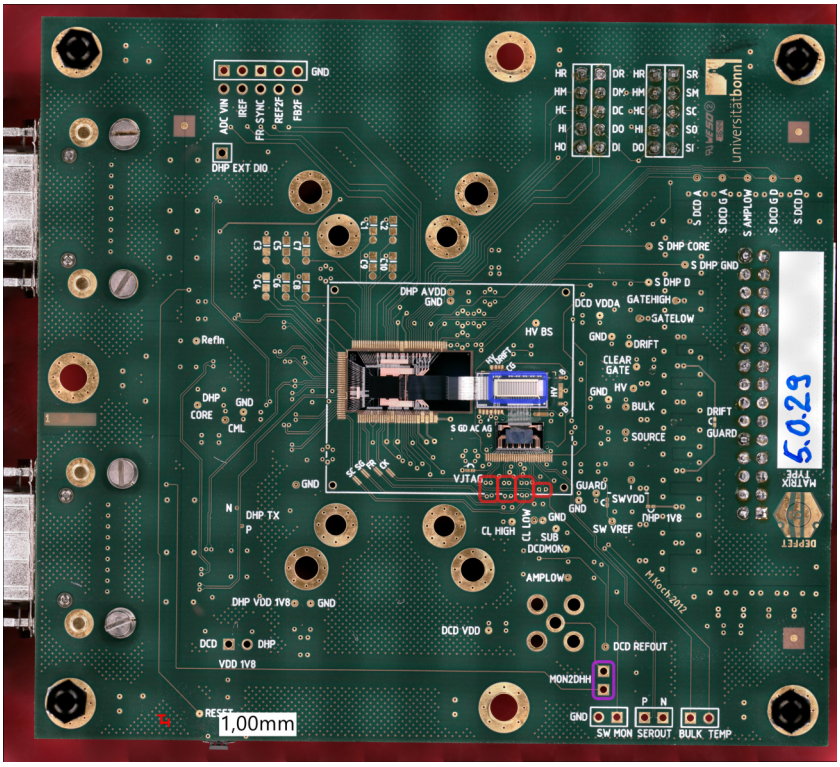


Figure 3.3: Hybrid5 circuit board. The DEPFET matrix (blue) is located at the center. Beneath the matrix is the Switcher ASIC. To the left, in sequence, are the DCD and DHP ASICs. Four test contacts (red) below the Switcher allow probing of the Switcher digital steering signals; from left to right: `SerIn`, `StrC`, `StrG`, `CLK`. These contacts are also accessible from the backside. At the bottom, the `MON2DHH` monitoring jumper (purple) provides a connection to measure the DHE current source (section 4.1.3) or to route it to the DCD for measuring ADC transfer curves.

The Hybrid5 board incorporates several test and monitoring features. Of particular relevance to this work are the following:

Digital signals controlling the Switcher (`SerIn`, `StrG`, `StrC`, and `CLK`) are accessible via monitoring points highlighted in Figure 3.3. Short 4 cm cables are soldered directly to these points, for monitoring. A separate surfboard with monitoring pins is wire-bonded to a subset of Switcher gate and clear output channels. All these outputs can be probed with oscilloscopes.

The DHE incorporates an internal current source to record ADC transfer curves. In order to inject this current into the DCD, it is necessary to set the `MON2DHH` jumper. The same jumper can also be used to read out the DHE current source externally and to calibrate it using a Source Measurement Unit (SMU).

The board also provides mechanical mounting holes to attach a cooling block on the backside, directly beneath the DCD ASIC to ensure adequate thermal dissipation, as the DCD dissipates the most heat in the module [36].

To prevent damage from excessive dark currents, the DEPFET matrix must be shielded from ambient

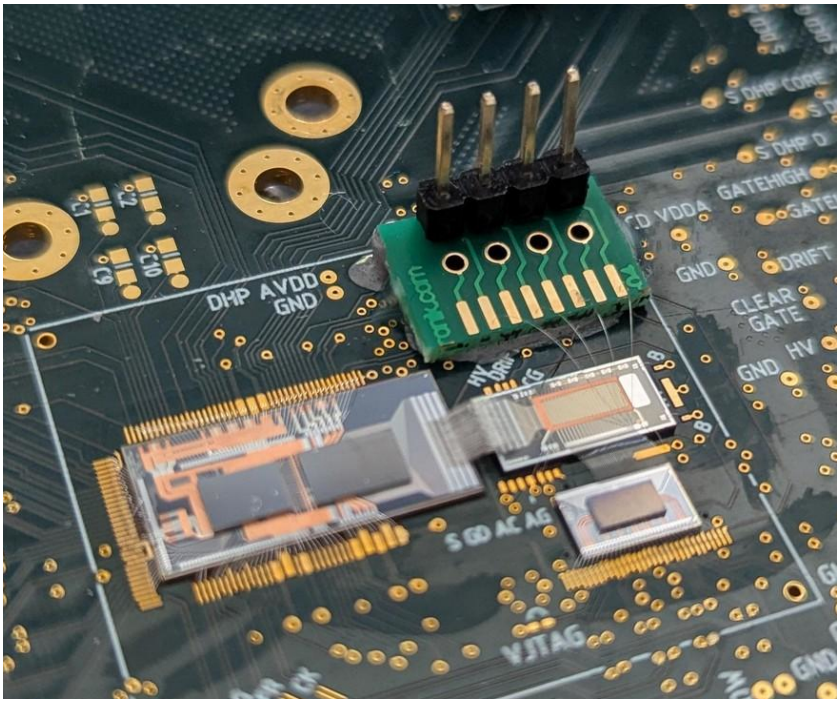


Figure 3.4: Close-up photograph of the Hybrid5 DEPFET matrix together with the Switcher, DCD, and DHP ASICs. In addition, the surfboard with pins to monitor several Switcher output channels is visible. It is directly wire-bonded to two gate/clear Switcher channel pairs.

light during operation. Exposure can lead to increased currents that may damage both the sensor and readout electronics.

Each Hybrid5 used in the lab has an individual identification code. The main board used for the scope of this work was H5032[1].

3.2 X-Ray Tube

For the irradiation of the Switcher and DCD ASIC, an X-ray tube was employed.

An X-ray tube operates by accelerating electrons toward a metal anode using a high voltage U. When these electrons strike the target, their kinetic energy is partially converted into electromagnetic radiation. This results in a continuous bremsstrahlung spectrum along with discrete characteristic lines, the latter determined by the anode material. The maximum photon energy is given by $E_{\max} = e \cdot U$, where e is the elementary charge. The intensity of the emitted spectrum is controlled by the tube current and the choice of target material [37].

[1] ASICs: DHPT1.2b , DCDBv4.2; Waver: PXD9-8 W47_A05

To modify the spectral distribution, metallic filters are commonly placed in the beam path to remove low-energy X-rays. These low-energy photons contribute to the overall dose, yet do not effectively penetrate the irradiated target [38].

X-ray beams are usually not completely uniform. Spatial variations in intensity and spectrum can occur due to internal tube geometry. A notable example is the *anode heel effect*, where the angled anode causes a lateral gradient in flux and energy. X-rays exiting the anode at shallow angles toward the anode side traverse a longer path through the anode material and are thus more strongly attenuated. This leads to a reduction in intensity in the direction of the anode [39]. Such inhomogeneities must be considered when positioning sensitive devices.

X-Ray Chamber The X-ray tube used for this work is mounted to the ceiling of a large shielded irradiation chamber, as shown in Figure 3.6. The target is positioned below the tube, either on the threaded mounting plate or on the height-adjustable rack. Feedthroughs allow cables and cooling lines to be routed into the chamber. Two alignment lasers, fixed next to the X-ray tube, project a crosshair onto the chamber floor that defines the beam center.

Nominal Operating Point For the irradiations performed in this work, the X-ray tube equipped with a tungsten anode is operated at an acceleration voltage of 40 kV and a tube current of 50 mA. A 150 µm thick aluminum filter is installed in the beam line to suppress the low-energy spectral component. The distance from the tube exit to the target is set to 30.5 cm, yielding a typical dose rate in the range of 0.4 to 0.5 Mrad/h at the target plane.

Beam Calibration Prior to any irradiation, the X-ray beam in the target plane is mapped to determine the spatial distribution of the dose rate. For this purpose, an *xy* motor stage is installed beneath the tube. A reverse-biased silicon photodiode mounted to the stage is connected to a SMU. The diode is aligned with the laser crosshairs and then scanned across the X-ray beam. The resulting current map provides the beam profile and enables positioning of the target in a homogeneous area.

The dose rate $\dot{D}$ is calculated from the measured photo diode current I according to:

$$\dot{D} = \frac{I}{\eta} \cdot \frac{\varepsilon_{\text{eh}}}{q \cdot m},$$

where η is the charge collection efficiency, ε_{eh} is the average energy required to create an electron-hole pair, q is the elementary charge, and m is the mass of the active diode volume [40].

3.2.1 Hybrid5 Assembly for Irradiation

For the irradiation of the DCD and Switcher ASIC, the Hybrid5 module was placed inside the X-ray chamber, while the DHE, PXD PS, and two oscilloscopes were positioned on a table next to the chamber.

A cooling block was mounted to the backside of the Hybrid5 and connected to a chiller, providing cooling fluid to maintain the DHP and DCD at approximately 15 °C.

The Hybrid5 was shielded with a 5 mm thick brass plate, which includes cutouts exposing the DCD and Switcher. During irradiation, one of the cutouts was selectively covered with a lead piece, depending on which ASIC was targeted.

Feedthroughs in the chamber floor were used to route:

- Power lines to the Hybrid5
- Tubes for cooling fluid
- Two InfiniBand cables (for control and high-speed data)
- Six oscilloscope probe cables

The digital Switcher signals were monitored with differential probes. These have an active element at the tip of the cable, for amplification, that is sensitive to radiation. As these probes were attached close to the Hybrid5 they were close to the X-ray beam and had to be additionally shielded.

For secure installation of the setup, the Hybrid5 was mounted to the height-adjustable rack inside the chamber using a custom mounting bracket, as shown in Figure 3.6. A close-up photograph of the Hybrid5 assembly with installed shielding, power and data connections, oscilloscope probes, and the cooling block is presented in Figure 3.5.

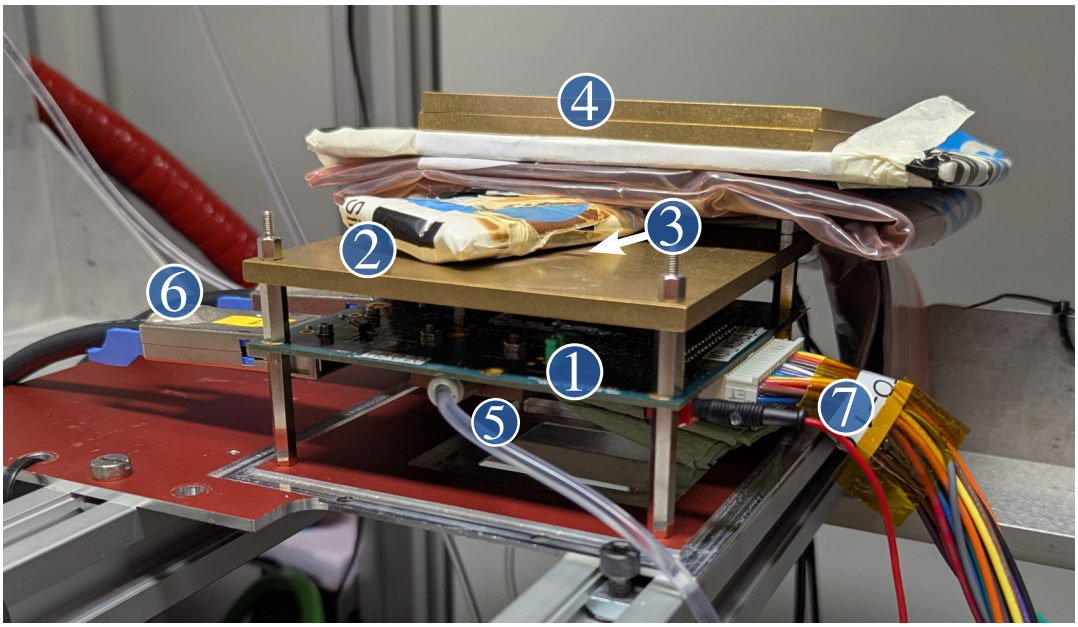


Figure 3.5: Close-up photograph of the Hybrid5 assembly installed in the X-ray irradiation chamber. The Hybrid5 ① is protected by a 5 mm thick brass shielding plate ②. This plate contains two cutouts for the DCD and Switcher ASIC ③, one of which is covered by an additional lead piece wrapped in white tape. Oscilloscope probes for monitoring the Switcher signals are connected at the rear and enclosed by brass and lead plates to provide radiation shielding ④. A cooling block with its corresponding cooling lines ⑤ is mounted to the underside of the Hybrid5. From the left and right sides, power cables ⑦ and two InfiniBand cables ⑥ provide the high-speed data link and JTAG control connections.

Figure 3.6: Photograph of the X-ray irradiation chamber. The X-ray tube is mounted at the top and angled downward toward the irradiation target. The Hybrid5 module is mounted on the height-adjustable rig at the center. Oscilloscope probes are connected from the back and are covered with lead shielding, while power and InfiniBand cables are routed from the sides. Cooling fluid circulates through transparent tubes from front to back. A brass shield with cutouts for the DCD and Switcher is placed over the Hybrid5 to expose specific ASICs.

CHAPTER 4

DCD and Switcher Irradiation Campaign

The investigation into the underlying factors contributing to the observed increase in pedestal noise due to radiation exposure of the PXD modules at Belle II (section 2.4.2) resulted in dedicated irradiation campaigns, in which DCD and Switchers were individually irradiated. In this chapter, the procedures of both irradiation and measurement are presented. Subsequent to this, an interpretation of the measurement results is presented.

Both, the DCD and Switcher irradiation campaigns were carried out with the same Hybrid5 (H5032). Therefore, careful consideration had to be given to which ASIC should be irradiated first. It was decided to irradiate the Switcher first and the DCD second. Even if the Switcher is damaged, the DCD's performance can still be evaluated. In contrast, a damaged DCD makes the study of any effects in the Switcher hard. Nevertheless, the goal was to irradiate both ASICs up to their maximum stated radiation hardness [41]. This decision was supported by previous test campaigns, carried out on another Hybrid5 (H5020[1]). However, this had already been irradiated with electrons at the Mainz Microtron (MAMI) particle accelerator.

Besides the question whether the pedestal noise increases with the irradiation of the ASICs, the irradiation campaigns were designed to find out whether a re-optimization of the DCD could mitigate this effect.

4.1 Measurements

Within this section all measurements that were performed during the irradiation process are introduced. Prior to each measurement the systems configuration is logged, including all voltages and currents of the Hybrid5 module, settings for the ASICs including the settings of various register entries.

[1] ASICs: DHPT1.2b, DCDBv4.2; Wafer: PXD9-7 W31_A05

4.1.1 Pedestals Measurement

Pedestal measurements are conducted to determine the *dark current* of each pixel in the absence of any charge in the internal gate. This current serves as a reference for the extraction of true signal amplitudes during subsequent measurements and data compression. An accurate determination of the pedestal is therefore essential for precise signal reconstruction. Since the pedestal is subtracted from the signal, noise in the pedestal has a direct influence on the signal-to-noise ratio and thus the overall PXD performance. Consequently, optimization of pedestal noise is of high interest.

Pedestals are determined by recording a series of raw frames with the DEPFET matrix operated under standard conditions and without incident radiation. The acquired data thus represent the intrinsic drain currents of the pixels. To ensure statistical stability, a large number of frames is recorded. A pixel map of the mean values is calculated, and the noise is defined for each pixel as the standard deviation across all frames. This procedure is necessary since each pixel has a slightly different pedestal due to imperfections in the production of the DEPFET sensor. In addition, small differences in the drain voltage between lines and voltage drops in the distribution of gate and source voltages across the matrix also affect the pedestal values. These effects are negligible for small structures like the Hybrid5 but become relevant in a full-scale PXD module.

In order to analyze the pedestal data, two sets of plots are generated, considering only the connected DCD and Switcher channels selected via a mask. One set shows the pedestals, the other the noise (see Figure 4.1). The pedestal plot includes a histogram where all pedestal values are individually accounted (not mean values per pixel), and a pixel map of the pedestal means. Similarly, the noise is visualized using a pixel map and a histogram. In the noise histogram, each pixel contributes only one value since the standard deviation is calculated over all frames. Gaussian fits are applied to both histograms to extract the median pedestal and noise values.

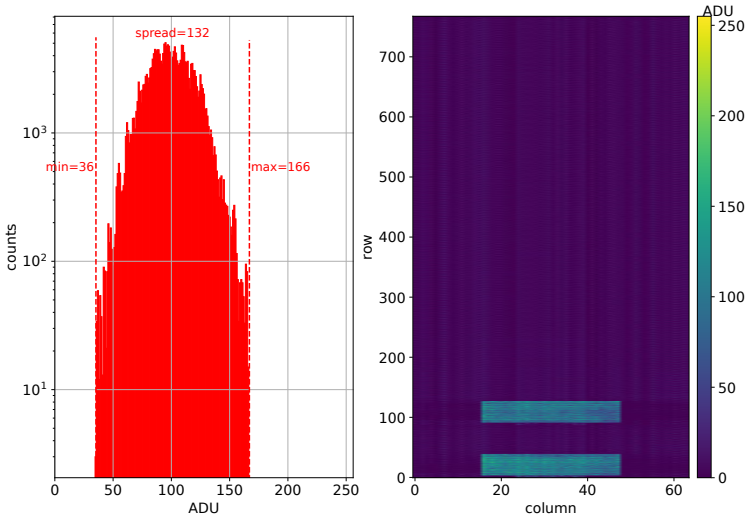
The pixel map is only partially filled, since only a subset of DCD and Switcher channels is connected due to the reduced DEPFET matrix size. In this particular example setup, the first and last ten Switcher channels are connected. The resulting gaps in the vertical direction correspond to the unconnected twelve channels and the five missing Switchers from a full module.

The Hybrid5 used for the irradiation study exhibits an unusually broad pedestal distribution (see Figure 4.2). To reduce the influence of DCD non-linearities near the lower and upper ADC limits, a filter is applied during the noise analysis. Only pixels with a mean pedestal value between 50 and 200 ADU are considered for calculating the average noise, to suppress distortions caused by non-linearities near the boundaries of the DCD dynamic range.

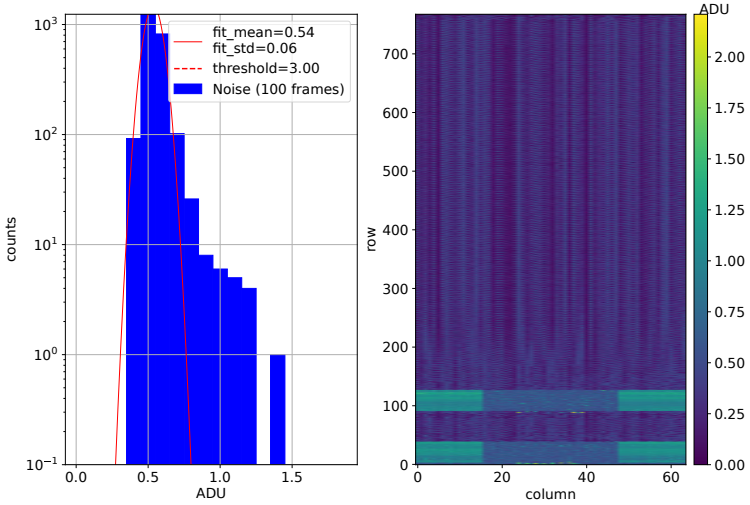
Automatic Pedestal Shifting Additionally, a safety mechanism is implemented into the pedestal analysis to prevent pedestal values from shifting out of the dynamic range of the DCD. If the median pedestal moves beyond predefined thresholds, the VNSubIn parameter is adjusted (increased or decreased accordingly) to shift the pedestal back into the ideal range for operation. VNSubIn is a defined current, that is subtracted from an incoming current before it becomes amplified in the DCD (compare Figure 2.9).

Due to the large sample size of each pedestal measurement, the statistical error is extremely low for the median pedestal value and pedestal noise. Therefore, in the following analysis, it is refrained from

including error for pedestal related plots and analysis. Furthermore, this decision makes the plots considerably clearer.

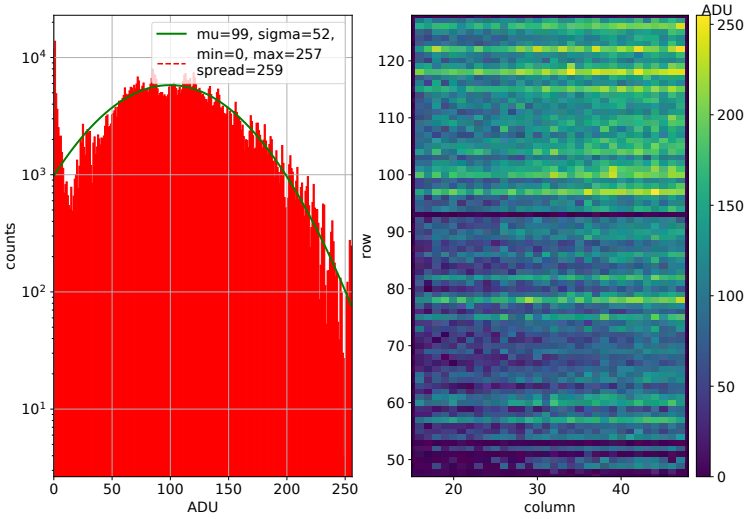


(a) Pedestal distribution (left) and pixel map (right). Each pixel contributes per frame one entry to the histogram.

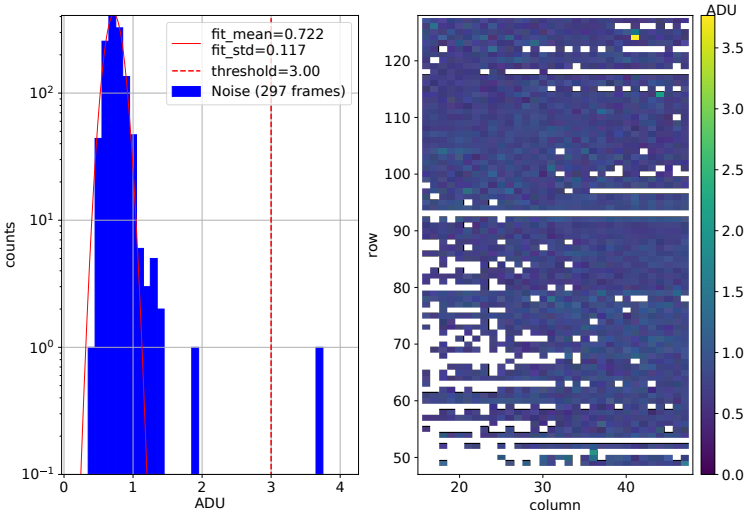


(b) Noise distribution (left) and pixel map (right). The histogram includes one entry per pixel, the standard deviation over all frames.

Figure 4.1: Example pedestal and noise analysis for a Hybrid5 module with the first and last ten Switcher channels connected to the DEPFET matrix.



(a) Pedestal distribution and pixel map. An unusual broad pedestal spread is visible across the module.



(b) Noise map and corresponding histogram. White pixels indicate filtered channels with a mean pedestal below 50 ADU or above 200 ADU, and disconnected pixels.

Figure 4.2: Initial pedestal and noise evaluation of the Hybrid5 module used for the irradiation campaign prior to exposure. The pedestal distribution shows an unusually wide spread across the entire ADC range. Only pixels within the range of 50 ADU to 200 ADU are included in the noise plot and calculation to suppress distortions caused by non-linearities near the ADC boundaries. The last 20 Switcher channels are connected to the DEPFET matrix.

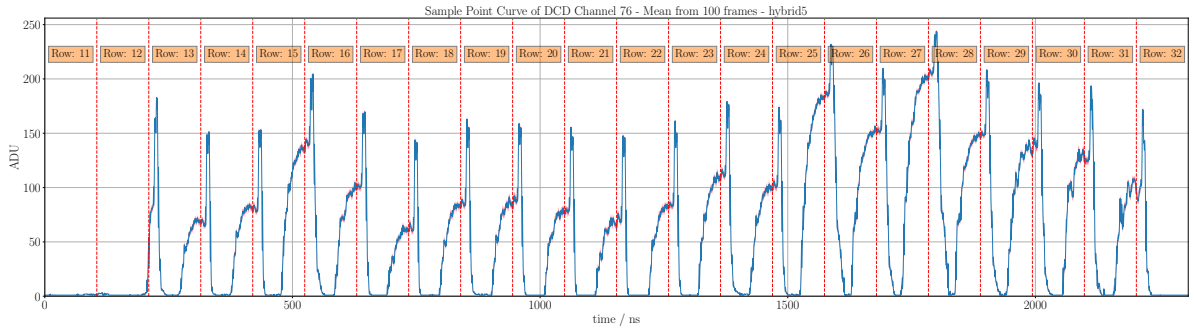


Figure 4.3: Sampling point curve (for DCD channel 76, before irradiation): Sampling point for each row (Switcher channel) is marked by the dashed red line. The current requires a few nanoseconds to rise and stabilize. Sampling occurs just before the internal gate is cleared, when the current reaches a plateau. The clearing mechanism can be identified by the current peak following the sampling point, succeeded by a current drop.

4.1.2 Sampling Point Curve Scan

To identify and confirm the optimal sampling point within the DEPFET readout sequence, a sampling point curve scan is performed. This measurement captures the temporal evolution of the Drain currents, enabling a detailed characterization of the analog signal response as a function of the sampling phase. It serves to determine the most stable point in time, ideally a plateau where the drain current is sampled and converted into a digital value by the DCD.

The scan is realized by systematically shifting the Switcher sequence bit-wise and recording DEPFET frames for each bit shift, while the sampling point of the DCD remains unaltered. After 32 bit shifts, the full time evolution of the drain current is acquired. In fine scan mode, the DHP applies 16 delay increments between each bit step, effectively increasing the temporal resolution by a factor of 16. The resulting drain current for DCD channel 76 is shown in Figure 4.3.

The red dashed lines mark the sampling point. For each row, the drain current requires a short time interval to rise and stabilize at a plateau. This plateau represents the optimal sampling window, just prior to the pixel clearing event. The clearing process is identified by a sharp current peak, succeeded by a current drop. After clearing, the gate is deactivated and the next gate is activated. This timing structure is explained in detail in section 2.3.1 and illustrated in Figure 2.7.

In the presented case, only the last 20 of the 32 Switcher channels are connected. The DCD requires an adjustment period after receiving no current from disconnected channels, which results in a diminished current response for channel 12. This behavior is also evident in the pedestal measurement, as shown in the right plot of Figure 4.2. The pixels at the bottom of the plot tend to have pedestal values close to zero.

A more detailed view of the sampling point curve is provided in Figure 4.4, obtained by calculating the median over all DCD and Switcher channels. A combined function of an exponentioal function followed by a gausian function, is fitted to the data to extract information on e.g. rise time of the current. Approximately 14 ns elapse after the gate activation before a noticeable increase in current is observed by the DCD. After an additional 50 ns, the current plateau reaches 95% of its height. Sampling takes place shortly after, and just before the onset of the clearing-induced current peak.

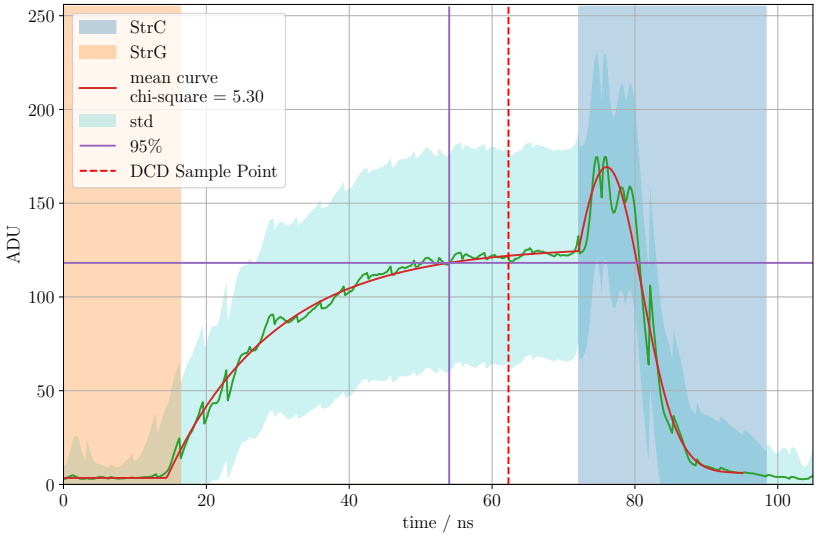


Figure 4.4: Median sample point curve, calculated over all connected DCD and Switcher channels. The dashed red line indicates the sampling point. Orange and blue areas represent `StrG` and `StrC` Switcher signals, respectively. Purple lines indicate the point at which 95% of the maximum current pedestal is reached, immediately before the clearing event.

4.1.3 ADC Curve Scan and DCD Parameter Optimization

The precise and linear digitization of the analog drain current signals from DEPFET pixels is essential for the performance of PXD. To achieve optimal performance, several parameters that affect DCD performance must be tuned using so-called ADC curve scans. These scans measure the response of the ADC as a function of variable input currents and serve to evaluate the quality of each readout channel and determine optimal operating conditions.

DCD Parameters

The transfer characteristics of the ADCs are primarily determined by six parameters. These influence internal current mirrors, memory cell stages, and comparator reference thresholds [42].

The following DCD parameters are set directly in the DCD shift register:

`IPSource` and **`IPSource_middle`** control the reference current used in the comparators and therefore determine the LSB granularity and total dynamic range of the DCD. The analog channels are arranged in a 16×16 pattern. `IPSource` is used for the upper half matrix and `IPSource_middle` for the lower half matrix. This split minimizes voltage drop effects between analog channels.

`IPSource2` sets the working point (WP) of the transconductors in the current memory cells (CMC) and comparators. From design, it is expected to match `IPSource` to maintain symmetry and optimal operation.

IFBPBias biases the feedback path of the transconductors in the Current Memory Cell (CMC) and comparators. Alongside IPSource, it controls the CMCs dynamic range. From design, it should also match IPSource.

The following analog supply voltages are provided by the PXD PS:

RefIn is a voltage reference used throughout the analog blocks. It stabilizes several nodes in the CMC and comparator circuitry.

AmpLow sets the ground potential for the amplifier stages. Shifting AmpLow affects the input characteristic and usable current range of the CMCs.

The optimization algorithm supports both one-dimensional (1D) and two-dimensional (2D) parameter scans. In 1D scans, a single parameter is varied while all others are kept fixed. In 2D scans, two parameters are scanned simultaneously across their combined configuration space. This allows for efficient identification of optimal settings in correlated parameter regimes. Usual two-dimensional scans are IPSource-IPSource2, where the relative offeset between IPSource and IPSource_middle is preserved when varying IPSource and for RefIn-AmpLow. Optimal IPSource_middle and IFBPBias are determined with one-dimensional scans.

Input Current Sources for ADC Scans

Two distinct current sources can be employed for ADC curve acquisition [12], each offering complementary advantages:

DEPFET Current Source The DEPFET matrix itself can be used as a controlled current source by varying the gate-on voltage during readout. By scanning this voltage in discrete steps, a pseudo-linear input current ramp is generated. The primary advantage of this method is its ability to simultaneously measure the transfer curves of ADC channels in a module. This parallelization significantly reduces the measurement time, compared to other methods. However, the relationship between gate voltage and drain current is non-linear ($I_D \propto V_G^2$) [43]. Furthermore, the absolute current values are not known, so only relative non-linearities such as DNL and INL can be reliably extracted. Nevertheless, for parameter optimization, the DEPFET current source is sufficient, and the consistent variation in input current allows robust quality grading across channels [26].

DHE Current Source For precise and calibrated input currents, the DHE current source can be used. It injects a known current directly into selected DCD channels via a programmable high-resolution DAC. A dedicated DAC calibration is required to map output codes to absolute currents (see section 4.1.3). Unlike the DEPFET source, the DHE allows absolute measurements of gain and LSB size. The precision of the DHE current source enables accurate evaluation of INL and DNL and the identification of clamping or bit-stuck conditions. The main limitation is that only one channel is measured at a time, and the DCD must be reconfigured for every channel. However, measuring a single transfer curve is very fast. Consequently, the DHE current source is well suited to measure a few channels over a large parameter space, whereas the DEPFET current source is best suited for measuring all channels over a small parameter space.

DCD Current Source Finally, the DCD contains an internal current source itself, that can be used to record ADC transfer curves. Its resolution is too coarse to investigate fine differential or integral non-linearities. In addition, its extremely slow, compared to the other methods. Consequently, the internal current source is mainly suitable for basic functionality checks and was therefore not used within this thesis.

Metrics for Channel Evaluation

The ADC curves are analyzed using a variety of metrics to quantify their performance. The following criteria are computed for each channel and are most important for scoring of the channels. Additionally, there are a few further criteria, which will not be discussed here. All criteria are detailed in [26, 31, 42].

Gain: A linear fit to the central portion of the ADC curve yields the slope. Low gain reduces resolution, while high gain reduces the available dynamic range.

Offset: The y-intercept of the linear fit defines the offset. Large offsets lead to poor centering of the digitization window.

Differential Non-Linearity (DNL): The deviation in step width for each individual output code from the ideal value (LSB). Values exceeding +1 or −1 LSB signify missing or wide codes. This affects the uniformity of ADC response and contributes to digitization artifacts.

Integral Non-Linearity (INL): The deviation of the actual ADC transfer curve from an ideal linear fit. The peak-to-peak INL is used as a global indicator of curve linearity. High INL degrades the accuracy of charge reconstruction and can distort energy deposition measurements.

Noise: Defined as the standard deviation of ADC outputs at a fixed input current.

Code Range: The range of output codes observed during the transfer curve measurement. Output codes can be limited at the upper and lower end, thus reducing the usable output range.

These metrics are combined using a configurable scoring algorithm. Each channel is graded, and a merit score is calculated for each configuration based on the number of good-scoring channels. The configuration with the highest number of good-scoring channels is defined as the optimal WP and is selected for the operation of the DCD. This process ensures that the modules achieve consistent and reproducible ADC performance across all channels. An example for the resulting figure of merit for a `IPSource-IPSource2` scan is shown in Figure 4.5.

In addition to channel scoring, diagnostic plots of the transfer curve, DNL, INL, and noise are produced for each channel. An example is shown in Figure 4.6 in the appendix. Each input current is sampled multiple times. The resulting output codes are plotted in a 2D-histogram, forming the transfer curve. In this example one can see the most common imperfections pretty clear, where the range is limited, particularly in the lower end, the linearity is only partially given, indicated by the INL and there are a few long codes, where DNL surpasses 1 LSB.

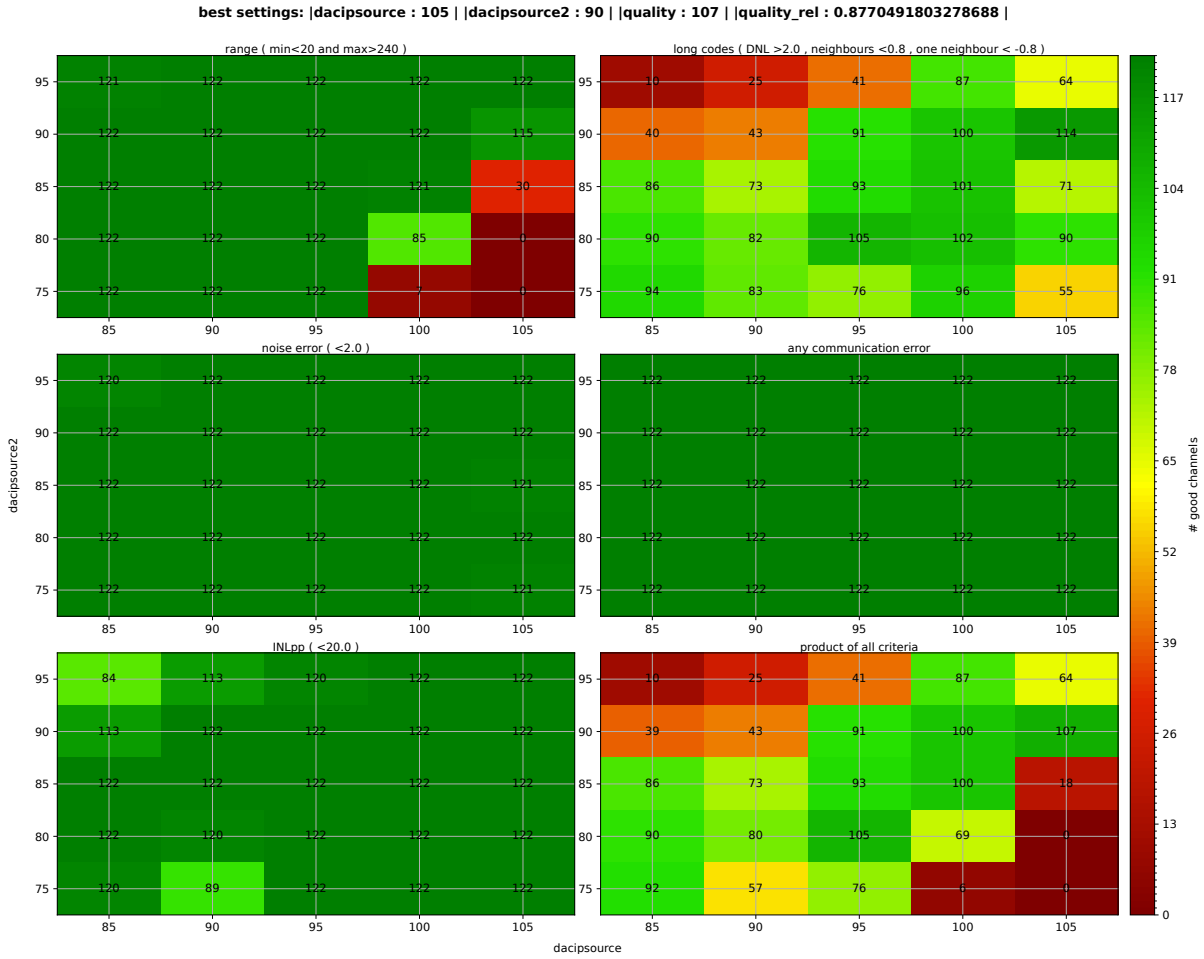
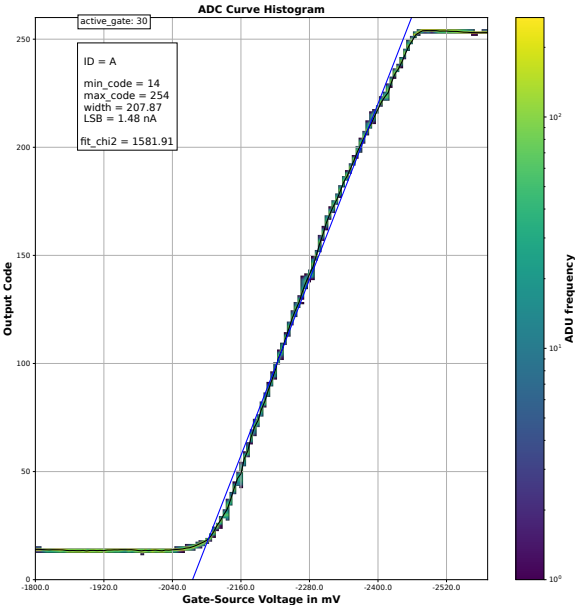
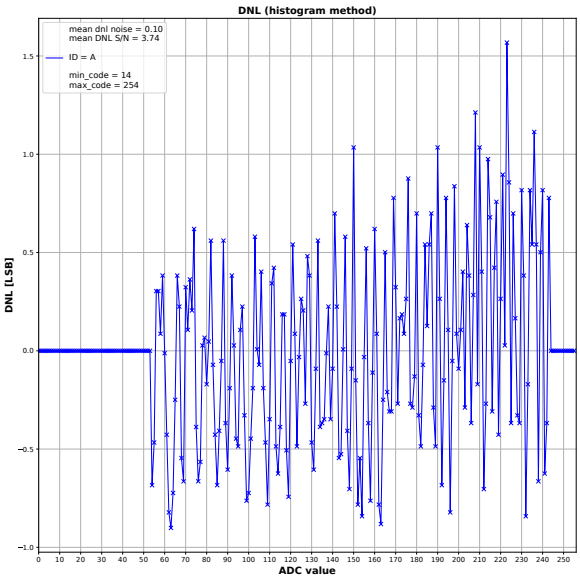


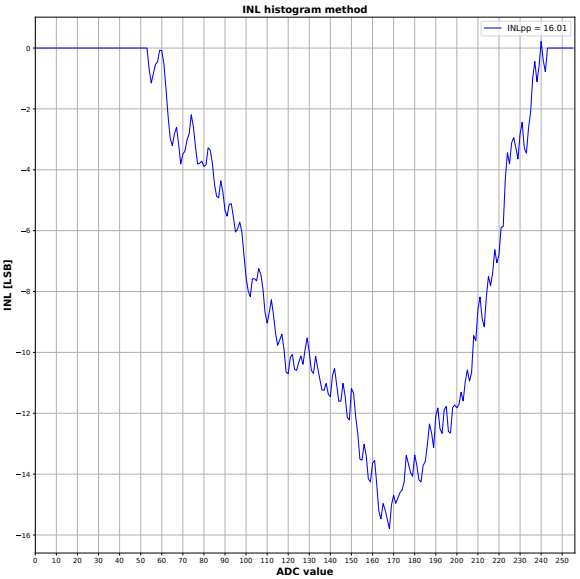
Figure 4.5: Two-dimensional optimization scan of `IPSource` and `IPSource2`, using the DEPFET current source. Every tile represents an unique parameter combination. The sub-panels display the number of good channels according to different evaluation criteria: total range, long-code suppression (DNL), noise error, communication errors, and INL. The bottom-right panel summarizes all criteria into a single figure of merit. The maximum number of good channels (107 out of 122) is achieved at `IPSource` = 105 and `IPSource2` = 90.



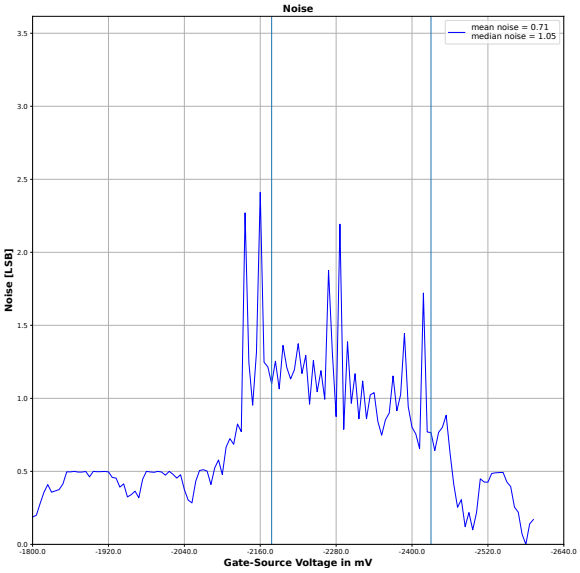
(a) ADC transfer curve (histogram created from multiple samplings per gate voltage)



(b) DNL per output code (ADU) in units of LSB



(c) INL per output code (ADU) in units of LSB



(d) Noise as a function of gate voltage in units of LSB

Figure 4.6: Example diagnostic plots for a single DCD channel: transfer curve, DNL, INL, and noise level. The transfer curve was recorded using the DEPFET current source.

DHE Current Source Calibration

In order to assign a current to each DAC code of the DHE current source, it must be calibrated. The DHE current gets injected into the DCD by setting the `MON2DHH` jumper on the Hybrid5 board. Connecting a SMU to this jumper enables direct measurement of the DHE current source and its calibration.

The DHE's DAC current source is swept over the usable code range. For each code c, the current is measured multiple times and averaged to obtain a transfer curve. A linear function, $I(c) = I_0 + k\,c$, is fitted to the data points to extract the offset I_0 and the effective LSB size k (in A/c). For the DHE used in this work, the calibrated transfer curve, shown in Figure 4.7 was measured. For high codes, the curve is no longer linear and was therefore excluded from the fit. However, this has no effect on the ADC curve scans, as only the lowest section of the DACs range is required for these.

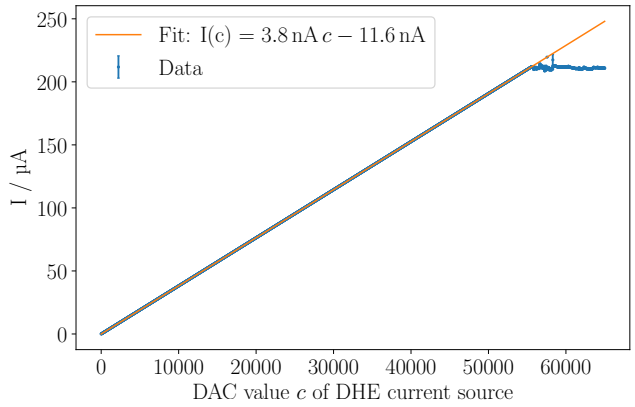


Figure 4.7: DAC transfer curve of the DHE used in this thesis. $I(c) = (3.8150000 \pm 0.0000003)\,\text{nA} \cdot c - (11.556 \pm 0.009)\,\text{nA}$

The fitted mapping $I(c)$ is used in ADC curve scans to convert DAC codes into absolute input currents. This enables absolute determinations of gain and LSB size.

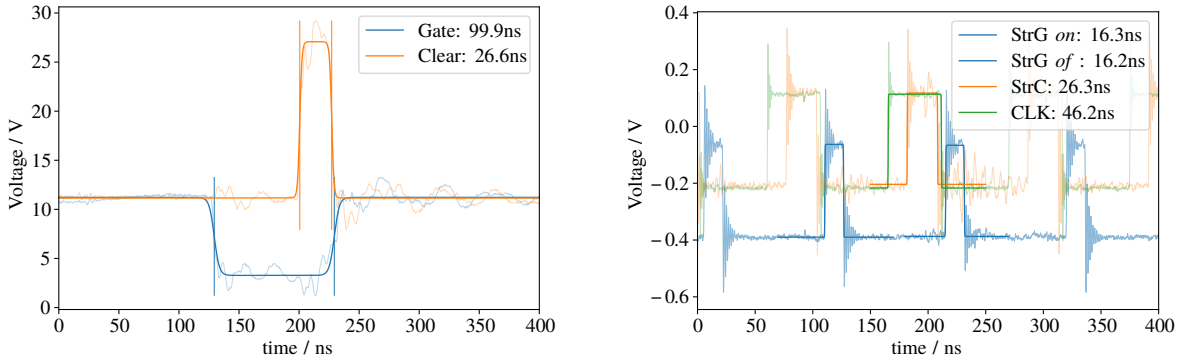
4.1.4 Oscilloscope-Based Switcher Signal Measurements

To capture and analyze the temporal structure of the Switcher signals, oscilloscopes with at least six input channels are required. Four channels are used to record the digital control signals `SerIn`, `CLK`, `StrC`, and `StrG`, while the remaining two channels are dedicated to the analog outputs of a pair of gate and clear channels.

As most oscilloscopes offer a maximum of four input channels, synchronization between two devices becomes necessary. One oscilloscope must generate a trigger signal for the other to ensure temporal alignment of the recorded signal waveforms. For this purpose, either the gate or the clear signal is selected as the trigger source. The digital steering signals are unsuitable for triggering, as they are transmitted continuously, in contrast to the analog signals which occur only once per readout cycle per channel, as described in section 2.3.1.

To preserve signal integrity during the measurement of the digital steering signals, differential probes with active amplification elements at the probe tip are employed. These are connected to the Hybrid5 via short cables, as described in section 3.1.

For an accurate representation of the temporal evolution of the measured signals, smoothed rectangular functions with sigmoid-shaped rising and falling edges are fitted to the data, accounting for the finite rise and fall times. The measured data, along with the fitted functions for both digital and analog signals, are shown in Figure 4.8. The signal duration is defined as the interval between the midpoints of the rising and falling sigmoid functions, which are indicated by vertical lines in the plots.

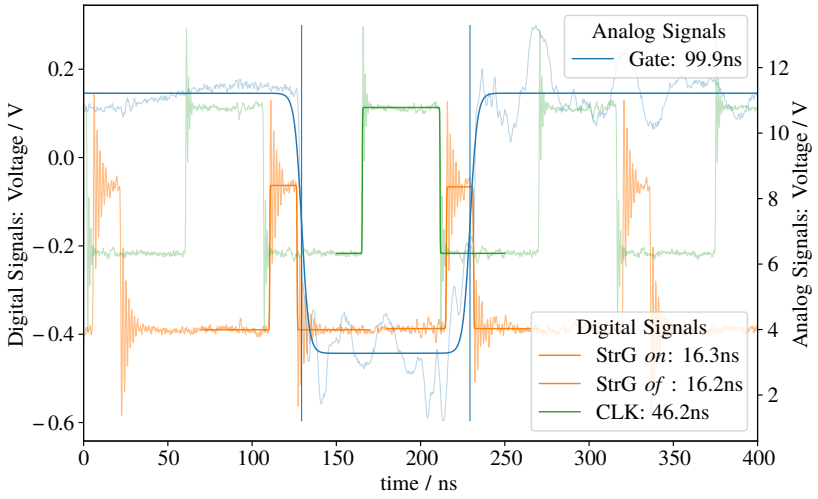


(a) Analog outputs of a gate and clear channel pair.

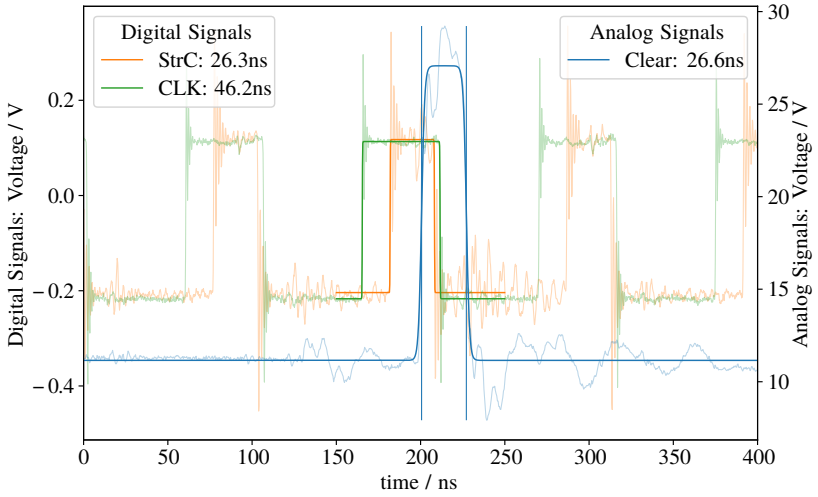
(b) Digital steering signals `StrG`, `StrC`, and `CLK`.

Figure 4.8: Measured waveforms and fitted functions. The gate and clear signals exhibit finite rise and fall times, while the digital signals rise and fall almost immediately.

In addition, the timing between digital and analog signals can be extracted from the measurements. The plots in Figure 4.9 show the delay between the `StrC` signal and the analog clear pulse, and between the `StrG` signal and the analog gate pulse, respectively. The observed delay arises from two effects. Firstly, there is a translation delay within the Switcher ASIC between the digital steering signals and the analog outputs. Secondly, minor timing offsets may result from synchronization inaccuracies between the two oscilloscopes.



(a) Delay between `StrG` and analog gate signal.



(b) Delay between `StrC` and analog clear signal.

Figure 4.9: Temporal offsets between digital steering signals and analog outputs for gate and clear channels. Delays arise from internal ASIC translation time and inter-device synchronization.

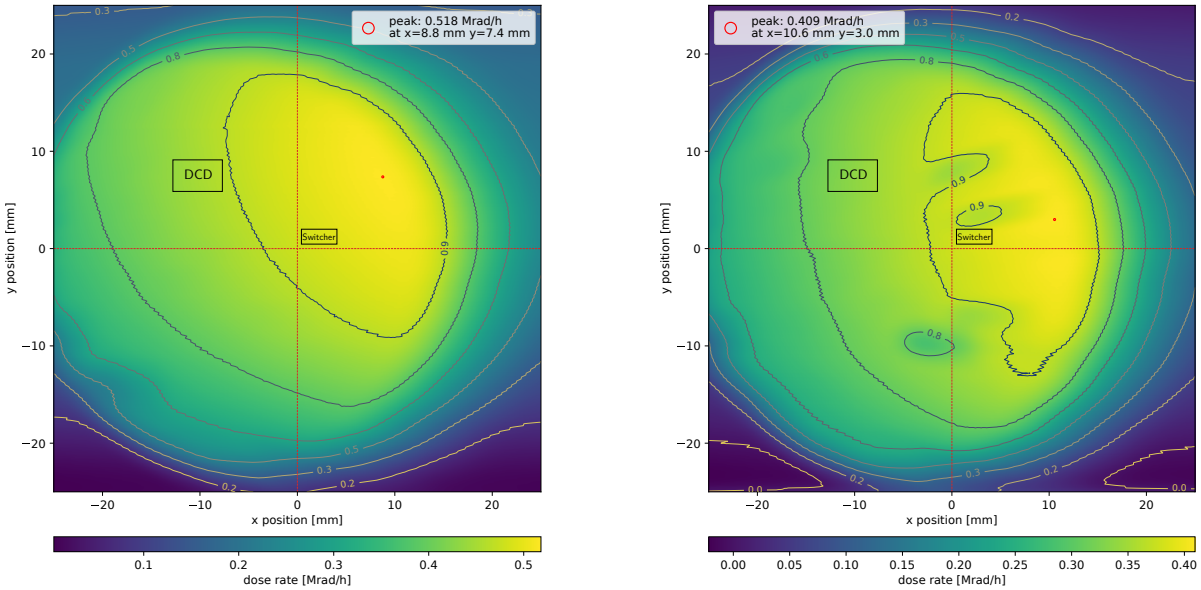
4.2 X-Ray Tube Calibration and Campaign Planning

Prior to and subsequent to each irradiation campaign, the X-ray beam is calibrated to quantify the absolute dose rate and to monitor changes in the beam profile over time. The procedure follows the mapping described in section 3.2, using a photodiode, monitored by a SMU, in the target plane.

The recorded dose-rate distributions are shown in Figure 4.10 and Figure 4.11. During irradiation, dust particles accumulated on the X-ray filter, leading to localized low-intensity regions in the post-irradiation dose-rate maps. The origin of these particles is unclear, but the repeatedly actuated shutter mechanism is a potential source. Cleaning the filter prior to each irradiation campaign was sufficient to eliminate the observed intensity drops, as seen in Figure 4.10(b) and 4.11(a).

Before the Switcher irradiation, the peak dose rate was 0.518 Mrad/h. Afterwards, it decreased to 0.409 Mrad/h. For the DCD campaign, the peak dropped from 0.483 Mrad/h to 0.463 Mrad/h. These variations confirm the necessity of both pre- and post-irradiation calibrations to accurately quantify the received dose and to monitor profile changes over time.

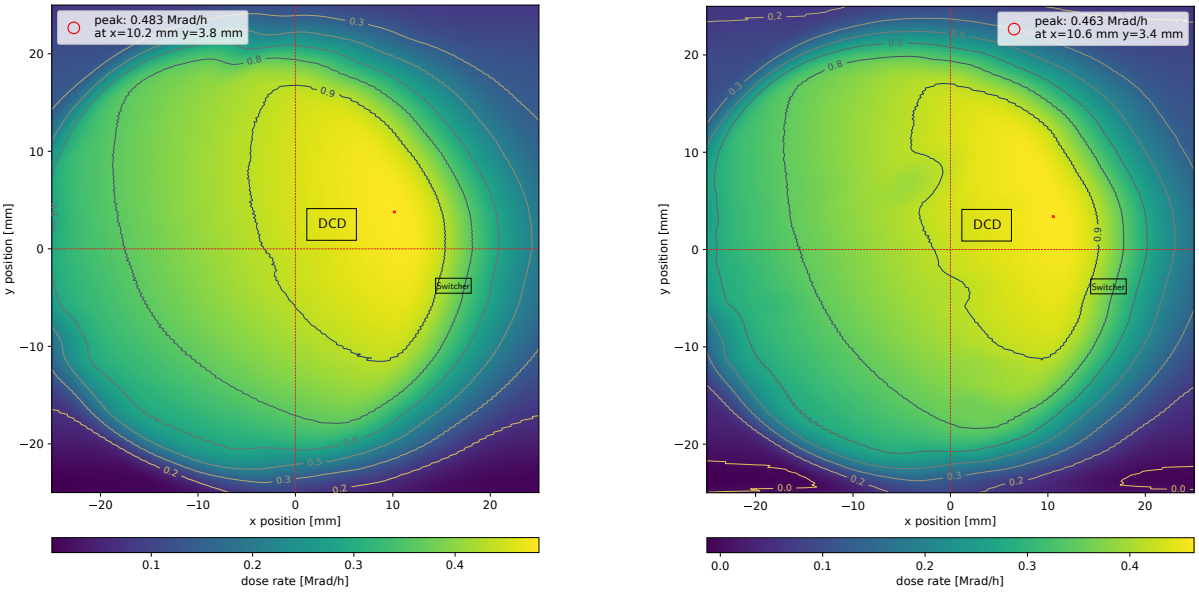
Target Placement and Alignment The ASICs are positioned to maximize dose homogeneity while maintaining precise alignment with the laser crosshair. Thus, the Hybrid5 was placed such that the ASIC under test lies in the upper-right quadrant of the laser crosshairs, as shown in Figure 4.10 and 4.11.



(a) X-ray tube dose rate before the campaign, peak 0.518 Mrad/h

(b) X-ray tube dose rate after the campaign, peak 0.409 Mrad/h

Figure 4.10: Dose rate distributions of the X-ray beam from the Switcher irradiation campaign.



(a) X-ray tube dose rate before the campaign, peak 0.483 Mrad/h

(b) X-ray tube dose rate after the campaign, peak 0.463 Mrad/h

Figure 4.11: Dose rate distributions of the X-ray beam from the DCD irradiation campaign.

4.2.1 Campaign Planning

Based on the pre-irradiation calibration, a dose rate of 0.48 Mrad/h was assumed for the Switcher campaign. The irradiation proceeded in exponentially increasing steps designed to accumulate a TID of 36 Mrad, the stated radiation hardness of the Switcher [41]. Table 4.1 lists the planned stepwise doses and the cumulative TID based on this dose-rate assumption.

For the DCD, the planned TID goal was 20 Mrad, based on its minimum required radiation hardness [25], at an assumed dose rate of 0.45 Mrad/h. However, a planning error led to a maximum TID of 10 Mrad. The corresponding stepwise and cumulative doses are documented in Table 4.2.

Effective TID in the Electronics Layer Both, the Switcher and DCD ASIC are flip-chipped to a silicon carrier board and glued onto the Hybrid5 board such that the silicon substrate faces upward. As a result, radiation is attenuated by a 300 µm thick silicon layer before reaching the active circuitry [36]. The attenuation follows the Beer-Lambert law,

$$I = I_0 \, e^{-\mu(\nu)\, d} \, ,$$

where I_0 is the incident intensity, d is the material thickness, and $\mu(\nu)$ is the wavelength-dependent linear attenuation coefficient [33]. This attenuation is taken into account to calculate the effective TID in the Electronics Layer (EL). The average of the pre- and post-irradiation calibration measurements is used as the basis (I_0) for this calculation. The final TID values in the EL after each step are shown as well in Tables 4.1 and 4.2. These values are used throughout the subsequent discussion and plots.

Table 4.1: Planned irradiation steps for the Switcher campaign. Listed are dose values per step, cumulative TID in the Electronics Layer (EL), and unattenuated X-ray tube TID.

Irradiation step	0	1	2	3	4	5	6	7
Dose/step (EL) / MRd	0	0.00024	0.00036	0.00060	0.0010	0.0017	0.0027	0.0046
Cum. TID (EL) / MRd	0	0.00024	0.00060	0.0012	0.0022	0.0039	0.0066	0.011
Tube TID / MRd	0	0.001	0.003	0.005	0.01	0.02	0.03	0.05
Irradiation step	8	9	10	11	12	13	14	15
Dose/step (EL) / MRd	0.0075	0.012	0.020	0.034	0.055	0.083	0.12	0.16
Cum. TID (EL) / MRd	0.019	0.031	0.051	0.085	0.14	0.22	0.34	0.50
Tube TID / MRd	0.08	0.14	0.2	0.4	0.6	1.0	1.50	2.20
Irradiation step	16	17	18	19	20	21	22	23
Dose/step (EL) / MRd	0.22	0.31	0.44	0.61	0.85	1.19	1.66	2.31
Cum. TID (EL) / MRd	0.72	1.04	1.47	2.08	2.93	4.12	5.78	8.09
Tube TID / MRd	3.20	4.60	6.50	9.20	13.00	18.20	25.60	35.80

Table 4.2: Planned irradiation steps for the DCD campaign. Listed are dose values per step, cumulative TID in the Electronics Layer (EL), and unattenuated X-ray tube TID.

Irradiation step	0	1	2	3	4	5	6	7	8
Dose/step (EL) / MRd	0	0.00028	0.00045	0.00077	0.0013	0.0021	0.0034	0.0056	0.0092
Cum. TID (EL) / MRd	0	0.00028	0.00073	0.0015	0.0028	0.0048	0.0082	0.014	0.023
Tube TID / MRd	0	0.001	0.003	0.005	0.01	0.017	0.029	0.05	0.083
Irradiation step	9	10	11	12	13	14	15	16	17
Dose/step (EL) / MRd	0.015	0.025	0.041	0.068	0.11	0.14	0.14	0.14	0.14
Cum. TID (EL) / MRd	0.038	0.063	0.10	0.17	0.29	0.42	0.56	0.70	0.84
Tube TID / MRd	0.14	0.23	0.38	0.62	1.02	1.52	2.02	2.52	3.02
Irradiation step	18	19	20	21	22	23	24	25	26
Dose/step (EL) / MRd	0.14	0.14	0.15	0.18	0.21	0.25	0.29	0.34	0.41
Cum. TID (EL) / MRd	0.98	1.12	1.27	1.45	1.66	1.90	2.19	2.54	2.94
Tube TID / MRd	3.52	4.02	4.56	5.19	5.94	6.82	7.87	9.10	10.55

4.3 Switcher Irradiation Campaign

Before starting the irradiation campaign, the Hybrid5 module was fully configured by performing a series of tests. Most importantly, the pedestal values were centered by adjusting `VNSubIn`, and the DCD was calibrated by scanning all relevant parameters listed in section 4.1.3. In addition, a delay scan was performed to ensure proper communication between the DCD and DHP, and a high-speed link scan was carried out to verify a stable connection between the DHE and DHP. Further details on these procedures can be found in [12].

The Switcher ASIC was irradiated in 23 steps to a cumulative TID of 35.8 Mrad, corresponding to an effective dose of 8.09 Mrad in the electronics layer after attenuation in the silicon substrate. Throughout the irradiation, the Hybrid5 module remained powered, with both the Switcher and the DCD supplied, and the DEPFET matrix biased. Except for a short downtime between the irradiation steps to power cycle the Hybrid5 to make sure the system is configured correctly.

Each irradiation step was followed by one hour of annealing, after which the following measurement sequence was performed:

- Pedestal measurement (duration: a few seconds)
- Oscilloscope-based Switcher signal measurement (duration: a few seconds)
- Sampling point curve scan, fine scan (duration: ~25 min)
- ADC curve scan, using the DHE current source to record transfer curves for 15 individual DCD channels and 5×5 `IPSource`–`IPSource2` configurations (step size = 5; `IPSource` range = 85-105; `IPSource2` range = 75-95) (duration: ~25 min)

After each sequence, an additional 20 min annealing period was applied before proceeding to the next irradiation step. Additionally, pedestal values and Switcher signals were continuously monitored at a rate of a few seconds throughout both the irradiation and annealing periods.

4.3.1 ADC Curves and DCD Optimization

The ADC transfer curves remained highly consistent throughout the campaign, without any significant TID dependent changes. This stability is expected, as the quality of the ADC curves is primarily determined by the DCD performance and its operating conditions, which remained stable due to the shielding from direct irradiation and controlled thermal conditions. Minor deviations observed in the measurements are attributable to statistical fluctuations.

An example figure of merit from the measurement after the last irradiation step is shown in Figure 4.5. Given the absence of significant deviations, this single example is sufficient for illustration. The stability is further demonstrated in Figure 4.12, where the most relevant parameters are plotted as curves of accumulated TID. The WP quality (defined as the number of *good* channels at a given WP), the median INL, the median LSB, and the optimal WP settings (`IPSource` and `IPSource2`) all exhibit only random fluctuations without any recognizable trend.

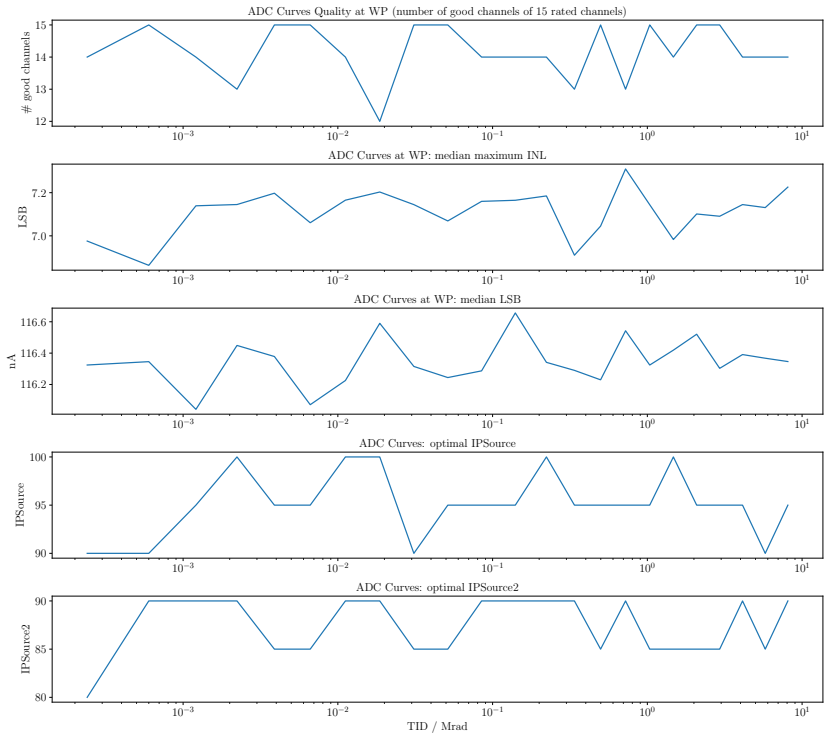


Figure 4.12: Development of key ADC curve characteristics as functions of TID, shown on a logarithmic scale. No significant changes are observed; only statistical fluctuations are visible.

4.3.2 Switcher Signals

A comparable stability was observed for the Switcher signals. Both the signal length and the relative timing between the individual signals remained constant. Figure 4.13 shows the width of the gate and clear pulses with increasing TID, while the residual metrics (temporal delays, digital signal length) can be found in the appendix in Figure 6.1. The temporal delay is defined as the timing between the rising edge of the clear/gate signal and its corresponding `StrC`/`StrG` steering signal. The post-irradiation waveforms are indistinguishable from the pre-irradiation ones shown in Figures 4.8 and 4.9.

In previous Switcher irradiation studies, a broadening of the clear signal was observed [21, 25], leading to an overshoot of the clear signal beyond the gate signal. This behavior was also observed in the preceding test campaign with H5020. The clear signal broadened 2 ns over the entire TID range, while the gate width stayed almost unchanged, as shown in Figure 4.14. However, in that campaign, the clear signal was already broadened from the start (see Figure 4.15), as the Switcher had previously been irradiated with electrons at MAMI in a separate study. Additionally, the temporal delays between digital and analog, and digital signal length can be seen in Figure 6.2.

It is important to note that the earlier results were obtained with the older Switcher version SwitcherB18V2.1, whereas the present campaign used the new SwitcherB18V2.3. The absence of clear signal broadening in the current study provides strong evidence that the newly implemented radiation-hardening measures are effective in preventing this type of degradation.

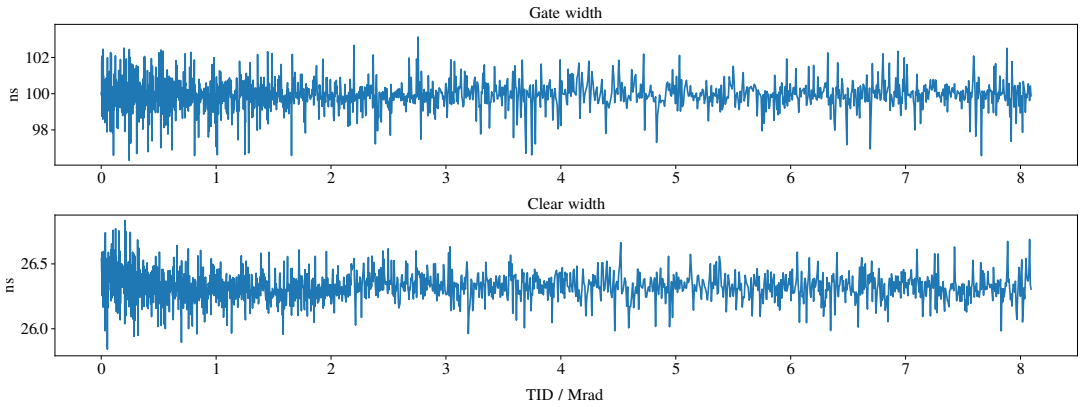


Figure 4.13: Measured gate and clear width with increasing TID. Both parameters remain constant with minor statistical fluctuations, indicating no measurable TID-induced degradation in the Switcher performance.

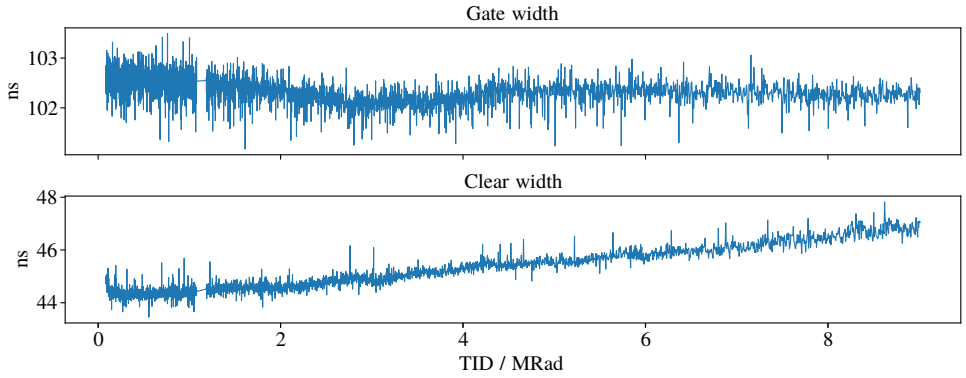


Figure 4.14: Measured gate and clear width with increasing TID for the preceding test campaign with Hybrid5 H5020 and SwitcherB18V2.1. A broadening of the clear signal is clearly visible.

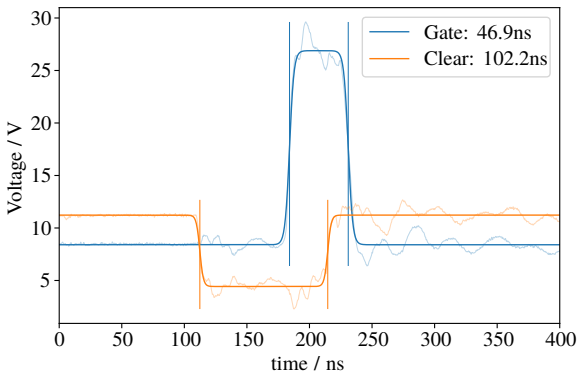


Figure 4.15: Analog Switcher signals before the test campaign with H5020. The clear signal is already broadened and surpasses the gate signal.

4.3.3 Pedestals

The primary objective of this irradiation campaign was to determine whether irradiation of the Switcher has any affect on pedestal noise. During irradiation up to a total dose of 10.5 Mrad, no significant change in pedestal noise was observed. Figure 4.16 shows the pedestal noise during irradiation, together with the mean pedestal value, assessed from the continuous measurements during irradiation. The latter clearly decreases with increasing TID. Once the median pedestal value drops below 80 ADU, the pedestals are automatically shifted upward by a `VNSubIn` adjustment, as described in section 4.1.1. The dotted red lines indicate the start of a new irradiation step. For the last step, `VNSubIn` was configured manually slightly different, leading to a higher median pedestal value. However, this has no effect on other metrics.

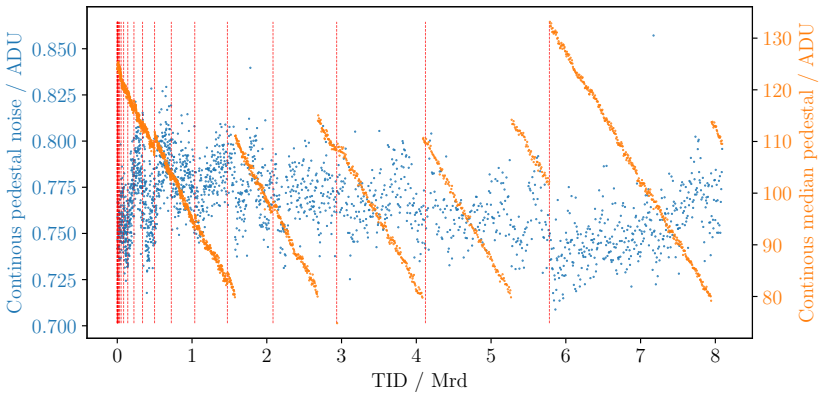


Figure 4.16: Continuous measurements of pedestal noise (blue, left y-axis) and median pedestal value (orange, right y-axis) as a function of TID during the Switcher irradiation campaign. The dotted red lines indicate the start of each new irradiation step.

The step-wise measurements taken one hour after each irradiation step (Figure 4.17) show the same overall behavior as the continuous measurements. However, the linear decrease in pedestal value is only apparent up to a TID of approximately 1.5 Mrad, after which the automatic `VNSubIn` adjustment is first applied. Beyond this point, the irradiation step size becomes large enough that consecutive measurements have different `VNSubIn` settings, preventing direct comparison of median pedestal values. Nevertheless, in both the continuous and step-wise data, the pedestal noise remains constant within minor fluctuations, indicating no TID induced noise degradation.

A possible origin of the observed linear decline in the pedestal is discussed in detail in section 4.3.5.

In between irradiation steps, during the annealing period, a slow recovery of the pedestal value is observed, as shown in Figure 4.18. This effect proceeds slower than the pedestal decrease observed during irradiation and therefore cannot compensate for it. A longer annealing time would further benefit the restoration of the pedestal value and might come close to full recovery. However, full annealing to the state before irradiation is not possible.

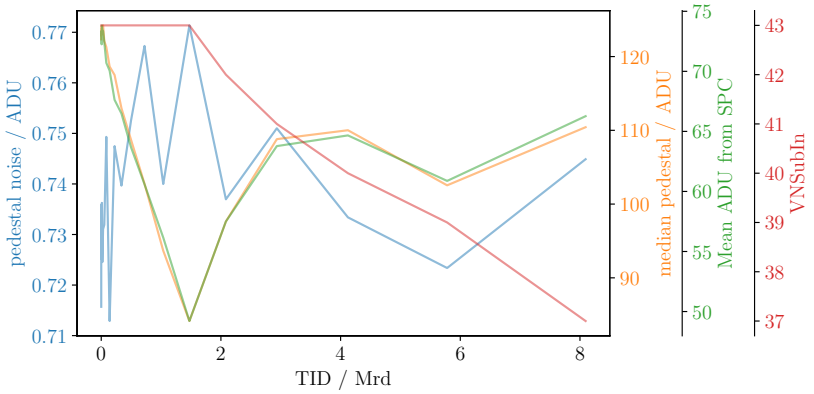


Figure 4.17: Pedestal noise (blue, left y-axis), median pedestal value (orange, first right y-axis), and mean ADU from the sampling point curve (green, second right y-axis) as a function of TID for the step-wise measurements taken one hour after each irradiation step. The `VNSubIn` setting for each measurement is shown in red (third right y-axis). Each curve has an independent y-scale.

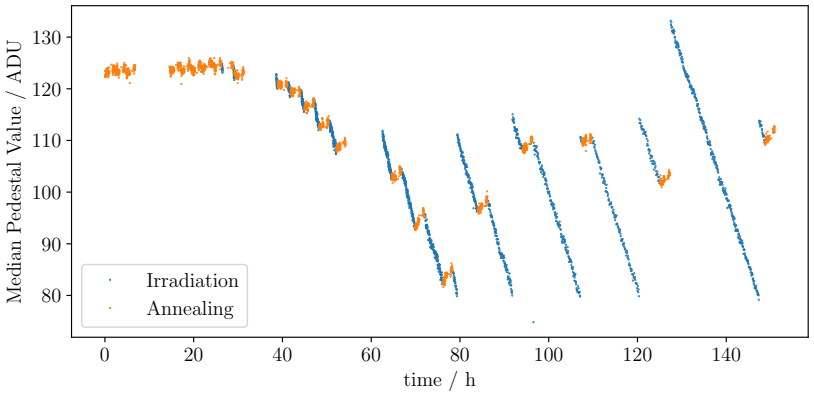


Figure 4.18: Mean Pedestal values during irradiation and annealing period. During irradiation, a linear decrease in median pedestal value is observed. During the annealing period, pedestal values increase again. The time gaps are due to pausing times during night.

4.3.4 Sampling Point Curve

The sampling point curves remain largely unchanged over the course of the irradiation campaign, exhibiting only minor deviations. For each row, the drain current begins to rise a few ns after the corresponding gate is activated. Once the current saturates, the clear pulse produces a sharp current peak followed by a drop. In some DCD channels, the current does not return fully to 0 ADU (Figure 4.19), an effect unrelated to TID and instead caused by the limited dynamic range of those channels, as represented by the example in Figure 4.6.

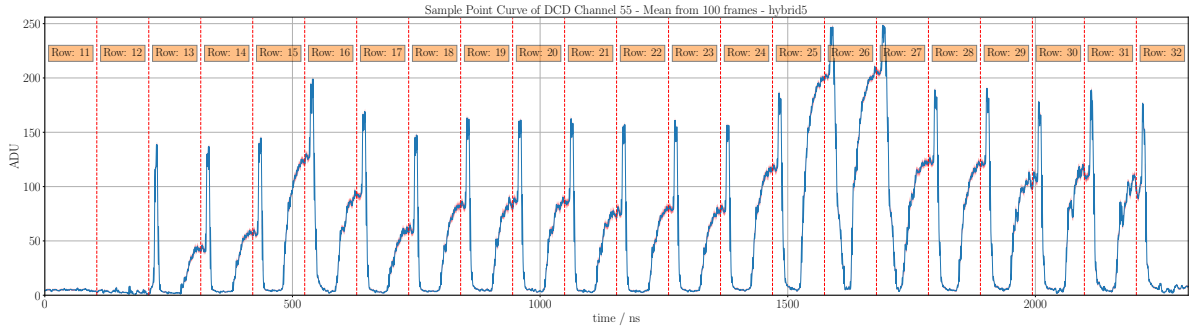


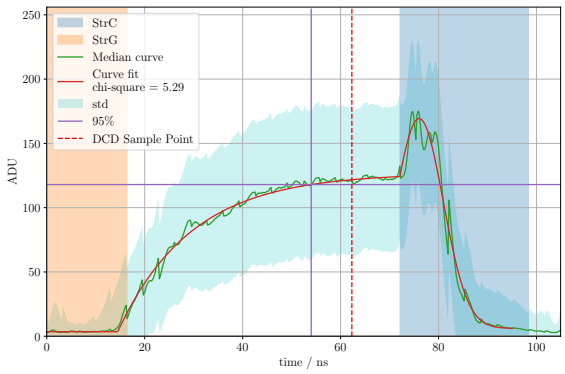
Figure 4.19: Sampling point curve for column 55, showing the drain current development in the connected and a few adjacent rows (Switcher channels).

The only noticeable TID dependent change is a slight downward shift of the sampling point curve with increasing dose. This is evident when comparing the mean sampling point curve of the first and 18th (1.47 Mrad) irradiation step in Figure 4.20. To quantify this effect, the mean ADU value was calculated over all connected Switcher channels (rows 12–31) and all connected DCD channels. The resulting trend is shown in Figure 4.17. Up to a TID of 1.5 Mrad, the mean ADU value decreases linearly by approximately 24 ADU. Beyond this dose, regular `VNSubIn` adjustments to compensate for the pedestal shift break the linear trend.

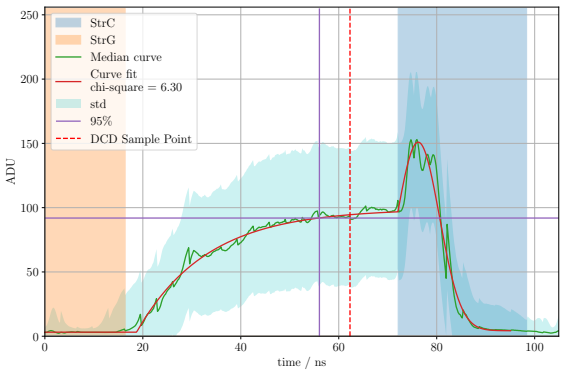
The mean ADU curve extracted from the sampling point data closely follows the mean pedestal curve, though with a slightly narrower range. This behavior is expected, as the pedestal values shift accordingly and are derived from the plateau region of the sampling point curve prior to the clear pulse. A general vertical shift of the sampling point curve, which represents the drain current as measured by the DCD, necessarily leads to a corresponding change in the pedestal value. However, because the pedestal is sampled only at the plateau, while the mean ADU value reflects the entire temporal development of the current, the decrease in the pedestal value is more pronounced than the decrease in the mean ADU. An important observation is that the limited dynamic range of the DCD clips the drain current at 0 ADU, even though the actual drain current likely decreases further. Consequently, the observed mean ADU shift probably overestimates the true shift of the drain current.

4.3.5 Source Current Decrease

From the preceding analyses, changes in the Switcher signals can be excluded as the origin of the observed pedestal and sampling-point curve shifts. Among the remaining monitored quantities, only



(a) Mean sampling point curve before the first irradiation step.



(b) Mean sampling point curve after the 18th irradiation step (1.47 Mrad).

Figure 4.20: Comparison of the mean sampling point curves from before the irradiation and after the 18th irradiation step. A small but noticeable downward shift is visible after irradiation, consistent with the trend in Figure 4.17.

the source current shows a potential correlation with these effects. However, during the Switcher irradiation campaign, the resolution of the source current measurement was insufficient to make a definitive statement about its variation.

To improve the measurement precision, a digital multimeter was connected in-line between the power breakout board and the Hybrid5 source-voltage supply cable during the subsequent DCD irradiation campaign. This setup enabled high-resolution monitoring of the source current. The measurements revealed that the source current also decreases during the DCD irradiation campaign. Applying a linear fit to the source current evolution for both campaigns yields comparable slopes. However, the fit for the Switcher campaign data must be interpreted with caution due to the extremely coarse resolution, where the recorded current value alternated only between two discrete levels. Both trends are shown in Figure 4.21. For both the Switcher and DCD irradiations, such a decrease was not anticipated.

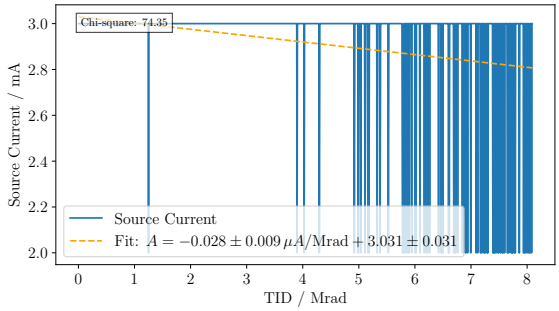
TID damage to the DEPFET matrix leads to a threshold voltage shift and therefore a shift in the source current [36]. This suggests that, despite the brass shielding, the matrix still received a non-negligible radiation dose. Possibly through stray radiation from the brass shielding or X-ray chamber.

The shielding attenuates the incident X-ray beam by a factor of approximately 10^{10} according to the Beer-Lambert law,

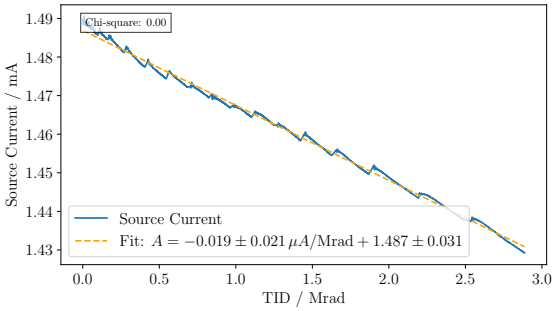
$$I(d) = I_0 e^{-\mu d}$$

where d is the brass shield thickness (0.5 cm) and μ is the attenuation coefficient. Assuming a 1:2 zinc-copper composition, the attenuation coefficient at 40 keV is $\mu = 41.9\,\mathrm{cm}^{-1}$ [44]. Therefore, any residual irradiation of the matrix may originate from stray X-rays scattered at surrounding structures such as PCB[2] layers and ASIC surfaces, from the cutouts in the brass shielding, or from reflections within the X-ray chamber. A dedicated test measurement demonstrated that the shielding was effective within the measurement accuracy, although the PCB and ASICs were not present during that test.

[2] Printed Circuit Board (PCB)



(a) Source current as a function of accumulated TID during the Switcher irradiation campaign. The measurement resolution was limited to two discrete current levels. The linear fit indicates a weak negative slope, but has a large χ^2 due to the coarse resolution. An uncertainty of 1 µA was assumed for each data point.



(b) Source current as a function of accumulated TID during the DCD irradiation campaign, measured with a high-resolution external multimeter. The linear fit reveals a negative slope, consistent in magnitude with the Switcher campaign results, but determined with significantly better resolution.An uncertainty of 1 nA was assumed for each data point.

Figure 4.21: Comparison of source current behavior during the Switcher (left) and DCD (right) irradiation campaigns. In both cases, a small but consistent decrease in source current is observed with increasing TID. The Switcher data suffer from low measurement resolution, while the DCD data benefit from high-resolution monitoring via an external multimeter.

To quantify the correlation between pedestal value and source current, the analysis was restricted to measurements up to approximately 1.4 Mrad, before the first automatic `VNSubIn` adjustment. In this range, the median pedestal value decreases by 36 ADU. Using the measured ADC conversion factor of 116 nA/ADU (Figure 4.12), this corresponds to a reduction in the average drain current of 4.35 µA. Over the same period, the fitted source current decreases by only (0.04 ± 0.25) µA (Figure 4.21). Since the source current is averaged over time and the Hybrid5 employs a 192-row sequence while only 20 rows are connected, the source current must be scaled by a factor of approximately 10, yielding (0.39 ± 0.25) µA when considering only the connected rows. This value remains about an order of magnitude smaller than the current change inferred from the pedestal measurements.

A likely explanation is provided by a look at the sampling point curves, which represent the full temporal evolution of the drain current rather than the single instantaneous value captured in the pedestal measurement. Since the drain current continues to decrease between pedestal sampling instances, pedestal derived changes systematically overestimate the actual current variation. This behavior was already evident from the comparison of the mean ADU change in the sampling point curves (24 ADU) with the pedestal derived shift. The corresponding current change from the sampling point data amounts to 2.79 µA, which lies closer to, but still exceeds, the measured source current decrease. The remaining discrepancy can be explained by considering the limited dynamic range of the DCD: the drain current is clipped at zero ADU, while it likely continues to decrease further. As a result, the observed mean ADU shift still overestimates the true current drop. A correction for this overestimation might bring the current decrease extracted from the sampling point curves and the source current measurement into agreement.

4.4 DCD Irradiation Campaign

The irradiation procedure for the DCD was the same as for the Switcher. The device was irradiated up to a total dose of 10.55 Mrad, corresponding to 2.94 Mrad in the electronics layer. This exposure was performed in 26 irradiation steps, as listed in Table 4.2. During the entire campaign the Hybrid5 remained powered, except for a short period before each irradiation step where the system was power-cycled to ensure correct configuration.

A preliminary test campaign had indicated a shift of the optimal WP of the DCD under irradiation. Therefore, after one hour of annealing following each irradiation step, the following measurement sequence was carried out:

- Pedestal measurement at the initial WP (duration: a few seconds).
- Pedestal measurement at the current WP (duration: a few seconds).
- ADC curve scan over 15 channels covering an extended 11×7 `IPSource` – `IPSource2` parameter space (step size = 5; `IPSource` range = 80 – 130, `IPSource2` range = 70 – 100) using the DHE current source (duration: ~45 min).
- ADC curve scan at the initial WP over all channels using the DEPFET current source (duration: ~7 min).
- ADC curve scan around the current WP for 3×3 `IPSource-IPSource2` configurations (`IPSource/IPSource2` = current WP ±5) using the DEPFET current source (duration: ~60 min).

The current WP was determined from the 3×3 scan around the previous setting. If a shift of the optimal WP was observed, the `IPSource` and `IPSource2` values were adjusted and defined as the current WP for the subsequent irradiation step.

In addition to this defined sequence, pedestal values were continuously monitored during both irradiation and annealing periods.

Between the measurement sequence and the subsequent irradiation step, an additional 20 min of annealing time was provided.

4.4.1 ADC Curve Scan

For the following analysis, the DCD metrics are defined as the mean value over all channels.

ADC Curves at the Initial Working Point

Up to an accumulated dose of about 0.5 Mrad, no significant change was observed in the performance of the DCD. Between 0.5 Mrad and 1.5 Mrad, however, several key parameters changed rapidly (see Figure 4.22). The ADC noise and INL increased steeply, while the LSB width decreased, corresponding to an increased slope of the transfer curve or gain. Simultaneously, the minimum output code shifted to higher values, limiting the dynamic range. Beyond this dose, the effects saturated and no further significant degradation was observed.

In contrast to the other measurements, the INL exhibited a discrete jump of approximately 4 ADU at around 1 Mrad. Before and after this jump the INL fluctuated around 12.5 and 16.5 ADU.

Although the saturation behavior of the minimum output code is less obvious, the trend is compatible with saturation once a possible outlier at the second-to-last measurement point is disregarded.

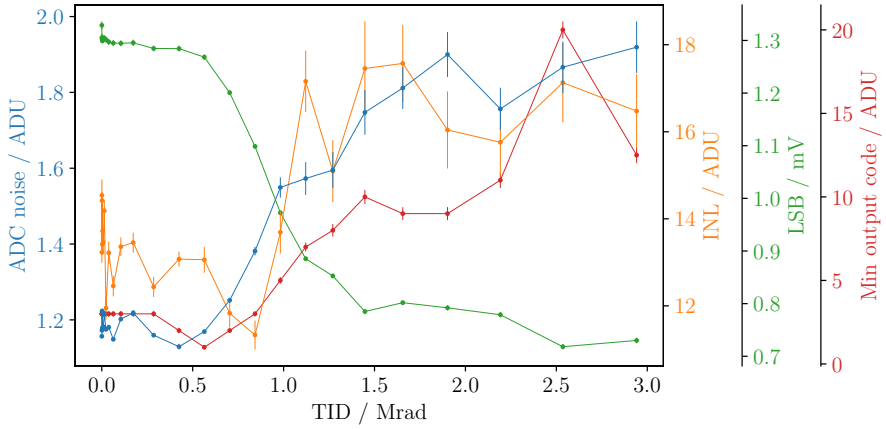


Figure 4.22: Measured evolution of ADC metrics with accumulated TID. Shown are the ADC noise (blue), INL (orange), LSB width (green), and minimum output code (red). Each curve is scaled to its own vertical axis. A steep deterioration is visible between 0.5 Mrad and 1.5 Mrad, followed by saturation.

For a quantitative description a sigmoid function

$$f(x) = \frac{a}{1 + e^{-k(x - x_0)}} + c$$

is fitted to the data, where a describes the maximum change, x_0 is the location of the inflection point ($f(x_0) = \frac{a}{2} + c$), k determines the steepness (larger k means a faster increase or decrease around x_0), and c is a the vertical offset. The resulting fits are shown in Figure 6.3 in the appendix and in Table 4.3.

The PXD PS provides the following voltages to the DCD: `AVDD` and `DVDD` power the analog and digital blocks, respectively, while `AmpLow` serves as the ground potential for the amplifiers in the current-memory

Table 4.3: Sigmoid fit results for the ADC metrics. c is the metric value at the start of the irradiation campaign, a describes the maximum change, therefore $a + c$ is the metric value at the end. x_0 is the location of the inflection point and k the steepness. The fitted functions are shown in the appendix (Figure 6.3).

Metric	a	k / Mrad^{-1}	x_0 / Mrad	c
ADC noise	0.69 ADU	4.56	1.05	1.17 ADU
INL	3.46 ADU	171.17	0.99	13.13 ADU
LSB	-0.54 mV	5.96	0.93	1.31 mV
Min output code	7.44 ADU	8.59	1.11	2.73 ADU

cells and comparators of the pipeline ADC, and `RefIn` defines the global reference potential distributed to multiple nodes of these stages [25, 42]. The corresponding supply currents exhibit changes at similar TID levels as the ADC metrics, as shown in Figure 4.23.

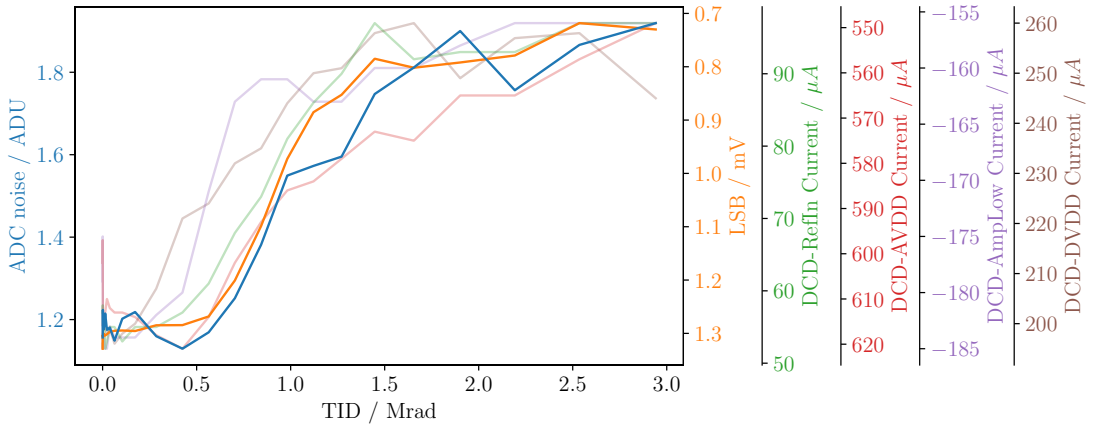


Figure 4.23: ADC noise (blue) and LSB width (orange, flipped y-axis) compared to DCD currents `RefIn` (green), `AVDD` (red, flipped y-axis), `AmpLow` (purple), and `DVDD` (brown).

A close correlation is observed between the LSB width and the `RefIn` current. Similarly, the increase in ADC noise follows the behavior of both `RefIn` and `AVDD` currents, indicating that changes in the analog operating conditions are primarily responsible for the observed noise development. By contrast, no clear correlations are visible for INL or the minimum output code. This suggests that these parameters are influenced by more localized effects within the circuitry that are not directly reflected in the global supply currents. `AmpLow` and `DVDD` currents also vary during irradiation, but their changes set in earlier and do not correspond directly to any ADC metric.

The same sigmoid fit as for the ADC metrics was repeated for the DCD currents. The fits are shown in the appendix (Figure 6.4) and summarised in Table 4.4.

DCD Working Point Shift

The shift of the optimal DCD WP was determined at each step by the 3×3 `IPSource–IPSource2` ADC curve scan with the DEPFET current source. However, an broader overview of development is

Table 4.4: Sigmoid fit results for the DCD current development. c is the current value at the start of the irradiation campaign, a describes the maximum change, therefore $a + c$ is the current value at the end. x_0 is the location of the inflection point and k the steepness. The fitted functions are shown in the appendix (Figure 6.4).

Current	a / µA	k / Mrad^{-1}	x_0 / Mrad	c / µA
`RefIn`	40.79	5.33	0.86	54.24
`AVDD`	-57.89	2.90	1.14	614.83
`AmpLow`	23.87	11.90	0.57	-183.14
`DVDD`	64.53	3.88	0.54	190.16

obtained from the ADC curve scans with DHE current source covering a 11×7 parameter space. These results are shown in Figure 4.24. The WP shift is predominantly in the `IPSource` domain and sets in at approximately 0.5 Mrad, consistent with the observations at the initial WP (Figure 4.22). Between 0.5 Mrad and about 1.5 Mrad the optimal `IPSource` setting shifted by roughly 30 units toward higher values.

At higher doses, the WP shifted beyond the accessible configuration range. Since `IPSource` is limited by its 7-bit register [25], values above 128 could not be set. Consequently, no good channels were obtainable for `IPSource` values of 130.

The WP appears stable above 1.5 Mrad. However, due to the register limitation a reliable statement is difficult. This behavior is nevertheless consistent with the evolution of the ADC metrics at the initial WP, which also showed no additional degradation beyond 1.5 Mrad.

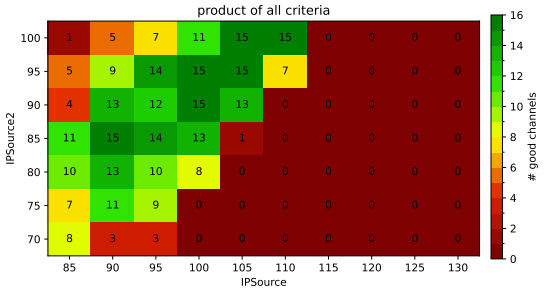
In contrast to the initial WP, the ADC metrics for the adjusted WP remained essentially stable, as shown in Figure 4.25. These metrics are derived from the ADC curve scan around the current WP with the DEPFET current source.

4.4.2 Pedestal Noise

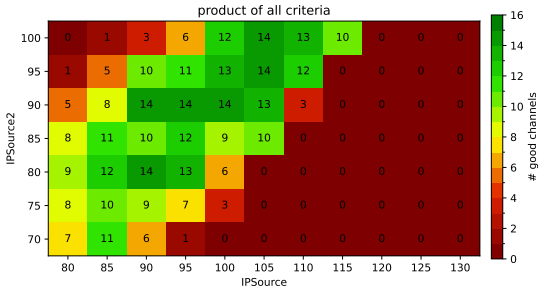
Similar to the ADC metrics, a degradation of the pedestal noise is observed (see Figure 4.26). Up to approximately 0.5 Mrad, no TID-induced effect is visible. Beyond this point, the pedestal noise increases steeply by 0.498 ADU, from 0.74 ADU to 1.24 ADU, as extracted from the sigmoid fit shown in Figure 4.26. Afterwards, the noise saturates without further significant degradation.

Comparing the pedestal noise at the initial and the current (adjusted) DCD WP shows that retuning `IPSource` and `IPSource2` almost completely mitigates the degradation. A minor residual increase remains, which might be explained by the measurement procedure. The current WP used for the pedestal measurement is the one determined in the preceding measurement sequence, i.e. before the subsequent irradiation period. Consequently, the pedestal measurement does not account for any additional shift caused by the latest TID and may be taken at a slightly outdated WP. Nonetheless, above approximately 1.5 Mrad almost no further WP shift is observed, thus a minor residual increase may also be intrinsic and not removable by re-optimization.

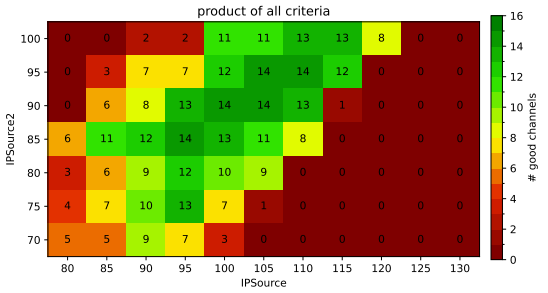
The pedestal degradation exhibits a comparable trend to the LSB size and ADC noise (Figure 4.27). However, the curves do not align perfectly, indicating an interplay among these quantities rather than a



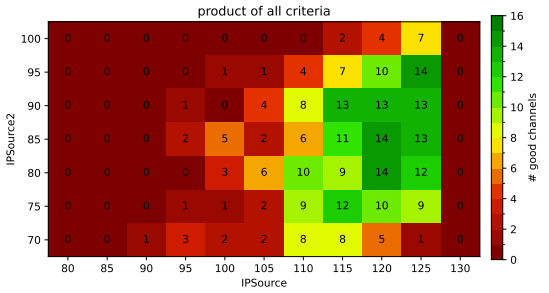
(a) 0 Mrad



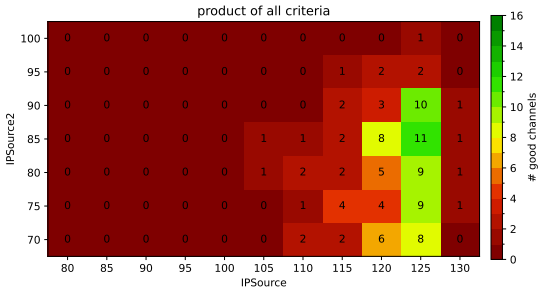
(b) 0.43 Mrad



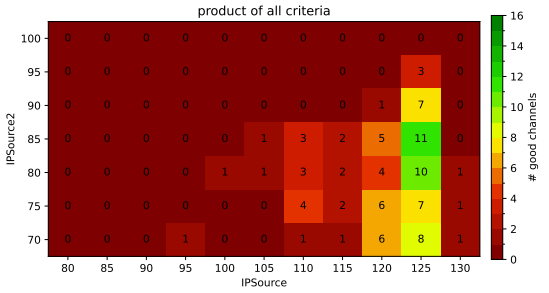
(c) 0.56 Mrad



(d) 0.98 Mrad



(e) 1.45 Mrad



(f) 2.94 Mrad

Figure 4.24: ADC curve scan results obtained with the DHE current source for a 11×7 `IPSource`–`IPSource2` parameter space at different accumulated TID. A clear WP shift in the `IPSource` domain sets in at about 0.5 Mrad and continues up to around 1.5 Mrad.

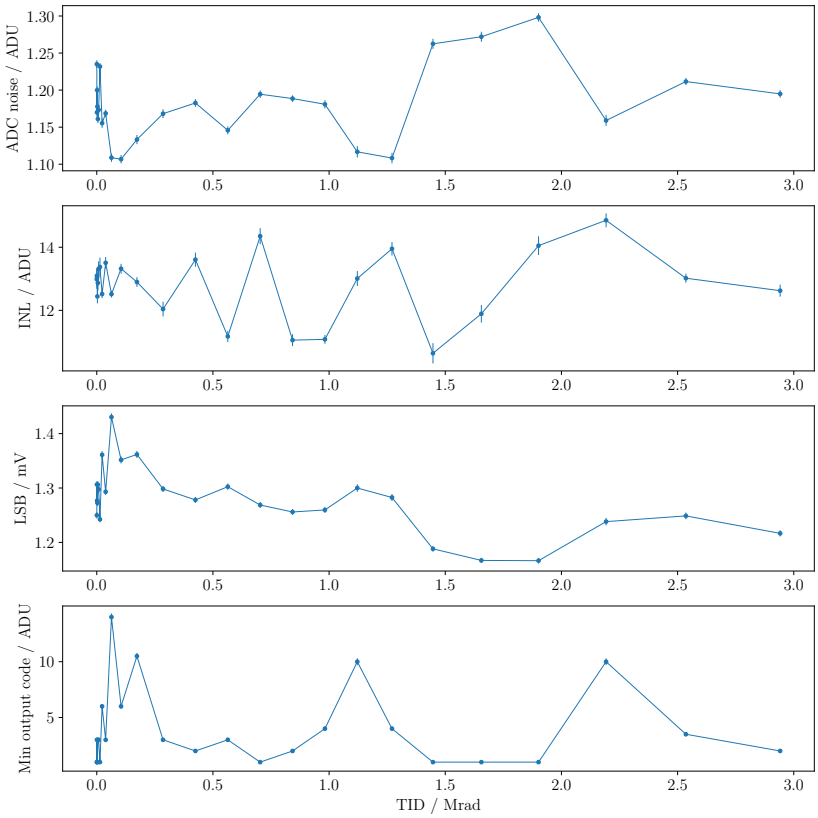


Figure 4.25: Measured evolution of ADC metrics with accumulated TID at optimal WP. All metrics are stable for the most part. only minor fluctuations are visible.

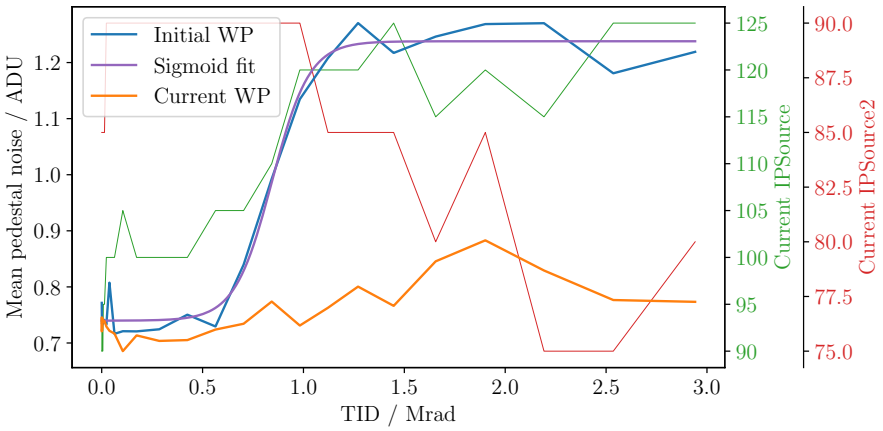


Figure 4.26: Measured pedestal noise at the initial and adjusted (current) DCD WPs. A sigmoid function is fitted to the initial WP data: $\text{noise}(\text{TID}) = 0.50\,\text{ADU}/(1 + \exp(10.82/\text{Mrad}(\text{TID} - 0.84\,\text{Mrad}))) + 0.74\,\text{ADU}$. The adjusted `IPSource`/`IPSource2` values used for the current WP are shown in addition for reference.

single controlling variable. In particular, a smaller LSB corresponds to a higher gain of the transfer curve. Consequently, pedestal current fluctuations translate into larger code variations, increasing the measured pedestal noise.

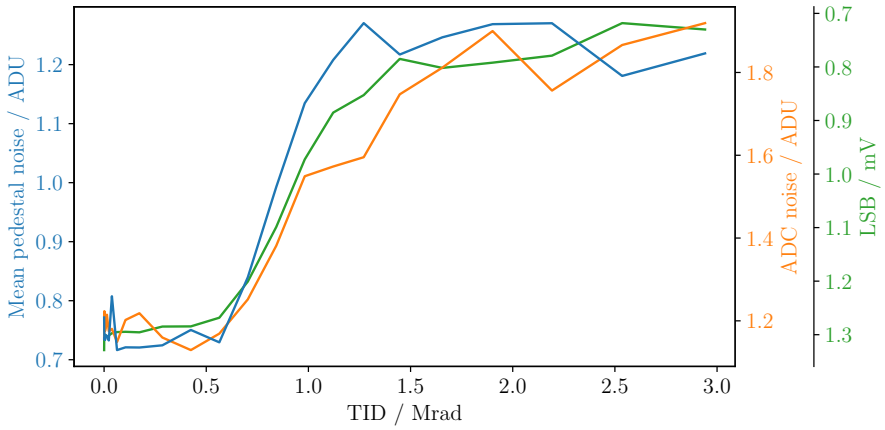


Figure 4.27: Pedestal noise at the initial DCD WP compared with the ADC noise and LSB width.

Linking the pedestal noise increase to a single DCD current is difficult because the pedestal depends on several DCD characteristics that themselves do not map uniquely onto distinct currents supplied by the PXD PS. Nevertheless, a correlation between the pedestal noise and the `RefIn` current appears more pronounced than for the currents as shown in Figure 4.28.

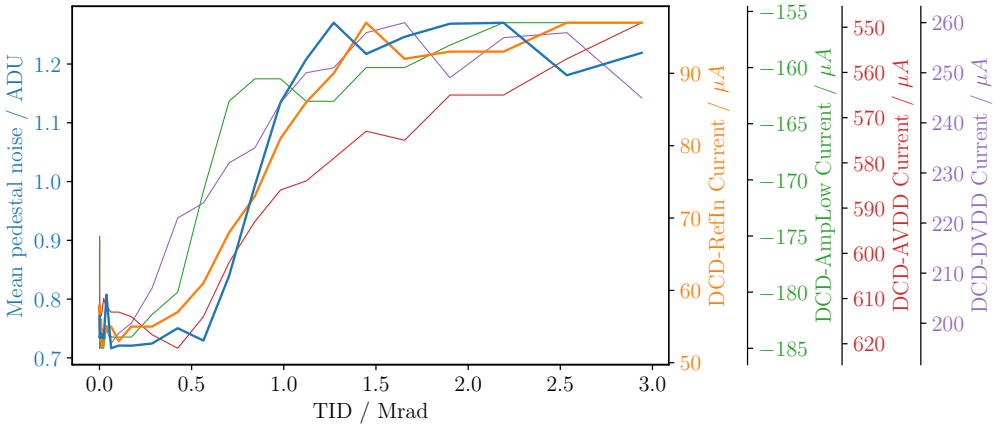


Figure 4.28: Pedestal noise at the initial DCD WP compared with the DCD currents (`RefIn`, `AVDD`, `AmpLow`, `DVDD`).

Continuous Pedestals

The continuous monitoring of the pedestals confirms stable operation up to a TID of approximately 0.5 Mrad, in accordance with previous described measurements. Beyond this point, the pedestal noise increases steeply during each individual irradiation step. As the TID per step increases, so does the

peak value reached within each step. Once the pedestal noise approaches 1 ADU (around 1.5 Mrad) a saturation behavior sets in that limits the maximum noise. For the last three irradiation steps, the observed peak decreases again while the saturation behavior persists. Figure 4.29 shows this development. This behavior contrasts with all other measurements, where no significant change is observed beyond 1.5 Mrad.

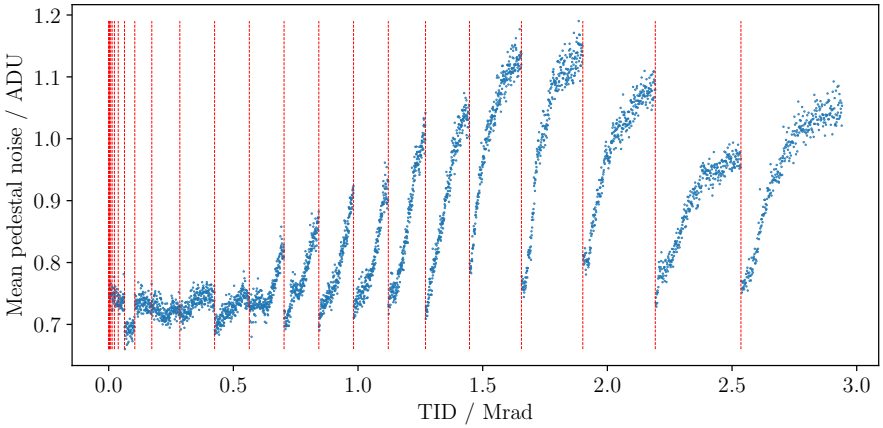


Figure 4.29: Measured pedestal noise from the continuous monitoring at the current WP during irradiation. After about 0.5 Mrad, each irradiation step exhibits a steep increase that eventually saturates close to 1 ADU. The vertical red dashed lines indicate the start of each irradiation step.

Between irradiation steps, during the annealing periods, the pedestal noise recovers almost completely. This is verified by the continuous monitoring performed during the irradiation and annealing periods (see Figure 4.30). Note that these measurements are performed at the optimized WP rather than the initial WP. During the annealing period, the pedestal noise follows an exponential like decrease. The DCD ASIC had approximately 3.5 h of annealing time between irradiation steps.

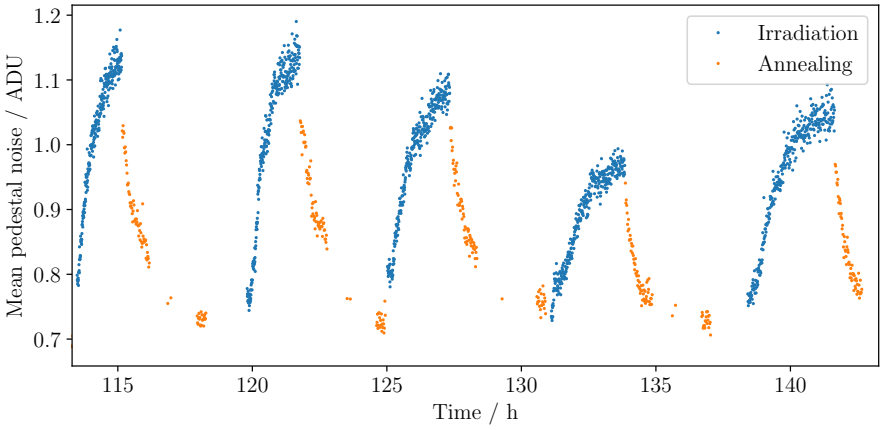


Figure 4.30: Measured pedestal noise from the continuous monitoring at the current WP across irradiation and annealing periods, plotted versus time. The pedestal noise recovers almost completely during each annealing interval.

A direct correlation between pedestal noise and a single DCD current is difficult to establish from the continuously monitored data. Nevertheless, the DCD current curves in Figure 4.31 show similar trends to the pedestal noise. The reduction of maximum pedestal noise during the last three irradiation steps coincides with a decrease in the `RefIn` current. Meanwhile, the steady increase in step-wise maxima between 0.5 Mrad and 1.8 Mrad aligns better with the behavior of `AVDD` and `AmpLow`. No comparable trend is observed for `DVDD` (see Figure 6.5 in the appendix).

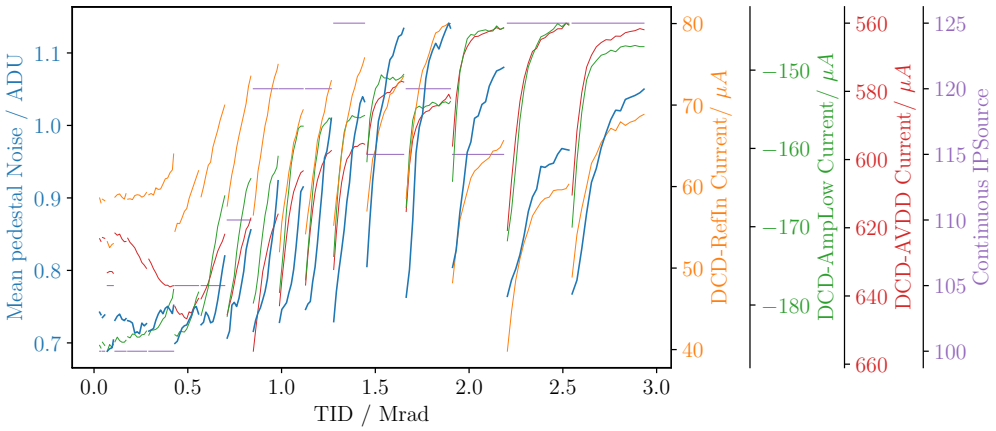


Figure 4.31: Pedestal noise from the continuous monitoring at the current WP during irradiation compared with the DCD currents `RefIn`, `AmpLow`, and `AVDD`. The `DVDD` current is dropped due to missing correlations. The adjusted `IPSource` used for the current WP is shown in addition for reference. For readability, each curve represents the mean over ten consecutive measurements.

4.4.3 Pedestal Value

As described in section 4.3.5 and shown in Figure 4.21(b), a continuous source current decrease was observed during the DCD irradiation campaign. In the Switcher campaign this led to a corresponding linear pedestal shift. For the DCD campaign, however, no such clear linear correlation was present. Nevertheless, the pedestal values were not stable, as shown in Figure 4.32. Up to about 0.5 Mrad, the pedestal value increased almost linearly with TID, while the single other measurable change was the decrease in source current. Based on the Switcher irradiation results, a down shift of the pedestals would have been expected from the current decrease. This indicates that additional effects, already present at low dose, counteract the source current dependent change.

Once the pedestal noise increases and changes in the DCD currents set in, the pedestal behavior becomes more complex. At the start of each irradiation step the pedestals rise before reversing and shifting downwards. For the last three steps this trend is partly broken, with a slower decrease following the initial rise. Between irradiation steps, partial recovery of the pedestal value was observed, but with varying amplitude. Altogether, this points to a complex interplay of several mechanisms within the DCD.

The pedestal distribution at the initial WP also changed with rising TID. Already at 0.8 Mrad the distribution had broadened considerably compared to the initial state, as shown in Figure 4.34(a) and 4.34(b). This broadening reduces the reliability of the Gaussian fit used to determine the median

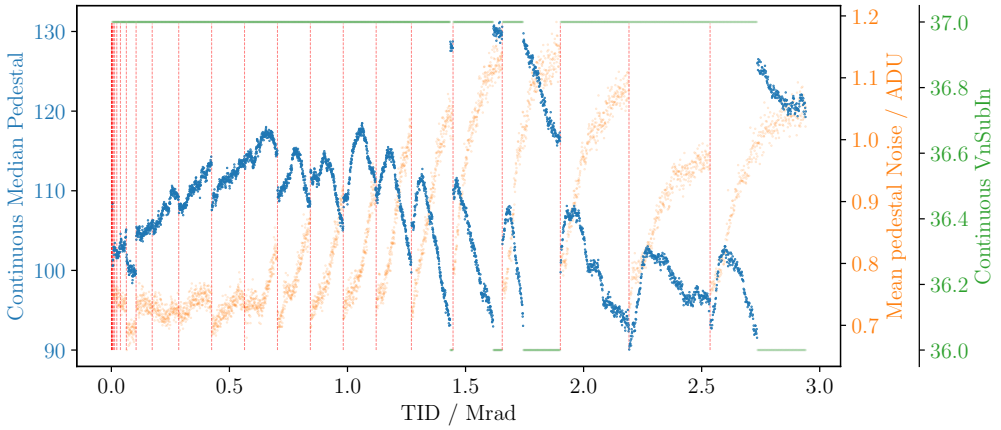


Figure 4.32: Development of the median pedestal during the irradiation phase. Additionally the pedestal noise and `VNSubIn` are shown for reference.

pedestal, as indicated by the long error bars in Figure 4.33 and visible in the pedestal distribution plot in Figure 4.34(c). Furthermore, the broadening pushes many pixels out of the dynamic range of the DCD, visible as white pixels in the pedestal maps (Figure 4.34).

Up to 1.8 Mrad, the median pedestal development at the initial WP (Figure 4.33) roughly resembles the shift behavior observed within a single irradiation step: an initial upward shift followed by a downward shift. Beyond this dose, the measurements were either performed with different `VNSubIn` settings or suffer from large uncertainties, which prevents a reliable statement on the further trend.

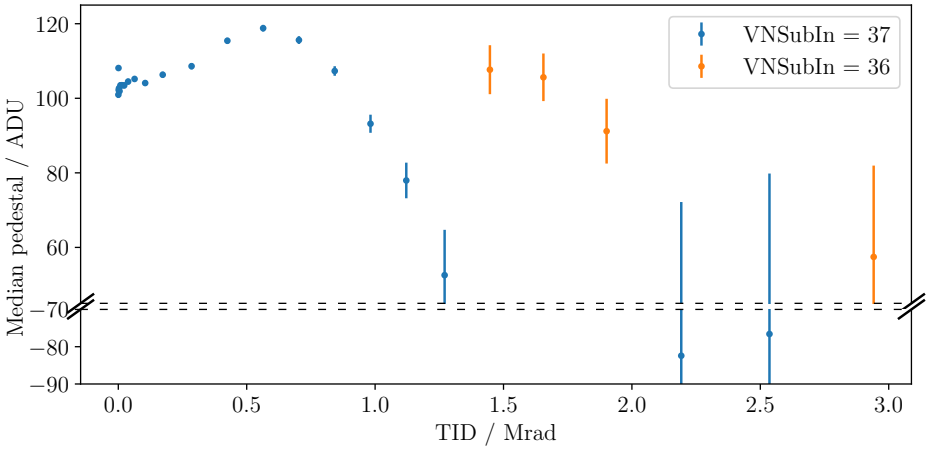
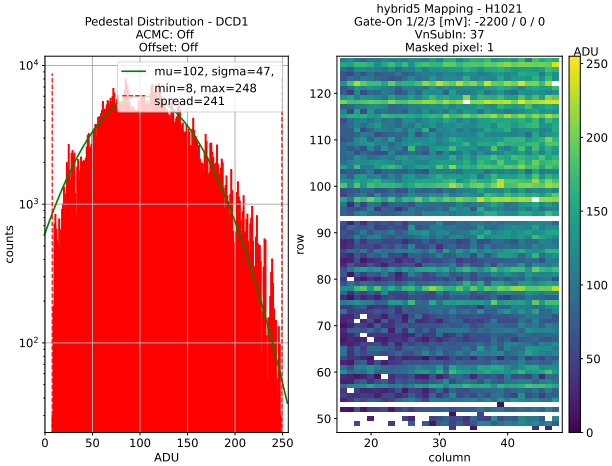
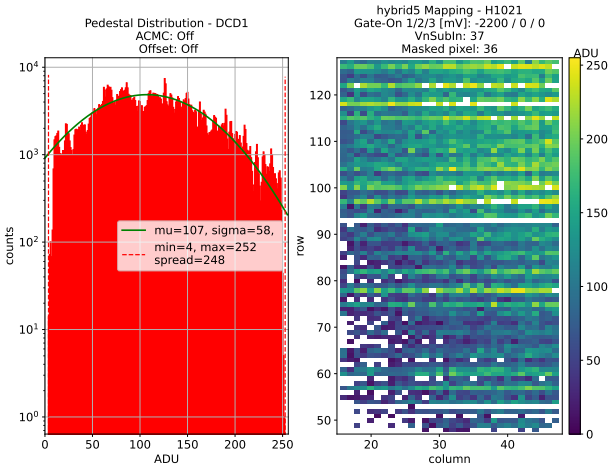


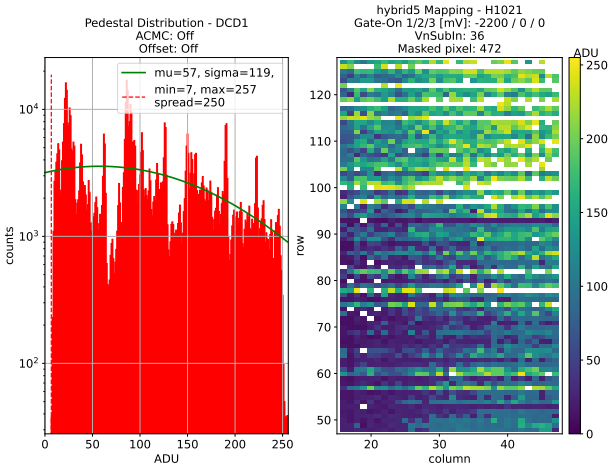
Figure 4.33: Median pedestal value at the initial WP during the irradiation campaign. Vertical axis is split up in middle for better scaling.



(a) 0 Mrad: Initial pedestal state before DCD irradiation



(b) 0.8 Mrad: Broadening pushes pedestals of some pixels out of dynamic range of DCD → white pixels



(c) 3 Mrad: Gaussian fit is unreliable

Figure 4.34: Pedestal distributions at the initial WP for different accumulated TID.

4.5 Comparison to Other Irradiations

In the following, the results of the irradiation campaigns conducted within the scope of this thesis are compared to other irradiations. In contrast to the analysis in this thesis, those experiments did not consider the TID in the electronics layer but instead considered the TID incident on the device under test. The TID reaching the Switcher/DCD ASIC and the corresponding TID in the electronics layer for the campaigns of this thesis are compared in Table 4.1 and 4.2.

4.5.1 Full PXD Module Irradiation Campaign

In separate laboratory irradiation studies, two complete PXD modules were irradiated up to 20 Mrad [45]. The pedestal noise evolution was similar to that observed in the dedicated DCD irradiation campaign (Figure 4.35). Up to approximately 2 Mrad no change is seen. Between 2 Mrad and 8 to 10 Mrad (depending on the module) the noise increases steeply, followed by a saturation. This behavior is consistent with the observations of the dedicated DCD campaign when taking into account the different dose definitions: the PXD module study considers the incident X-ray dose on the module, whereas the TID in the ASIC electronics layer is used for the DCD irradiation study. Taken together, these results suggest that the dominant contribution to the noise increase originates from TID damage in the DCD.

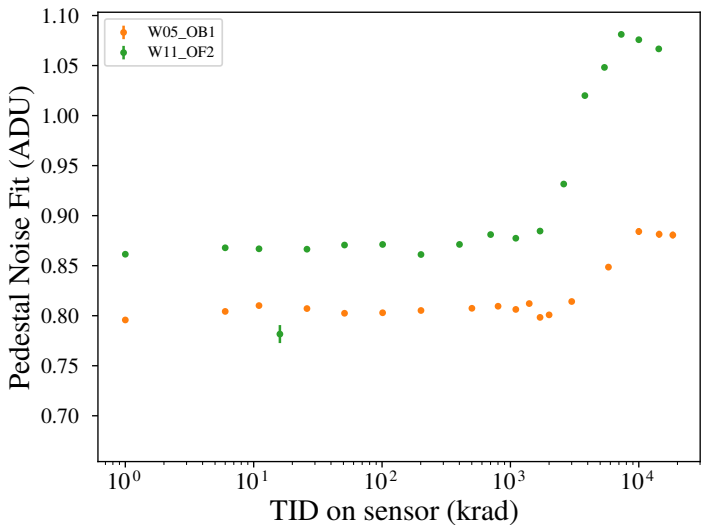


Figure 4.35: Pedestal noise during irradiation of entire PXD modules `W05_OB1` and `W11_OF2`

4.5.2 PXD Noise Increase at Belle II

The pedestal noise increase observed in Belle II (Figure 2.14) behaves differently from the trends seen in the DCD and full-module irradiation campaigns. It starts at substantially lower doses, grows approximately linearly with accumulated TID, and does not saturate within the observed range. This deviation may arise from the different operational environment at Belle II compared to laboratory

irradiations, including differences in dose rate, particles, temperature, and humidity. Nevertheless, both the Belle II data and the DCD campaign show a clear increase of pedestal noise with increasing TID, indicating that radiation damage to the DCD is a likely contributor to the observed pedestal noise increase in the PXD.

In contrast, no pedestal noise increase was observed in the Switcher irradiation campaign. Radiation damage to the control ASICs can therefore be excluded as the origin of the pedestal noise increase in Belle II, within the limits of comparability imposed by the different irradiation conditions.

CHAPTER 5

Conclusion

An increase in pedestal noise is observed, for the PXD at Belle II. Due to its impact on the signal-to-noise ratio and therefore on the overall detector performance, this effect requires dedicated investigation. This motivated the ASIC irradiation campaigns, carried out in the scope of this thesis. Both the readout ASIC (DCD) and the control ASIC (Switcher) of the DEPFET sensor were irradiated individually. An X-ray tube provided high energetic photons to study the correlation between accumulated TID and performance degradation of a Hybrid5 module, a full system demonstrator.

The irradiation of the Switcher showed no measurable influence on the pedestal noise. In addition, the new SwitcherB18V2.3, installed on the Hybrid5 used for the irradiation studies, showed improved radiation hardness compared to the older SwitcherB18V2.1, installed in PXD at Belle II. Preliminary measurements with the older version revealed a broadening of the clear pulse under irradiation, whereas this effect was absent for the newer version during the main campaign.

In contrast, the irradiation of the DCD revealed significant degradation in the performance of the ADC channels, leading to an increase in pedestal noise. The noise increase was highly non-linear, with a steep rise, setting in only after some dose accumulation, followed by saturation. This contrasts with the almost linear increase without saturation observed in PXD. However, the comparison to radiation campaigns of full-scale modules under laboratory conditions, indicated that the TID damage in the DCD is the primary source of pedestal noise degradation.

An important finding of this work is that pedestal noise degradation can be substantially mitigated by re-optimization of the DCD settings. During the irradiation campaign only `IPSource` and `IPSource2` were re-optimized, while significant shifts were observed for DCD-RefIn and DCD-AmpLow currents. Further studies including the re-optimization of the corresponding voltages may provide additional improvements.

CHAPTER 6

Appendix

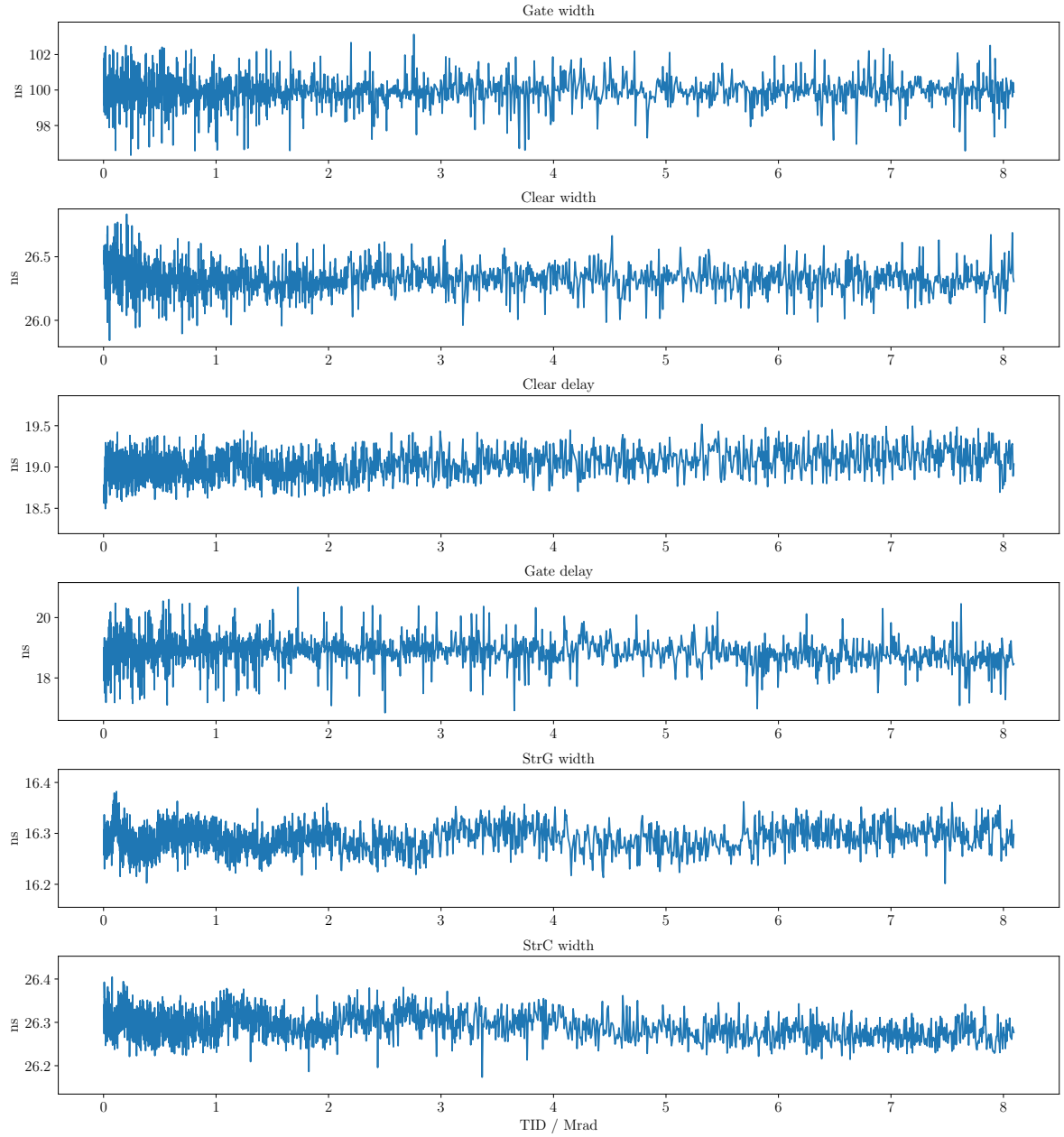


Figure 6.1: Measured Switcher signal timing parameters as a function of accumulated TID. Shown are the gate width, clear width, gate delay, clear delay, `StrG` width, and `StrC` width. All parameters remain constant with minor statistical fluctuations, indicating no measurable TID-induced degradation in the Switcher performance.

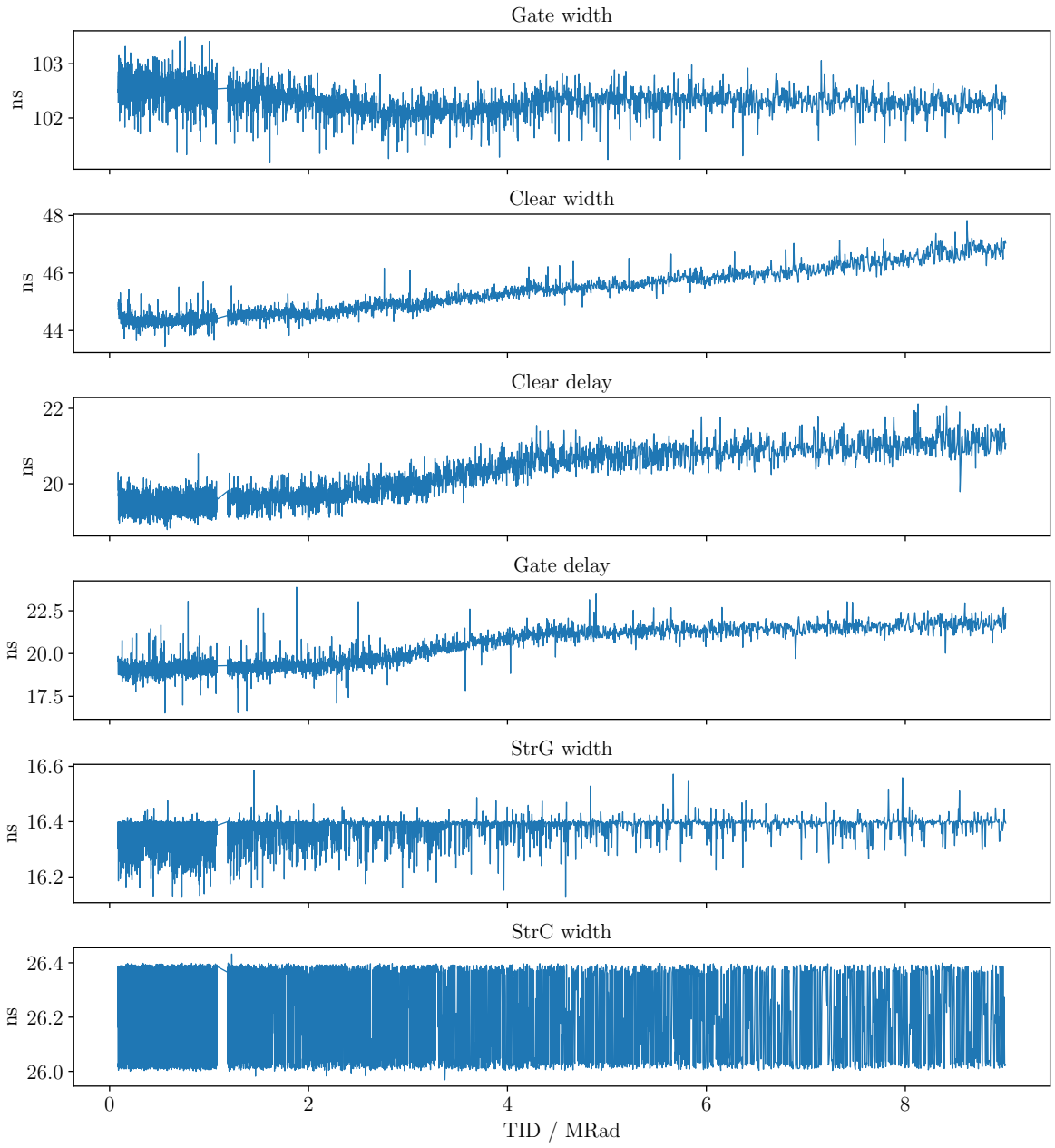
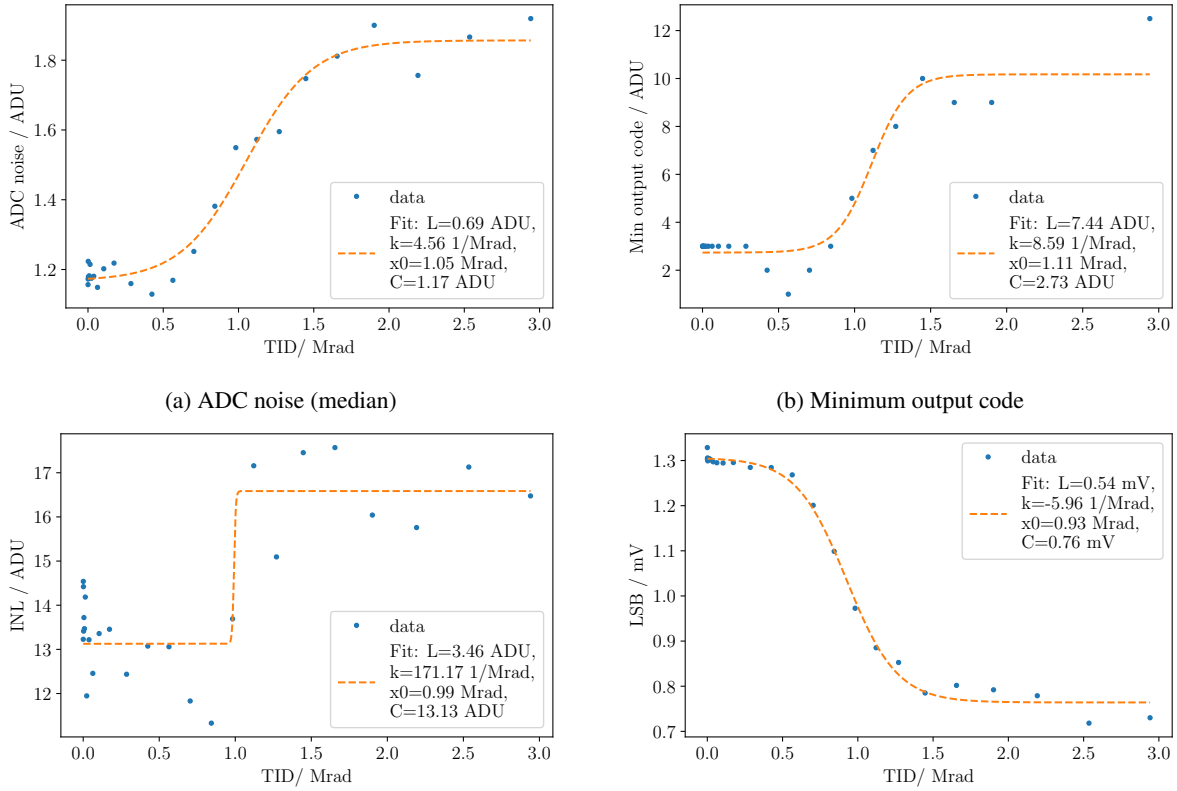


Figure 6.2: Measured Switcher signal timing parameters as functions of accumulated TID for the preceding test campaign with Hybrid5 H5020 and SwitcherB18V2.1. The gate width, clear width, gate delay, clear delay, `StrG` width, and `StrC` width are shown. A broadening of the clear signal is clearly visible.



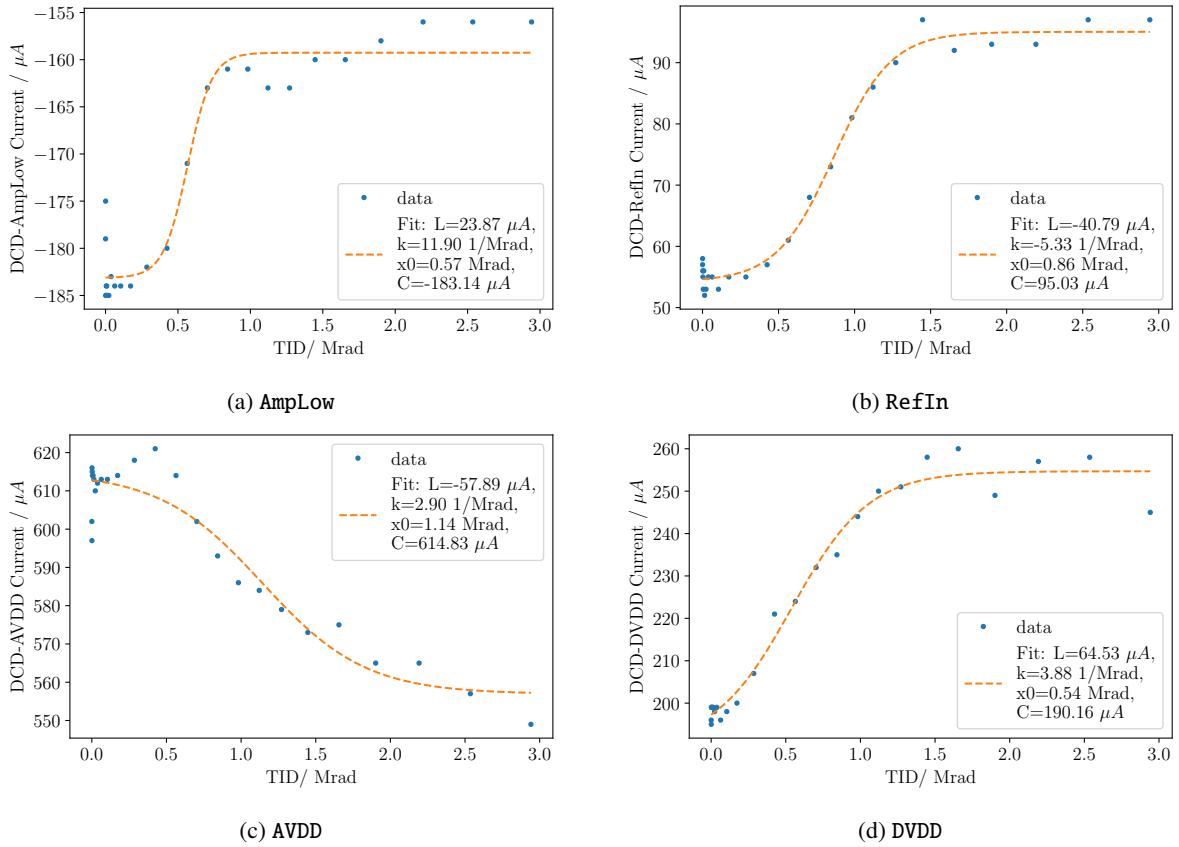
(a) ADC noise (median)

(b) Minimum output code

(c) ADC INL

(d) LSB size

Figure 6.3: Sigmoid fits for ADC metrics at the initial DCD WP.



(a) `AmpLow` (b) `RefIn`

(c) `AVDD` (d) `DVDD`

Figure 6.4: Sigmoid fits for DCD currents at the initial DCD WP.

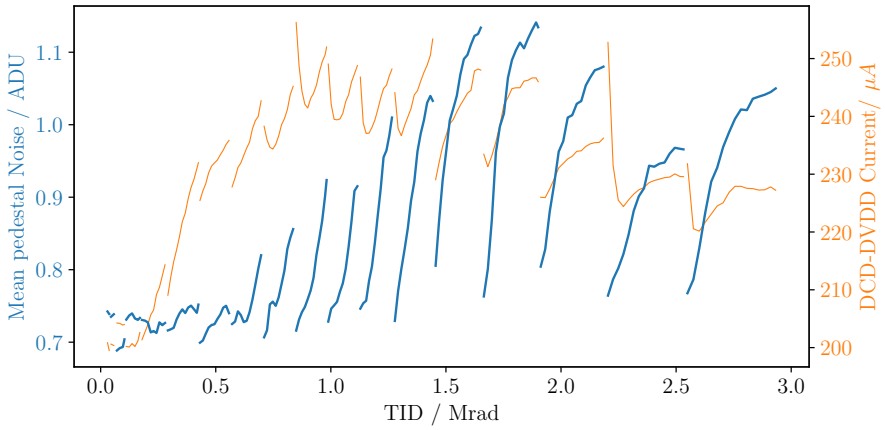


Figure 6.5: Pedestal noise from the continuous monitoring at the current working point during irradiation compared with the DCD current `DVDD`.

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List of Figures

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List of Acronyms

ADC Analog-to-Digital Converter. 11, 12, 17, 18, 20–22, 28, 34, 36, 38–40, 43, 49, 50, 56–63, 70

ADU Arbitrary Digital Unit. 21, 34, 36, 42, 52–54, 56, 58–60, 64

ARICH Aerogel Ring Imaging Cherenkov Detector. 5, 6

ASIC Application-Specific Integrated Circuit. 1, 2, 10, 11, 14, 15, 21, 22, 25–33, 44–47, 49, 55, 64, 68–70

CDC Central Drift Chamber. 5, 6

CMC Current Memory Cell. 19, 39

DAC Digital-to-Analog Converter. 18, 20, 22, 39, 43

DAQ data acquisition system. 15, 22, 23

DCD Drain Current Digitizer. 2, 11, 12, 15, 17, 18, 21–23, 25–34, 37–40, 43, 46–49, 54–60, 62–70

DEPFET DEpleted P-channel Field Effect Transistor. 1, 2, 6, 9–15, 17, 22–24, 26–29, 34–39, 41, 49, 55, 57, 59, 60, 70

DHC Data Handling Concentrator. 23, 26

DHE Data Handling Engine. 15, 22, 23, 26–28, 30, 39, 43, 49, 57, 60, 61

DHH Data Handling Hybrid. 22, 23, 26

DHI Data Handling Insulator. 23

DHP Data Handling Processor. 15, 22, 27–30, 33, 37, 49

DNL Differential Non-Linearity. 21, 39–42

ECL Electromagnetic Calorimeter. 5

EL Electronics Layer. 47, 48

HER High Energy Ring. 4, 5, 7

INL Integral Non-Linearity. 21, 39–42, 49, 58, 59

IP Interaction Point. 4–8

JTAG Joint Test Action Group. 15, 22, 26, 31

KLM K_L and μ Detector. 4, 5, 7

LER Low Energy Ring. 4, 5, 7

LSB Least Significant Bit. 20, 21, 38–40, 42, 43, 49, 58–60, 63

MAMI Mainz Microtron. 33, 50

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor. 11, 12

NIEL Non-Ionizing Energy Loss. 23

OnSeN Online Selection Nodes. 23

PCB Printed Circuit Board. 55

PS Power Supply. 22, 26, 30, 39, 58, 63

PXD PiXel Detector. 1, 2, 6, 7, 9, 10, 12–17, 21–27, 29, 30, 33, 34, 38, 39, 58, 63, 68–70

QCS quadruple magnet system. 5, 7, 8

ROI Region Of Interest. 23

RSD Redundant Signed-Digit. 18, 19

SM Standard Model. 1

SMU Source Measurement Unit. 28, 30, 43, 46

SR Synchrotron Radiation. 7

SVD Silicon Vertex Detector. 6, 9

TID Total Ionizing Dose. 23–25, 47–56, 58–63, 65, 67–70

TOP Time-of-Propagation. 5, 6

VXD VerteX Detector. 5, 6

WP working point. 38, 40, 49, 57, 59–67

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