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**Characterization of new Belle-type  
DEPFET pixel test structures**

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I hereby declare that the work presented here was formulated by myself and that no sources or tools other than those cited were used.

Bonn, 5.10.2025

Ort, Datum

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## 1 Introduction

Many particle detectors worldwide are used to gain deeper insights into the mechanisms of the universe's smallest constituents.

Some detectors use natural particle sources, for example radioactive isotopes or cosmic radiation from the sun. In this case, the particle type and its properties are determined by external conditions. However, to meet specific experimental requirements, scientists developed particle accelerators as tunable sources.

The most common use of particle accelerators is in colliders, where particles with adjustable properties collide and produce new particles. Typical tunable properties include energy, particle type and collision symmetry (symmetric or asymmetric). Since the resulting particles strongly depend on these conditions, various collider configurations have been built to study their characteristics.

One example is the SuperKEKB accelerator in Japan, whose collisions are studied with the Belle II detector. A major goal of Belle II is to investigate CP violation in B-meson decays.

To reconstruct interactions, the detector measures various particle properties including their trajectories. Therefore the detector consists of many elements. The innermost layer of the detector is the Pixel vertex Detector (PXD), which employs DEPFETs (DEpleted P-channel Field Effect Transistors) as pixels to reconstruct the particle tracks. DEPFET technology combines particle detection and in-pixel amplification, making it a self-amplifying active pixel sensor. This thesis focuses on the analysis of a new prototype of DEPFET matrices, compared to those currently used in the BELLE II experiment.

Chapter 2 and Chapter 3 provide an overview of the BELLE II experiment and the DEPFET technology. In Chapter 4, static measurements are presented to later validate tests done with full assemblies. The results for assemblies of the known PXD9 type are presented in chapter 5 and compared to the PXD13 matrices. Chapter 6 presents additional studies done with similar structures.

## 2 SuperKEKB and Belle II

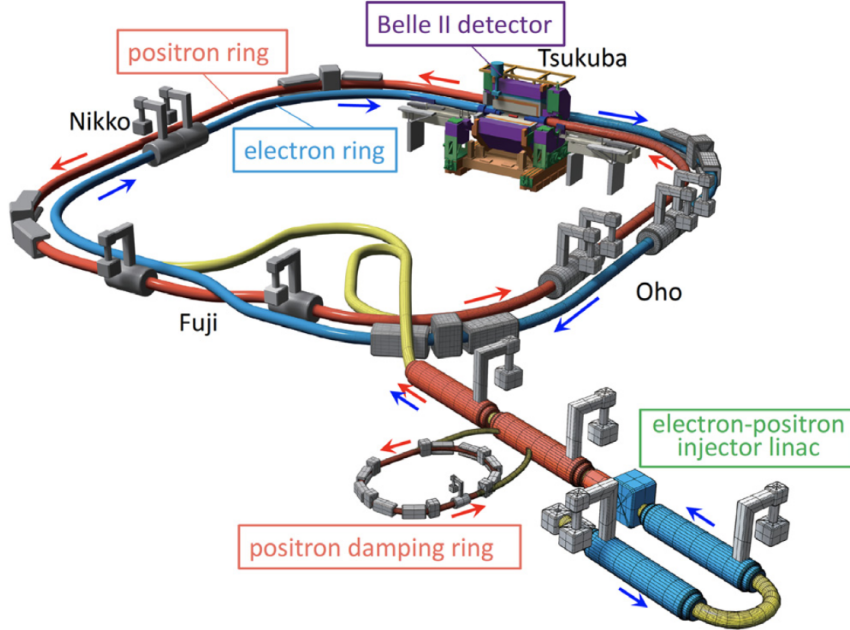


Figure 1: Schematic view of the SuperKEKB accelerator [1]. Electrons travel in the blue tube, with their flight direction indicated by the blue arrows. Positrons travel in the orange tube in the opposite direction. Before injection into the main ring, positrons are stored in the damping ring. The first acceleration step is provided by the linear accelerator (green), while the interaction point is located inside the Belle II detector (purple).

From 1999 to 2010 the KEKB accelerator in Japan produced particles for the BELLE-experiment [2]. It was an asymmetric-energy positron-electron collider and the measured total integrated luminosity amounts to  $1041 \text{ fb}^{-1}$ . It led to important insights into CP-violation and the overall flavor structure of elementary particles [3]. Building on this success, the KEKB accelerator was upgraded to become SuperKEKB. SuperKEKB has a higher luminosity, smaller bunches, a higher particle current and several other improvements [3]. As shown in Figure 1, it consists of a 7 GeV electron ring (high energy ring HER) and a 4 GeV positron ring (low energy ring LER). The leptons are primarily accelerated with a linear accelerator. The positrons are stored in a 1.1 GeV damping ring and later used in the greater positron ring. The leptons are further accelerated and then brought into a near head-on collision. The setup was successfully tested without the final-focus superconducting magnets and the Belle II experiment in 2016 [1]. The first collisions with the Belle II detector installed occurred in 2018.

SuperKEKB is a so-called B-factory. It is operated at a center-of-mass energy which equals the mass of the resonance  $\Upsilon(4S)$ ,  $m_{\Upsilon(4S)} = 10.58 \text{ GeV}/c^2$ . This

resonance is a meson build from a  $b$ -quark and  $\bar{b}$ -quark. It decays into  $B^+B^-$  and  $B^0\bar{B}^0$  in more than 96% of the cases. This offers an interaction with low background, thereby enabling high-precision measurements. Due to the asymmetric-energy collision, the center-of-mass system has a boost of  $\beta\gamma = 0.28$  with respect to the detector. Therefore the produced B-mesons travel along the detector before they decay. For the neutral B-mesons this allows measurements of the violation of charge-parity (CP) symmetry.  $B^0\bar{B}^0$  mesons can oscillate via second-order Feynman processes. With the two produced B-mesons this oscillation can be measured, allowing the extraction of asymmetries. This is done by measuring the distance between the decay points of the B-mesons and determining their flavor. Since the B-mesons decay quickly and for this experiment even in the beam pipe, only the decay products can be measured, and the B-mesons must be reconstructed. This is achieved with the Belle II detector.

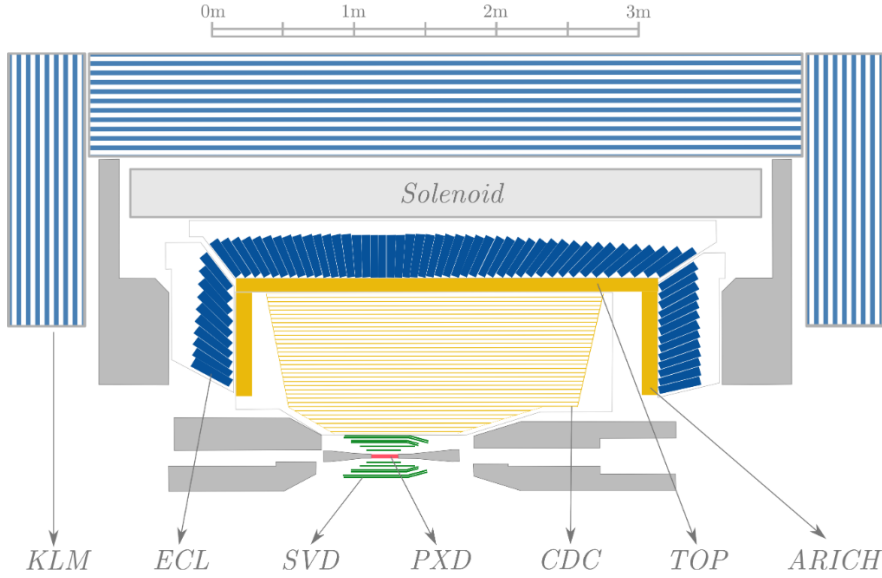


Figure 2: Schematic view of the Belle II detector [4]. The innermost part is the vertex detector, consisting of the Pixel Vertex Detector (PXD, red) and the Silicon Vertex Detector (SVD, green). Surrounding it is the Central Drift Chamber (CDC, yellow lines). This is followed by the Time of Propagation Detector (TOP, yellow bar) and the Aerogel Ring Imaging Cherenkov Detector (ARICH, yellow bar on the right). Next comes the Electromagnetic Calorimeter (ECL, darkblue), followed by the solenoid and finally the  $K_L^0$ -Muon detector (KLM, blue).

Belle II consists of many different elements with the purpose of identifying particles and measuring their type, direction and energy. A schematic can be seen in Figure 2. The layered structure of Belle II ensures detailed measurements of the particles. While outer detectors specialize in energy measurement and particle identification, inner detectors focus on trajectory and vertex resolu-

tion. The outermost detector is the  $K_L^0$ -Muon detector (KLM). It is built from thick iron plates, thin resistive plate chambers and scintillator bars to induce and measure hadronic showers from the  $K_L^0$  mesons and electromagnetic energy from muons, which are the only particles not stopped in the electromagnetic calorimeter (ECL). The ECL forms the layer below the KLM, only separated by the Solenoid, which produces an axial magnetic field of 1.5 T in all inner detectors. The ECL captures the energy of electromagnetic interacting particles with thallium-doped cesium iodide (CsI(Tl)) crystals, arranged in a barrel around the inner detectors and two endcaps for particles flying in the forward and backward directions. The ECL measures the energy of the particles and allows reconstruction of the angular distribution of neutral particle decays.

The next layer of Belle II is divided into two parts. The Time of Propagation Detector (TOP) is located in the barrel area and consists of quartz radiator bars connected to photomultipliers. The particles traversing the bars emit Cherenkov photons and the angle and time of propagation can be used to distinguish kaons and pions. The endcap in forward direction includes an Aerogel Ring Imaging Cherenkov Detector (ARICH). Particles traversing the silica aerogel again emit Cherenkov photons, which form a characteristic Cherenkov ring. This ring depends on the particle and can therefore be used for particle identification.

The Central Drift Chamber (CDC) is a wire chamber filled with a helium-methane mixture. Incoming particles will ionize the gas, the field configuration of the chamber leads to secondary ionization, and an avalanche of electrons hits the sense wires. The signal includes information about the primary electrons and therefore the energy and momentum of the particle, and also provides precise spatial information for track reconstruction.

The innermost layer is the Vertex Detector (VXD). It is split into two components, the outer Silicon Vertex Detector (SVD) and the inner Pixel Vertex Detector (PXD). The SVD has a cylindrical shape built from four layers of double-sided silicon strip sensors at different radii. Particles pass the detector and interact with the material, leaving a trace of electron-hole pairs. These drift to the strips placed on each side of the material and create a current signal. The PXD has two layers of sensors and is closest to the interaction point. The pixels provide high resolution on particle trajectories and thereby enabling vertex identification. In the following chapters, the functionality of the PXD modules will be further described and assemblies of the DEPFETs will be tested.

### 3 DEPFET and hybrid5

#### 3.1 Depleted P-channel Field Effect Transistor

For the Belle2 experiment, the innermost detector must meet many requirements due to the high irradiation and limited space. The DEPFET structures have a low material budget and can also be thinned to  $50\text{ }\mu\text{m}$  [5], avoiding an impact on the flight path of incoming particles. They resist the irradiation of SuperKEKB, by having a radiation hardness up to  $20\text{ kGy}/10^7\text{ s}$  [6]. DEPFETs have a low power consumption such that they do not need active cooling, which would increase the material budget of the detector. The active pixel design combines signal detection and internal amplification, and it also provides a high signal-to-noise ratio. This is why the DEPFET pixel design was chosen for the Belle II Pixel Vertex Detector.

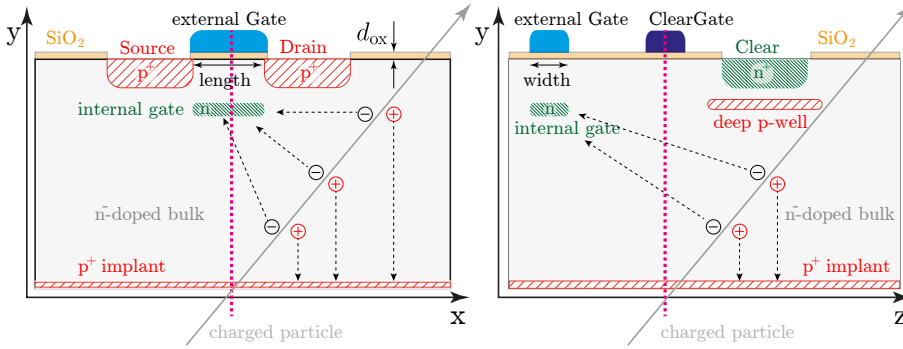


Figure 3: Layout of a DEPFET pixel cell [7]. A p-channel MOSFET (with source/drain implants in red, silicon oxide in yellow and external gate in blue) is embedded in an n-type silicon bulk. An additional  $n^+$ -implant (green) forms an internal gate, which modulates the current between source and drain. The bulk is fully depleted, so that incoming particles create electron-hole pairs. The electrons drift to the internal gate, while the holes drift to the backside. A clear implant (green) can be activated via the ClearGate contact (darkblue) to empty the internal gate. The clear implant is shielded by a deep p-well to prevent unwanted clearing of electrons.

##### 3.1.1 Working principle of DEPFET

The DEPFET consists of a p-channel Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) embedded into a high-resistivity n-type silicon bulk. A high voltage between the  $p^+$  backside and the front side depletes the silicon bulk. Less than  $1\text{ }\mu\text{m}$  beneath the p-channel of the MOSFET, there is an additional highly doped  $n^+$ -implant. This implant serves as an internal gate. If a particle traverses the depleted silicon bulk, it creates electron-hole pairs. While the holes drift to the  $p^+$ -backside of the DEPFET, the electrons accumulate inside the internal gate. Due to the capacitive coupling between the internal gate and the p-channel, this creates a mirror charge in the p-channel, modulating the current flowing between source and drain. To avoid saturation, the internal

gate has to be cleared. This is done with a high voltage applied to the  $n+$  clear implant, which creates an  $n$ -channel between the internal gate and the clear implant, removing the collected electrons. The implant is shielded with a  $p^+$  deep well so that the generated electrons first travel to the internal gate and do not get instantly removed. An additional electrode, the ClearGate, is used to support the clear mechanism. When the pixel is in collection mode, the ClearGate forms a potential barrier between Clear and the internal gate. It suppresses back-injection from the clear implant into the internal gate, which would result in signal distortion. Clear and ClearGate have a capacitive coupling. When the clear voltage is applied, the ClearGate potential rises and the potential barrier decreases. The electrons overcome the low barrier by thermionic emission and reach the clear implant.

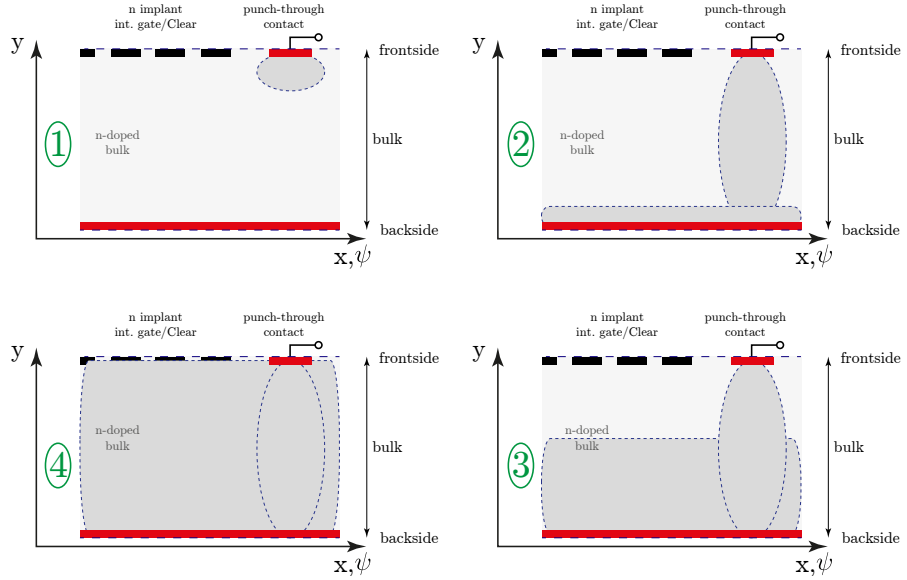


Figure 4: Working principle of front-side depletion [7]. A high voltage is applied to the punch-through contact to start depleting the silicon bulk (1). The depletion region extends from the implant towards the backside (2). It then expands back towards the front-side (3) until the full bulk is depleted (4).

### 3.1.2 Depletion and Voltages

For the DEPFETs, all voltages are set relative to source unless stated otherwise. Since the silicon bulk serves as the detection volume, the full volume has to be depleted. In these DEPFETs the depletion is achieved via the punch-through mechanism. A punch-through contact is established on the front side by connecting an electrode to a  $p^+$ -implant. This implant is biased with a high voltage. When the voltage is increased, the depletion region starts growing around the implant. At about  $-35$  V, the depletion region reaches the backside, and a small current starts to flow. As the voltage increases, the depletion further develops from the backside, growing back into the silicon bulk. At about  $-70$  V the de-



pletion reaches the front side. This voltage is called the depletion voltage. Now the full silicon bulk is depleted and sensitive to incoming particles.

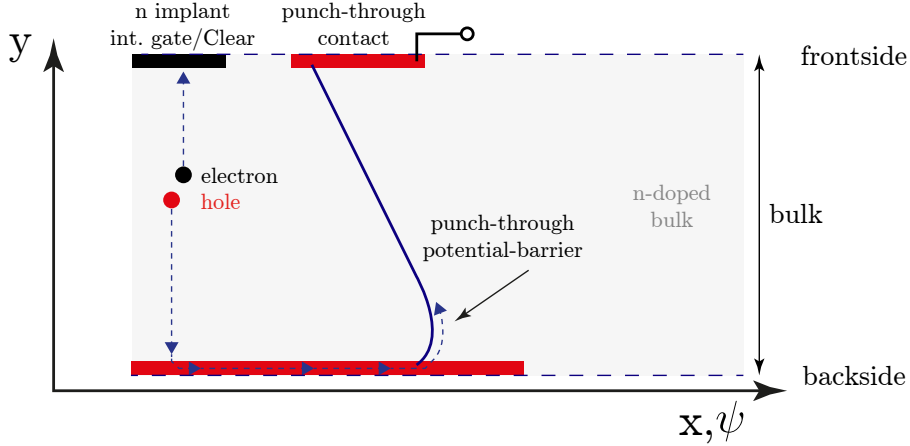


Figure 5: Punch-through current for the DEPFET [7]. Thermally generated holes drift towards the backside and can pass the punch-through potential barrier, resulting in a measurable current.

A small punch-through current can be observed due to leakage currents at the surface and thermally generated electron-hole pairs. The holes drift to the backside and then they overcome a small potential barrier to travel further to the punch-through contact, creating a small but noticeable current.

There are two drift fields influencing the path of the electrons. Within nanoseconds [7] the electrons travel to the vertical potential minimum. The electrons then travel horizontally to the internal gate under a much weaker field. The lateral/horizontal drift is enabled by an unstructured p-implant which has an applied drift voltage of  $-5\text{ V}$ .

Additionally, the matrix is surrounded by an  $n^+$  bulk implant, which is set to a voltage of  $10\text{ V}$ . It helps depleting the silicon bulk on the edges and intercepts electrons coming from the outside of the sensitive area. A  $p^+$  guard ring between the active pixel area and the bulk implant is set to  $-5\text{ V}$ , which also intercepts electrons drifting into the sensitive area. With this configuration, signal distortions from outside the detection volume are minimized.

### 3.1.3 Pixel Layout

The DEPFET pixels are arranged in a grid to form a large sensitive area. These DEPFET matrices for the PXD have 250 by 768 pixels. However for the tests in this thesis a smaller variation is used with only 32 by 80 pixels.

The pixel layout is shown in Figure 6. The purple shape is the ClearGate. It is built from a polysilicon layer and separates the MOSFETs from the clear implants and the drift region. The red structure is a second polysilicon layer and serves as the external gate for the MOSFETs. The  $n^+$  implants of the Clear are shown in green. They are located at both sides of the internal gate to

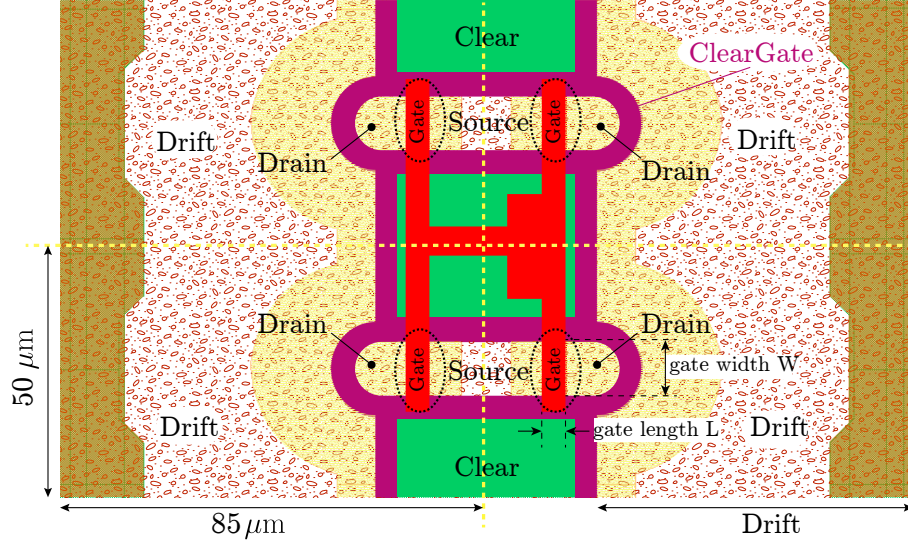


Figure 6: DEPFET pixels combined in a  $2 \times 2$  pixel array [7]. The pixels share a Gate structure with individual contacts (red) and a clear implant (green). Two pixels share one source contact, while each pixel has its own drain contact and internal gate. The Clear region is shielded from the other parts by the ClearGate (purple).

enable a complete and fast clearing. The brown and yellow areas show the drift configuration, which guides the electrons toward the internal gate.

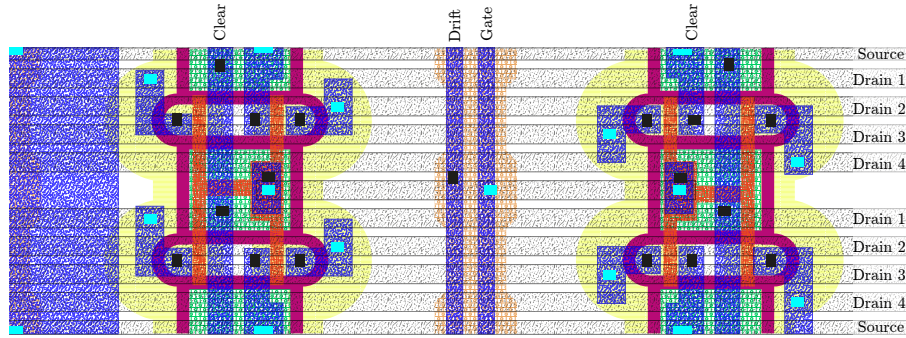


Figure 7: Electrical connections for 8 DEPFET pixels [7]. Two aluminum layers provide drain and source lines (horizontally) as well as clear, gate, and drift lines (vertically). Connections between the aluminum layers are shown in turquoise, while contacts to the DEPFET cells are shown in black.

For the electrical connection, the DEPFET pixels are combined in batches of eight pixels. Two aluminum layers are placed on top of the DEPFETs. Horizontally there are individual drain lines for every pixel and also two source lines. For the correct connection, this aluminum layer also contains connections

for the gate lines. Vertically, there are lines for clear, gate, drift, and source. Connections between the two aluminum layers are shown in turquoise, while connections to the DEPFET cells are shown in black. The individual drain lines are used to measure the current.

### 3.1.4 Pedestals

The measured drain current consists of two parts. The actual signal current is superimposed with an additional dark current, the pedestal current. The MOSFETs are operated in the on-state and therefore already exhibit a current even when no signal electrons are present in the internal gate. This pedestal current is slightly different for every pixel because of various reasons, such as inhomogeneous doping, tiny variations in the dimensions of each pixel and voltage drops for source, drain and gate because of the long metal lines. To get the actual signal, this pedestal current has to be subtracted from the full drain current. This can be done either by sampling the current twice — once with signal and once directly after the clear pulse — or done only once. This method of single sampling is viable for the PXD because of a low occupancy and used because of time constraints. The pedestals have to be stable to obtain an average pedestal current such that

$$I_{signal} = I_D - \langle I_{pedestal} \rangle \quad (1)$$

For single sampling, the analog-to-digital converters require a higher dynamic range compared to the double sampling, since they must resolve both the signal and the pedestal current.

### 3.1.5 Transconductance and Internal Amplification

The structure of the DEPFET introduces two gates, one is the MOSFET gate and the other is the internal gate. Both gates modulate the drain current. The DEPFETs are operated in the saturation region of the drain current. The full formula for the drain current in saturation is [8]:

$$I_D = -\frac{W}{2L}\mu_h C_{ox} \left( f \frac{Q_{sig}}{WLC_{ox}} + V_G - V_{th} \right)^2 \quad (2)$$

$W$  and  $L$  denote the width and the length of the transistor.  $f$  is the coupling factor between the internal gate and the p-channel with a value between 0 and 1 and  $\mu_h$  is the hole mobility.  $C_{ox}$  is the oxide capacitance per unit area and defined as:

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_{ox}}{d_{ox}} \quad (3)$$

where  $\varepsilon_0$  is the vacuum permittivity,  $\varepsilon_{ox}$  the dielectric constant of the oxide, and  $d_{ox}$  the oxide thickness.  $V_{th}$  is the threshold voltage for the transistor,  $V_G$  is the applied gate voltage and  $Q_{sig}$  is the signal charge accumulated in the internal gate. The gate voltage is applied by a power supply, while the internal gate depends only on charges produced inside the detection volume. This is why they are classified as external and internal amplification.

The external amplification, also called transconductance, is defined as:

$$g_m = \frac{\partial I_{\text{drain}}}{\partial V_{\text{gate}}} \quad (4)$$

It describes the dependence of the drain current on the applied gate voltage. For the DEPFET in saturation this relates to:

$$g_m = \frac{\partial I_{\text{drain}}}{\partial V_G} = -\frac{W}{L} \mu_h C_{\text{ox}} \left( f \frac{Q_{\text{in}}}{WLC_{\text{ox}}} + V_G - V_{\text{th}} \right) = \sqrt{\frac{2W\mu_h C_{\text{ox}}}{L}} \cdot I_D \quad (5)$$

The transconductance can be determined by applying different gate voltages to the DEPFET pixel and measuring the drain current.

The internal amplification, also referred to as charge gain, describes the dependence of the drain current on the electrons inside the internal gate.

$$g_q = \frac{\partial I_D}{\partial Q_{\text{sig}}} = -\frac{f\mu_h}{L^2} \left[ V_G - V_{\text{th}} + f \frac{Q_{\text{sig}}}{WLC_{\text{ox}}} \right] = f \sqrt{\frac{2\mu_h}{WL^3 C_{\text{ox}}}} \cdot I_D \quad (6)$$

To measure the internal amplification, the number of electrons accumulated in the internal gate must be known and the source current must be measured accordingly. This is most straightforwardly achieved using a gamma source of known energy. If the gamma ray deposits its energy inside the DEPFET pixel cell, the number of electrons can be calculated and the corresponding change in source current can be measured.

The external and internal amplification are related through the following equation:

$$g_q = g_m \frac{f}{WLC_{\text{ox}}} \quad (7)$$

### 3.2 Application-Specific Integrated Circuits (ASICs)

For control, readout and data handling of the DEPFET pixels custom-made ASICs are needed. They are located outside the sensitive area, but remain closely connected to the matrices. For the communication, all ASICs are configured with a Joint Test Action Group (JTAG) chain.

#### 3.2.1 Switcher and Readout

The switchers are used to control the states of the DEPFETs. They are configured with a switcher sequence, which consists of four different signals. A single switcher has 32 output channels for the clear and gate lines, with each line connected to four pixels at once (see Figure 7). The switcher sequentially cycles through all lines in rolling-shutter mode. The Gate line is enabled, the current is read out and then the Clear line is activated. The switcher then turns off the transistor and advances to the next row. For the hybrid5 assemblies, only one switcher is needed.



(ADU).

The DCD also features Current Memory Cells (CMCs), which function as cyclic ADCs and improve the performance of the pipeline ADCs by adding or subtracting current. These are calibrated in an ADC scan prior to measurements, using six adjustable settings: IPSource, IPSource2, IPSourceMiddle, IFBPBias, dcd-refin and dcd-amplo. A detailed explanation can be found in the manual [10]. The ADCs are calibrated concerning the following issues:

- Integral non-linearity: deviation of the real to the ideal ADC curve accumulated over the full range
- Differential non-linearity: deviation of the real to the ideal step width in the ADC curve
- Missing codes: an ADU value gets skipped
- Long codes: an ADU value is obtained for more than one current setting
- Offset errors: the ADC curve lies systematically above or below the ideal ADC curve
- Gain errors: the ADC curve has a different slope than the ideal ADC curve
- Bit errors: the ADC curve includes jumps because of wrongly assigned bits
- Noise errors: the used settings lead to a higher noise
- Reduced Range: the used settings lead to a reduced range of the ADC

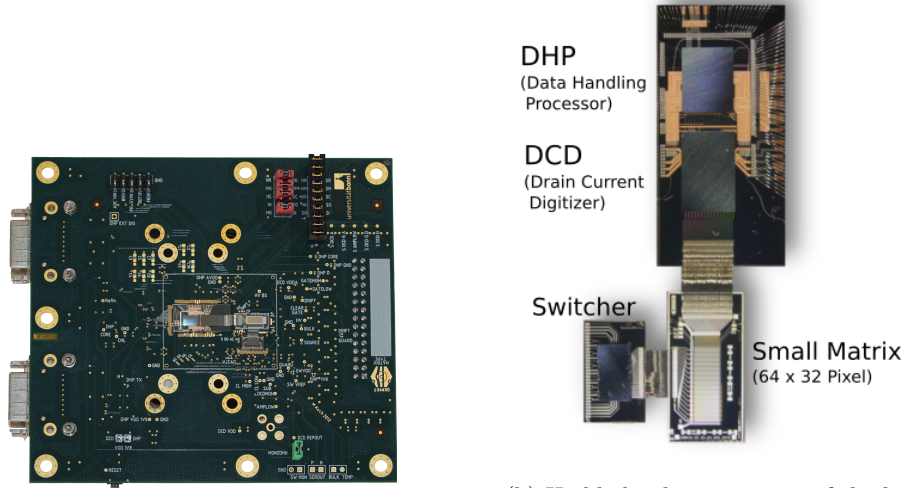
The ADCs can be calibrated with different current sources. The drain current can be used to calibrate the ADCs by changing the gate voltage. This scan takes only a short time, since all ADCs can be calibrated simultaneously. However, non-linear behavior has to be taken into account. Alternatively the DHE, which is explained in the following, features a current source, which can be calibrated and used for the ADC Scan. This scan takes more time, since only one ADC at a time can be measured, but it has a higher precision and a linear slope. With a calibrated DHE current source, this method can also be used to convert the ADU in Ampere.

### 3.2.3 Data Handling Processor (DHP)

The main task of the DHP is to preprocess the data and transmit it to the Data Handling Engine (DHE). It receives the signals from 256 DCD channels via 64 transfer lines and a dedicated submission protocol. The DHP applies pedestal subtraction and zero-suppression to discriminate hits from noise. Only signals above an adjustable threshold are selected for further processing. The DHP provides dedicated memory for pedestal values, DCD data, the switcher sequence, and individual pixel offset corrections (IPDAC). The switchers and the readout are controlled via JTAG, distributed by the DHP. It also performs common-mode correction by calculating the average noise of each quadruple row

segment and subtracting it from the signal. After preprocessing, the selected data is transmitted to the DHE via a high-speed link, while a JTAG connection between DHE and DHP provides the control communication.

### 3.3 Module Structure



(a) Full assembled hybrid5 module [11]. The DHE connections are on the left, the power is supplied from the right. The matrix and the ASICs are located in the middle of the PCB.

(b) Highlighted components of the hybrid5 module [11]. The switcher is connected to the matrix from one side. The drain lines are connected to the DCD and the signal is further processed with the DHP.

Figure 9: Hybrid5 module. On the left: picture of the full module. On the right: matrix and ASICs. These parts are placed in the white square in the middle of the left picture.

The full assembly can be seen in Figure 9a. The data and control connections to the DHE are on the left side, while the connections to the power supply are on the right. The matrix and the ASICs are in the middle of the module and highlighted in Figure 9b.

The PXD9-type matrix has a size of 64 by 32 pixels, while the PXD13-type matrix has 80 by 32 pixels. Both matrices have a pixel size of  $50\text{ }\mu\text{m} \times 55\text{ }\mu\text{m}$ . The switcher is placed on one of the long sides of the matrix to steer the rolling shutter readout by sequentially applying Gate and Clear signals. It has a size of about  $1470 \times 3600\text{ }\mu\text{m}^2$  [7]. There are two different switcher versions in use, the one used in the Belle II experiment, Switcher v2.1, and a new one, Switcher v2.3. Switcher v2.3 is designed to mitigate vulnerability to prompt irradiation in beam loss events. The new one is used for the new PXD13-type matrices. On one of the short sides, wirebonds connect the drain lines to the DCD. Because of new wirebond adapters, the mapping for the old PXD9-type hybrids is different from that of the new PXD13-type. This mapping is important to ensure the correct assignment of matrix pixel to ADC readout channel. The other two



sides of the matrices are used to connect other voltages, such as drift and guard. The PXD13-type no longer features a bulk contact, and depletion is performed from the backside. This is also necessary due to the different thicknesses. The PXD9-type matrices have a thickness of about  $525\text{ }\mu\text{m}$ , while the active area is thinned to a thickness of about  $75\text{ }\mu\text{m}$  [12]. The new PXD13-type matrices have a thickness of about  $450\text{ }\mu\text{m}$ , requiring a higher depletion voltage, which would be even greater if depletion were performed from the front.

The DCD and DHP are both bump-bonded to a wirebond adapter and connected by metal lines. Both are supplied with necessary voltages via wirebonds. The DCD has a size of  $3240 \times 4969\text{ }\mu\text{m}^2$  [13] and the DHP has a size of  $3280 \times 4200\text{ }\mu\text{m}^2$  [11].

### 3.4 PXD13

Since the implementation of the PXD9 technology in the Belle II experiment, the Max Planck Semiconductor Laboratory (Halbleiterlabor, HLL) has carried out further studies and developments. The newest version is the PXD13 technology.

There are three different variations of the PXD13 technology (see Figure 10).

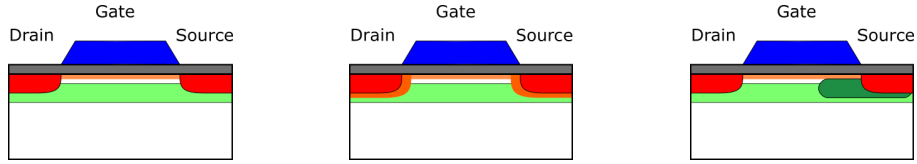


Figure 10: The variations of the new PXD13 DEPFET matrices. The standard PXD13 type on the left has the same dimensions as the PXD9 technology. Only the bulk thickness is higher and the bulk is depleted from the backside. The advanced PXD13 type has an additional HALO implant around the drain and source implant, which smoothes the electrical fields. The super- $g_q$  PXD13 type on the right has a deep n-implant located close to the source implant, which increases the charge gain. [14]

The first configuration is the standard PXD13 technology, it has the same dimension, for example gate length, pixel size and implant size, as the PXD9 technology. The only change is the matrix thickness, which increased to  $400\text{ }\mu\text{m}$  instead of  $75\text{ }\mu\text{m}$ . Also the depletion is no longer provided by a punch-through contact, but from a contact from the backside of the matrix. The new depletion should not affect the properties of the DEPFET pixel. Furthermore, the increased thickness should not affect the behavior of the DEPFET pixel, as it only adds material below the transistor and does not influence its electrical connections or fields. Therefore properties such as transconductance and internal amplification should remain the same as for the PXD9 matrices.

The second configuration is the advanced PXD13 technology. It has HALO implants around the drain and source implants. The HALO implants are p-doped areas, which have a lesser doping concentration than the drain and source implants and lead to a smoother field configuration. In this configuration, the internal amplification can be increased by about 10% [14].



The third configuration is the super- $g_q$  PxD13 technology. It has a highly doped n-implant close to the source implant. The sizes of the internal and external gates are decoupled, and accumulated electrons are confined to only a part of the channel. This increases the sensitivity of the drain current on a single electron and the internal amplification is estimated to reach values around 1.3 nA per electron, which is more than twice the estimated internal amplification of the PxD9 technology, at about 500 pA per electron [14].

In this thesis, the focus will mainly be on testing the standard PxD13 technology and comparing it to the PxD9 technology. The super- $g_q$  technology is currently under investigation, first results will be shown in the end of Chapter 5.

## 4 Static measurements of PXD9 matrices

Before getting to the measurements with the hybrid5, three of the PXD9-type matrices are investigated on a very basic level. The matrices are powered with common bench power supplies and a raw drain current is obtained. These measurements eliminate any possible effects from the ASICs and can be used to validate the measurements with the hybrid5.

### 4.1 Experimental Setup

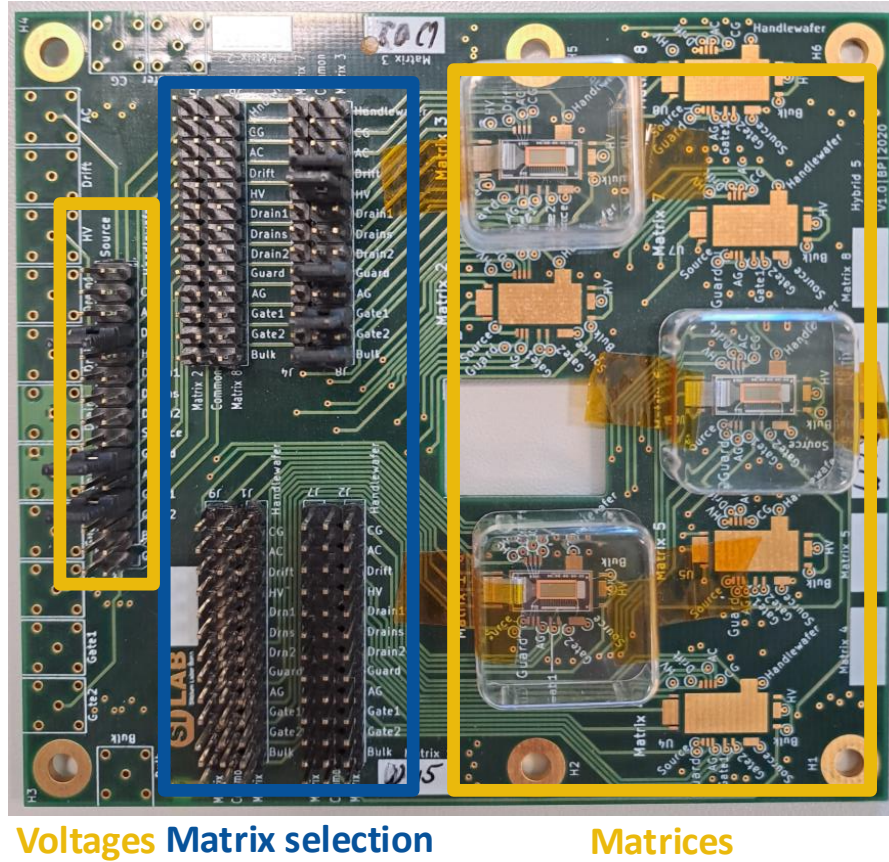


Figure 11: The test board for static measurements. Voltages can be applied on the left side, the matrices can be selected with jumpers and on the right the matrices are placed and connected.

For the static measurements, a dedicated test board is used. Instead of a PCB with all ASICs connected, this board only provides necessary electronic connections. The layout of the PCB is shown in Figure 11. The board provides eight possible slots for DEP-FET matrices, of which three are equipped during the studies. The slots are numbered from one to eight and contain matrices

from different wavers. Matrix one is from waver W45, matrix three is from waver W02 and matrix six is from waver W32. Only one matrix at a time can be activated by jumpers. The voltages are supplied via the pins on the left. As for the hybrid5, all voltages are referenced to source. Multiple SMUs are used to apply the voltages and measure the currents. Additional bench power supplies can be used to bias the matrix without measuring the current.

Since there is no DCD, the readout differs from that of the hybrid5. The drain

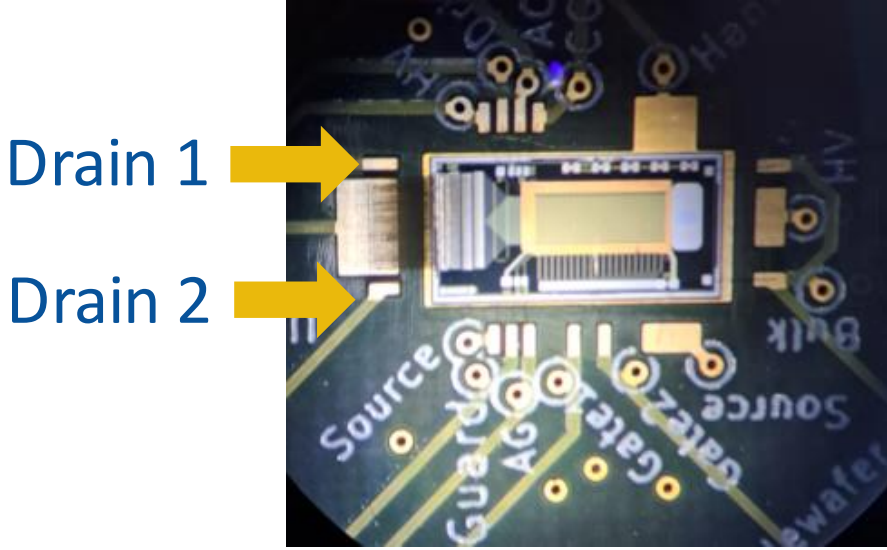


Figure 12: Close-up of a matrix on the test board for static measurements. The drain lines are connected on the left side. The voltages are applied on all sides of the matrix, for example bulk from the right, Gate1 from the bottom and AllClear (AC) from the top.

voltage can be applied in three different configurations. Two single drain lines (Drain1 and Drain2) are located on either side of the matrix and can be operated individually (see Figure 12). In addition, all other drain lines are combined into a single connection (Drains).

Connections also exist for All-Gate (AG) and All-Clear (AC) which change the voltages globally, and Gate1, which controls a single gate line. Lastly, the silicon bulk can be depleted using a high-voltage (HV) connection and a bulk connection.

The tests are performed inside a light-blocking box. The DEPFETs are sensitive to visible light, the photons are absorbed and lead to a higher source current, that could possibly damage the DEPFET, but also introduce noise. The measurements are performed at room temperature.

## 4.2 Gate IV measurements

To activate the transistor, two main voltages need to be applied. The drain voltage is set to  $-5\text{ V}$  and the Gate1 voltage is swept from  $5\text{ V}$  to  $-2\text{ V}$ . The

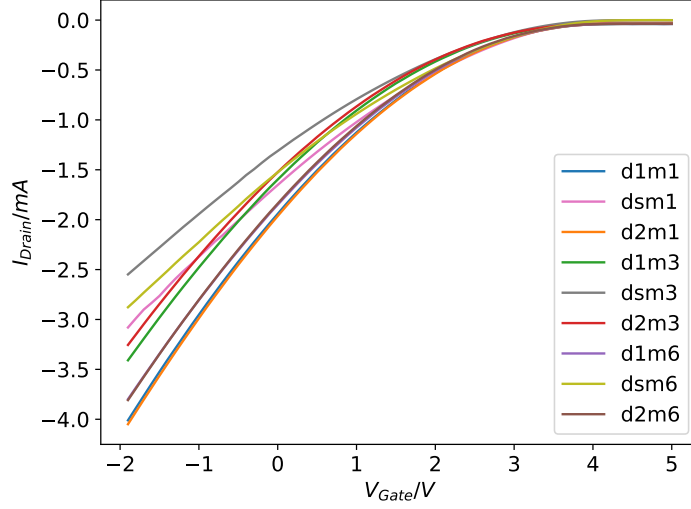


Figure 13: Gate IV curve for different configurations (matrix X as mX, drain 1, 2, or combined drain lines as d1, d2, ds). The current from the combined drain lines is normalized by a factor of 126. The drain current rises with a decreasing gate voltage.

resulting IV curves are shown in Figure 13. For visualization, the current of the combined drain lines is normalized by the number of connected drain lines, i.e. 126. The drain current rises non-linear with a decreasing gate voltage. The transistor is operated in the saturation regime for which Equation 2 is valid apart from correction terms. The non-linear behavior is therefore expected and it resembles a quadratic function with additional terms. The curves display variations in slope with a difference in drain current of up to 23% at  $-2$  V. There are various reasons for these differences. As shown by Equation 2, differences in gate width and length result in a modified drain current. The variation of the gate length for the PXD9 DEPFETs was measured to be up to 11% [15]. There are also variations in the oxide capacitance and the position of the internal gate, which also changes its capacitance. Furthermore, the matrices have a deviation in doping level of up to 23%. The deviations in doping happen between different wafers, but even for a single wafer, a ring structure in doping levels has been observed, which happens in the production [15]. These differences are much smaller for the single drain lines of the same matrix (see Figure 13). The combined drain lines differ from the single drain lines of the same matrix. The single drain lines lie on the outer edges of the matrix and experience edge effects. The current is not only affected by the inner part of the matrix, but also experiences leakage currents from the outside, which increase the current for the outer drain lines. This can be compensated with the established guard rings and partially with the bulk voltage. For the combined drain lines, the variations in transistor dimensions are also partly compensated by averaging over multiple pixels. Additionally, no AllGate voltage is applied so far, so the gate voltage of the pixels connected to the same drain line, but not the Gate1 line are floating and contribute to the drain current. This will be adjusted in the measurements later on.

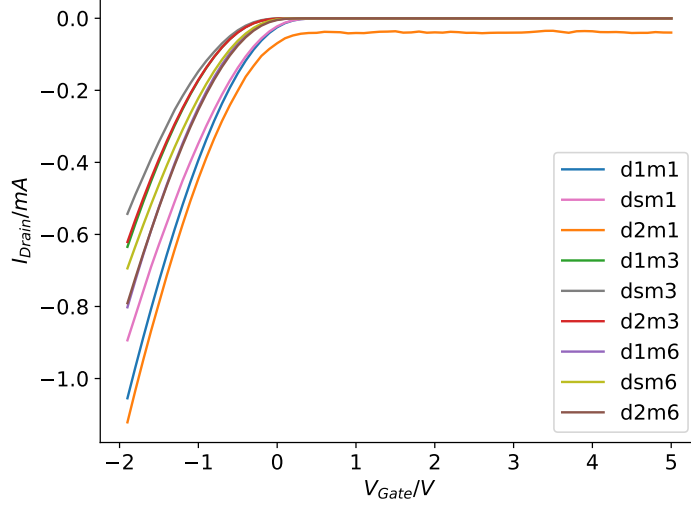


Figure 14: Gate IV curve for different configurations (matrix X as mX, drain 1, 2, or combined drain lines as d1, d2, ds) with a Clear voltage of 19 V applied. The current from the combined drain lines is normalized by a factor of 126. The drain current rises with a decreasing gate voltage. It displays a reduced current and an increased effective threshold voltage compared to the uncleared state.

In measurement with only gate and drain voltages applied, the internal gate accumulates electrons until it reaches saturation. The internal gate therefore modulates the drain current up to its maximum value. When a Clear voltage of 19 V is applied, as later used for the hybrid5, the internal gate is emptied. Because of the missing switcher, the clearing process occurs continuously, and the internal gate remains empty. This results in a reduced current and an increased effective threshold voltage (see Figure 14). The drain current still rises with a decreasing gate voltage. The drain current is reduced by a factor of four, the drain lines with the highest currents do not remain the same as for the uncleared state. This suggests that the internal gates differ between pixels, which affects the drain currents in the uncleared state. The variation of the drain current at  $-2$  V is up to 35%. The reasons are similar to those mentioned without the clear voltage applied. For this measurement, the internal gate should contribute less to the deviations, since it is emptied. However, since no ClearGate voltage is applied, the clear channel might establish differently than expected. Therefore the effectiveness of the clear process might also differ for the different pixels and lead to a variation in drain current.

To approximate more closely the actual state of the matrices on the hybrid5, additional voltages can be applied. In addition to the Clear voltage of 19 V, an AllGate voltage of 5 V is applied. This ensures that all transistors, except those connected to Gate1, are turned off. Additionally, a voltage of 10 V is applied to the bulk and  $-70$  V to HV. The results for the single drain lines are shown in Figure 15. Compared to the case where only the Clear voltage is applied, the

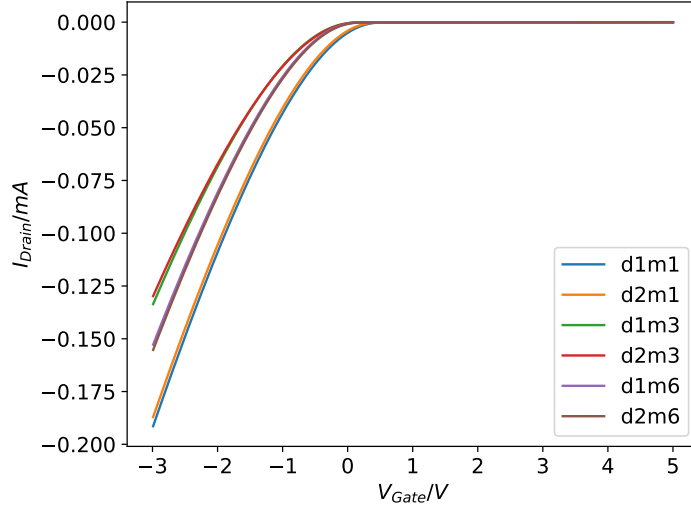


Figure 15: Drain-Gate IV curves for the single drain lines (drain 1 or 2, matrix mX) with the matrix fully biased. The Clear voltage is 19 V, AllGate is 5 V, bulk is 10 V and HV is  $-70$  V. The drain current increases with decreasing gate voltage.

current is further reduced due to the AllGate voltage. Because of the grid structure of the gate and drain lines, only a single pixel is turned on and measured. The drain current still rises with a decreasing gate voltage. The differences in the slope mostly vanish, but the effective threshold voltage is different for every pixel. This leads to a difference in drain current of about 19% at  $-3$  V. The difference within each matrix is only about 1%. Every matrix is powered with a high voltage of  $-70$  V, but the required voltage to deplete the silicon bulk depends strongly on the doping level. With the estimated changes in doping level of about 20%, this highly influences the Gate IV curve since the potential minimum is shifted depending on the voltage. If the voltage is too large or too small, the potential minimum will not overlap with the internal gate anymore and signal electrons are lost.

The high voltage also acts as a back gate for the transistor and shift the effective threshold voltage. For the small matrices, this difference becomes more prominent between different wavers, for the big PXD9 modules, this effect is visible within one module [15]. For the PXD9 modules, the working point is set around a drain current of  $-0.1$  mA. With the new settings, this current is reached at a gate voltage of about  $-2$  V. The working point varies across the different drain lines about 15%. This highlights that the pedestal current of each pixel at a given gate voltage differs and must be subtracted individually to isolate the signal.

Similar results are obtained for the combined drain lines. They are shown in Figure 16 without normalization. The current is strongly reduced compared to the previous voltage configuration and reaches a value of  $-12.6$  mA, which corresponds to the expected working point of the DEPFETs for 126 pixels.

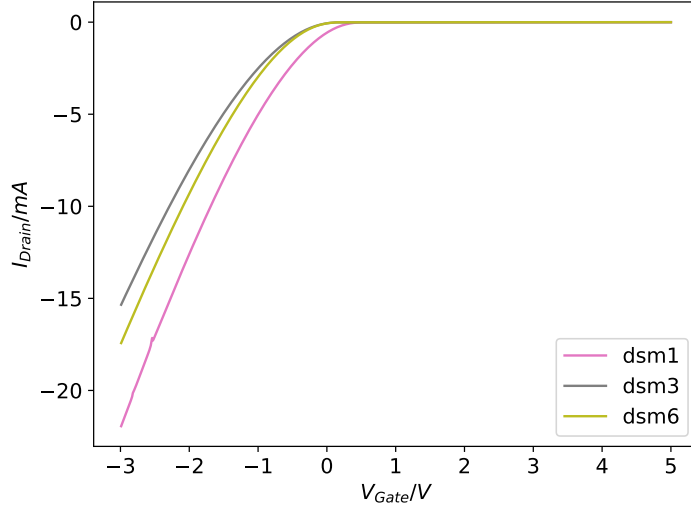


Figure 16: Drain-Gate IV curves for the combined drain lines (matrix mX) with the matrix fully biased. The Clear voltage is 19 V, AllGate is 5 V, bulk is 10 V and HV is  $-70$  V. The drain current increases with decreasing gate voltage.

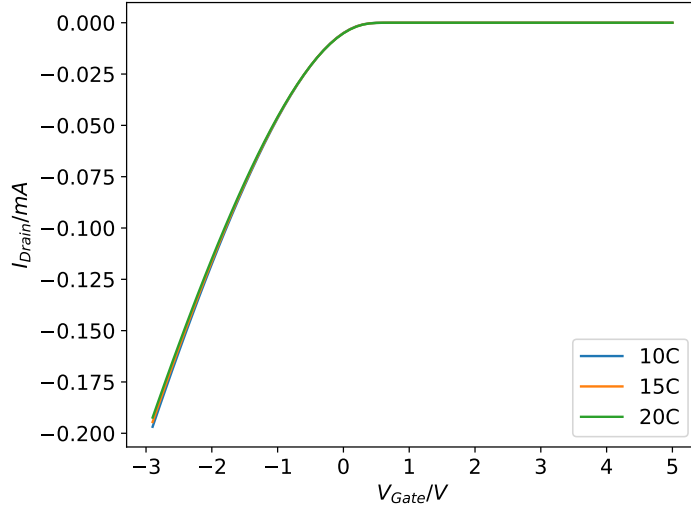


Figure 17: Drain-Gate IV curve for matrix one, drain one, at different temperatures with the matrix fully biased. The Clear voltage is 19 V, AllGate is 5 V, bulk is 10 V and HV is  $-70$  V. The IV curve changes only marginally with temperature.

The previous measurements were performed at room temperature. It is important to verify that the uncontrolled temperature does not affect the mea-

surements. Therefore, the fully biased matrices were also tested in a climate chamber (the same climate chamber as in Chapter 6) at three different temperature settings. The results are shown in Figure 17. The three curves change only by about 1%, which is a much smaller difference than the differences between the matrices (for example in Figure 15). Therefore, it is sufficient to measure the matrices at room temperature without active temperature control.

#### 4.2.1 Transconductance

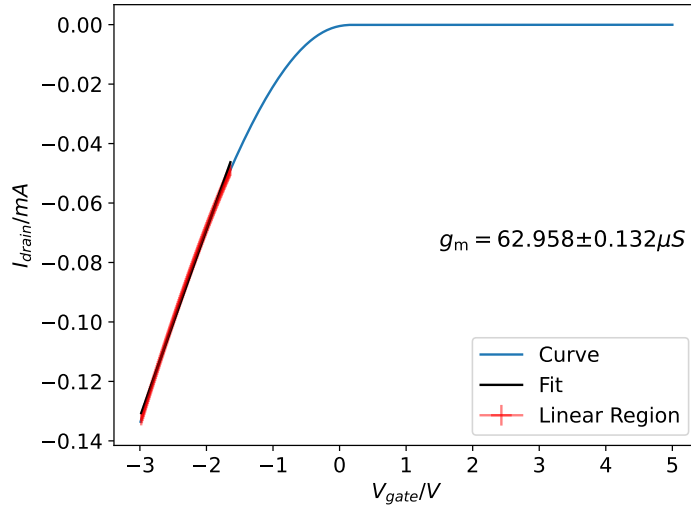


Figure 18: Drain-Gate IV curve for matrix 3, drain 1 with the matrix fully biased. The Clear voltage is 19 V, AllGate is 5 V, bulk is 10 V, and HV is  $-70$  V. The curve allows the extraction of the transconductance  $g_m$  by applying a linear fit at the working point.

The Drain-Gate IV curves for the fully biased configuration can be used to determine properties of the DEPFETs. As explained in Chapter 3, one such property is the transconductance. It is defined as the variation of the drain current with respect to the applied gate voltage. The value of the transconductance at the working point can be obtained from the IV curves by applying a linear fit. An example is shown in Figure 18. The fit yields a transconductance of  $g_m = (62.958 \pm 0.132)$ ,  $\mu\text{S}$ . The results for all configurations can be found in Table 1. The mean transconductance of  $g_m = (69.611 \pm 7.288)$ ,  $\mu\text{S}$  can later be compared to measurements performed with the hybrid5.

#### 4.2.2 Threshold voltage

Additionally, the Drain-Gate IV curves can be used to determine the effective threshold voltage. When plotting the square root of the drain current against the gate voltage, the effective threshold voltage can be obtained by extrapolating the



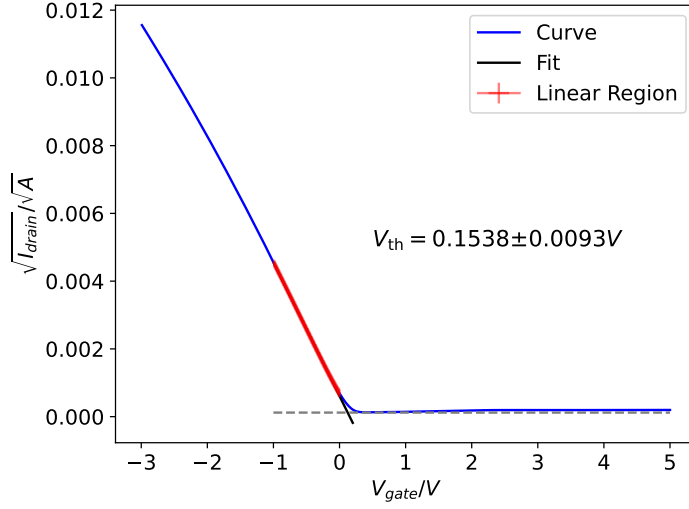


Figure 19: Square root of the drain current against gate voltage for matrix 3, drain 1 with the matrix fully biased. The Clear voltage is 19 V, AllGate is 5 V, bulk is 10 V, and HV is  $-70$  V. The curve allows the extraction of the threshold voltage by extrapolating to the zero crossing.

baseline of the transistor current and calculating its intersection with the linear fit at low gate voltages. This is a consequence of the drain current equation in the saturation regime:

$$I_D = -\frac{W}{2L}\mu_h C_{\text{ox}} \left( f \frac{Q_{\text{sig}}}{WLC_{\text{ox}}} + V_G - V_{\text{th}} \right)^2 \quad (8)$$

This method is shown in Figure 19 for matrix three drain one and yields an effective threshold voltage of about  $V_{\text{th}} = 0.1538(93)$  V. The threshold voltage indicates the gate voltage at which the transistor switches to the on state. The results for the different pixels are presented in Table 1, the mean effective threshold voltage is  $0.2860(1692)$  V. Typically, a p-channel MOSFET has a negative gate threshold voltage. However, the backside of the DEPFETs also acts as an additional gate for the p-channel, effectively reducing the required threshold voltage. Therefore, the effective threshold voltage can even become positive. The variation of the effective threshold voltage depends on the silicon dioxide along with the other explanations as before. The silicon dioxide sits between the gate and the p-channel and its thickness affects how many mirror charges build up inside the p-channel. A thicker dioxide leads to less mirror charges for the same applied voltage and the voltage has to be increased to activate the p-channel.

### 4.3 Clear IV measurements

Apart from the influence of the external gate, the drain current also changes because of the internal gate. In the unbiased case, the internal gate was satu-

#### 4 STATIC MEASUREMENTS OF PXD9 MATRICES

| Matrix/Drain | $g_m/\mu\text{S}$  | $V_{th}/\text{V}$   |
|--------------|--------------------|---------------------|
| m1d1         | $78.237 \pm 0.099$ | $0.5299 \pm 0.0052$ |
| m1d2         | $77.205 \pm 0.098$ | $0.4745 \pm 0.0053$ |
| m3d1         | $62.958 \pm 0.132$ | $0.1538 \pm 0.0093$ |
| m3d2         | $60.195 \pm 0.126$ | $0.1760 \pm 0.0092$ |
| m6d1         | $69.048 \pm 0.116$ | $0.1794 \pm 0.0074$ |
| m6d2         | $70.023 \pm 0.117$ | $0.2027 \pm 0.0072$ |
| mean         | $69.611 \pm 7.288$ | $0.2860 \pm 0.1692$ |

Table 1: Transconductance and effective threshold voltage for the single drain lines of each matrix.

rated and a higher current was measured than for the biased case, where the internal gate was empty. This change can also be quantified by changing the clear voltage and measuring the drain current. For this measurement, the gate voltage is set for every matrix and every drain individually to the working point of  $-100\text{ }\mu\text{A}$  for a clear voltage of 19 V. All the other voltages are set as for the biased measurement. The clear voltage sweeps from 19 to 1 V to start with an empty internal gate that slowly fills with electrons. The settling time is 10 s since lower settling times reduced the reproducibility. The reproducibility also determines the sweep direction, the clear voltage is swept from positive values to zero since the results differed when the measurement was taken from zero to positive values multiple times. Therefore, the internal gate should start in a well known empty state.

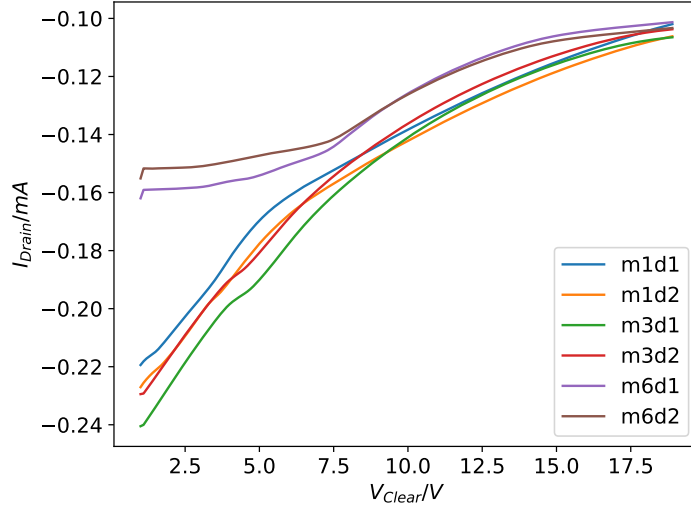


Figure 20: Drain current against clear voltage for the single drain lines with the matrix fully biased. The Gate voltage is set to a value where the drain current equals the working point of  $-100\text{ }\mu\text{A}$ , AllGate is 5 V, bulk is 10 V, and HV is  $-70\text{ V}$ . The drain current rises with a lower clear voltage.

The IV curves for the single drain lines are shown in Figure 20. The current increases with decreasing clear voltage, as expected, since the internal gate accumulates electrons. The drain current has a quadratic dependence on the charges deposited in the internal gate 2. The drain current follows a quadratic dependence with additional contributions by other effects, only matrix six deviates from this behavior. The internal gate cannot accumulate as many electrons as in matrix one or three, and the current saturates before reaching a clear voltage of zero. The deviations of the drain current for matrix one and three from a pure quadratic dependence may arise from the clearing process. The Clear-Gate contact is floating, such that the channel between the internal gate and the clear implant does not establish the same way as with a ClearGate voltage applied. This influences the effectiveness of the clear process. Further on, every internal gate is cleared with two clear implants (visible in Figure 6), the two clear channels that are established lead to an overlap of two clear curves. This further alters the clear curve from a pure quadratic dependence, in case the two clear channels are different, for example due to dimensional variations. Additionally, all matrices are depleted with a high voltage of  $-70$  V. Due to the doping variations, this can lead to an over or under depletion. When the silicon bulk is over or under depleted, the potential minimum no longer overlaps with the internal gate and less electrons are accumulated. Since this measurement specifically measures the influence of the internal gate, this deviation should be more visible in this measurement and could explain the saturation of matrix six. All of these effects can lead to a deviation from a pure quadratic dependence.

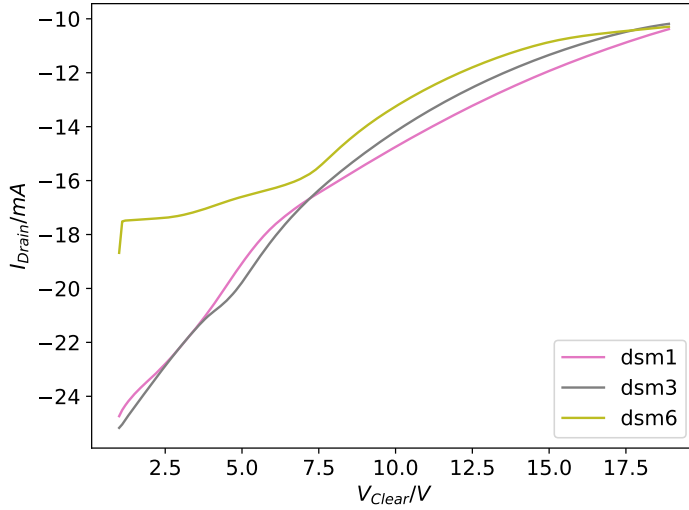


Figure 21: Drain current against clear voltage for the combined drain lines with the matrix fully biased. The Gate voltage is set to a value where the drain current equals the working point of  $-100$   $\mu A$ , AllGate is  $5$  V, bulk is  $10$  V, and HV is  $-70$  V. The drain current rises with a lower clear voltage.

These deviations are also visible for the combined drain lines (see Figure 21). The saturation effect of matrix six persists for the combined drain lines. The

deviations from the pure quadratic dependence also remain.

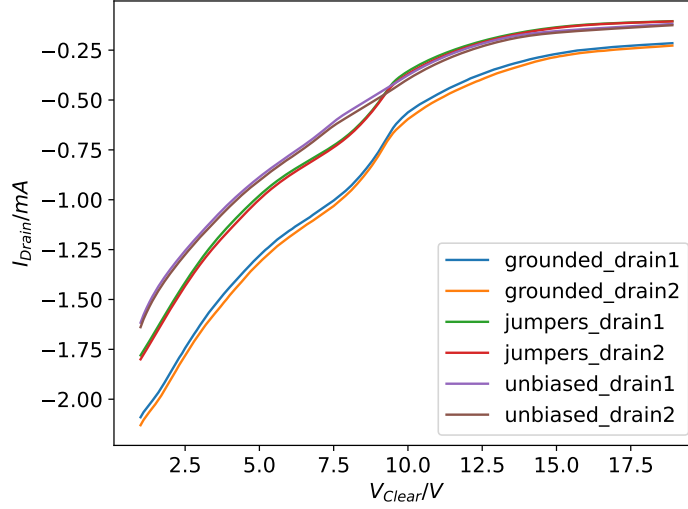


Figure 22: Drain current against clear voltage for matrix one, drain one or two with the matrix unbiased. Gate is  $-1$  V. AllGate, bulk, HV are either floating (unbiased), all set to source (jumpers) or set to source and source is grounded (grounded). The drain current rises with a lower clear voltage, the different configurations change the shape of the curves.

To get a deeper understanding of the deviations, the matrix is biased differently than before. The possible influence of additional voltages is removed by keeping all biasing voltages floating or at a fixed ground. The results in Figure 22 are for matrix one. This time the gate voltage is fixed to  $-1$  V, since the working point of  $-100$   $\mu$ A is achieved at very different voltages, making the curves not easily comparable. The case, where only gate, drain and clear are applied, shows only slight variations from a quadratic dependence. As soon as the other voltages are not floating anymore, but are fixed to the source potential, the deviations are much more pronounced. Furthermore, when the source is grounded, the deviation becomes even more pronounced and the current increases for all clear voltages. This again suggests that the potentials inside the DEPFET pixel influence both the internal gate and the channel that forms between the internal gate and the clear implant.

Similar DEPFET pixels were tested by the Semiconductor Laboratory of the Max Planck Society [16]. The Drain-Gate IV curves of the standard devices resemble the IV curves measured in the previous section (see Figure 23). However, the respective clear curve for the standard device does not show the same shape. The clear curve shows a kink at one specific voltage, which indicates that the channel between the internal gate and the clear implant is fully established. This kink is not visible for the measured clear curves and the multiple changes in slope are also missing from the curves measured by the Max Planck Society. It was not possible to retrieve the exact measurement configuration from the

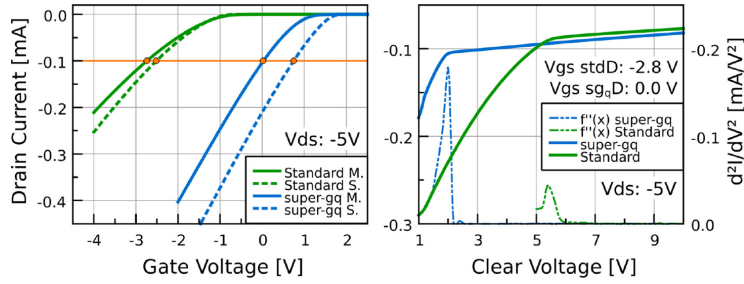


Figure 23: On the left: Drain-Gate IV curve for the new super- $g_q$  device and the standard device. The standard device has a similar IV curve as in the previous section. On the right: Drain-Clear IV curve for both devices and the second order derivative. The knee point of the curve indicates an empty internal gate. [16]

corresponding paper, and the setup might therefore differ. Especially an applied ClearGate voltage could alter the clearing process. The shape differences and the influence of other voltages on the clearing behavior of the pixel should be further investigated and the results of the super- $g_q$  device should be checked.

#### 4.4 Depletion and leakage currents

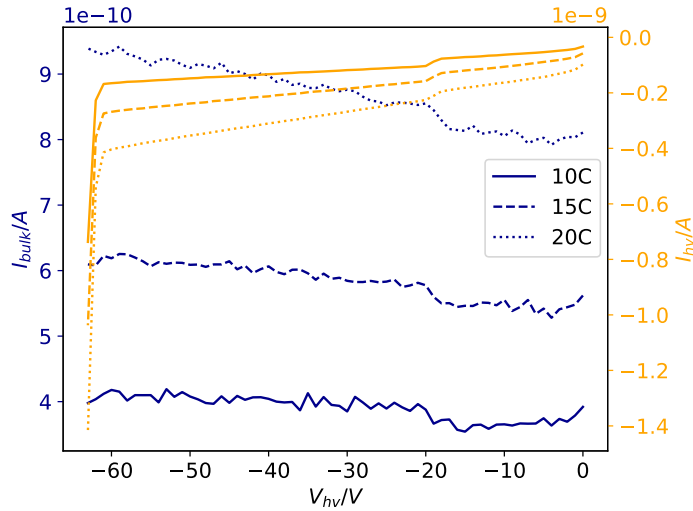


Figure 24: Bulk and HV current for matrix one for different high voltages and different temperatures. The backside is reached at about  $-20$  V, full depletion happens at about  $-64$  V. The temperature has a significant effect on the currents.

Lastly, the electronic tests can be used to measure the depletion of the DEPFET pixels. Due to the currents in the range of nanoampere, these mea-

surements are much more sensitive than the previous ones. Therefore the setup has to be moved inside a dark climate chamber (more information about the climate chamber can be found in Chapter 6). For this measurement, only the bulk properties are important and all voltages of the FET are not needed. Guard and drift are set to source and bulk is set to 10 V. HV is swept from 0 V to  $-65$  V in 1 V steps and a settling time of 10 s. The temperature is either 10, 15 or 20 degrees. The results for matrix one are shown in Figure 24. For a decreasing high voltage, the currents change only slightly because of the high resistance silicon bulk. At about  $-20$  V, the depletion reaches the backside (compare to explanation in Chapter 3 and Figure 4) and the HV current increases. This current flows between bulk and HV. A further decrease in high-voltage changes the current marginally until the depletion reaches the front side. Then the current increases a lot as explained in Figure 5. The ideal high voltage for depletion has to be determined later with a source scan. The source scan is sensitive to the depletion and the high voltage can be adjusted.

The different temperatures have a high impact on the actual amplitude of the current, but they do not affect the shape. To actively suppress the electrons in overcoming the potential barrier, the temperature has to be much lower. The leakage current are expected to have an exponential dependence on the temperature, by Figure 24 it becomes clear, that the dependency for this measurement is also non-linear, since the difference for 10 to 15 degrees is higher than for 15 to 20 degrees by a factor of about 1.6.

## 5 Hybrid5 Measurements for PXD9 and PXD13

The measurements in this chapter are done with the hybrid5 H5026, which is equipped with a minimatrix of the PXD9 technology and the hybrid H5033, which is equipped with a minimatrix of PXD13 standard technology. The results will feature the pedestals of each hybrid, the DCD optimization and calibration, DEPFET IV curves and the transconductance as well as source measurements. For H5033 additionally the response to the depletion voltage is measured, for H5026 an energy calibration is performed and the internal amplification is determined.

In the end of this chapter some first result for H5034 will be presented. H5034 is equipped with a minimatrix of the super $g_q$  PXD13 technology.

### 5.1 Experimental Setup

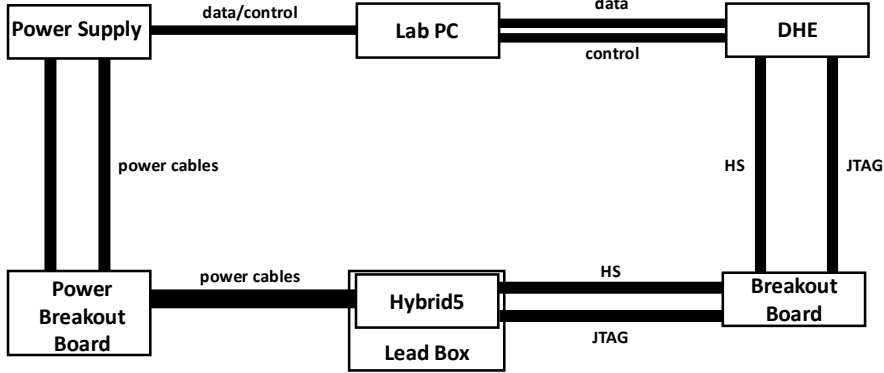


Figure 25: Sketch of the hybrid5 setup. The module is placed inside a lead box and connected to the power supply and the DHE. For both connections an additional breakout board is used to convert different cable types. The power supply and the DHE communicate with a PC to receive commands and provide data.

The lab setup consists of all essential components of the actual PXD detector for Belle II and uses the same framework and GUI. This ensures that all measurements and tests can be performed on a smaller scale while still producing results that are comparable to those of the full detector.

Figure 25 presents a schematic overview of the setup, while Figure 26 shows a photograph of the hybrid outside the lead box. A view of the hybrid5 module inside the lead box is provided in Figure 27. The lead box shields the environment from the radioactive sources used in matrix measurements. It also protects the matrices from light exposure and is covered with a black cloth to further reduce incoming light. The box has two outlets, one is used for the communication with the hybrid5 and one is used for supplying power to the module.

Power is provided by a custom-made power supply (LMUPS). It is operated at a base voltage of 24V which is delivered by a commercial bench power supply. The LMUPS is controlled from a Lab-PC via Ethernet. It features two outputs

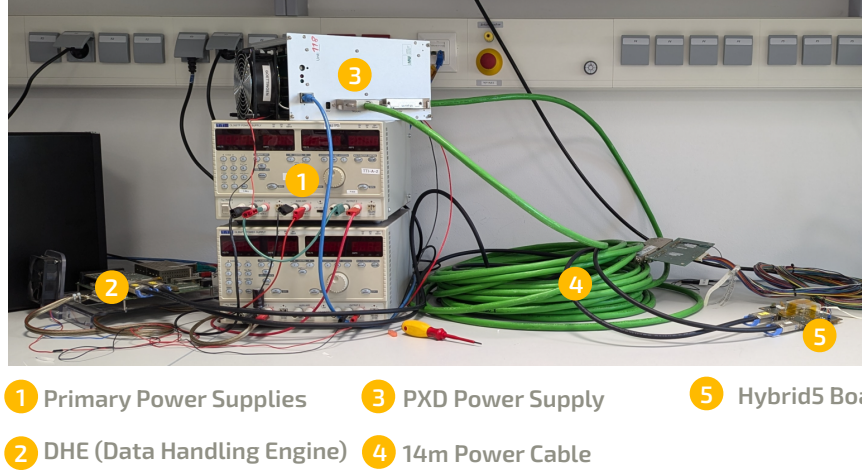


Figure 26: Photo of the hybrid5 setup. The module is connected to the power supply with 14m long power cables. The power supply is connected to two primary power supplies. Further on, the hybrid5 is connected to the DHE for data exchange. [17]



Figure 27: Photo of the hybrid5 inside the lead box. The data and control cables to the DHE are connected from the left. The power supply is connected from the right. The minimatrix is shielded with a cover to prevent damages to the wirebonds

for the analog and digital domains, which are connected to a power breakout board through two 14 m-long cables identical to those employed in Belle II. From the breakout board, the supply is routed directly to the hybrid5. Due to



design modifications during development, an additional jumper cable is required to deliver the correct voltage to the switcher.

Communication between the hybrid5 and the Lab-PC is established via the DHE. The DHE connects to the Lab-PC through two Ethernet links, one dedicated to data transmission and the other to control signals. The DHE is connected to the hybrid5 by a high-speed data line and a lower-rate control line. Control signals are routed through a JTAG breakout board, which is required due to design changes for the DHE and modification to the transmission of the control line. The breakout board requires 3.3 V, while the DHE itself operates at 5.2 V, both are supplied by a second commercial power supply. The power supplies are connected to the Lab-PC via USB, enabling remote control.

To measure the internal amplification, the setup is extended with a source holder. The source holder has an adjustable height and a central opening to mount the radioactive source. Measurements are performed at various photon energies using the sources listed in Table 2. Copper, barium and terbium are excited by an americium source and emit characteristic x-rays. The  $^{55}\text{Fe}$  source decays into manganese, which produces characteristic x-rays. The  $^{109}\text{Cd}$  source decays into silver, also leading to characteristic x-ray emission. Finally, the  $^{241}\text{Am}$  source undergoes  $\alpha$ -decay, populating excited states of  $^{237}\text{Np}$ . The neptunium de-excites by emitting  $\gamma$ -rays.

| Element           | origin of $\gamma$ -rays               | expected energy/keV |
|-------------------|----------------------------------------|---------------------|
| $^{55}\text{Fe}$  | $K_{\alpha}$ ( $^{55}\text{Mn}$ )      | 5.899               |
| Cu                | $K_{\alpha}$                           | 8.048               |
| $^{109}\text{Cd}$ | $K_{\alpha}$ ( $^{109}\text{Ag}$ )     | 22.163              |
| Ba                | $K_{\alpha}$                           | 32.194              |
| Tb                | $K_{\alpha}$                           | 44.483              |
| $^{241}\text{Am}$ | nuclear emission ( $^{237}\text{Np}$ ) | 59.541              |

Table 2: List of the sources used in the measurements, the origin of  $\gamma$ -rays and the expected energy [18][19].

For the PXD13 matrices, the LMUPS cannot provide the required high voltage to deplete the silicon bulk. This voltage is therefore applied using an external source measuring unit (SMU). A small PCB is inserted into the analog voltage line, allowing external voltages to be applied (see Figure 28). The PCB can be connected to either the analog or digital voltage output of the power supply. Since the high voltage is part of the analog domain, the PCB is placed between the analog voltage output and the connector cable. The high voltage is applied between HV and Steer GND, while the original high-voltage line is disconnected. Steer GND shares the same potential as the source. All other voltages remain unaffected.

## 5.2 HV IV curves

Using the external SMU, an HV IV curve of the PXD13 minimatrix can be recorded (see Figure 29). The high voltage is swept from 0 to  $-160\text{ V}$  in 1 V steps with a settling time of 10 s. Since the silicon bulk thickness has increased

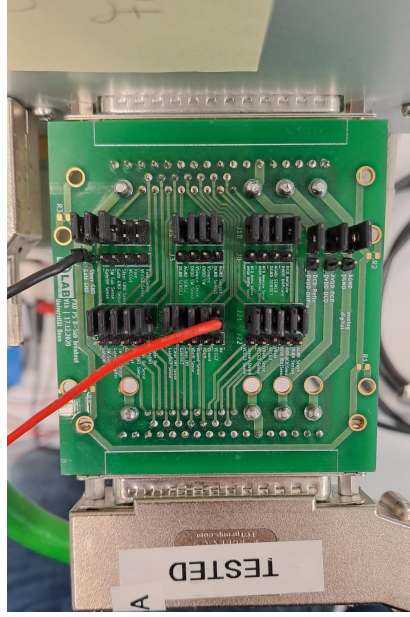


Figure 28: A small PCB is used to apply an external high voltage. The PCB is connected to the analog voltage output of the power supply, the high voltage is applied between HV and Steer Ground, while the actual high voltage line is disconnected. Steer Ground is on the same potential as source.

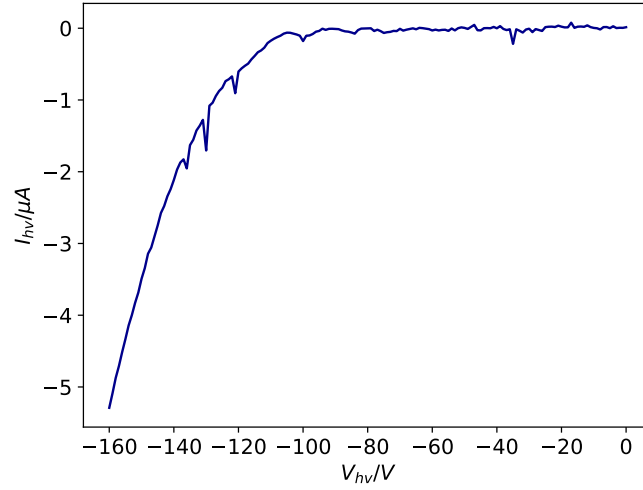


Figure 29: HV IV curve for the PXD13 matrix. The current remains constant up to approximately  $-110$  V, where a pronounced increase is observed.

from  $75\ \mu\text{m}$  to  $450\ \mu\text{m}$ , the depletion voltage is expected to be higher than for PXD9. In the PXD13 minimatrix, depletion no longer occurs from the front side via the punch-through contact but instead proceeds from the backside.

This reduces the required voltage, as the depletion front traverses the bulk only once. The IV curve displays a constant current up to about  $-110$  V, after which the depletion reaches the front side and the current rises sharply. The optimal depletion voltage will be determined later with the source scan, which reveals signal losses in cases of over- or under-depletion. Compared to the static measurements of the PXD9 minimatrices (see Figure 24), the onset of the high-voltage current increase shifts from  $-63$  V to  $-110$  V. Furthermore, the current spike observed near  $-20$  V disappears due to the different depletion approach. The IV curve also shows deviations from the overall trend at certain voltages, suggesting that the settling time of 10 s may not be sufficient for the thicker silicon bulk. Electrons and holes require additional time to adjust to the newly applied electric field according to their mobilities.

### 5.3 Pedestal Scan

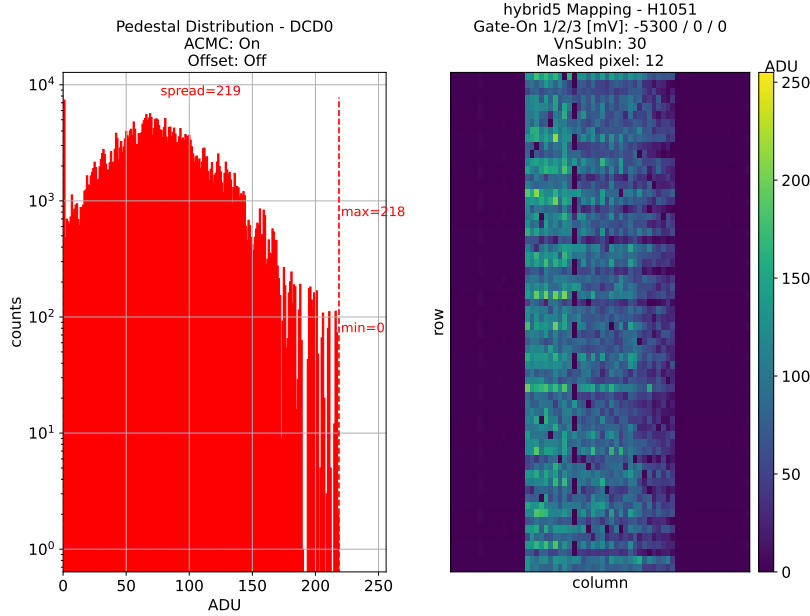


Figure 30: Pedestal distribution for the PXD9 minimatrix of H5026 for a gate voltage of  $-5300$  mV. ACMC is turned on, Offsets are turned off. The pedestals are distributed around 75 ADU. The pedestals decrease with columns to the right side.

The hybrid5 setup enables the extraction of pedestals for all DEPFET pixels in a single measurement. The pedestal current is the dark current of the DEPFETs. Figure 30 presents the pedestal distribution of H5026, equipped with a PXD9 minimatrix, in arbitrary units (ADU). At the top of the plot, additional measurement parameters are listed. These pedestals were recorded at a Gate-On 1 voltage of  $-5300$  mV (Gate-on 2 and 3 unconnected) and a VnSubIn value of 30. The Analog Common Mode Correction (ACMC) was en-

abled, while offsets remained disabled. The distribution peaks around 75 ADU and decreases towards both sides. Most pixels remain below 150 ADU (note the logarithmic y-axis). The maximum pedestal is 218 ADU, the minimum zero ADU. The distribution is asymmetric. The DCD records the pedestal current over multiple frames, 200 in this case. Every pedestal current can be mapped to a single pixel and the mean value of the 200 frames for every pixel is shown on the right side of Figure 30 in ADU. Since the PXD9 matrix provides only 128 drain lines instead of the 256 possible DCD channels, the outer columns remain unconnected and are not measured. Ideally, the pedestal distribution is as homogeneous as possible to ensure a correct signal measurement. There must remain sufficient head space for the signal to add to the drain current without saturating the DCD, and the drain current should lie near the middle of the DCD's dynamic range, where the linearity of the DCD is optimal (see Section 5.4).

The pixel map of the pedestal current reveals a column-wise decrease of the pedestal current from left to right. This happens because of voltage drops along the metal lines that supply the gate voltage. The last columns do not see the full  $-5300$  mV that are applied to the gate lines, leading to a lower drain current. APMC partly compensates for this effect. However, the module was irradiated up to 2 Mrad, creating oxide traps in the gate oxide that shift the threshold voltage towards lower values [20]. As the absolute applied voltage increases, the voltage drop along the gate line also increases and cannot be fully corrected by APMC.

In column eleven, pairs of two pixels exhibit a pedestal current followed by two pixels without signal. This is caused by two dead drain lines that run vertically across the matrix and connect to every fourth pixel. This artifact will remain visible throughout all subsequent measurements.

The pedestals depend on the applied Gate-On voltage, when the Gate-On voltage is further decreased, the drain current increases and the pedestals are shifted to higher values (see Equation 2). When the Gate-On voltage is increased, the drain current decreases and the pedestals shift to lower values. The DEPFET working point is set to about  $100\text{ }\mu\text{A}$  per pixel, this determines the Gate-On voltage. Because this module is irradiated, it requires a lower Gate-On voltage than a non-irradiated module. Unless otherwise stated, all following measurements with H5026 use a Gate-On voltage of  $-5300$  mV.

The drain current must be adjusted before entering the DCD (as explained with Figure 8). Prior to APMC, pedestals are shifted within the dynamic range by using the VNSubIn current sink. A higher VNSubIn value shifts the pedestals to the left, while a lower VNSubIn value shifts the pedestals to the right. The effect is partially removed by APMC, which is applied after VNSubIn (see Section 3.2.2). For H5026, APMC leads to a more narrow distribution and is therefore enabled.

Figure 31 displays the pedestals of H5033, equipped with a standard PXD13 minimatrix, at a Gate-on voltage of  $-3700$  mV. APMC and offsets were disabled. The matrix has 20 gates instead of 16 gates as for the PXD9 minimatrix. Therefore, the switcher uses a 32 gate sequence instead of a 16 gate sequence. This produces more rows in the matrix plot, while the number of columns remains fixed at 128 drain lines. The new hybrid5 H5033 also uses a new wirebond adapter, requiring an updated electronic mapping between drain lines and pix-

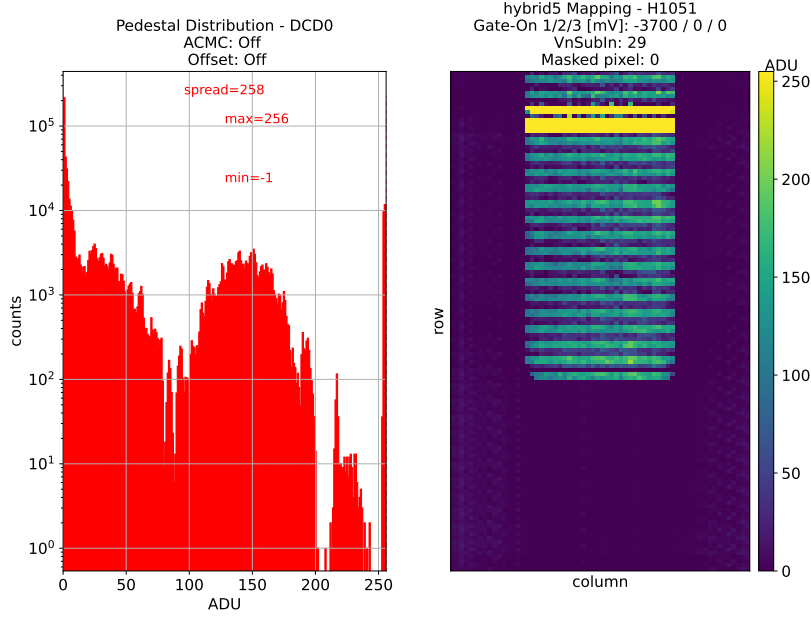


Figure 31: Pedestal distribution for the PXD13 minimatrix of H5033 for a gate voltage of  $-3700$  mV. ACMC and Offsets are turned off. The pedestals show a double row pattern with one peak at about 150 ADU and one around 20 ADU. Furthermore some of the pixels are saturated.

els.

The pedestal distribution exhibits two peaks (near 20 and 150 ADU) instead of a single peak as for the PXD9 minimatrix. This is also visible in the matrix plot, where a double row pattern arises. This pattern is created by differences in the source lines, which connect pixels in pairs of rows (see Figure 7 in Section 3.1.3) and affect the drain current. The differences of the source lines are under further investigations [14]. For the following tests, this double row effect should be compensated to improve measurement quality.

The tested PXD13 minimatrix also shows additional anomalies. In the upper half of the matrix, several rows of pixels reach 255 ADU, saturating the DCD and preventing measurements of the drain current. This behavior happens due to a short between the source and the clear metal layers, which are connected to the pixels. The short is an error that has been already introduced in the design of the standard PXD13 type matrices. The short directly affects four rows, but because the DCD cannot fully reset its state before the next current is measured in the rolling shutter mode, residual currents add to the next measurement, saturating additional pixels. This malfunction remains visible in all measurements with H5033.

The double row pattern can be mitigated with the offset compensation that uses the electronic components of the DCD introduced in Section 3.2.2. All drain currents are reduced by a constant amount via the VNSubIn current sink, and a multiple of the IPDAC current is individually added per pixel using a

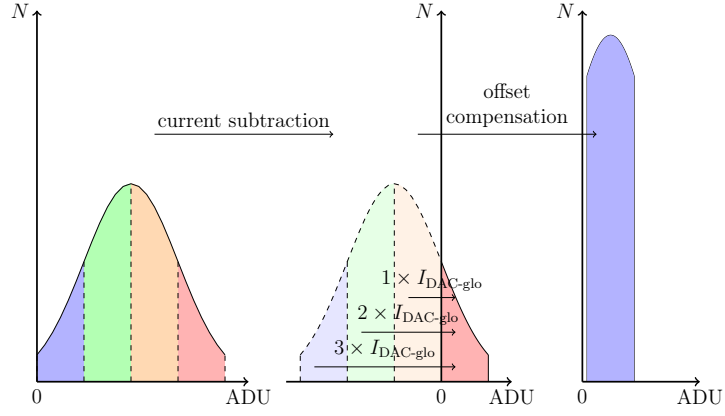


Figure 32: Working principle of the offset compensation [7]. All drain currents are reduced by a certain amount. Then a multiple of the current source IPDAC is added. This reduces the distribution width pixel-wise.

two bit register (see Figure 32). This narrows the distribution and corrects the double row pattern.

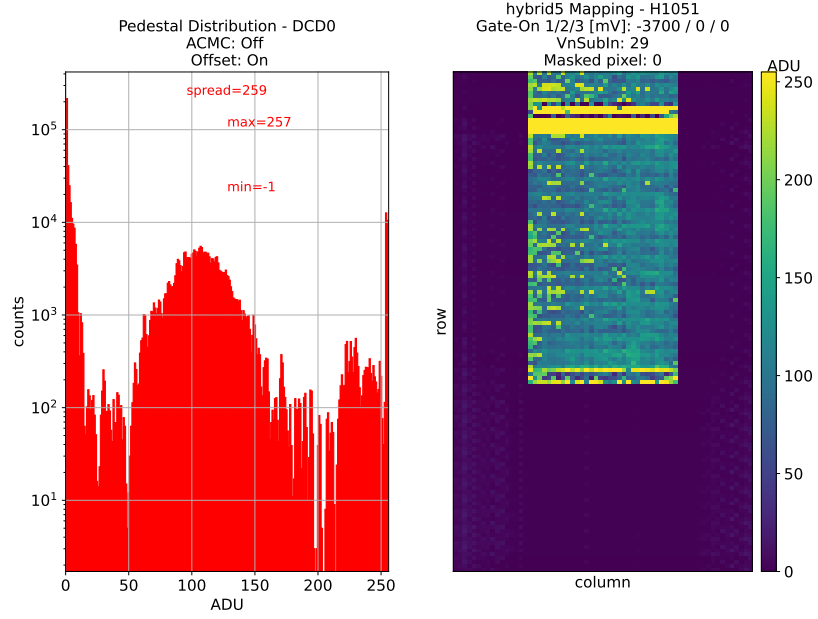


Figure 33: Pedestal distribution for the PXD13 minimatrix of H5033 for a gate voltage of  $-3700$  mV. APMC is turned off and Offsets are turned on. The pedestals show a peak around 100 ADU. The saturated pixels remain.

The results after offset compensation for H5033 are shown in Figure 33. The pedestal distribution now peaks around 100 ADU, and the double row pattern

disappears. Because the double rows had a difference of about 130 ADU, the required IPDAC current has to be high. The settings of the two bit register therefore have a greater impact than for smaller IPDAC values. As a result, neighboring pixels may differ up to 50 ADU even if their initial currents were nearly identical (see lighter dots in Figure 33). With a peak around 100 ADU, the pixels now provide sufficient head space to fit a signal and operate in the linear region of the DCD.

For the H5033, the APMC remains disabled. Due to the saturating pixels, the APMC does not work properly and instead shifts all pedestal values upwards. The current setting are sufficient to perform the required measurements.

## 5.4 ADC optimization

Prior to the following measurements, the ADCs must be optimized. As discussed in Section 3.2.2, six parameters have to be optimized to minimize ADC-related issues, such as INL, DNL and missing codes. For parameter optimization, the ADC scan uses the DEPFETs as a current source, as this method is approximately 100 times faster than using the DHE current source and the measurements are performed over a large parameter space. The gate voltage is swept across a range that covers the full dynamic range of the DCD. So at the highest gate voltage all pedestals should be at zero ADU and at the lowest gate voltage all pedestals should be at 255 ADU. For H5033, the defective pixels are excluded from the analysis.

The ADC scan follows a defined sequence. First IPSource and IPSource2 are optimized, followed by dcd-refin und dcd-amplo. After that, IFBPPBias is tuned and finally IPSourceMiddle. For each optimization step, all ADCs are graded with respect to the issues introduced in Section 3.2.2. The figure of merit is determined by the rating of the combined grades.

Figure 34 displays the ADC curve of a single channel from H5026. The activated gate for this measurement is gate zero. At a gate voltage of  $-4600$  mV, the output code of the DCD is close to zero. Around  $-5000$  mV, the output code rises with a pronounced curvature for about 100 mV and then it rises almost linear until it reaches the maximum value of 255 ADU at about  $-5600$  mV. The curvature of the ADC curve happens since the DEPFETs are used as a current source. Even though the measurements are taken far off the threshold of the DEPFET pixels and shifted out of the dynamic range with the VNSubIn current sink, the transfer characteristic of the DEPFET pixel is not linear. The pronounced curvature in the onset of the ADC curve also happens since the DCD is less linear for very low and very high ADU values. Since every DCD channel is measured with a different DEPFET pixel, the ADC curves start at different gate voltages. This is comparable to the gate IV curves of Chapter 4. Therefore a wide gate-voltage range must be scanned to capture all ADC curves. Apart from that, some of these curves have bit errors or behave non-linear, an example is shown in the appendix in Figure 70. These issues, discussed in more detail in Section 3.2.2, are minimized by the optimization scan, to get the reliable ADC response shown in Figure 34.

Figure 35 presents the ADC curve of a single channel from H5033. The

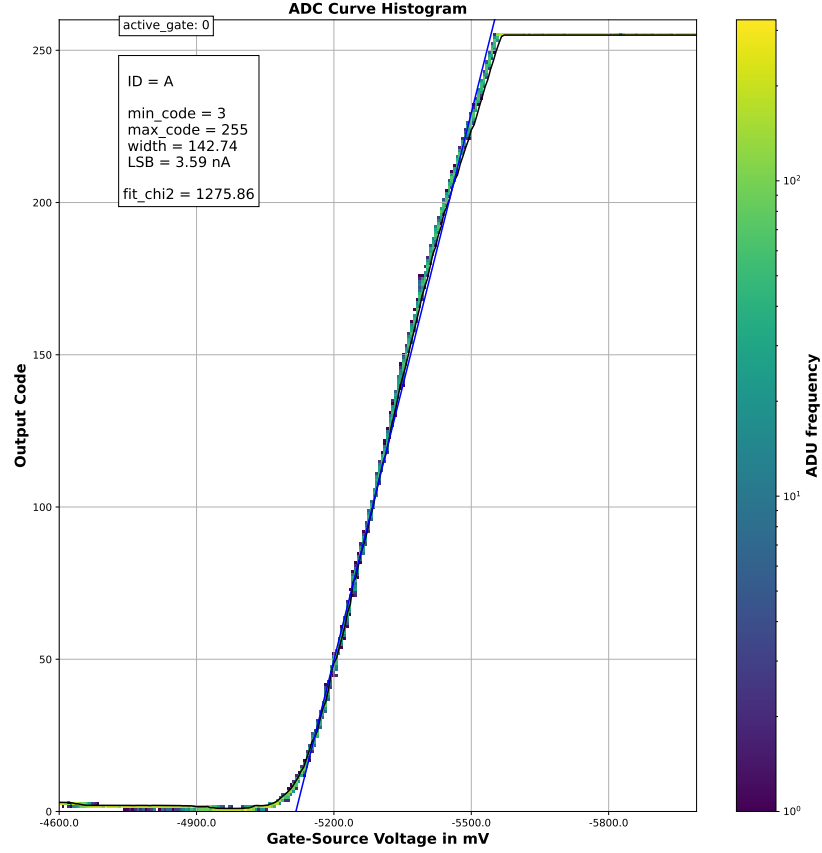


Figure 34: ADC curve of a single channel of H5026 using the DEPFETs as a current source. The ADC curve starts close to zero, a non-linear onset happens around  $-5000$  mV and after that the curve rises linearly until the cutoff at the maximum of 255 ADU.

activated gate for this measurement is gate 16. The gate-voltage range differs from the previous measurement with H5026. H5034 is not irradiated, resulting in a working point at a higher gate voltage than for H5026. The scan is performed close to the working point. For H5033, at a gate voltage of  $-3200$  mV, the output code is zero. Around  $-3500$  mV, the ADC curve rises with a pronounced curvature and at approximately  $-4000$  mV the output code reaches the maximum of 255 ADU. Parameter optimization for this hybrid follows the same procedure as for H5026.

The ADC curve of H5026 appears steeper than that of H5033. This could be either a difference in the DCD characteristics or the drain-current response to the gate voltage differs between PXD9 type and standard PXD13 type DEPFET pixels.



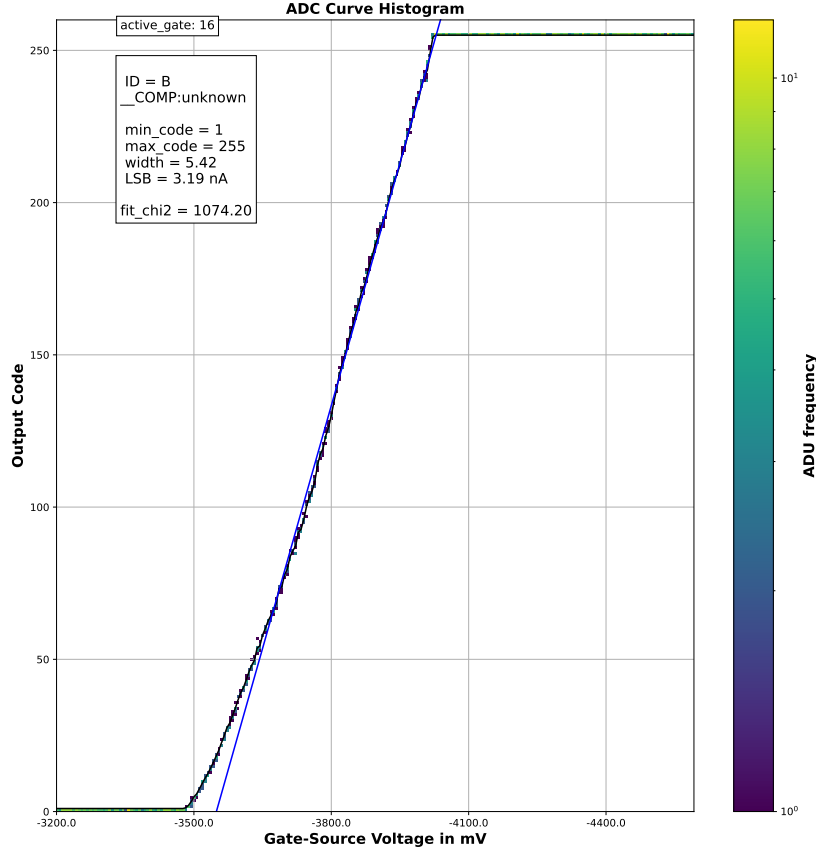


Figure 35: ADC curve of a single channel of H5033 using the DEPFETs as a current source. The ADC curve starts close to zero, a non-linear onset happens around  $-3500$  mV and after that the curve rises linearly until the cutoff at the maximum of 255 ADU.

## 5.5 DCD Calibration

The ADC scan can be used either to optimize the parameters of the DCD or to calibrate the DCD itself. For the DCD calibration, only the optimal configuration of the six adjustable parameters is required. Therefore the more time intensive scan using the DHE current source can be applied. The ADC scan with the DHE offers a higher resolution and features a linear current source. By calibrating the DHE current source with an external reference, the DCD output code can be converted into an absolute current expressed in physical units. With these calibrated ADC curves, it is possible to compare the DCDs of both hybrids and also compare the results that depend on the drain current, such as the transconductance.

Figure 36 displays the calibration curve of a single channel of H5026. The DCD output code depends on the digital arbitrary current (DAC) value generated by the DHE. The calibration curve remains at zero up to approximately

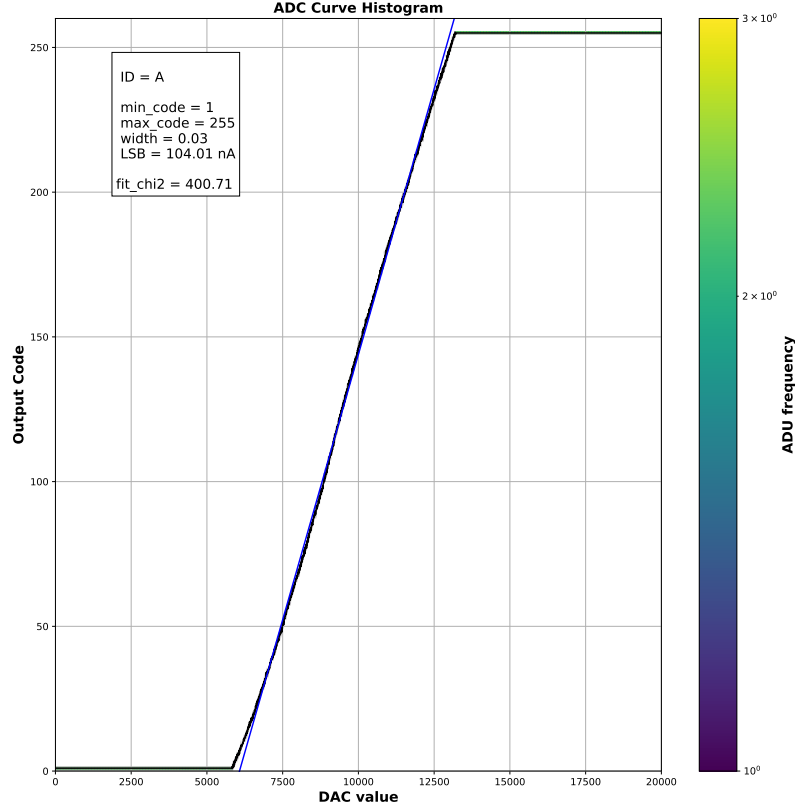


Figure 36: DCD calibration of a single channel of H5026 using the DHE current source. The calibration curve starts at zero, at around 6000 DAC the curve rises linearly until the cutoff at the maximum of 255 ADU.

6000 DAC, then rises linearly until around 13 000 DAC, where it saturates at the maximum output of 255 ADU. A linear fit can be applied to the rising section. The slope of the linear fit relates the DAC current to the DCD output code. Across all channels of the DCD, the slope ranges between 6500 and 7500 DAC/255 ADU.

To express the current in physical units, the calibration factor of the DHE must be determined. This factor is obtained by connecting the DHE to an external source meter and sweeping the DHE current in DAC steps while the external source meter measures the corresponding current. The resulting calibration curve for the DHE is shown in Figure 37. The current increases linearly with the DAC value until it approaches the current limit of the source meter at approximately 200  $\mu$ A. The calibration factor is extracted from a linear fit, excluding the non-linear region.

The resulting calibration function is given by:

$$f = (3813.66 \pm 0.01)\text{pA/DAC} + (22600.13 \pm 9.19)\text{pA}$$

Because this calibration is specific to the used DHE, it applies to measurements

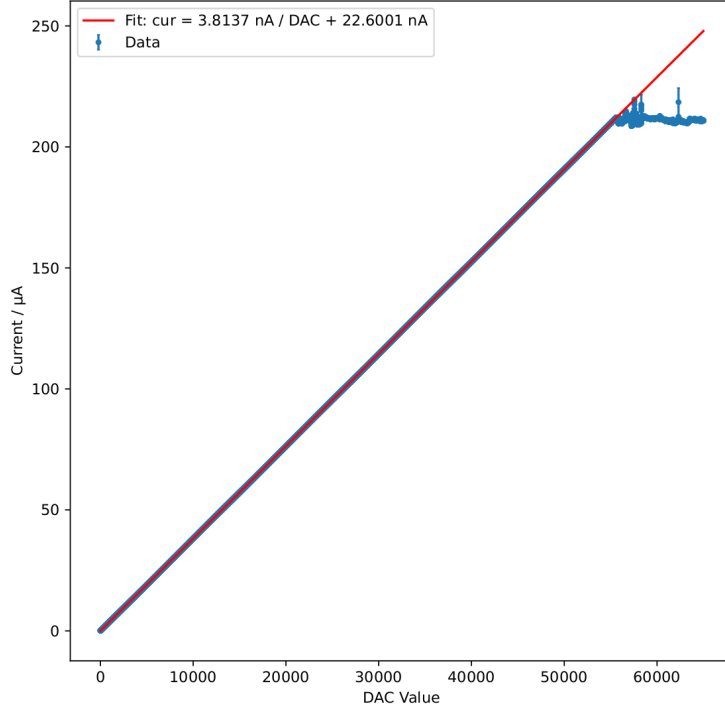


Figure 37: DHE calibration with an external current source. The current rises linearly until it reaches the current limit of the SMU.

of both H5026 and H5033. The slope of this calibration and the slope of the DCD transfer curve together defines the DCD gain, expressed in ADU/A. The DCD gain will be essential for converting the transconductance and the internal amplification into physical units.

Figure 38 presents the calibration curve of a single channel of H5033. The calibration curve remains at zero up to approximately 7000 DAC. It then increases linearly until it saturates around 13 500 DAC. The slopes of the calibration curves for the DCD channels of H5033 range between 6500 and 7500 DAC/255 ADU. This is consistent with the range of the slope of the DCD channels obtained for H5026. This agreement is expected, as both DCDs belong to the same generation and should exhibit similar behavior.

## 5.6 Transconductance

The transconductance of the hybrids is determined by measuring the pedestal of each pixel for several gate-on voltage settings around the working point. The resulting DEPFET IV curves are comparable to the static measurements of Chapter 4.

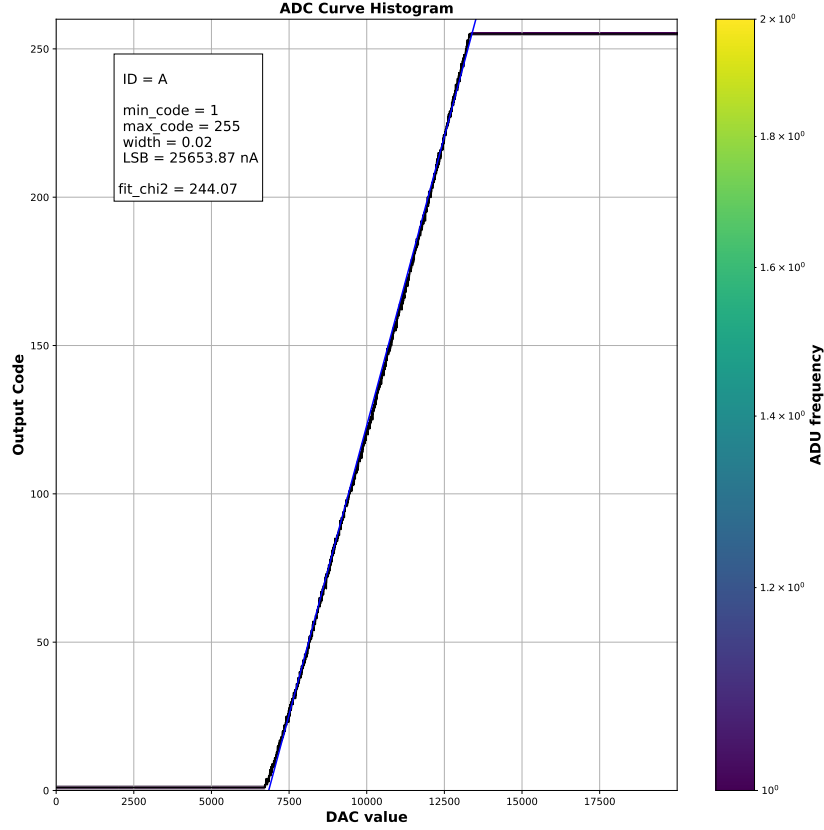


Figure 38: DCD calibration of a single channel of H5033 using the DHE current source. The calibration curve starts at zero, at around 7000 DAC the curve rises linearly until the cutoff at the maximum of 255 ADU.

### 5.6.1 DEPFET IV curves

The DEPFET IV curves are obtained by sweeping the gate-on voltage around the working point of each hybrid while recording the drain current with the DCD. To artificially increase the 8-bit dynamic range of the DCD, the VN-SubIn setting can be adjusted. Increasing VNSubIn reduces the drain current reaching the DCD for all pixels with a linear shift and the drain current remains within the dynamic range.

Figure 39 presents the DEPFET IV curve for a single pixel of H5026. At  $-4500$  mV, the drain current lies outside the dynamic range of the DCD. As the gate-on voltage decreases, the drain current rises and enters the dynamic range of the DCD around  $-4800$  mV. The pronounced curvature originates from the DCD response, as also seen in the ADC scan. Since the applied gate-on voltage is at the working point rather than the DEPFET threshold, this curvature does not indicate an activation of the FET, the FET remains in its on-state for all applied gate-on voltages in this measurement.

The drain current increases from approximately 40 ADU at  $-4900$  mV to about

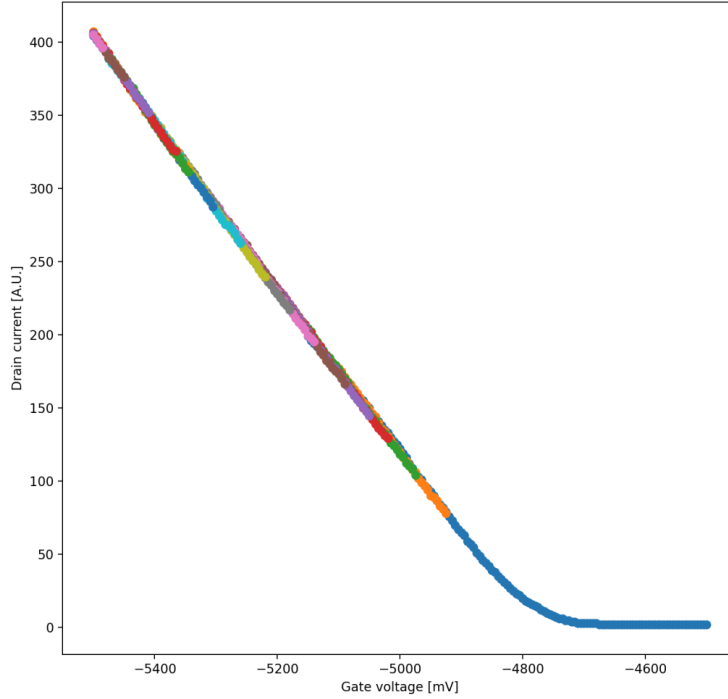


Figure 39: DEPFET IV curve for a single pixel of H5026. The applied gate-on voltage varies from  $-4500$  mV to  $-5500$  mV. The drain current starts at zero ADU and when the gate-on voltage decreases, the current gets inside the dynamic range of the DCD and starts rising. Different colors indicate different VNSubIn values.

400 ADU at  $-5500$  ADU. Additional DEPFET IV curves, taken at different VNSubIn settings, overlap with the blue curve. Since the VNSubIn current sink reduces the drain current before the ADC, the current remains within the dynamic range of the DCD. These curves are then shifted back to their expected ADU values through best-fit alignment with the baseline (blue curve). Combining them allows the effective range to exceed 255 ADU. This enables a more precise determination of the transconductance by fitting a wider range of the IV curve. Because the DCD exhibits a strong curvature for low ADU values, only data points between 50 and 200 ADU are considered for the combined curves.

The average DEPFET IV curve for a single pixel of H5026 is displayed in Figure 40. Up to about  $-4900$  mV, the DEPFET IV curve is derived from a single VnSubIn setting. Data points above  $-4900$  mV are the average of several VnSubIn configurations. These averaged values are used to determine the transconductance of the full H5026 hybrid, as discussed in the following section.

Figure 41 presents the average DEPFET IV curve of a single pixel from H5033. Due to the required offsets for this hybrid, the DEPFET IV curve does not begin at zero ADU and lacks the non-linear part in the DCD response for low ADU values. Nevertheless, the measurement quality remains unaffected,

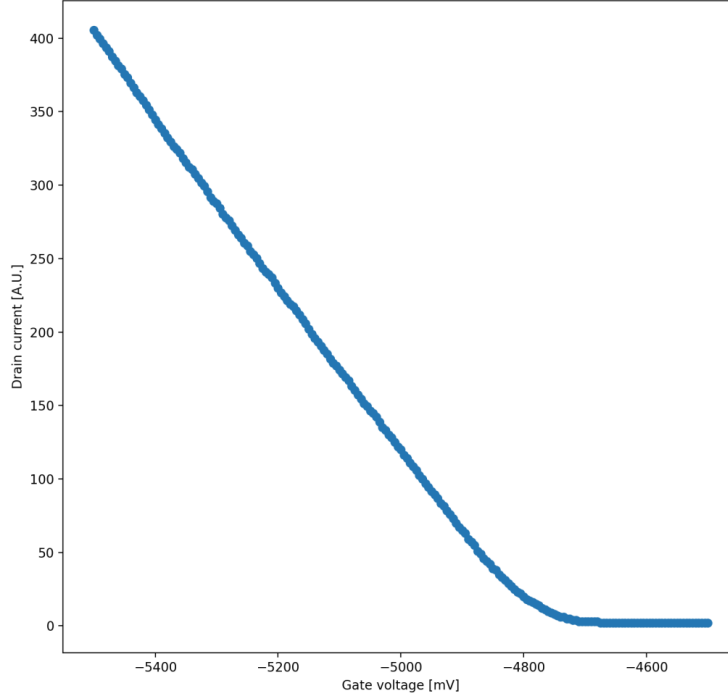


Figure 40: DEPFET IV curve for a single pixel of H5026. The current for high gate-on voltages is only measured with one VnSubIn setting. The curve above  $-4900$  mV is determined from the average of the curves of Figure 39.

as the DEPFET IV curve is still taken around the working point. For H5033, the applied gate-on voltage ranges from  $-3200$  mV to  $-4200$  mV. The ADU values increase from approximately 80 ADU to about 500 ADU. A comparison between the DEPFET IV curves for H5026 and H5033 reveals that the slope of H5026 is steeper, indicating a higher transconductance for this module.

### 5.6.2 Transconductance for full hybrid5 modules

Since the slope of the DEPFET IV curve directly corresponds to the transconductance (see Section 3.1.5), these curves can be used to extract the transconductance for each individual pixel of the hybrid5 modules. A linear fit is applied within the approximately linear regime of the DEPFET IV curve to obtain the transconductance values.

The resulting transconductances for H5026 are displayed in Figure 42. The left side shows the pixel-wise transconductance distribution within the minimatrix. The first seven columns exhibit noticeably higher transconductance values than the following columns. This is similar to the behavior observed for the pedestals, which have a higher value for the columns on the left than on the right. This correlation arises from voltage drops along the gate lines, resulting in higher effective voltages for the first columns. If the voltage drop along the

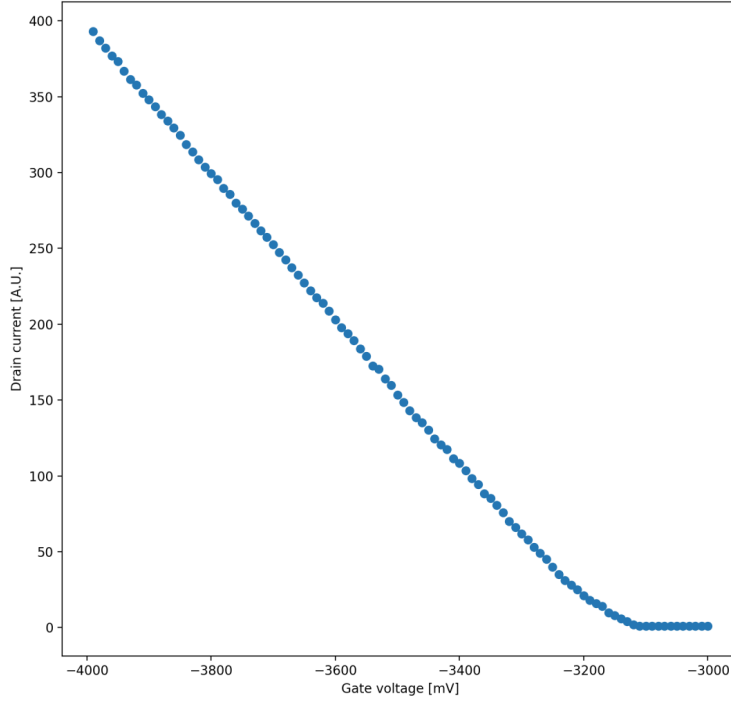


Figure 41: DEPFET IV curve for a single pixel of H5033. The applied gate-on voltage varies from  $-3000$  mV to  $-4000$  mV. The curve is determined from the average over multiple VNSubIn settings, similar to Figure 39.

gate line varies non-linearly with the applied gate voltage, it directly influences the extracted transconductance values.

The right side shows the overall transconductance distribution. The mean transconductance is approximately  $602$  ADU/V with a standard deviation of  $35$  ADU/V. The distribution is asymmetric and decreases towards both ends, reflecting the non-uniform voltage drop across the matrix. The characteristic two dead drain lines, running vertically and connected to every fourth pixel, are also visible, resulting in alternating pixels with zero or normal transconductance along these lines.

Figure 43 presents the results for H5033. The left side maps the transconductance of every pixel onto the minimatrix. The distribution differs in several aspects from that of H5026. Due to the new wirebond adapter, only a part of the matrix is measured in the DEPFET IV scan, so fewer columns are displayed, while all 80 rows of the matrix are measured and shown. The first rows of the matrix exhibit an increased transconductance. This effect is caused by the DCD electronics and does not reflect a physical difference. The DCD requires time to recover when unconnected rows pull drain lines outside the dynamic range, which is also visible in the pedestal maps. Likewise, defect rows that do not respond to the gate voltage still saturate the DCD, and the DCD's recovery time affects the next rows. Therefore, the transconductance values for the four rows following the defect region are also unreliable.

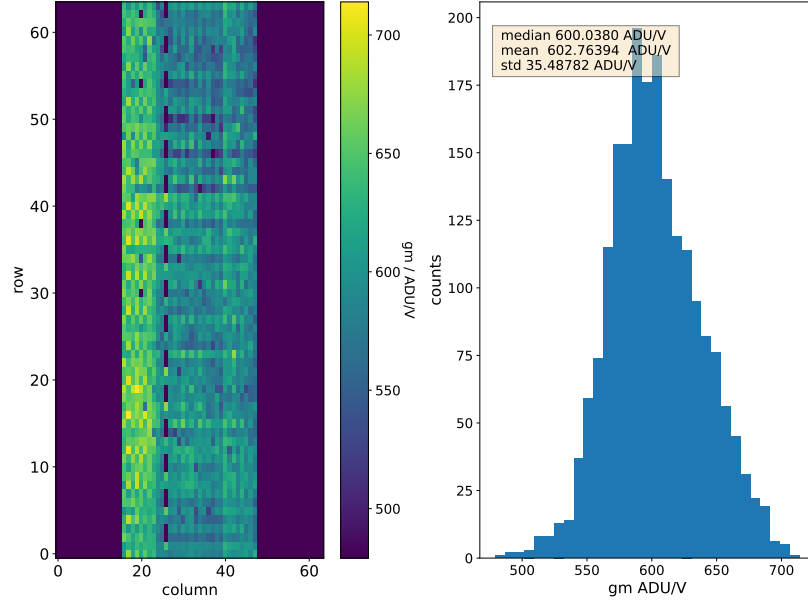


Figure 42: Transconductance for every pixel of H5026. The transconductance is higher for the first seven columns than for the other columns. The mean transconductance is approximately 600 ADU/V, the distribution is asymmetric.

The remaining pixels exhibit a transconductance of approximately 480 ADU/V with a standard deviation of about 36 ADU. The mean transconductance is roughly 20% lower than that of H5026. However the standard deviation is comparable, indicating similar variations within one matrix. According to Equation 5, this suggests that variations in gate dimensions and the oxide layer are of comparable magnitude within a single minimatrix.

These results still depend strongly on the specific DCD used. The systematic uncertainties introduced by the DCD were thoroughly investigated using several PXD9 modules [21]. It was found that the statistical uncertainties of the DEPFET IV curve measurements are significantly smaller than the variations caused by the DCD and by differences in production. The DCD variations observed in the full PXD9 matrices were smaller than the difference between H5026 and H5033, which indicates a production related variation.

| Module | mean $g_m$ /ADU/V | std $g_q$ /ADU/V |
|--------|-------------------|------------------|
| H5026  | 602.76            | 35.49            |
| H5033  | 483.06            | 36.25            |

Table 3: Transconductance of the measured minimatrices in arbitrary units per volt. The mean transconductance of H5033 is about 20% lower than that of H5026. The variations per minimatrix are comparable.

The systematic variations due to the DCD can be reduced by considering the influence of the DCD calibration. Figure 44 shows the transconductance dis-



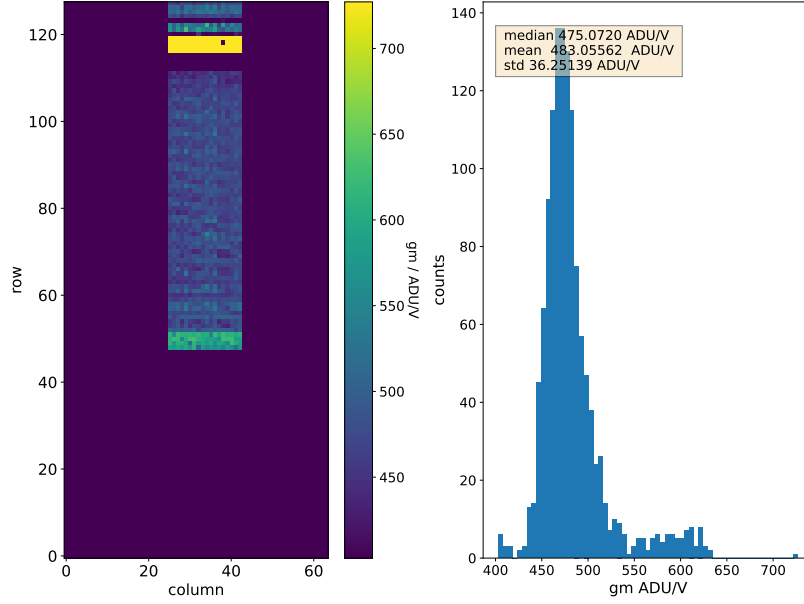


Figure 43: Transconductance for every pixel of H5033. The transconductance is higher for the first four rows and for the rows after the dead part of the matrix than for the other rows. The mean transconductance is approximately 480 ADU/V.

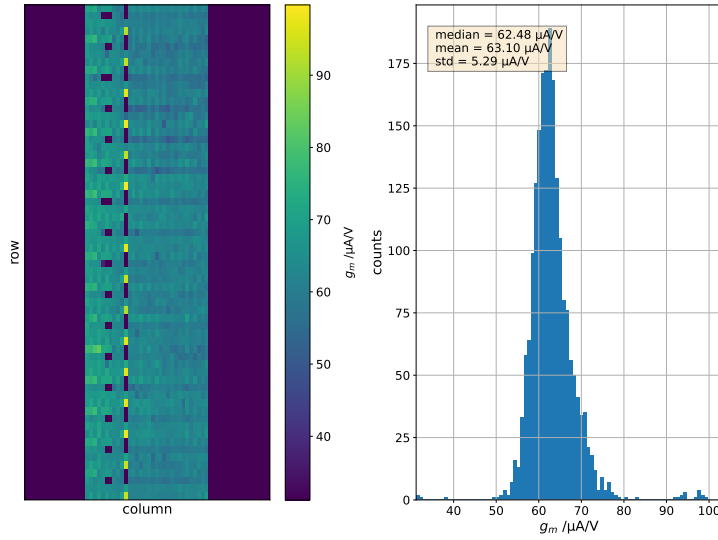


Figure 44: Transconductance for every pixel of H5026 in natural units. The conversion is achieved with the DCD calibration. The distribution has a mean value around 63  $\mu\text{A/V}$ .

tribution of H5026 expressed in physical units. Conversion of ADU to  $\mu\text{A}$  was performed using the calibrated DCD transfer functions. The DCD calibration

was unsuccessful for three drain lines, the ADC curve measurement failed for these specific channels. Therefore some pixels in columns six and seven lack calibrated values. The calibrated distribution remains asymmetric, the calibrated mean transconductance is  $63.10 \mu\text{A}/\text{V}$  with a standard deviation of  $5.29 \mu\text{A}/\text{V}$ . This calibrated mean can be compared to the results of Chapter 4, where the transconductance was found to be  $69.611 \pm 7.288 \mu\text{S}$ .

The results can also be compared to the results of previously measured full PXD9 modules tested in Bonn in 2022 [21]. Selected results are listed in Table 4. The transconductance of H5026 agrees with the values found for the full PXD9 modules. Similar to the static tests, the transconductance variation within a single matrix exceeds any systematic uncertainties introduced by the measurement itself.

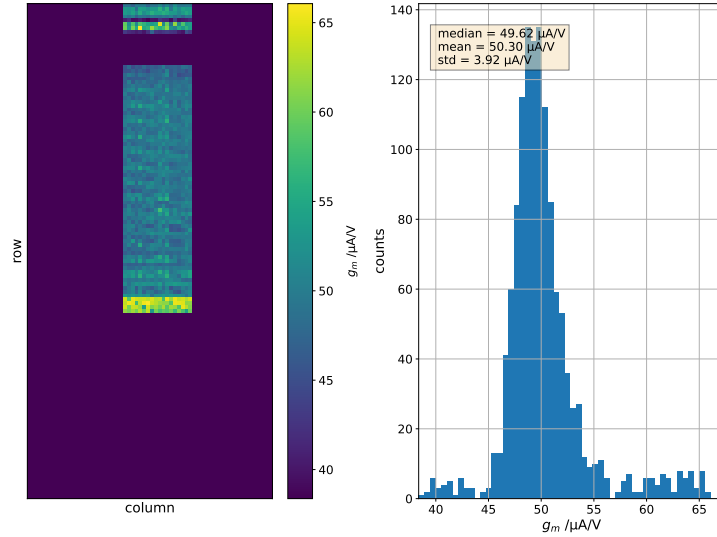


Figure 45: Transconductance for every pixel of H5033 in natural units. The conversion is achieved with the average DCD calibration of H5026. The distribution has a mean value around  $50 \mu\text{A}/\text{V}$ .

For H5033 the DCD calibration did not produce valid results for all drain lines and some conversion factors could not be obtained. Because the DCD calibration curves of H5033 closely resemble those of H5026 and both DCDs are of the same generation, it is reasonable to convert the ADU value to  $\mu\text{A}$  using the average calibration factor obtained from H5026. Applying this approach yields the distribution shown in Figure 45. The mean transconductance for H5033 is  $50.30 \mu\text{A}/\text{V}$  with a standard deviation of  $3.92 \mu\text{A}/\text{V}$ . Using the H5026 calibration preserves the observed difference of 20% in mean transconductance. This does not reduce the systematic uncertainty of the measurement either, as the transconductance is not corrected for the specific DCD characteristics used in this setup. However the difference is larger than any DCD related expected uncertainties and the difference in transconductance is unexpected for the new standard PXD13 type DEPFETs, since relevant device parameters were intended to remain unchanged [14]. However, previous tests

on PXD9 modules revealed module W67IB with a similarly reduced transconductance ( $46 \mu\text{A/V}$  [21]).

The observed differences in transconductance could inherit from doping variations or from variations in transistor dimensions. Changes in the oxide layer are another possible cause [14]. From Equation 5 for an empty internal gate ( $Q_{in} = 0$ ), a reduced gate width or smaller oxide capacitance would lead to a lower transconductance. Also a longer gate would have a similar effect. The results require further investigation and improved statistics by characterizing additional standard PXD13 matrices.

| Module             | mean $g_m/\mu\text{A/V}$ | std $g_q/\mu\text{A/V}$ |
|--------------------|--------------------------|-------------------------|
| H5026              | 63.10                    | 5.29                    |
| H5033              | 50.30                    | 3.92                    |
| static measurement | 69.611                   | 7.288                   |
| W56OB1             | 72.8                     | 11.8                    |
| W57OF2             | 65.9                     | 4.8                     |
| W67IB              | 46.0                     | 6.6                     |

Table 4: Transconductance of the measured minimatrices compared to the static measurement and selected full PXD9 modules [21].

## 5.7 Source Scan

To evaluate the particle detection of the DEPFET pixels, their response to photon irradiation is measured. This is achieved by positioning a radioactive source above the matrix and recording the resulting signals. The signals are obtained by subtracting the pedestals from the drain current (see Chapter 3). The following results were obtained using a Cd109 source with a total runtime of 50 000 s for both hybrids.

Figure 46 illustrates the response of H5026 to the Cd109 source. Cadmium decays into silver and emits characteristic x-rays. The hitmap (left) shows the number of events per pixel, where a charge deposit exceeded a defined threshold. The threshold depends on the noisiness of the minimatrix and was set to three ADU for this measurement. The distribution is uniform across the active matrix area, the dead drain lines exhibit no response. The seedmap (right) indicates the pixel that records the highest energy deposit for each event. This seed pixel (or cluster seed) serves as a reference to reconstruct the total deposited energy when secondary particles extend over multiple pixels. Because the sensors are relatively thin and have a comparatively large pixel pitch, most interactions are confined to one or two pixels. The seedmap also shows a homogeneous distribution and no response in the dead drain lines.

Figure 47a shows the seed charge distribution. The seed charge is the charge collected by the cluster seed. The seed charge distribution peaks around 43 ADU.

The corresponding cluster charge distribution is shown in Figure 47b. The cluster charge is the sum of the charge of all pixels within one cluster. The resulting

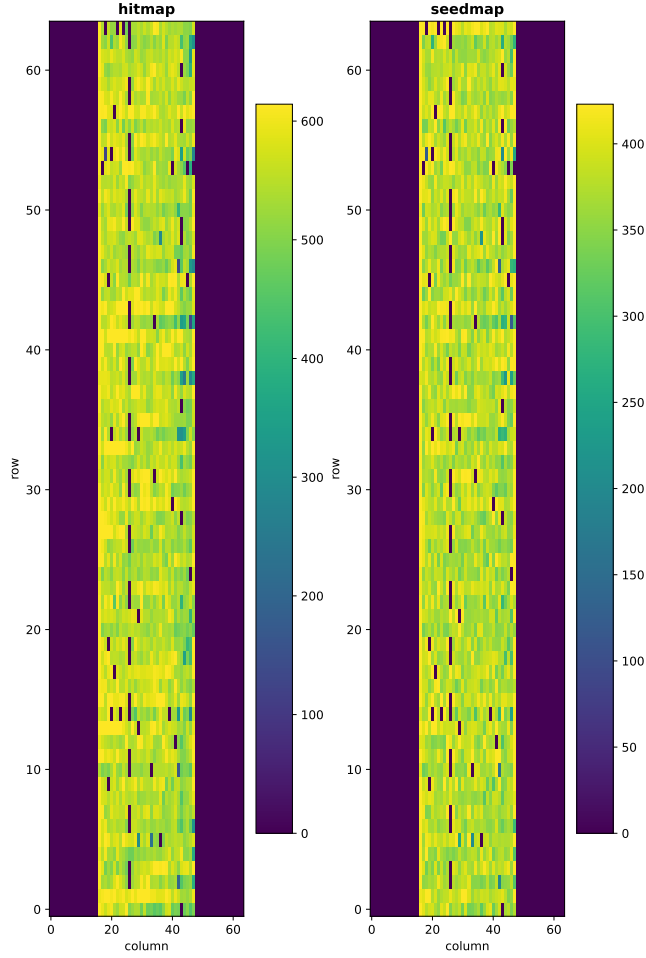


Figure 46: Hitmap and seedmap of H5026 for a Cd109 source scan. The hits and seeds are uniformly distributed across the matrix.

spectrum follows a Gaussian shape. As Cd109 decays into silver, emitting  $K_\alpha$  and  $K_\beta$  photons, the cluster charge distribution is fitted with a double Gaussian. The mean value for the  $K_\alpha$  and  $K_\beta$  lines are approximately 42 ADU and 44 ADU.

The cluster size distribution in Figure 48 reveals that more than two thirds of the events are registered in a single pixel. The remaining events extend over multiple pixels and are combined to determine the total cluster charge displayed in Figure 47b.

Figure 49 shows the response of H5033 to the Cd109 source. The hitmap exhibits an overall uniform distribution, the dead pixel rows show no response and the pixels in the following rows record only some responses. Two unconnected pixels appear noisy, contributing to the background. Rows 100 to 104 display an atypical hit pattern. For a smaller runtime, these pixels respond differently,

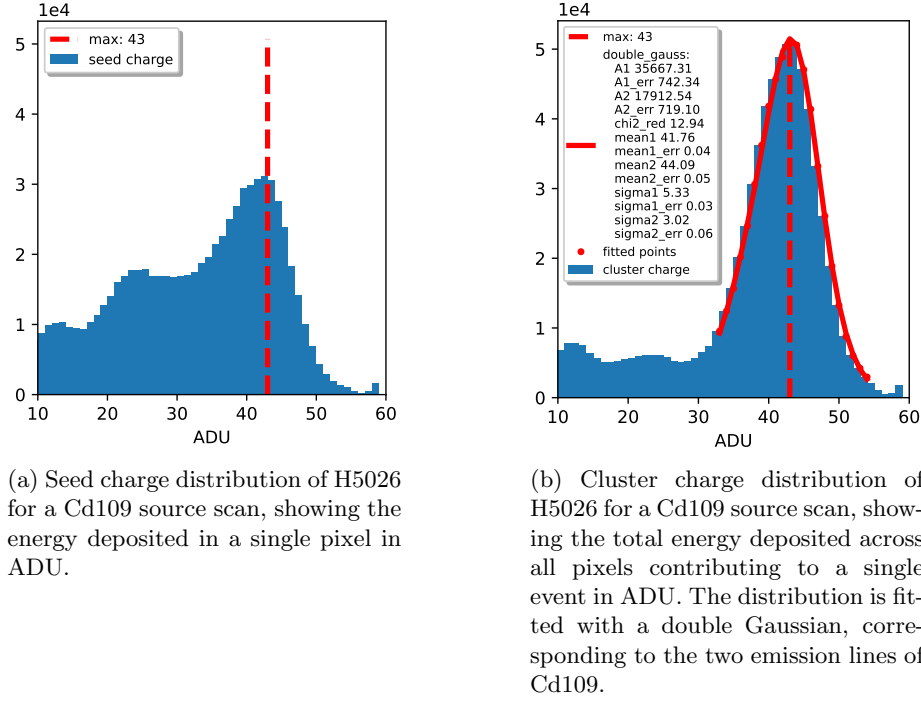


Figure 47: Comparison of seed and cluster energy distributions for H5026 measured with a Cd109 source. The left side shows the single-pixel energy deposits, while the right side displays the total cluster energies.

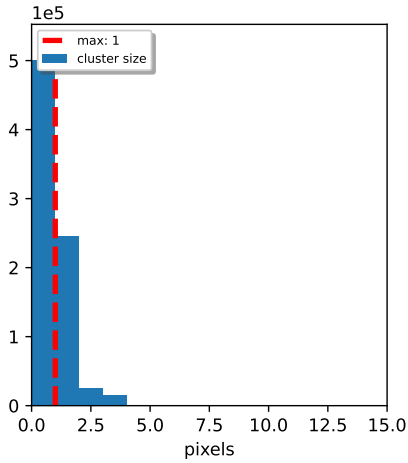


Figure 48: Cluster size distribution of H5026 for a Cd109 source scan. About one third of the events are shared between multiple pixels.

but as the runtime increases they show almost the same number of hits. This requires a further investigation, since it might originate in high background activity for these rows. The seedmap shows a similar distribution and no activity in the dead rows, as expected. Compared to H5026, H5033 registers approxi-

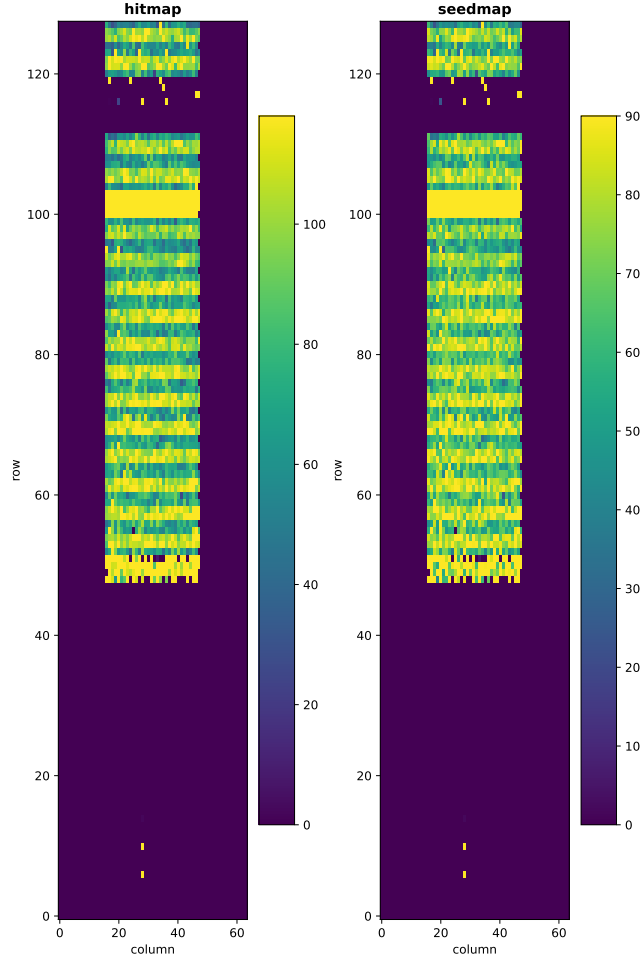
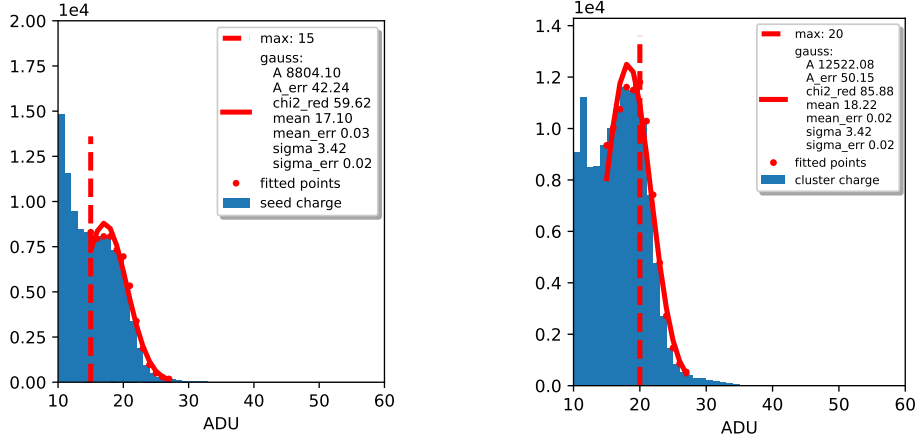


Figure 49: Hitmap and seedmap of H5033 for a Cd109 source scan. The hits and seeds are mostly uniformly distributed across the matrix.

mately six times fewer hits, which is unexpected for the new PXD13 standard type matrix.

The seed charge spectrum for H5033 is shown in Figure 50a. The distribution peaks at an energy of about 17 ADU. This is less than half of the value measured for H5026. Due to the lower signal amplitude, the two characteristic peaks of Cd109 cannot be resolved, and a single Gaussian is fitted. Figure 50b displays the corresponding cluster charge distribution. Similar to H5026, the spectrum follows a Gaussian shape. However, the measured signal amplitude is again reduced by more than a factor of two. The mean cluster charge is approximately 18 ADU.

The cluster size distribution for H5033, presented in Figure 48, shows that fewer than 10% of the events are registered in multiple pixels. Although a small cluster size is expected due to the thin sensor, the low signal amplitude leads



(a) Seed charge distribution of H5033 for a Cd109 source scan, showing the energy deposited in a single pixel in ADU.

(b) Cluster charge distribution of H5033 for a Cd109 source scan. Due to the low ADU values, the two Cd109 emission peaks cannot be resolved, and the distribution is fitted with a single Gaussian.

Figure 50: Comparison of seed and cluster energy distributions for H5033 measured with a Cd109 source. The left side shows single-pixel energy deposits, while the right side displays summed cluster energies.

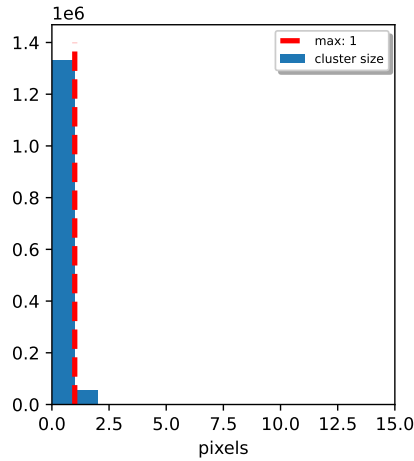


Figure 51: Cluster size distribution of H5033 for a Cd109 source scan. Fewer than 10% of the events extend over multiple pixels.

to many secondary pixels being suppressed by the noise filter, preventing their contribution to the reconstructed cluster charge.

| Element           | origin of $\gamma$ -rays               | expected energy/keV | measured peak/ADU |
|-------------------|----------------------------------------|---------------------|-------------------|
| $^{55}\text{Fe}$  | $K_{\alpha}$ ( $^{55}\text{Mn}$ )      | 5.899               | $11.92 \pm 0.01$  |
| Cu                | $K_{\alpha}$                           | 8.048               | $15.54 \pm 0.11$  |
| $^{109}\text{Cd}$ | $K_{\alpha}$ ( $^{109}\text{Ag}$ )     | 22.163              | $41.76 \pm 0.04$  |
| Ba                | $K_{\alpha}$                           | 32.194              | $62.85 \pm 0.69$  |
| Tb                | $K_{\alpha}$                           | 44.483              | $83.14 \pm 5.06$  |
| $^{241}\text{Am}$ | nuclear emission ( $^{237}\text{Np}$ ) | 59.541              | $112.51 \pm 0.05$ |

Table 5: List of the sources used for the energy calibration, the origin of  $\gamma$ -rays, the expected energy [18][19] and the measured peak value in ADU.

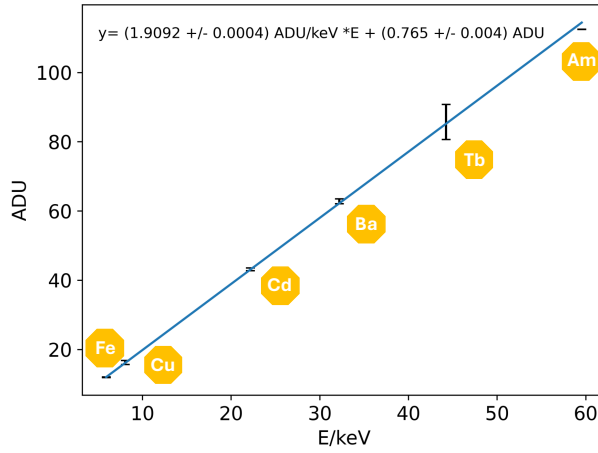


Figure 52: Energy calibration of H5026 using the different sources named in Table 2. The hybrid responds linearly to the increasing energy.

### 5.7.1 Energy Calibration

Various radioactive and X-ray sources were used to determine the energy response of the hybrid. Due to the low ADU values and limited statistics of H5033, the calibration was performed only for H5026. The corresponding results are summarized in Table 5 and illustrated in Figure 52. The complete spectra for each source are provided in the appendix (Figures 71, 72, 73, 74 and 75). For the low-energy sources iron and copper, the fitting process proved to be challenging because of the small signal amplitudes. The  $K_{\alpha}$  and  $K_{\beta}$  peaks of iron are located close to the electronic noise, which prevents a clear separation of the two lines. In the case of copper, multi-pixel events are partially suppressed because the charge collected in secondary pixels frequently falls below the detection threshold, producing a pronounced tail toward lower ADU values. Both spectra were therefore fitted with a single Gaussian corresponding to the  $K_{\alpha}$  transition, while the weaker  $K_{\beta}$  component was neglected. On the other hand, the high ADU values of americium introduce additional complications. Since the measured signal adds to the pedestal, the maximal measureable ADU value is effectively limited to 255 minus the pedestal value



of the corresponding pixel. Therefore, the high charge of approximately 120 ADU for americium leads to partial saturation of the DCD in several pixels, as already indicated by the pedestal distribution in Figure 30. Even below the saturation threshold, the DCD exhibits a reduced linearity at both high and low ADU values (see Figure 34). As a result, the measured mean charge for americium is slightly lower than the expected value (see Figure 52).

For barium, terbium and cadmium, the spectra are better represented by a double Gaussian fit. However, for the energy calibration only the dominant  $K_\alpha$  line was used, since the  $K_\beta$  peak is not clearly visible for all pixels.

The energy calibration yields a linear dependence between the measured ADU value and the photon energy:

$$y = (1.9092 \pm 0.0004) \text{ADU/keV} * E + (0.765 \pm 0.004) \text{ADU}$$

This calibration curve is valid exclusively for H5026 at the specific gate-on voltage of  $-5300 \text{ mV}$ . Systematic uncertainties are therefore negligible, as the calibration applies solely to this setup and repeated source measurements agreed within the uncertainties given in Table 5. The obtained conversion factor agrees well with the value determined for a full PXD9 module, which is  $m = 1.91 \text{ADU/keV}$  [21]. This conversion factor was derived from a two point calibration. Establishing a general energy calibration for various modules and working points would require accounting for systematic effects in the electronics as well as variations in FET geometry and doping concentration.

### 5.7.2 Internal Amplification

As described in Chapter 3, the internal amplification can be determined using a known gamma source. Alternatively to Equation 6, the charge gain can be expressed as:

$$g_q = \frac{\mu_{\text{fit}}}{E_\gamma} \cdot \frac{1}{\text{DCD gain}} \cdot \langle E_{eh} \rangle \quad (9)$$

which yields a unit of  $\frac{\text{nA}}{e}$  according to:

$$[g_q] = \frac{\text{ADU}}{\text{eV}} \cdot \frac{\text{nA}}{\text{ADU}} \cdot \frac{\text{eV}}{e} = \frac{\text{nA}}{e} \quad (10)$$

This means, that the calculation of  $g_q$  requires the mean energy per pixel in ADU, the number of electrons generated by the incoming photon, and the DCD gain, which converts the drain current into physical units.

The cadmium source was selected for this analysis because it provided the highest statistics among the available sources. To calculate the internal amplification, only events with a cluster size of one are considered.

The charge spectrum of a representative pixel is shown in Figure 53. The main  $K_\alpha$  peak appears at around 38 ADU, while a smaller structure at approximately 46 ADU corresponds to the expected  $K_\beta$  line. Due to limited statistics, this secondary peak is not visible for all pixels and is excluded from the analysis. Therefore the determination of the internal amplification only uses the  $K_\alpha$  peak.

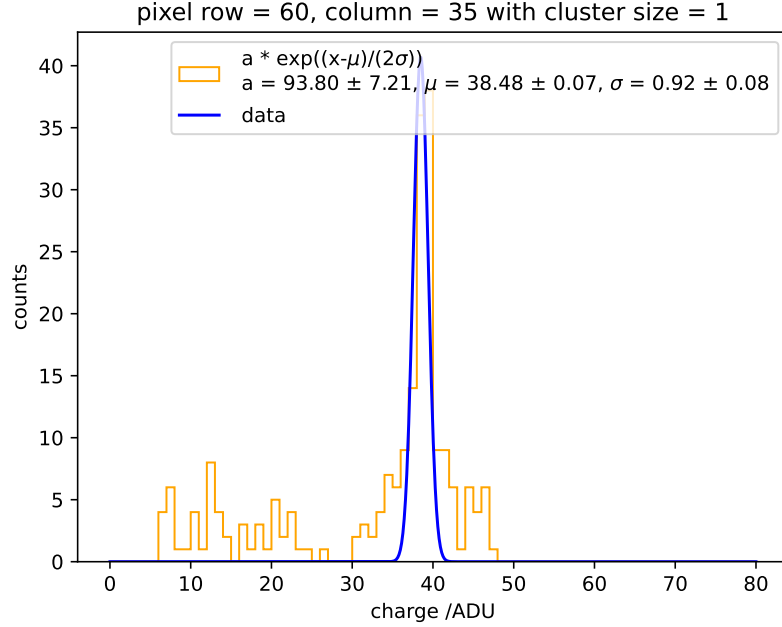


Figure 53: Charge spectrum of the pixel in row 60, column 35 of H5026 for the cadmium source. The dominant  $K_\alpha$  is located at approximately 38 ADU. The  $K_\beta$  peak appears near 46 ADU. Only the  $K_\alpha$  peak is fitted and used for the determination of the internal amplification.

The resulting internal amplification for all pixels of H5026 is presented in Figure 54. The mean amplification is approximately 735 pA/electron with a standard deviation of 69 pA/electron. The distribution exhibits a noticeable asymmetry, which is also reflected in the spatial distribution across the matrix. Pixels located in the right columns display a lower internal amplification than those on the left. This happens because of the voltage drop along the gate lines. This trend is consistent with the transconductance behavior, as both quantities are related through Equation 7.

The statistical uncertainty of  $g_q$  is dominated by the uncertainty of the fitted mean charge, which remains well below 1% for all pixels. Systematic effects mainly arise from variations in the DCD gain and the applied gate-on voltage. These effects were extensively studied for different PXD9 modules [21] and cannot be further constrained with a single minimatrix, since the DCD calibration already reduces such uncertainties significantly. Variations in the FET dimensions and doping concentration are reflected in the width of the distribution. The expected internal amplification from device simulations is approximately 500 pA/electron. The measured mean value exceeds this by roughly 50%. A similar enhancement has been observed for the full PXD9 modules [21] (see Table 6). It was found that any uncertainties do not explain this discrepancy. The most plausible explanation is that the internal gate lies closer to the p-channel than predicted by the design. This enhances the coupling of the internal gate

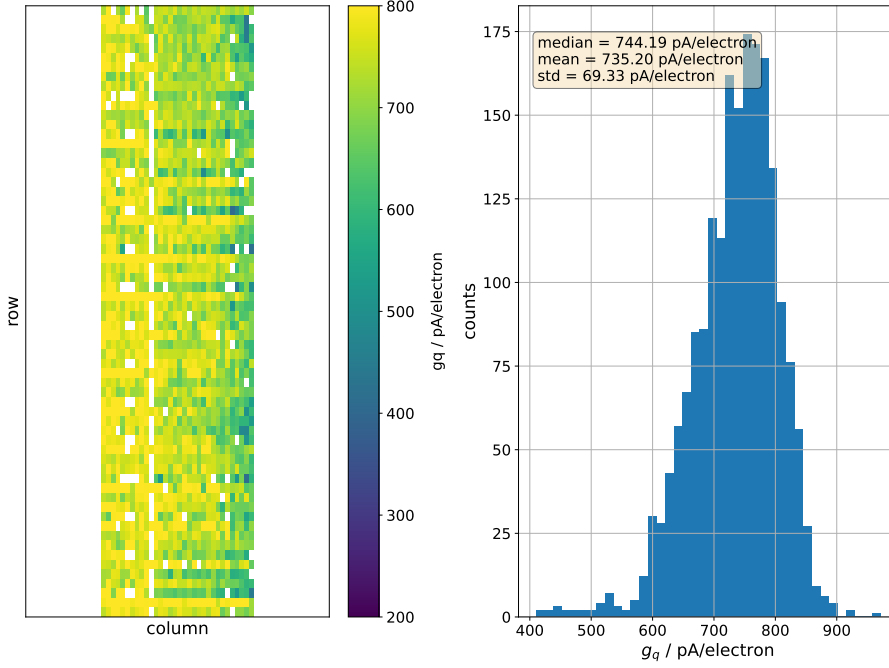


Figure 54: Distribution of the internal amplification of H5026. The mean value is approximately 735 pA/electron, with a standard deviation of about 69 pA/electron. The distribution shows a slight asymmetry.

and the p-channel and thereby increases the drain current per collected electron in the internal gate.

| Module            | mean $g_q$ /pA/electron | std $g_q$ /pA/electron |
|-------------------|-------------------------|------------------------|
| H5026             | 735.20                  | 69.33                  |
| H5033 (estimated) | 320.77                  | —                      |
| W67IB             | 517.40                  | 49.96                  |
| W57IB             | 648.55                  | 59.52                  |
| W60OF1            | 743.91                  | 62.35                  |

Table 6: Comparison of the internal amplification of H5026 and H5033 with full PXD9 modules. [21]

For H5033, the mean internal amplification can only be estimated. Under the assumption that the DCDs of H5026 and H5033 behave comparably, since they are of the same generation, the lower measured signal of 18.22 ADU instead of 41.76 ADU corresponds to a reduced internal amplification of approximately 321 pA/electron. This significant reduction requires further measurements on additional standard PXD13 matrices to clarify the origin of this difference.

### 5.8 First results for the super- $g_q$ PXD13 type DEPFET pixels

At the end of September, the first hybrid5 module was assembled with a super- $g_q$  PXD13 type DEPFET minimatrix. The initial measurement results obtained from hybrid H5034 are presented and discussed in the following section.

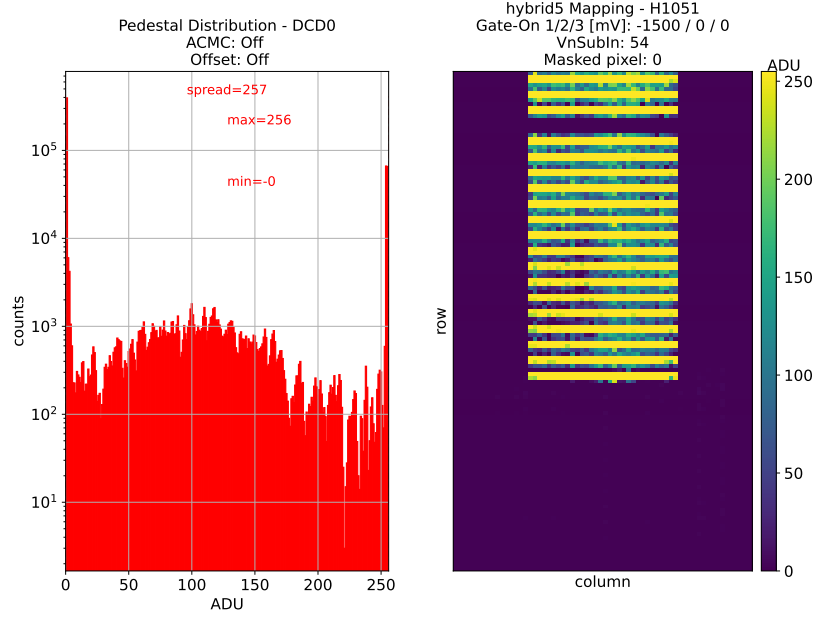


Figure 55: Pedestals of the new super- $g_q$  PXD13 type matrix for H5034. The VnSubIn setting is at 54. The matrix has a double row pattern, many pixels are saturated.

Figure 55 shows the pedestal distribution of H5034 measured at a gate-on voltage of  $-1500$  mV. This voltage corresponds to the expected working point, approximately  $1000$  mV below the threshold (see Figure 57). The pedestals exhibit a pronounced double-row pattern, originating from the source line structure as previously observed for H5033 [14]. However, for H5034 the pattern is significantly stronger. While the two peaks of H5033 differ by about  $130$  ADU, the peaks of the super- $g_q$  matrix extend beyond the dynamic range for identical settings. The new design appears more sensitive to source line variations and amplifies the double row pattern.

Pixels within the dynamic range show the expected response, the pedestal distribution peaks around  $100$  ADU and decreases to both sides. In the matrix mapping, pixels in the lower left corner appear darker, likely due to local doping variations. In the upper part of the matrix, four rows do yield no data, as their gate and clear lines were shorted at the switcher connection due to a design fault. This caused an increased gate-off current and the connections had to be disconnected.

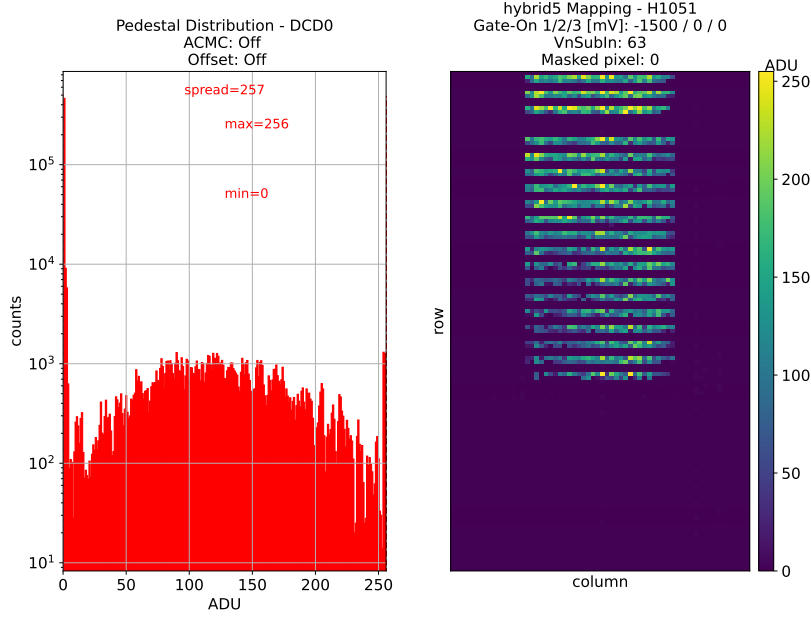


Figure 56: Pedestals of the new super- $g_q$  PXD13 type matrix for H5034. The VnSubIn setting is at 63. The double row pattern is shifted, the saturated pixels of Figure 55 are now in the dynamic range, the other pixels are below the dynamic range.

Since the pedestals of the rows are so far apart, the offset calibration cannot compensate for the double-row pattern. To observe the pixels saturated in Figure 55, the pedestals were shifted downward by adjusting the VnSubIn setting. As a result, pixels previously within the dynamic range moved below it, while saturated pixels entered the dynamic range. Their pedestals now form the expected distribution, now peaking around 120 ADU. Consistent with the previous pedestals, pixels in the lower left region of the matrix display systematically lower pedestal values than the rest.

Hybrid H5034 exhibits an increased base current between source and drain, instead of approaching zero current when all pixels are off, the measured current remains at 9 mA, measured with a source meter. Therefore the working point cannot be determined from the combined source-drain current of the matrix. Figure 57 presents the DEPFET IV curve of a single pixel of H5034. The gate-on voltage ranges from 500 mV to  $-1100$  mV. This range covers the threshold region of the FET. At higher gate-on voltages, the FET remains off, and as the voltage decreases, the FET changes into its on-state. The threshold voltage of this pixel is approximately  $-200$  mV. The working point is estimated to be about 1000 mV below the threshold voltage [16]. Due to variations of the threshold voltage, the working point for this hybrid corresponds to roughly  $-1500$  mV.

The DEPFET IV curve close to the working point is shown in Figure 58. For gate-on voltages between  $-1000$  mV and  $-1500$  mV, the drain current increases

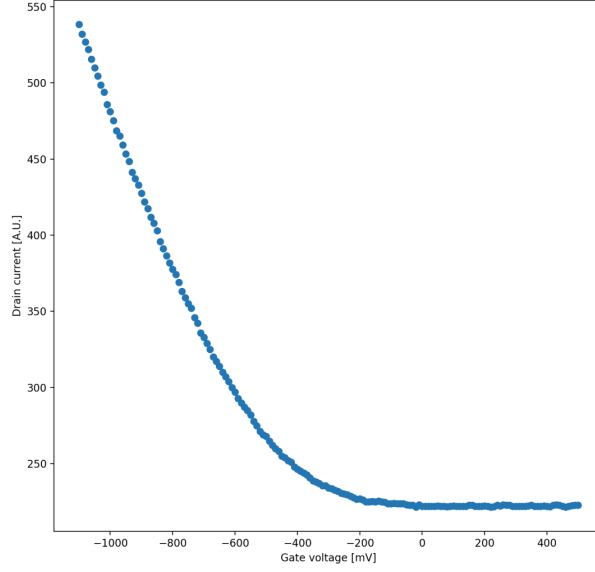


Figure 57: DEPFET IV curve for the new super- $g_q$  PXD13 type matrix for voltages close to the threshold. As for previous DEPFET IV curves, the curve is an average over multiple VnSubIn settings. The drain current increases at approximately  $-200$  mV

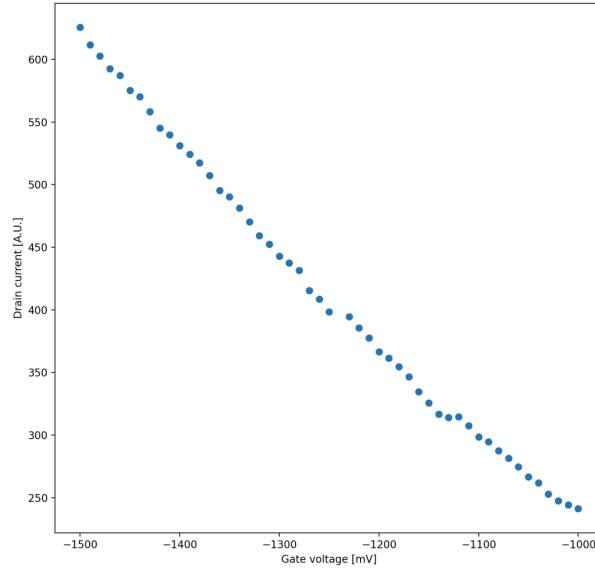


Figure 58: DEPFET IV curve for the new super- $g_q$  PXD13 type matrix at voltages close to the working point. As for previous DEPFET IV curves, the curve is an average over multiple VnSubIn settings. The drain current increases with decreasing gate-on voltage.

continuously with decreasing gate-on voltage. Over the full gate-on range, the drain current increases from approximately 240 ADU to about 620 ADU. This

corresponds to an estimated transconductance of approximately 760 ADU/V. This is more than 20% higher than of H5026. This result aligns with expectations, as the reduced effective internal gate length for the super- $g_q$  leads to an increased transconductance (see Equation 5). These values remain preliminary and rely on the assumption that the DCDs of H5026 and H5034, which belong to the same generation, have comparable transfer curves. To further quantify these values, additional measurements are required and the DCD of H5034 must be calibrated. Further studies on the internal amplification, which depends on the gate length more strongly (see Equation 6 and Equation 7) than the transconductance, will provide deeper insights into the characteristics of super- $g_q$  PXD13 type minimatrices.

## 6 CV measurements

For a further understanding of the DEPFET assemblies, additional studies are done with MOSFET test structures. These devices do not include a deep n-implant, but have similar dimensions and material. They are built in a simplified structure that is particularly suitable for the following CV measurements to characterize the silicon diode properties of the MOSFET.

### 6.1 Short theoretical introduction

For the MOSFET test structures,  $p^+$ -implants are embedded into an  $n^+$ -type silicon bulk. Therefore a pn-junction forms at the contact area. The majority carriers of both sides will recombine and form the depletion region. By applying an external voltage to the pn-junction, the depletion region can be increased or decreased. The voltage at which the full region is depleted, is called the full depletion voltage. The full depletion voltage is an important property of the pn-junction and can be determined for example with an LCR meter and a power supply.

An LCR meter can measure the inductance, capacitance and resistance of a device. This is either done in parallel-mode or in series-mode. Both modes are mathematically equivalent, however the mode depends on the location of the most significant parasitic impedance. In this case the series-mode is used due to the high resistivity of the bulk because of low doping and thus an increased parasitic series resistance. In the series mode, the LCR meter applies an AC-voltage to the DUT and measures the phase angle between the current and the voltage. The capacitance can be determined by:

$$C = \frac{1}{2 * \pi * f * |Z| * \sin(\theta)} \quad (11)$$

with  $Z = V/I$ .

This can be done for different voltages applied to the pn-junction. Each applied voltage results in a different capacitance value. The dependency of the capacitance value and the applied voltage can be used to determine the depletion voltage. Plotting the inverse capacitance squared versus the bias voltage, the high- and low-voltage regions can be extrapolated by a linear fit. The depletion voltage  $V_{dep}$  is defined by the intersection of the two lines. This is due to the fact that for the pn-junction  $\frac{1}{C^2} \sim (V_{bi} - V)$ , and the depletion voltage is defined by the point where the linear extrapolation of  $(V_{bi} - V)$  meets before and after depletion [22].

As written in Equation 11, the capacitance does not depend only on  $|Z|$  but also on the frequency. This dependency can also be tested with the LCR meter since different frequencies can be applied.

An LCR meter often offers the possibility for an open and a short correction. When done correctly, the open correction should compensate any effect of parasitic capacitors in parallel to the device under test (DUT). This is often done by measuring a dummy of the device, where the connectors are left unconnected and therefore open. The short correction is done to compensate parasitic capacitors in series with the DUT. This is achieved by electrically shorting the DUT and therefore bypassing it in the measurement. If these corrections are not done correctly or not done at all, they introduce systematic offsets in the



measurement.

## 6.2 MOSFET test structures

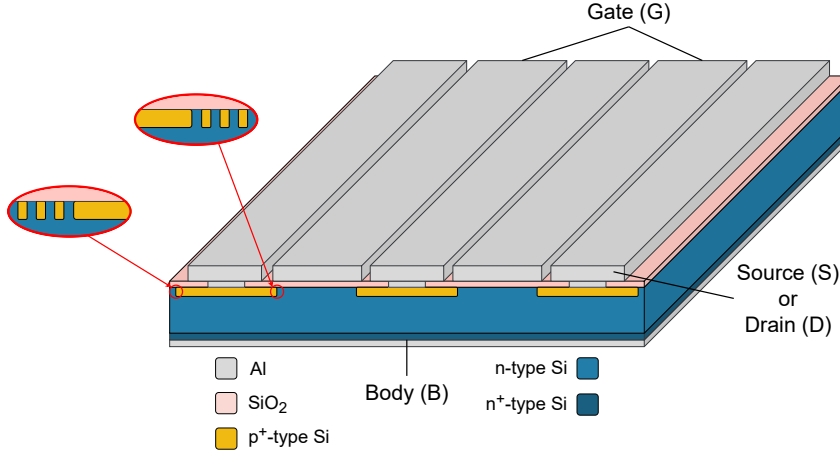


Figure 59: Schematic of the MOSFET structure, provided by [20]. The structure features two FETs that share one implant. The implants are surrounded by guard rings.

The test modules used in this study are based on simplified MOSFET structures. The handle and top wafer are produced by the Max Planck Semiconductor Laboratory (HLL), while the bonding is either done by IceMOS Technology or Shin-Etsu Chemical. The modules consist of an *n*-type silicon bulk with a higher doped *n*<sup>+</sup> backside (see Figure 59). Inside the bulk, there are three *p*<sup>+</sup>-implants surrounded by guard rings (see Figure 59 for a zoomed-in view of the implant region). The purpose of the guard rings is to smooth the electric field and avoid edge effects. A thin silicon oxide layer lies on top of the bulk, above which five aluminum strips are deposited. Three of the aluminum strips are connected to the *p*<sup>+</sup>-implants and act as the source and drain terminals for the MOSFET while two just rest on top of the oxide layer and form the gates. The nominal value of the bulk doping concentration is  $N = 1 \times 10^{13} \text{ cm}^{-3}$ , matching the doping used in the DEPFET modules. The nominal value of the *n*-type silicon thickness is about 75  $\mu\text{m}$ . The metallizations on the top and bottom add a few extra  $\mu\text{m}$  and for the IceMOS structures, there are a few  $\mu\text{m}$  of additional silicon-oxide layer.

In the bonding process IceMOS Technology grows an additional layer of silicon-oxide onto the handle wafer. Therefore Shin-Etsu has a smaller oxide thickness of about  $d_{Ox,Sh} = 350 \text{ nm}$ , while the IceMOS oxide layer adds up to about  $d_{Ox,Ice} = 560 \text{ nm}$  [23]. In this experiment, one module of each batch will be tested, namely the device Shin-Etsu W04 06 (hereafter referred to as ShinEtsu6) and the device IceMOS W01 05 (IceMOS5). This way the results can be verified and also checked for possible differences.

### 6.3 Experimental Setup

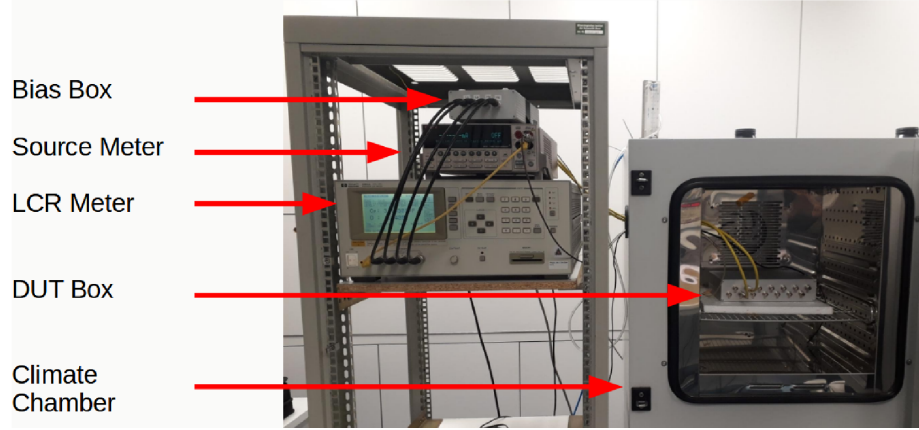


Figure 60: Measuring setup for the CV-measurements [24]. The DUT box is placed in a climate chamber. The LCR-Meter, the source meter and the bias box are mounted to a shelf close to the chamber.

The experimental setup comprises several components designed to minimize parasitic effects and ensure precise CV measurements. An overview is shown in Figure 60.

The used LCR-Meter is the HP 4284A LCR Meter. It uses a precisely known reference resistor to compare to the DUT by using the "auto-balancing bridge method". The capacitance can be measured to a precision of  $\pm 0.5$  pF [24]. To achieve such a low uncertainty, the LCR-Meter uses two high-potential ( $H_p$ ,  $H_c$ ) and two low-potential terminals ( $L_p$ ,  $L_c$ ). Combined with coaxial cables, this leads to a reduction of parasitic impedance and a low influence from outer electro-magnetic fields. There are a few settings which can be changed at the LCR-Meter. The AC-voltage is set to a value of 5 mV. The signal integration time is set to medium length to reduce the statistical uncertainty. In addition, for each measurement step, the average of five readings is taken. The LCR-Meter features a  $C_s R_s$  and a  $C_p R_p$  mode. Due to the significant bulk resistance of the device, the  $C_s R_s$  mode is selected. The bias voltage is swept from 0 to  $-30$  V in 300 steps. After each step, the system settles for ten seconds before the CV measurement is taken.

The LCR-Meter only features a power supply which creates a bias voltage up to 2 V. Since the internal supply cannot reach the required voltages, an external source meter unit (SMU) is connected to the setup. However the LCR-Meter is not equipped for higher voltages, therefore the SMU and the LCR-Meter cannot be connected directly to each other. To resolve this, a custom Bias Box was used [24].

While the ground of the SMU is connected to the LCR-Meter with a banana cable, the COM HV output is connected via a BNC connector to the Bias Box. Additionally the  $H_p$ ,  $H_c$ ,  $L_p$  and  $L_c$  ports of the LCR-Meter are connected via

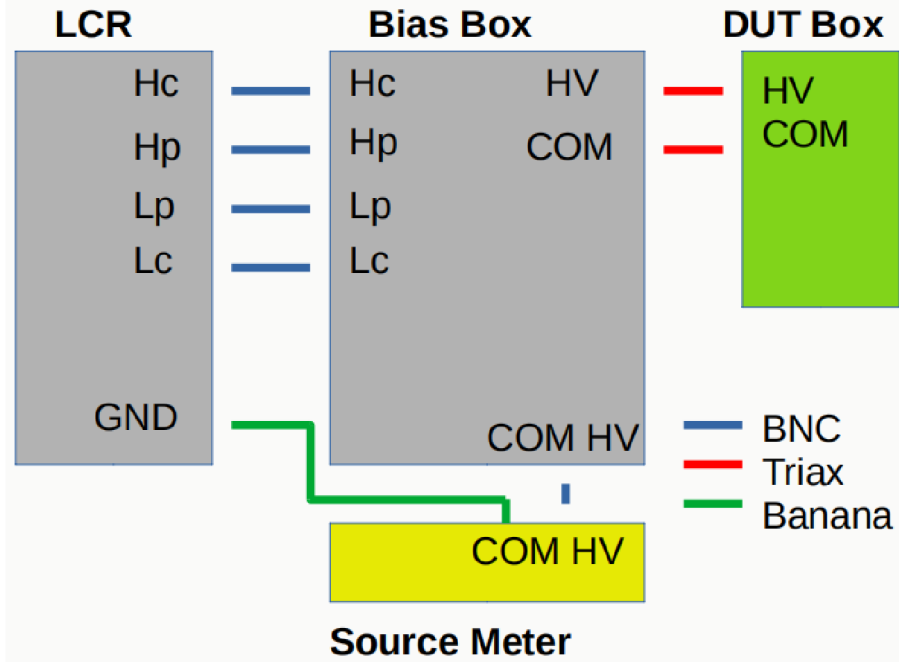


Figure 61: Electronic connections for the CV measurements [24]. The DUT box is directly connected to the bias box. The bias box itself is connected to the LCR-Meter and the source meter.

BNC connectors to the Bias Box. The Bias Box is connected via two triax cables (HV and COM) to the DUT Box with the mounted device under test inside. The DUT Box was also fabricated in Bonn. It has two BNC and fourteen triaxial input sockets which are all connected to a mounting unit in the center of the box. At the mounting unit, a module can be tightly fixated and the voltages can be applied by setting the appropriate jumpers on each side of the mounting unit. Additionally, power lines must be activated by placing jumpers at the corresponding sockets. The DUT Box is built from aluminum, providing shielding against external fields via the Faraday cage effect when closed. The DUT box is placed inside a climate chamber, maintaining a stable temperature of 20°C. A constant flow of dry air and a regulated nitrogen supply ensure low humidity. The chamber is lightproof, which is important since the modules are light-sensitive. For this reason, they are covered with dark tape (see Figure 62).

For the measurements, both drain implants and the source implant are shorted together to form the opposite side of the pn-diode, while the bulk forms the other side. This way the full bulk volume builds the diode volume. The two drain implants are connected to an overall drain line with the two green jumpers on the top and bottom. To short source and drain the white cable has to be used (see Figure 62). To minimize parasitic capacitances and external magnetic fields, the additional cable has to be secured with non-conductive tape at all times. The third green jumper is used to activate the bulk voltage. With the

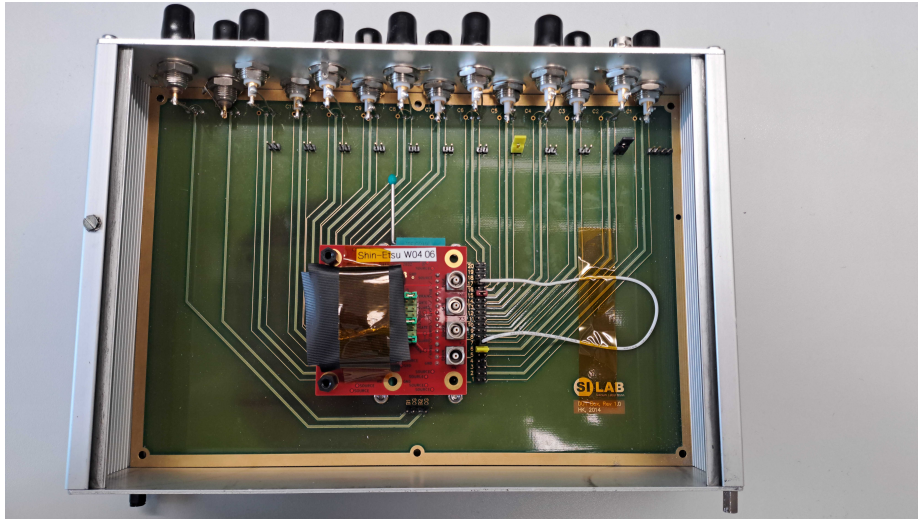


Figure 62: Mounted module used for the CV measurements. The drain and source implants are shorted, the short connection cable is fixed to minimize parasitic effects.

red jumper on the pin headers on the right side of the module, the connection to the triax connectors is enabled. At the triax connector, the yellow jumper is needed to set the ground of the whole setup to the ground of the LCR meter. The same thing happens to the drain line with the black jumper next to the connector and the yellow jumper on the right side of the module.

Before a measurement, the open and short correction has to be applied as explained in Section 6.1. The LCR-Meter features three different storage spaces such that three frequencies can be calibrated at once.

For the open correction, a dummy module is placed on the mounting. The connectors are set in the same way as for the actual CV measurement. The open correction is done for all three frequencies. During the open correction measurement, the aluminum box is closed to form a Faraday cage.

For the short correction, the actual device has to be mounted, which is later used in the CV measurements. For the short correction, a short circuit between drain and bulk must be established. This is done using a short cable near the device, to ensure that only the junction capacitance is affected and to avoid shorting external stray capacitances. This would lead to a wrong correction and therefore worse results. The cable has to be secured again and the DUT box is closed to shield external electro-magnetic fields. Again the short correction is done for all three frequencies.

These precautions ensure reproducible, low-noise CV measurements with minimized parasitic influences across different device configurations.

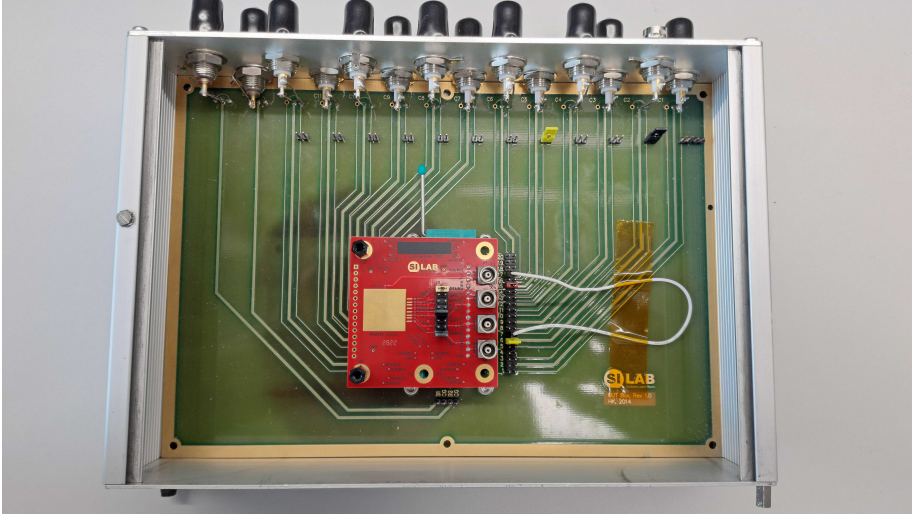


Figure 63: Open correction for the CV measurements. A dummy module is placed in the DUT box, while all connections remain the same.

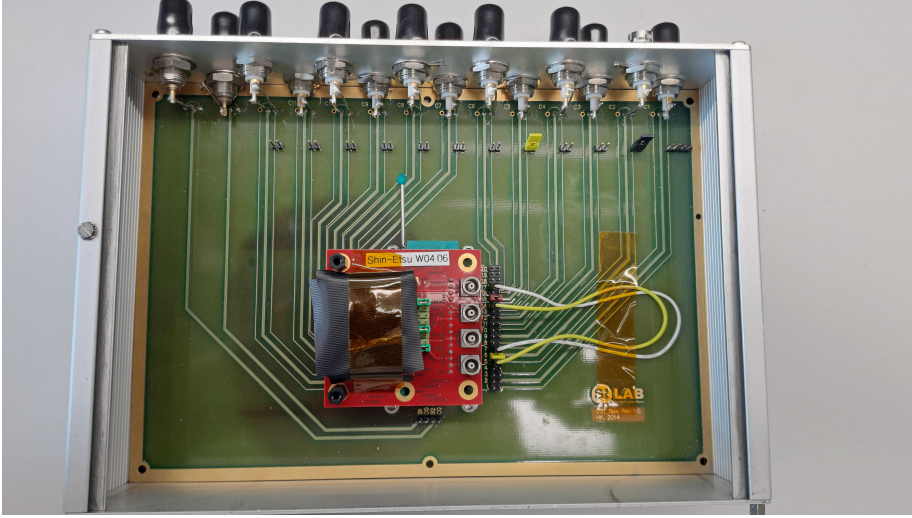


Figure 64: Short correction for the CV measurements. The actual device is placed in the DUT box and a short between drain and bulk is established. The short connection cable is fixed to minimize parasitic effects.

## 6.4 Measurements

The CV measurements are performed at different frequencies ranging from 1 kHz to 1 MHz. For each frequency, the capacitance value is determined along with a statistical uncertainty obtained from five consecutive measurements. Additionally, three complete measurements are performed with a time interval of approximately two hours between them. This procedure allows verification of stability within the statistical uncertainties and provides sensitivity to poten-



tial effects from external factors such as temperature or humidity. The mean capacitance value is obtained from these three measurements along with its associated uncertainty which combines (i) the statistical uncertainties of the individual series, (ii) the variation among the three series, and (iii) the systematic uncertainty of the LCR meter specified as 0.5 pF.

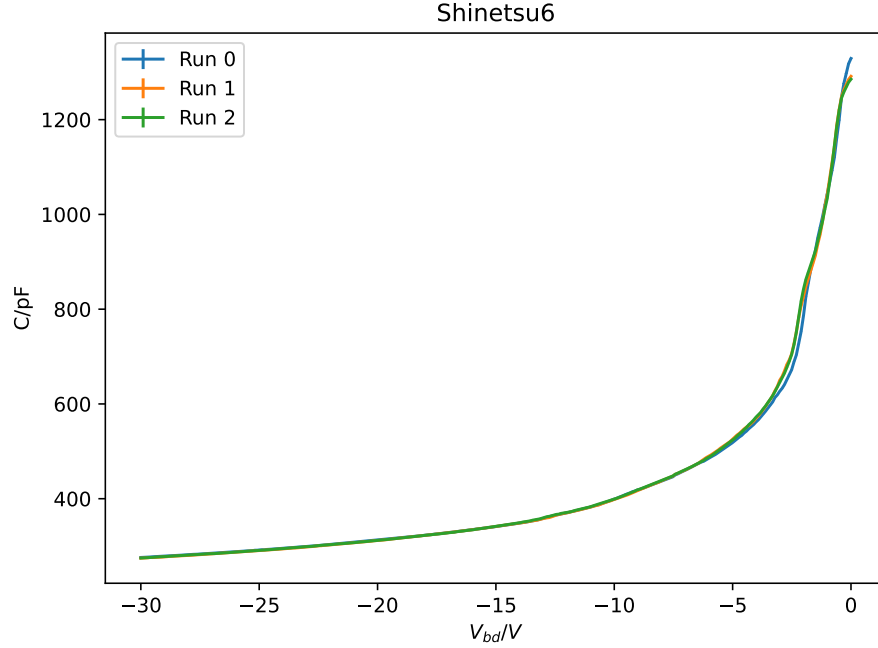


Figure 65: Example of a CV-measurement at 1000 Hz, including open and short correction. The measurement was repeated three times. The capacitance decreases with decreasing voltage applied between bulk and drain.

An example of the CV measurements can be found in Figure 65. The result is a steeply decreasing capacitance value on the order of 1 nF as the bulk-drain voltage  $V_{bd}$  decreases. As one can see by the plot, the statistical uncertainties of a single measurement are very low with less than 1‰. However the measured capacitance values slightly differ across the three repeats, especially in the range of 0 to  $-5$  V. This deviation confirms the necessity to extend the uncertainties as explained before. The differences can arise from changes in environmental temperature, humidity and also heating of the module itself, since it is powered with up to  $-30$  V, which can heat the silicon. These changes cannot arise from open or short correction, since the correction parameters are only measured and applied once.

At low  $V_{bd}$ , the capacitance saturates. This is because the bulk gets depleted and therefore depletion area and thickness do not change much anymore. Ideally, the curve would approach a horizontal asymptote since for a full depletion, area and thickness do not change at all. However for this module, the front and the backside do not build an ideal overlapping area, since the drain and source implant do not cover the full front side. This leads to an additional sideways

depletion for lower  $V_{bd}$  which further lowers the capacitance. Nevertheless the value does not change significantly and is comparable for all frequencies.

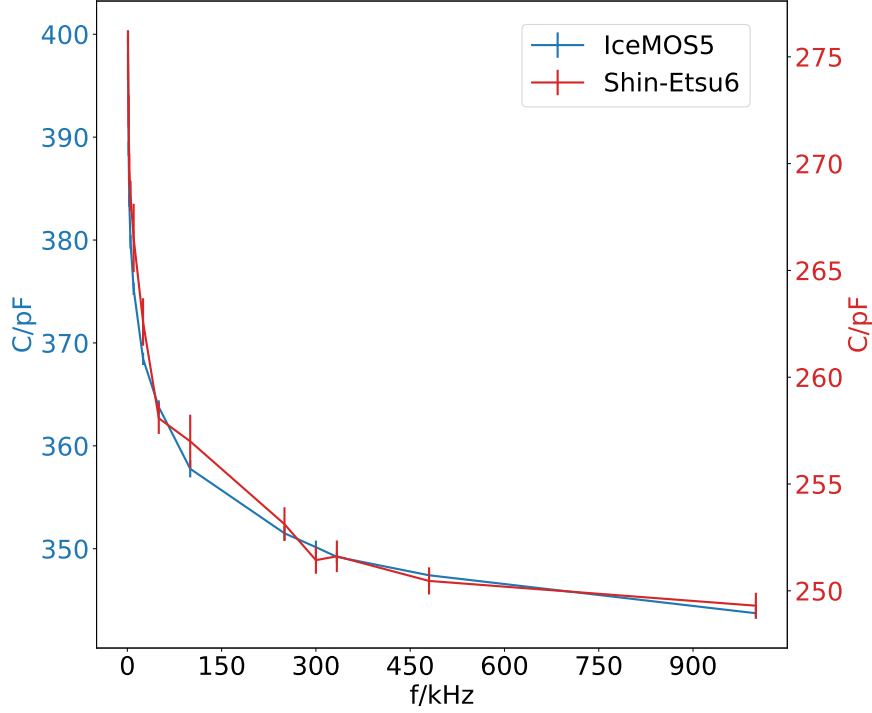


Figure 66: Capacitance values at  $-30$  V for different frequencies. At this voltage the bulk is in full depletion. The capacitance decreases with increasing frequency.

The capacitance values at high depletion can also be plotted against the frequency for both modules (see Figure 66). A sharp decrease in capacitance with increasing frequency is observed for both modules. The Shin-Etsu device has an overall lower capacitance, but the shape is very similar. The lower capacitance most likely arises from different doping levels of the two modules. The doping level variation was estimated to be up to 20% [15], this variation has a large effect on all the measurements taken. A lower doping level leads to a greater depletion width and therefore a lower capacitance.

The sharp decrease in capacitance with increasing frequency happens because the minority carriers can no longer follow the AC-signal of the LCR-Meter and therefore do not contribute to the capacitance anymore. For higher frequencies only the majority carriers contribute to the capacitance, which lowers the overall capacitance of the module. This is known as the 'freeze-out' effect and its extent depends on the specific material properties of each diode.

As explained in Chapter 6.1, the CV measurements can be used to characterize the pn-junction, particularly its depletion voltage and depletion width. This

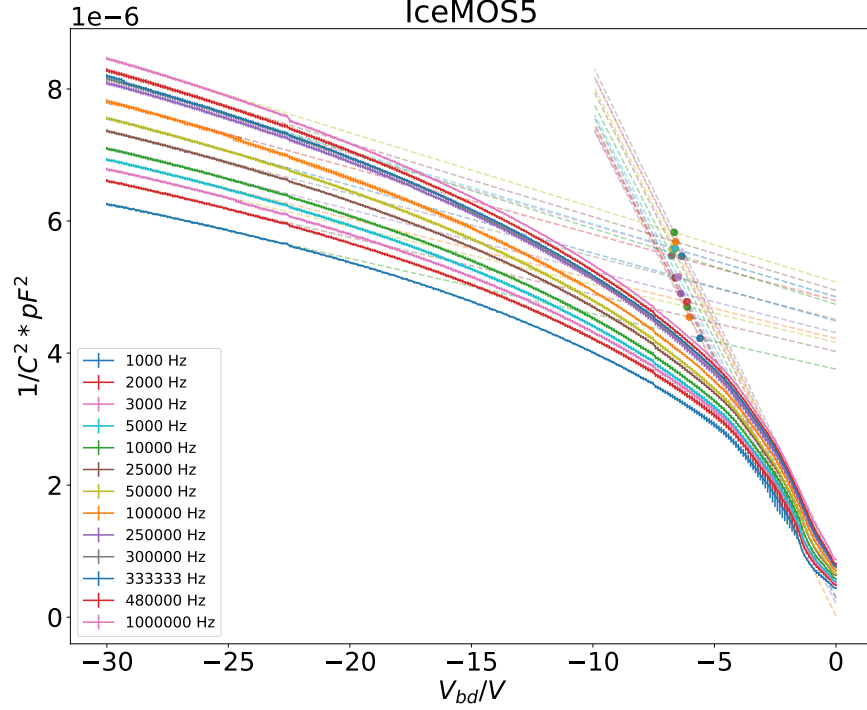


Figure 67: CV measurements done for IceMOS5 with open and short correction plotted in a  $1/C^2$  diagram to extract the depletion voltage. The curves shift in slope close to zero volts.

is done by plotting the CV measurement in a  $1/C^2$  diagram as in Figure 67. A linear fit is applied to the data near  $V_{bd} = 0$  V and  $V_{bd} = -30$  V. In the region close to  $V_{bd} = 0$ , secondary effects become apparent, indicated by a small kink in the curve. To obtain a reliable fit, only values between  $V_{bd} = -1.5$  V to  $V_{bd} = -2.5$  V are considered. The intersection of these fitted lines defines the depletion voltage.

The same procedure is applied to the Shin-Etsu6 module (see Figure 68). Since the Shin-Etsu device has a lower capacitance, the  $1/C^2$  values are larger, but also the slope is flatter and the uncertainties are higher. This makes the fitting process more challenging, especially since secondary effects again alter the behavior at small bias voltages. The fit range is therefore  $-2.5$  V to  $-4.5$  V. The intersection points vary more significantly than for the IceMOS5 device, primarily due to the shallower slopes of the fitted curves.

With the depletion voltage and known geometric data, it is also possible to determine the depletion width and thus the bulk thickness under full depletion [22].

$$d_{n,p} \approx x_{n,p} \approx \sqrt{\frac{2\epsilon\epsilon_0}{e} \frac{1}{N_{D,A}} (V_{bi} + V_{ext})} \approx 3.6 \times 10^7 \sqrt{\frac{V_{ext}/\text{V}}{N_{D,A}/\text{cm}^{-3}}} \mu\text{m} \quad (12)$$



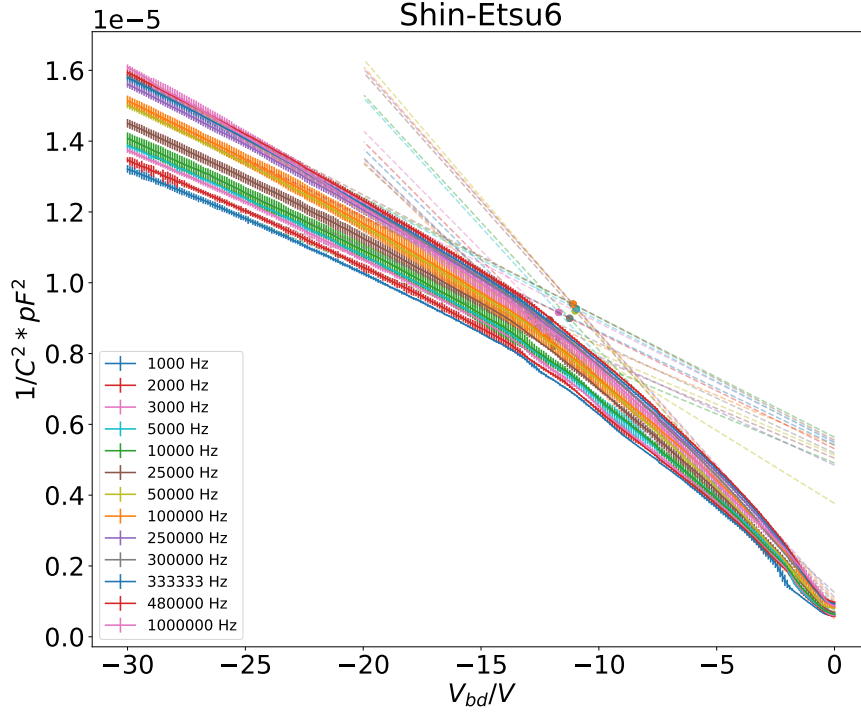
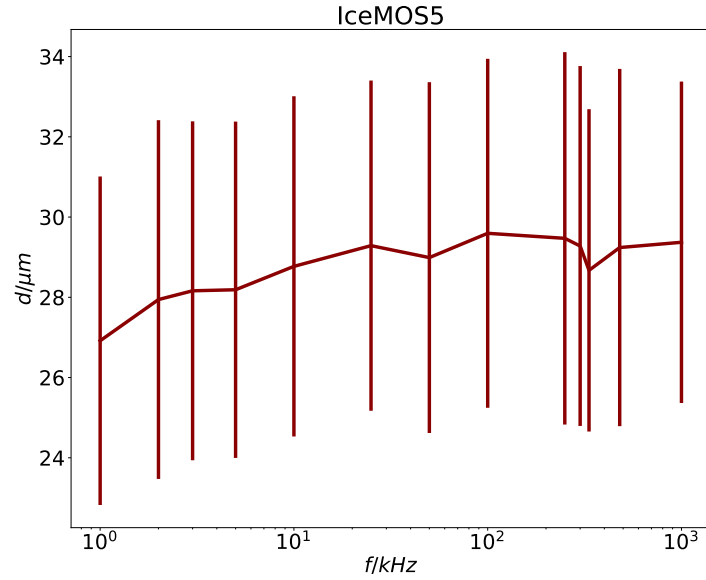


Figure 68: CV measurements done for Shin-Etsu6 with open and short correction plotted in a  $1/C^2$  diagram to extract the depletion voltage. The curves shift in slope close to zero volts.

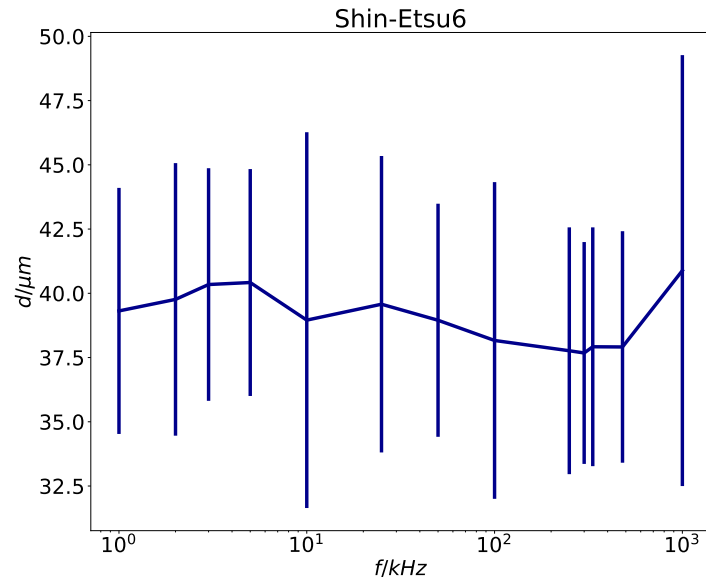
with  $N_{D,A} = 1 \times 10^{13} \text{ cm}^{-3}$  for both devices. The uncertainty of the full depletion voltage is taken from the fit, while the uncertainty of the doping concentration is still estimated to be 20% [15].

For the IceMOS5 module, the depletion width remains stable at around  $28 \mu\text{m}$  across all frequencies. This is expected, as the depletion width should be frequency-independent. The Shin-Etsu6 module shows stronger variation, however the variation is inside the uncertainty. The mean depletion width is around  $39 \mu\text{m}$ . As mentioned earlier, the full thickness of each module is approximately  $75 \mu\text{m}$ . The large doping variation explains the different values for the IceMOS5 and the Shin-Etsu6 module, but the measured full depletion width does not match the expected bulk thickness. The likely explanation is the presence of sideways depletion. As already discussed in Figure 65, the capacitance does not level off at low voltages, indicating the presence of sideways depletion. As a result, the depletion voltage can no longer be reliably determined using linear fits, since the relation  $\frac{1}{C^2} \sim (V_{bi} - V)$  assumes an ideal parallel-plate capacitor. The same assumption also underlies Equation 12, limiting its validity in this case.

Therefore, determining the depletion width becomes significantly more complex, requiring correction terms that cannot be evaluated with the current experimental setup.



(a) Depletion width for the IceMOS5 module for different frequencies. The mean depletion width is around 28 μm



(b) Depletion width for the Shin-Etsu6 module for different frequencies. The mean depletion width is around 39 μm

Figure 69: Comparison of the depletion width behavior for the IceMOS5 and Shin-Etsu6 modules at various measurement frequencies.

The limiting uncertainty for this experiment is the doping concentration. With a better knowledge of the actual doping of both modules, it might have been possible to observe an actual difference in the full depletion width. It would be expected, that the Shin-Etsu module has a larger depletion width, since the thicker oxide layer of the IceMOS module shifts the junction boundary deeper into the bulk. This effectively reduces the depletion region for the same applied voltage. The difference should be around 200 nm, which is far off the current uncertainty of about 4  $\mu\text{m}$  and therefore not resolvable in this experiment.

The depletion width is determined by the threshold voltage. The threshold voltage itself is determined with the interception of the two fitted curves. The fit range introduces a systematic uncertainty to the measurement, which might also explain the discrepancy between the expected width and the measured width. However the fit range was chosen such that disturbing factors should contribute less to the determination of the threshold voltage, which means that the side-wards depletion is the main contributor to the deviation of the depletion width from the expected depletion width.

## 7 Conclusion

Throughout this thesis, a variety of experiments involving field-effect transistors (FETs) were conducted to investigate their electrical behavior and particle response under different operating conditions.

DEPFET devices were characterized through static measurements and dynamic tests using hybrid5 modules, which imitate the operational environment in the Belle II detector system.

The static characterization focused on measuring the drain current response to variations in both the gate-on voltage and the clear voltage. For the gate-on voltage, measurements were carried out on unbiased as well as biased matrices, the biased measurements were used to determine the transconductance. The clear voltage studies revealed the dependence of the drain current on the internal gate. Future investigations should include the ClearGate contact to provide deeper insight into the formation of the conductive channel between the internal gate and the clear implant. This would improve the understanding of the clearing process.

The hybrid5 studies enabled a direct comparison between the established PXD9 technology and the newly developed PXD13 technology. A detailed comparison was carried out between H5026, containing a PXD9 type minimatrix, and H5033, equipped with a standard PXD13 type minimatrix. H5026 performed consistent with previous measurements of PXD9 matrices and with the results from the static measurements. In addition, an energy calibration was successfully performed for this hybrid.

In contrast, H5033 did not perform as expected. Compared to the H5026 it showed a reduced transconductance and measured a lower source signal, which indicates a lower internal amplification. The minimatrix exhibited a double-row pattern with originating from the source line structure of the matrix. Further measurements with additional standard PXD13 minimatrices are necessary to clarify the origin of these differences.

Preliminary results for the new super- $g_q$  PXD13 technology were also presented. H5034 exhibited a higher transconductance compared to the PXD9 technology. Also an even more pronounced double-row pattern than that for H5033 was observed. The super- $g_q$  minimatrices require a further characterization, particularly regarding transconductance and internal amplification.

The MOSFETs were tested in CV measurements to gain insight into bulk properties relevant for DEPFET-like devices. These measurements allowed observation of the freeze-out effect of the charge carriers and enabled determination of both the threshold voltage and the depletion width. Due to the structure of the MOSFETs, a discrepancy between the expected and the experimentally determined depletion width was identified. Addressing this discrepancy will require further investigation, including simulation of the depletion of the MOSFETs, refined measurement procedures, and tailored calculations.

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## Appendix

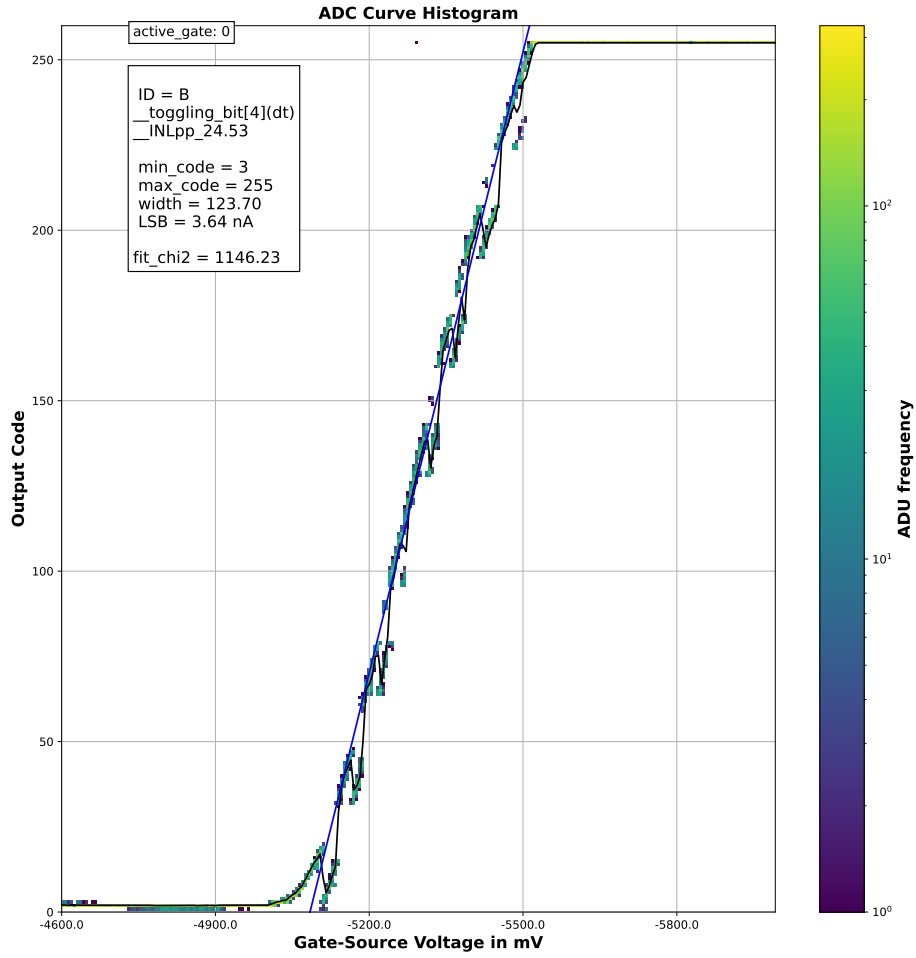


Figure 70: ADC calibration of a single channel of H5026 using the DEPFETs as a current source. The calibration curve starts near zero, exhibits a pronounced curvature around  $-5000$  mV and then increases until it saturates at the maximum of 255 ADU. A bit error in the ADC causes discrete jumps in the output code.

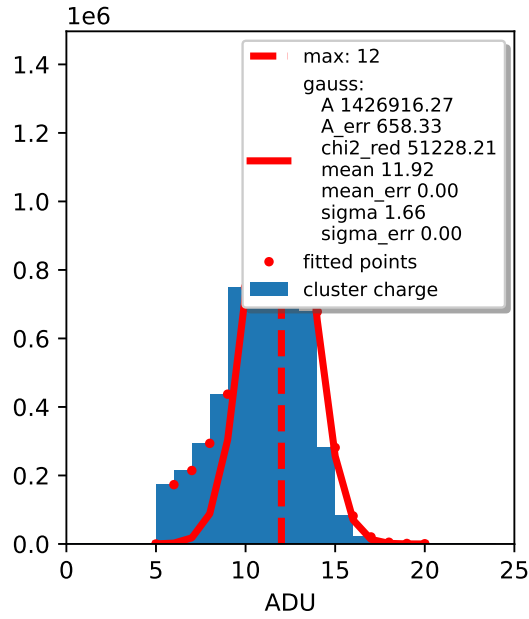


Figure 71: Cluster charge spectrum for  $^{55}\text{Fe}$ . A single Gaussian peak is fitted, as the signal lies close to the noise. The  $K_\alpha$  and  $K_\beta$  lines cannot be resolved. The events around five ADU originate from background and distort a double Gaussian fit. The mean charge is approximately 12 ADU.

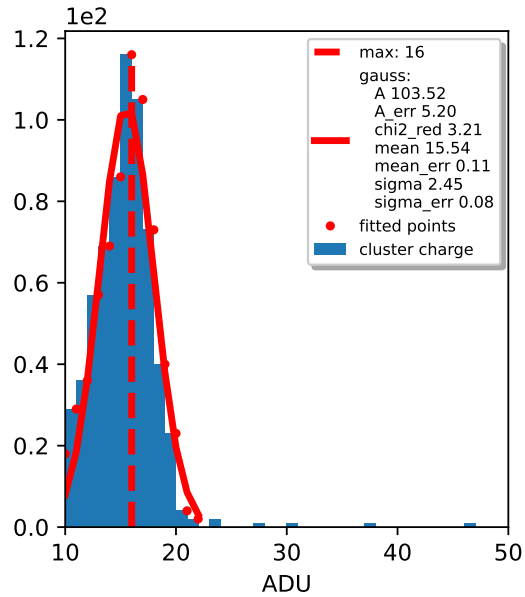


Figure 72: Cluster charge spectrum for copper. A single Gaussian peak is fitted, as the signal amplitude is low. The  $K_\alpha$  and  $K_\beta$  lines cannot be separated. The events around 10 ADU are likely background or misclustered and distort a double Gaussian fit. The mean charge is approximately 16 ADU.



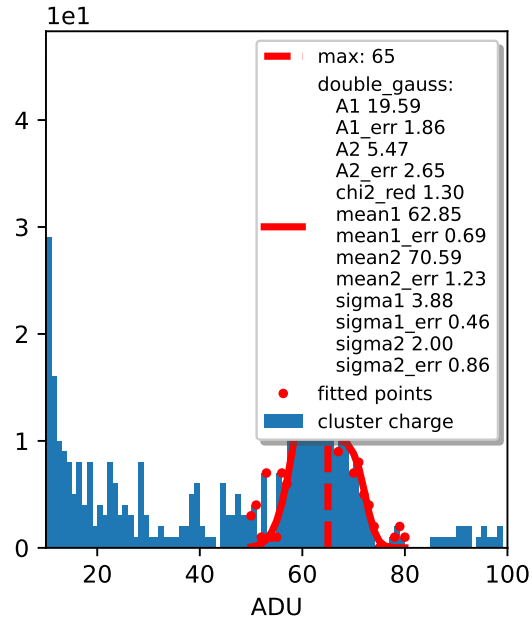


Figure 73: Cluster charge spectrum for barium. A double Gaussian function is fitted to distinguish between the  $K_\alpha$  and  $K_\beta$  lines. The mean charge of the  $K_\alpha$  line is approximately 63 ADU.

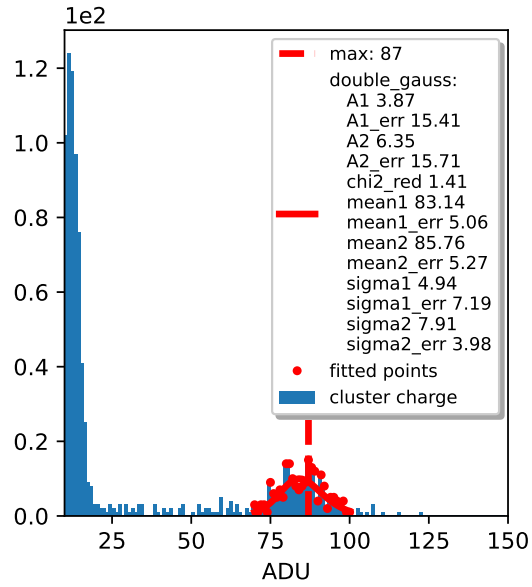


Figure 74: Cluster charge spectrum for terbium. A double Gaussian function is fitted to separate the  $K_\alpha$  and  $K_\beta$  lines. The mean charge of the  $K_\alpha$  line is approximately 83 ADU.

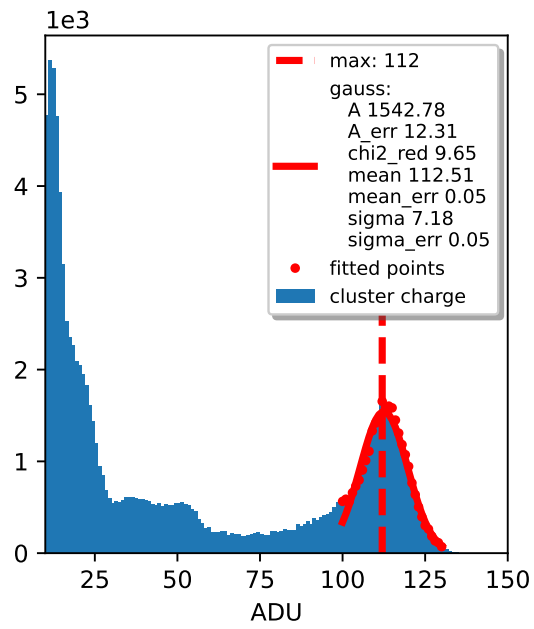


Figure 75: Cluster charge spectrum for  $^{241}\text{Am}$ . A single Gaussian function is fitted, as the decay of  $^{241}\text{Am}$  predominantly produces a single  $^{237}\text{Np}$   $\gamma$ -transition with an energy of about 60 keV. The mean charge is approximately 113 ADU.

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Zunächst möchte ich Professor Dingfelder und Professor Bernlochner danken, dass ich die Arbeit in ihrer Arbeitsgruppe durchführen durfte. Außerdem für die Beratung und Hilfe innerhalb und außerhalb der Meetings.

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