

DEVELOPMENT OF A READOUT SYSTEM FOR THE
TOP DETECTOR FOR BELLE II AT SUPERKEKB

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By

Matthew Zachary Andrew

Thesis Committee:

Keisuke Yoshihara, Chairperson

Thomas Browder

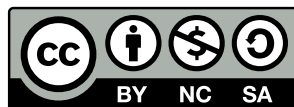
Jelena Maricic

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To my partner,

Jess,

who had to endure it all during the course of this work.

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Thanks to my dad who taught me to not be intimidated.

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Thank you all.

ABSTRACT

This thesis details the development of the readout electronics for the Time-of-Propagation (TOP) detector system, part of the Belle II detector located at the interaction point of the SuperKEKB electron-positron collider in Tsukuba, Japan.

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LIST OF ACRONYMS

ADC	Analog-to-Digital Converter	7, 16 f.
ASIC	Application-Specific Integrated Circuit	5, 7 f., 12, 15, 17–23, 31, 34, 36, 38 ff., 51
DAC	Digital to Analog Converter	18 f., 22
DAQ	Data AcQuisition	5–10, 14, 18 f., 21
DSP	Digital Signal Processor	15
FPGA	Field Programmable Gate Array	6 ff., 13 ff., 17–21, 23, 29, 31, 34 f., 38
GDL	Global Decision Logic	18, 21, 31
HV	High Voltage	iv, 23, 32 f.
LV	Low Voltage	iv, 33 f.
PCB	Printed Circuit Board	9, 14 f., 17, 21, 23, 29, 34 f., 39
PL	Programmable Logic	29, 38, 40, 50
PS	Processing System (“ARM cores”)	29, 40, 50
ROPC	ReadOut PC	14, 41
SCROD	Standard Control ReadOut Data	15, 19–23, 29, 31, 35, 38 f.
SLAC	Stanford Linear Accelerator Center	2, 40, 42, 78
TDC	Time-to-Digital Converter	6, 8, 16, 39
TRG	TRiGger	5–8, 10

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CHAPTER 1

INTRODUCTION

1.1 High-Energy Physics and the Standard Model

The Standard Model (SM) is the name given to the best description we have so far of three of the four fundamental forces (strong, weak and electromagnetic; only excluding gravity). The SM can be used to explain much about the elementary particles, interactions between them and the force mediators: W , Z , photon (γ) and gluons (g). The elementary particles (see Tab. 1.1) include three generations of quarks: up (u), down (d), strange (s), charm (c), top (t), bottom (b), three generations of leptons: electron (e), electron neutrino (e_ν), muon (μ), muon neutrino (μ_ν), tau (τ), tau neutrino (τ_ν), the corresponding 12 anti-particles, as well as the Higgs boson (H).

u	c	t	H	
d	s	b	g	
e	μ	τ	γ	
ν_e	ν_μ	ν_τ	W	Z

Table 1.1: Standard Model particles

The Cabibbo-Kobayashi-Maskawa (CKM) matrix describes the relative likelihood that quarks will undergo transitions from one flavor to another:

$$\begin{bmatrix} d' \\ s' \\ b' \end{bmatrix} = \begin{bmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{bmatrix}_{CKM} \begin{bmatrix} d \\ s \\ b \end{bmatrix}.$$

There are six unitarity triangles which are comprised of squares of the CKM matrix elements. The sides and angles of these triangles are measurable quantities related to the branching fractions of decaying quarks. Within the framework of the Standard Model, we expect these triangles to be closed, and pursuing this experimentally is an interesting test of the SM and to probe what might lie beyond.

1.2 Hadrons, Mesons and Quarks

Hadrons are combinations of quarks which are either the familiar baryons (protons, neutrons, etc) or the mesons (pions, kaons, etc). The forces holding quarks together in hadrons are such that attempting to split the quarks apart does not result in free quarks but rather requires so much energy that new quarks pop into existence to pair up with the initial ones, a process known as quark confinement.

Mesons are quark-antiquark pairs. An example is the B meson, which is a bottom antiquark paired with an up (B^+), down (B^0), strange (B_s^0) or charm (B_c^+), whereas a bottom antiquark bound together with a bottom quark is referred to as an upsilon meson (Υ). An Υ meson readily decays into a $B\bar{B}$ meson pair, which is comprised of a B meson and a $\bar{B}$ meson (an anti- B meson).

1.3 B -factories

Over roughly a decade after the experimental confirmation of the bottom quark (and upsilon meson) in 1977, the concept of a B -factory was proposed and developed [1]. A B -factory would collide electrons and positrons near the $\Upsilon(4S)$ resonance ($10.58 \text{ GeV}/c^2$) so that copious quantities of $B\bar{B}$ meson pairs would be produced *just* above the threshold for such a process. Each $B\bar{B}$ meson pair would emerge with relatively little center-of-momentum (CoM) energy. Wrapping the interaction point with a detector that measures the decay products would then allow collection of increasingly higher precision measurements just by running this type of facility continuously, hence the name B -factory [2].

Because $B\bar{B}$ mesons only last $\mathcal{O}(\text{ps})$ in their rest frame, it is advantageous to give the colliding beams different energies (that still sum to that of the $\Upsilon(4S)$ resonance) so that the B and $\bar{B}$ mesons are traveling relativistically in the lab frame, extending their lifetime in the frame of the detector and separating the primary and secondary vertices of subsequent decays [3].

1.4 KEKB and Belle and PEP-II and BaBar

Two experiments to pursue this concept were built in the 1990s: BaBar (located at the PEP-II collider at Stanford Linear Accelerator Center (SLAC) in Menlo Park, CA and ran from 1999-2008) and Belle (located at the KEKB collider at the KEK High-Energy Research Organization in Tsukuba, JP and ran from 1999-2010).

Instantaneous luminosity, L , is a measure of the rate of how many interesting collisions happen in a collider per unit time. Integrated luminosity, L_{int} , is the running total of L and is 513.70 fb^{-1} for BaBar and 710 fb^{-1} for Belle (at the $\Upsilon(4S)$ resonance). Combined, the two experiments accumulated data from approximately 1.22 billion $B\bar{B}$ meson pairs.

1.5 SuperKEKB: high-luminosity super B-factory

Because the branching fractions for some of the rare decays of interest are $\mathcal{O}(\text{one-in-a-billion})$, it is easy to see why many of the results are statistics-limited. Having a (much) larger dataset would enhance the signal and lower statistical uncertainties enhancing our ability to do precision measurements to verify the physics of the Standard Model as well as discover new physics.

SuperKEKB was designed to deliver 40x higher instantaneous luminosity compared to KEKB with the goal of collecting data from 50x as many $B\bar{B}$ meson pairs as Belle. It was built in the KEKB tunnel from 2010-2016 (see Fig. 1.1), using many of the original components, upgrading them where necessary [4].

In order to obtain higher precision measurements, Belle II needs to collect more data, and to collect more data, a higher instantaneous luminosity collider is desired to reduce the time required to run the experiment. Belle ran for about a decade and so to collect 50 times the data would have required running the same accelerator and detector for another 500 years(!). So the intention instead is to run with $\approx 40x$ the instantaneous luminosity, which means the same results will be available in a mere 15 years. This will ensure Belle II stays competitive with other high-energy physics experiments located throughout the world.

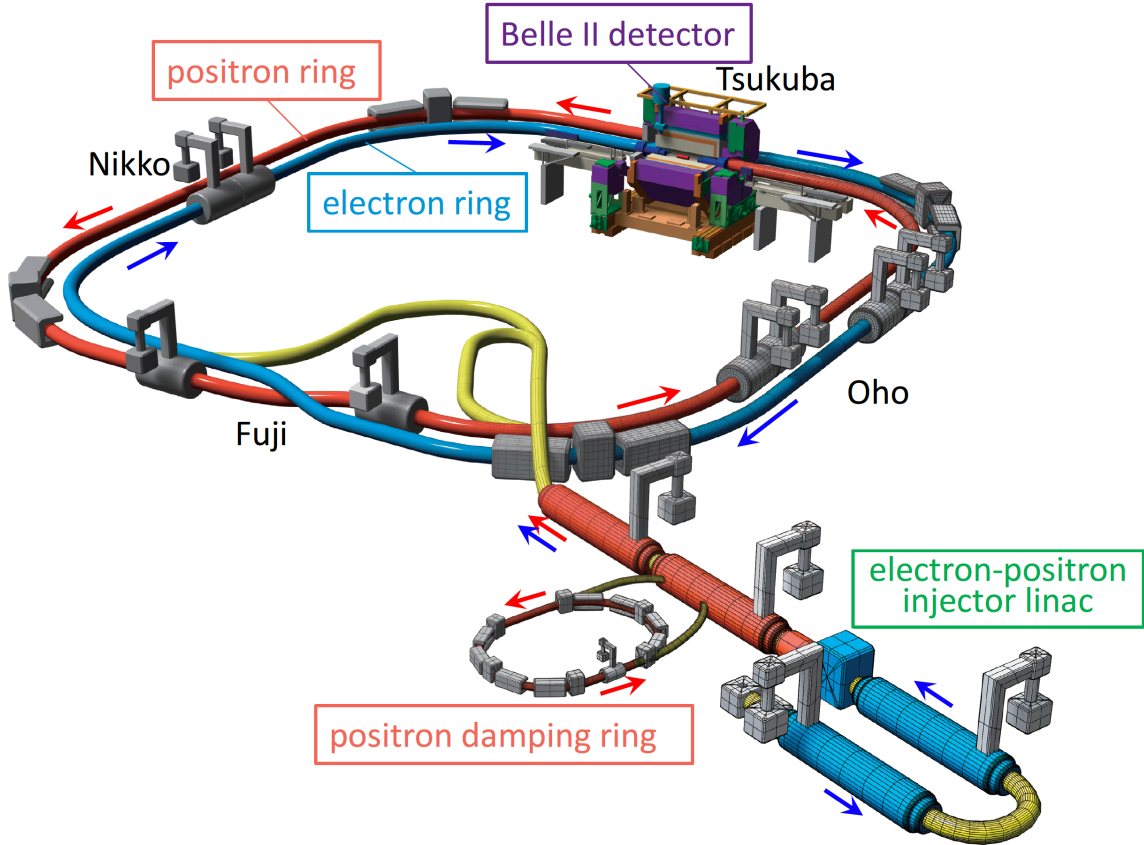


Figure 1.1: Schematic layout of SuperKEKB showing the linac, the damping ring, the electron and positron main/storage rings and the Belle II detector (courtesy SuperKEKB group)

The principal way SuperKEKB achieves a higher instantaneous luminosity compared to KEKB is by using the nanobeam scheme near the interaction region between the electron and positron beams (see Fig. 1.2 and Fig. 1.3). Decreasing the beam sizes by a factor of 20 increases the density

of charged particles in the overlap region which makes interactions proportionally more likely. For a similar reason, a second way SuperKEKB increases luminosity is by doubling the beam current in each ring. Both of these result in more particles per second per unit area crossing each other in the interaction region.

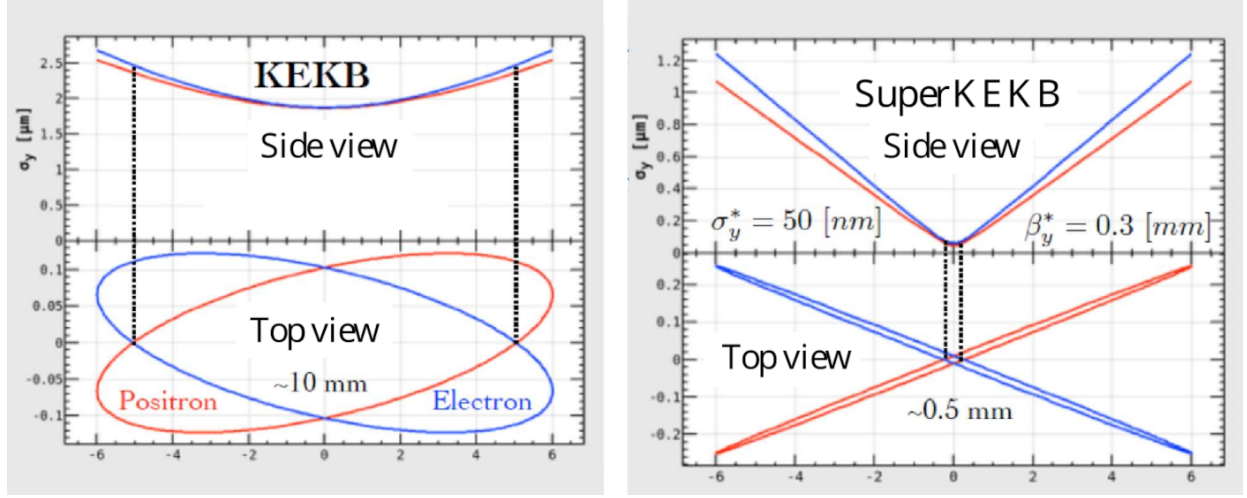


Figure 1.2: Comparing KEKB to SuperKEKB: schematic view of the interaction region (courtesy S. Uno)

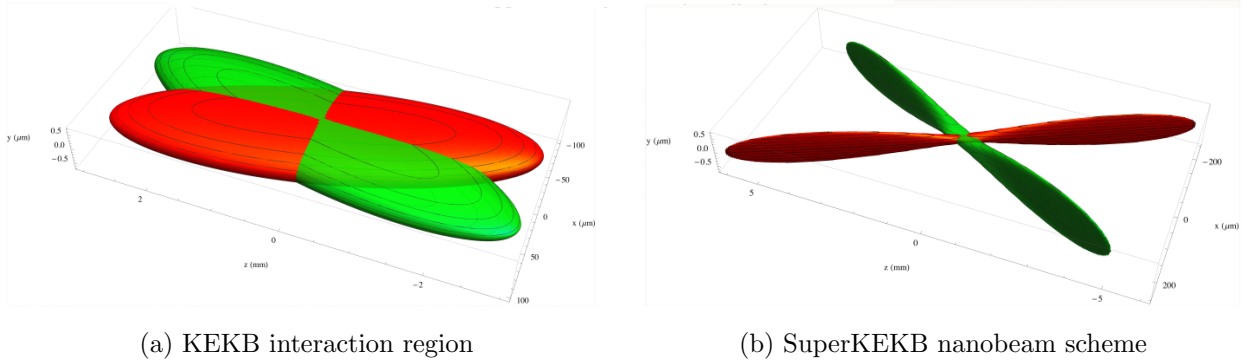


Figure 1.3: A 3D representation of the KEKB and SuperKEKB collision schemes (courtesy SuperKEKB group)

The energy of the particles in each ring is also changed relative to KEKB to increase the positron beam lifetime (from 3.5 GeV to 4 GeV) and decrease the electron beam synchrotron radiation power (from 8 GeV to 7 GeV).

The crossing angle of the beams was increased to help reduce beam overlap outside the *intended* interaction region.

TiN-coated aluminum beampipes with an antechamber are used instead of the TiN-coated copper beampipes of KEKB. The antechamber reduces the synchrotron radiation power density

and heating of the beam pipes as well as reducing the impedance which helps suppress unwanted high-order modes of oscillation.

A new positron damping ring reduces emittance before injection into the main ring. Low emittance in both rings is important for two reasons: To help minimize unwanted betatron oscillations; Low emittance also helps to ease injecting charge to top-up the beams (a process called continuous injection), a more pressing need now because using the nanobeam scheme shortens the beam lifetimes compared to KEKB [4].

1.6 Belle II detector

Belle II is the upgrade to the Belle detector to accommodate the much higher data rate that comes with a much higher L , as well as to deal with the higher background radiation environment that also comes with higher L .

Belle II is a universal spectrometer which means the data acquired is not just for one purpose and can be analyzed in multiple ways. This flexibility allows it to be used to measure not just branching fractions of rare decays of B mesons but also tau and charm physics, as well as many exotic processes and other tests of physics beyond the standard model (see Fig. 1.4). A technical design report [5] was compiled and published in 2010 that describes the effort needed to accomplish this.

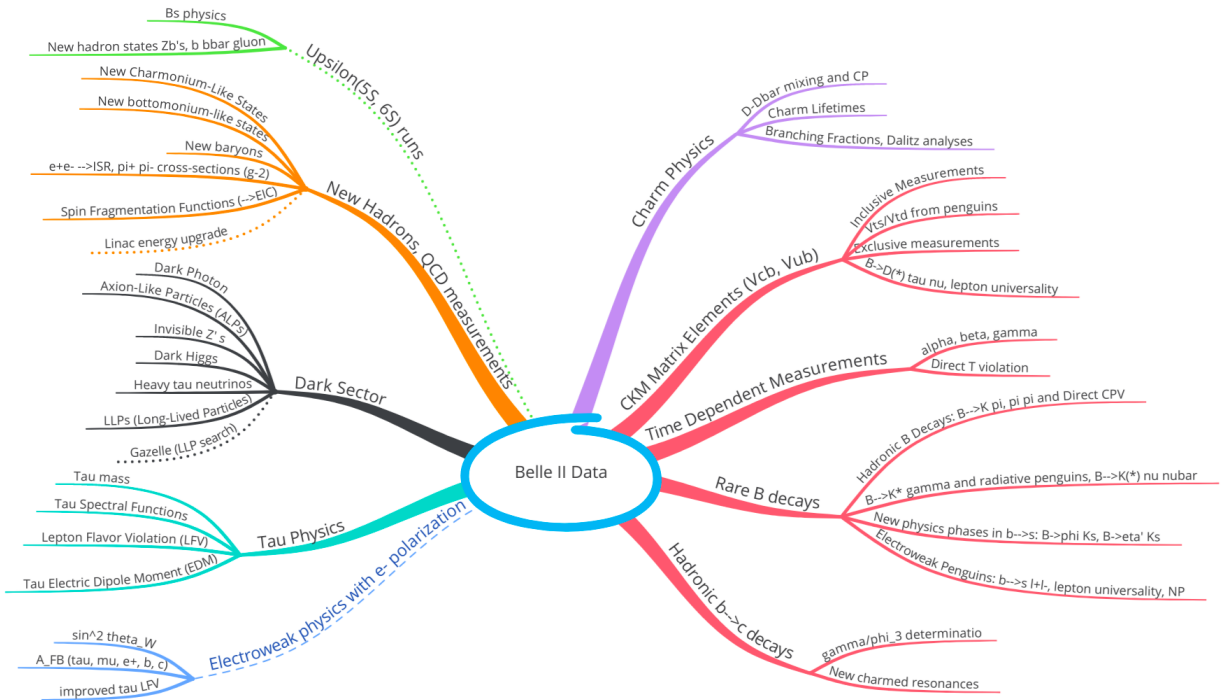


Figure 1.4: Physics reach of Belle II (courtesy T. Browder)

Belle II consists of a series of subdetectors (described below; see Fig. 1.5), a Data AcQuisition (DAQ) system and a TRiGger (TRG) system.

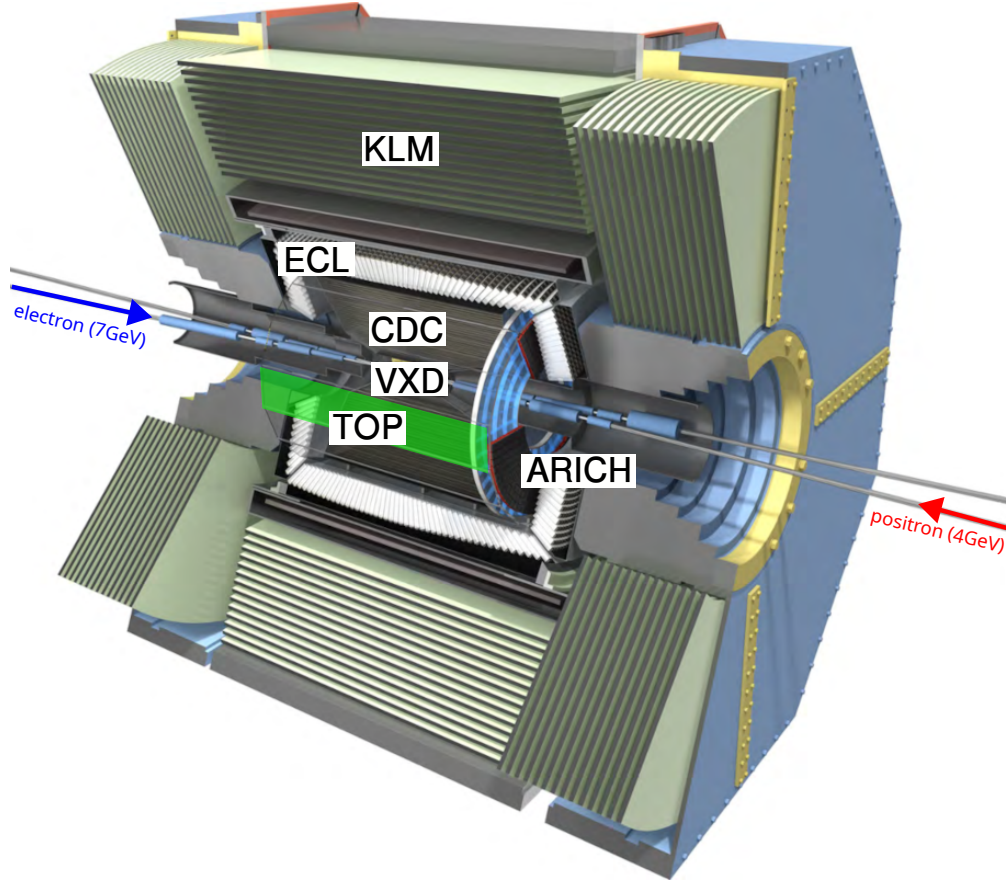


Figure 1.5: Belle II subdetectors showing incoming beams of e^+ and e^- (courtesy Belle II group)

1.6.1 SVD + PXD = VXD

The Pixel Detector (PXD) is comprised of two layers of DEpleted P-channel Field Effect Transistor (DEPFET) sensors. In total, there are $\mathcal{O}(8 \text{ million})$ channels. The two layers of the PXD surround the beam pipe and are located at radii of 14 mm and 22 mm (meaning the distance from the detector symmetry axis) [6].

The Silicon Vertex Detector (SVD) is comprised of 4 layers of double-sided silicon strip sensors, arranged in structures referred to as ladders. The 128-channel Application-Specific Integrated Circuit (ASIC) used to read the ladders out is called the APV25. There are 222,744 channels in total. The SVD is located between radii 39 mm and 135 mm (surrounding the PXD) [7].

Together the PXD and the SVD form what is called the Vertex Detector (VXD) which precisely locates the vertices of particle jets during analyses (crucial for doing time-dependent CP-violation

studies).

1.6.2 CDC

With the aid of a 1.5 T magnetic field, the Central Drift Chamber (CDC) tracks charged particles as they travel outward in helical trajectories. It is a multi-wire drift chamber with approximately 50% of the wires parallel to the symmetry axis of the detector (for determining the azimuthal angle ϕ and the distance *from* the symmetry axis) and the remainder at a stereo angle (for determining θ and/or the distance *along* the symmetry axis). Comprised of 14,336 high voltage conductors in a mixture of He and Ethane gasses, the CDC can measure the transverse momenta of charged particles to below 0.5 % all the way to 4 GeV/c [8]. The deposited charge is measured by Flash Analog-to-Digital Converters (FADCs) and the drift time is measured by a Time-to-Digital Converter (TDC) implemented inside the Field Programmable Gate Array (FPGA) which also connects to the TRG and DAQ systems. The CDC is located just outside the VXD and extends to a radius of 1130 mm.

1.6.3 ARICH

The Aerogel Ring Imaging Cherenkov (ARICH) is located in the forward endcap, just outside the CDC. There are two layers of aerogel with different indices of refraction that provide proximity focusing for the Cherenkov photons which then fall onto Hybrid Avalanche PhotoDetectors (HAPDs). Control and readout for each HAPD is done with four SA03-series readout ASICs connected to an FPGA, which passes the data to the TRG and DAQ systems [9].

1.6.4 ECL

Energy deposition in the barrel and endcap is measured with the Electromagnetic Calorimeter (ECL). The barrel part of the ECL is located just outside the TOP and the endcap sections are located just outside the ARICH in the forward direction and the CDC in the backward.

The ECL consists of 8,736 thallium-doped cesium iodide (CsI(Tl)) crystals, each coupled to a pair of S2744-08 photodiodes [10]. The two signals are amplified and then summed and shaped with another amplifier. A Flash Analog-to-Digital Converter (ADC) Module (FAM) then digitizes the signals which are then collected and passed on to the TRG and DAQ systems.

1.6.5 KLM

The endcaps and the first few layers of the barrel are instrumented with scintillating plastic fibers embedded with wavelength shifting fibers which are then coupled to Silicon Photomultipliers (SiPMs). The signals from these are amplified and sent to waveform sampling and digitization ASICs.

The remainder of the barrel is instrumented with Resistive Plate Chambers (RPCs), which use a discriminator and a TDC implemented in an FPGA.

Data from the two KLM subsystems are consolidated in a Data Concentrator (DC) board, which handles control, triggering and readout to the TRG and DAQ systems [11].

The KLM is located outside the ECL and is interspersed with the magnet iron that forms the return yoke of the 1.5 T field, so the charged particle tracks bend less on the outer layers.

CHAPTER 2

TIME OF PROPAGATION (TOP) DETECTOR SYSTEM

2.1 Overview and physics goals

2.1.1 Particle IDentification (PID)

In order to precisely determine the branching ratios for rare decays, it is necessary to distinguish particle species with high fidelity. The various subdetectors in Belle II can measure location, momentum, charge, time, energy and dE/dx (energy deposited per unit distance) in various combinations, but not all of these simultaneously and not all equally well across the range of particle momenta that can occur in an event.

The TOP detector system provides crucial PID information in the barrel region of Belle II (while the ARICH provides it in the forward endcap direction).

2.1.2 My contributions

This thesis (specifically chapters 4 “first generation” and 5 “second generation”) describe the development of the readout electronics for the TOP detector system from 2010 to 2016.

During the initial phase of this development, I entered schematics and planned and routed the layouts of most of the key Printed Circuit Boards (PCBs), including overseeing the manufacture, parts procurement and assembly stages. Simultaneous with the PCB design, I built a 3D CAD model of each PCB assembly to check for mechanical conflicts. I wrote much of the readout software used throughout, and I wrote a small part of the firmware. Later, to facilitate continued firmware and software development, I set up the Hawaii “pocketDAQ” which modeled the DAQ system of Belle II. I found flaws in some of the firmware and wrote regression test software to verify they got fixed and stayed fixed. For every incarnation of this system, I wrote documentation and made a variety of diagrams and other support materials to document the system for collaborators and others.

2.2 Principle of operation

2.2.1 Cherenkov effect

Cherenkov light is emitted by charged particles whenever they are traveling faster than the speed of light in that material, $v = \frac{c}{n}$ (here, c is the speed of light in a vacuum and n is the index of refraction of the material; see Fig. 2.1). In a high center-of-momentum energy collision like those in Belle II, any material with an index of refraction $n \approx 1.5$ will easily produce Cherenkov light when the charged decay products travel through that material (see Fig. 2.2 and Fig. 2.3).

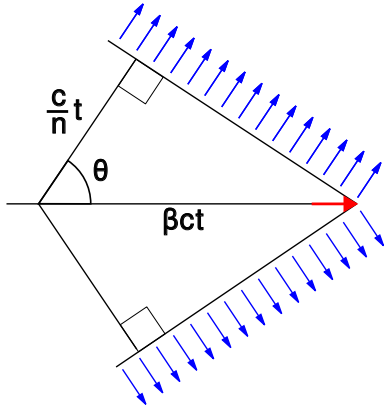
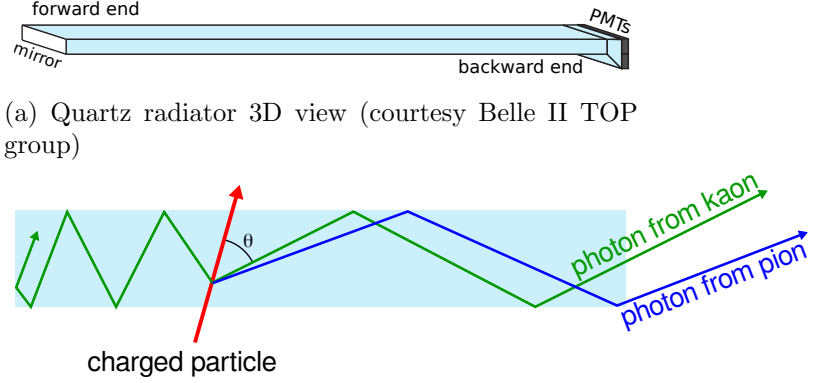


Figure 2.1: Cherenkov effect (courtesy A. Horvath)



(a) Quartz radiator 3D view (courtesy Belle II TOP group)
(b) Folded Cherenkov ring images can be used to distinguish kaons from pions

Figure 2.2: Time-of-Propagation (TOP) concept

The opening angle of the radiated light follows from the simple relation $\cos(\theta) = \frac{1}{n\beta}$ where $\beta = \frac{v}{c}$. Measuring the angle θ will then determine the speed of the charged particle that initiated the emission.

When the material is transparent, segmented photodetectors can be placed on the periphery and the result is called a Ring Imaging Cherenkov (RICH) detector system. When the transparent material is highly polished and the detector relies on the light being Totally Internally Reflected (TIR), the detector is referred to as a Detection of Internally Reflected Cherenkov light (DIRC) detector system [12].

2.2.2 TOP detector system

The TOP detector system is the DIRC part of Belle II responsible for distinguishing kaons (K) from pions (π) in the barrel region (just outside the CDC). Distinguishing K from π is of utmost importance because flavor tagging (determining the flavor of quarks in inclusive B decays) reduces unwanted backgrounds that distort results.

The active material, or radiator, for the TOP is highly polished fused-silica quartz bars. After photons from the folded Cherenkov ring image arrive at the end of the quartz, they are detected by an array of photodetectors. The signals from these photodetectors are readout by the electronics described in this thesis and the data are sent to the Belle II TRG and DAQ systems.

The photon arrival locations, times and the quantity of charge deposited are all that is stored for each event. It is with just these locations, times and charges, that the TOP is capable of distinguishing kaons from pions (among other species) at a high confidence level [13]. Combined with data from other subdetectors (primarily momentum data from the curved trajectories in the tracking chamber), this leads to a particle hypothesis used throughout physics analyses.

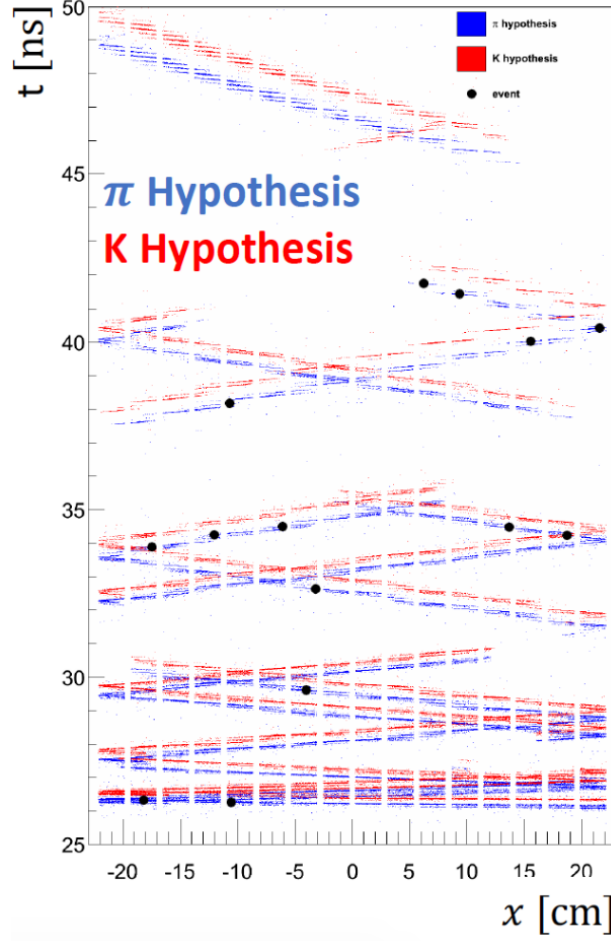


Figure 2.3: Simulation of folded Cherenkov rings unfolding over time (blue is the pion hypothesis and red is the kaon hypothesis; large black dots are from a single event from the simulation; courtesy Belle II TOP group)

2.3 Detector structure

2.3.1 Quartz radiator + mirror + expansion volume

The main active volume for the TOP is a 2.5 m highly polished fused silica quartz bar. These quartz bars have facets that have high perpendicularity/parallelism to each other. Quartz is used because it has $n \approx 1.5$ and is nearly transparent. All of these factors are crucial for the TIR that the TOP requires to propagate the light from Cherenkov light emission in the bulk to the detection plane at the end [13].

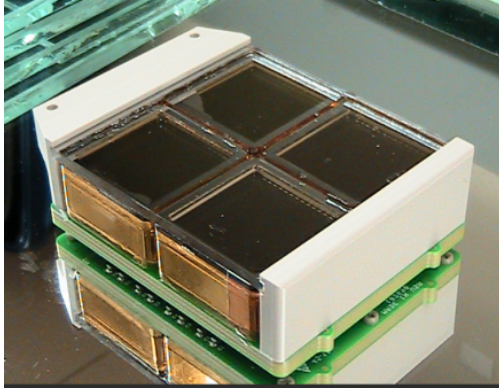
Each quartz bar is comprised of two 1.25 m lengths of quartz, a mirror and an expansion volume that were glued together. The mirror quartz was shaped on one face to be spherical and coated with a reflector. This is placed at the forward end. The expansion volume at the backward end

couples the rest of the quartz bar to the photodetectors.

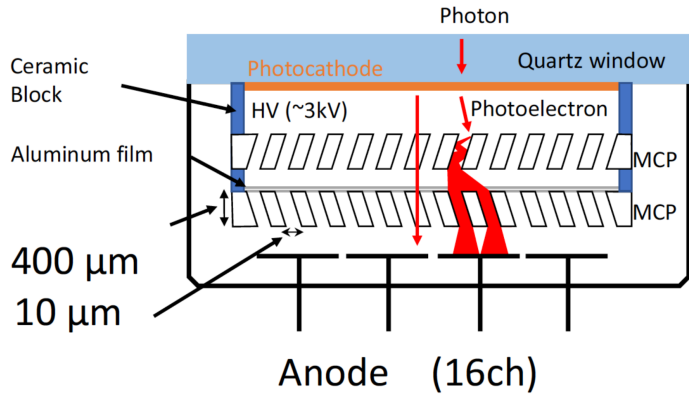
2.3.2 MicroChannel Plate PhotoMultiplier Tubes (MCP-PMTs)

Photodetection uses MicroChannel Plate PhotoMultiplier Tubes. These were developed by Hamamatsu in collaboration with Nagoya University specifically for the TOP in Belle II. They are physically compact, work in a 1.5 T magnetic field and have an extremely good ($\mathcal{O}(35\text{ ps})$) transit time spread (TTS) for individual photons [14]. The TTS is a measure of the timing resolution achievable with a photodetector. Since the quartz bars only produce a handful of photons per event, having a low TTS for each photon is crucial to the feasibility of the TOP concept.

Each MCP-PMT requires several distinct high voltage biases to operate properly in a 1.5 T field. The photocathode requires the highest (negative) voltage, followed by the front and back biases for each of two MCPs (see Fig. 2.4b). The anodes are held near ground potential by resistors on the carrier boards.



(a) Four MCP-PMTs mounted (courtesy Belle II TOP group)



(b) Cross-section diagram of PMT showing two back-to-back MCP plates (courtesy Y. Guan)

Figure 2.4: Hamamatsu MCP-PMT used in the TOP

2.3.3 Quartz Bar Box (QBB)

Each composite quartz bar, 32 PMTs and the readout electronics are housed in a Quartz Bar Box (see Fig. 2.5 for a 3D view of the readout electronics sitting at the end of the QBB, Fig. 4.1 for a 2D view and Fig. 4.2 for a cutaway view).

2.4 Readout electronics for the TOP

The readout electronics for each TOP module are comprised of 512 discrete amplifier circuits, 64 waveform sampling and digitizing ASICs, 20 FPGAs, 8 fiber transceivers and a variety of support

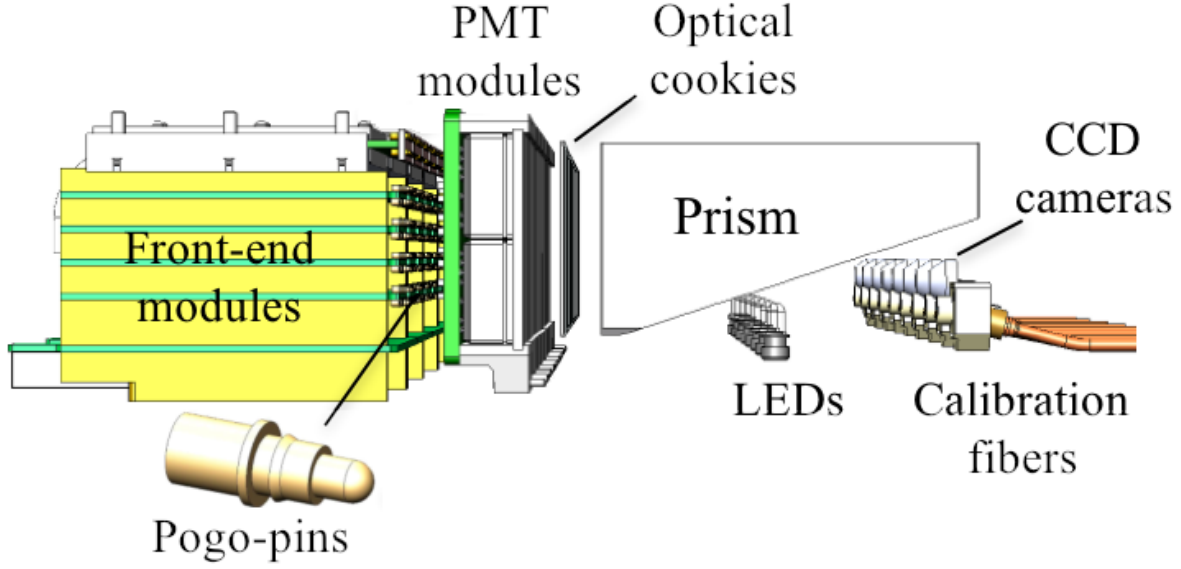


Figure 2.5: The three key technologies in the TOP detector system: readout modules, PMTs and quartz expansion prism (courtesy Belle II TOP group)

electronics. In total, there are 8,192 channels of TOP readout. Each aspect of this readout system is explained in detail in the following chapters.

2.5 Specifications

spec	quantity	notes
number of channels	8192	512 channels for each of 16 quartz bars
timing resolution	$< 100 \text{ ps}$	$\sqrt{PMT_{\text{TTS}}^2 + FTSW_{\text{jitter}}^2 + boardstack_{\sigma}^2}$
deadtime	$< 1 \%$ of the time	for a 30 kHz trigger rate
occupancy	1 %	channels hit in each event
lookback	$5 \mu\text{s}$	Global Decision Logic (GDL) trigger latency
mechanical	112 mm x 110 mm x 80 mm	(per boardstack) must fit in the detector
thermal	$< 80 \text{ W}$	(per boardstack) must not dump heat in the detector

Table 2.1: Specifications for the TOP detector system

CHAPTER 3

TECHNOLOGIES USED IN THE BELLE II READOUT

This chapter contains descriptions of some of the technologies used in Belle II and those upon which the TOP detector system is built.

3.1 Computing elements

3.1.1 COPPER/FINESSE

Developed as an upgrade to the Belle DAQ, the COmmon Pipeline Platform for Electronics Readout (COPPER) is a modified 9U Versa Module Eurocard (VME) motherboard that accepts Front-end Instrumentation Entity for Subdetector Specific Elements (FINESSE) and (Processor PCI Mezzanine Card) PrPMC boards.

3.1.2 Peripheral Component Interconnect (PCI)

Peripheral Component Interconnect (PCI) was developed in the early 1990s to increase the bandwidth available between components inside a Personal Computer (PC). The compact variant, cPCI, was intended for industrial/embedded computing tasks. Both PCI and cPCI transfer data on a parallel bus at $\mathcal{O}(66\text{ MHz})$. Speeds much faster than this were not possible as length-matching all 32 (or 64) data lines of the parallel bus is infeasible.

PCI express (PCIe) is the multi-gigabit serial version of PCI, developed in the early 2000s. In PCIe, multiple serial lanes can be bundled together to increase overall bandwidth between two devices while each serial link retains the ability to self-align with its data, avoiding the synchronization problems of parallel PCI while massively increasing the available bandwidth inside PCs.

3.1.3 PCIe40

In order to handle the steadily increasing luminosity from SuperKEKB, the DAQ group upgraded from the existing COPPER/FINESSE system to PCIe40. The PCIe40 board has 48 fiber-optic links and an FPGA to interface between the front-end electronics and the ReadOut PC (ROPC).

3.2 Electronic components

3.2.1 Field Programmable Gate Arrays (FPGAs)

FPGAs are reconfigurable logic devices that were developed as an alternative to either combining discrete logic on a PCB or designing an Integrated Circuit (IC) for a specific task. They are mainly

used in situations that do not easily lend themselves to running software on a microprocessor or microcontroller.

FPGAs contain several different types of resource that can be connected together in myriad ways to do whatever is required for a particular job. Reconfigurability is crucial in high-energy physics collider-detector experiments as this allows development to continue after the detector is built. This is also the main drawback. When contrasted with operation of a hypothetical system that has fixed capabilities and performance, for a reprogrammable system there is a continual pressure to further develop the firmware.

In many situations, the same FPGA/controller PCBs can be used at the prototype stage as the production stage. The reconfigurability also gives some flexibility when accelerator conditions change or detector components degrade from radiation damage or other factors.

3.2.2 Spartan6 FPGA

Spartan6 is a series of FPGA from Xilinx that was used for the KLM system and the first TOP prototypes. The specific part used is a XC6SLX150T-3FGG676I and it contains: 23,038 Configurable Logic Block (CLB) slices, 180 Digital Signal Processors (DSPs) as well as several multi-gigabit transceivers. Each Spartan6 CLB slice contains 4 Look-Up-Tables (LUTs) and 8 flip-flops.

3.2.3 Zynq FPGA + processors

The Zynq is a System-on-Chip (SoC) from Xilinx that includes FPGA resources but also some processor cores. By using processor cores, some of the development effort could be spent writing C code instead of VHDL or Verilog. The specific parts used for the second generation of TOP development are XC7Z045-2FFG900E (27,325 slices and 900 DSPs) for the Standard Control ReadOut Data (SCROD) revB-series (controller board) and XC7Z030-2FBG484E (9,825 slices and 400 DSPs) for the carrier revE-series (digitizer board). Both parts also contain several multi-gigabit transceivers. Each Zynq slice contains 8 LUTs and 16 flip-flops.

3.2.4 Waveform sampling

A common strategy in high-energy physics experiments is to continuously store an incoming signal in an analog ring-buffer and only make the decision to digitize and readout the data when the trigger system decides it is appropriate. This is the concept of a waveform sampling ASIC (see Fig. 3.1).

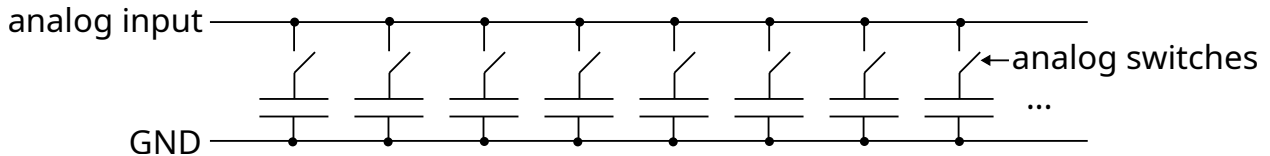


Figure 3.1: Waveform sampling uses a Switched-Capacitor Array (SCA)

The analog ring-buffer is implemented as a Switched-Capacitor Array (SCA) along with a programmable timing generator. The voltage on each capacitor in the SCA is allowed to follow the input signal for a moment and then it is disconnected. An array of these with slightly different delays from the timing generator causes a discretely time sampled waveform to be stored (and continuously overwritten).

This concept of waveform sampling always and digitizing sometimes is useful for two main reasons: It saves power over continuous digitization and readout; It automatically zero-suppresses uninteresting regions in space and time.

3.2.5 Wilkinson Analog-to-Digital Converter (ADC)

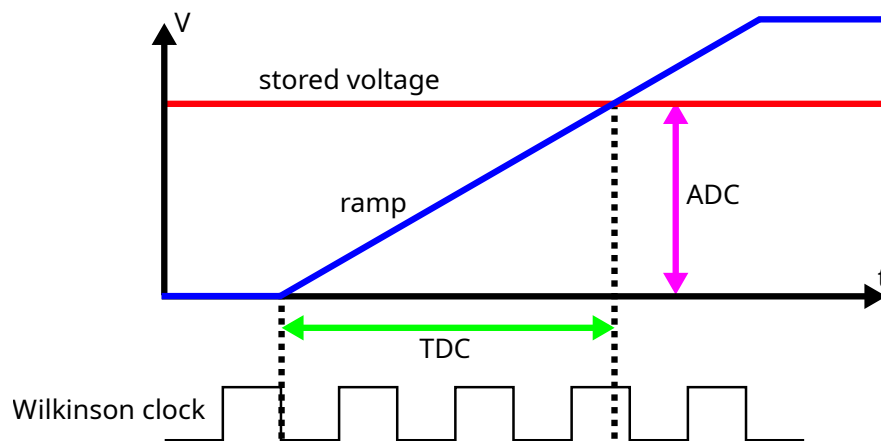


Figure 3.2: Wilkinson ADC uses a TDC and a ramp that is linear in time

A Wilkinson ADC digitizes a voltage stored on a capacitor by using a comparator connected to both the stored voltage of interest (red in Fig. 3.2) and to a ramp voltage (blue in Fig. 3.2). The comparator changing state after the ramp voltage passes the stored voltage stops a counter for each storage cell from continuing to increment, and so ends up measuring a duration. The ramp voltage increases linearly with time because it is connected to a constant current source and the voltage on a capacitor is $v = q/C$, where q is charge (the time integral of current) and C is capacitance. The time interval between the start of the ramp and the firing of the comparator constitutes a Time-to-Digital Converter (TDC) value (green in Fig. 3.2). Because of the linear relationship of v to t for the ramp, the TDC value is proportional to the stored voltage, and so this has the effect of also being an ADC (pink in Fig. 3.2).

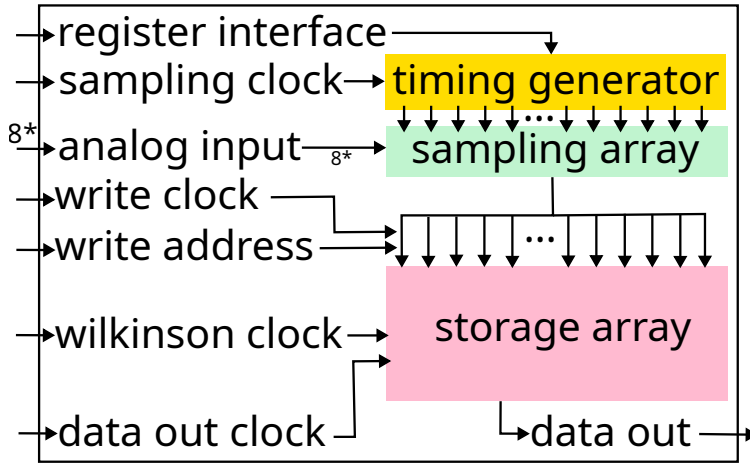
The waveform samplers used in the TOP and KLM contain built-in Wilkinson-style ADCs that can be operated selectively on the analog storage array.

3.2.6 LAB/IRS-series waveform sampler + digitizer

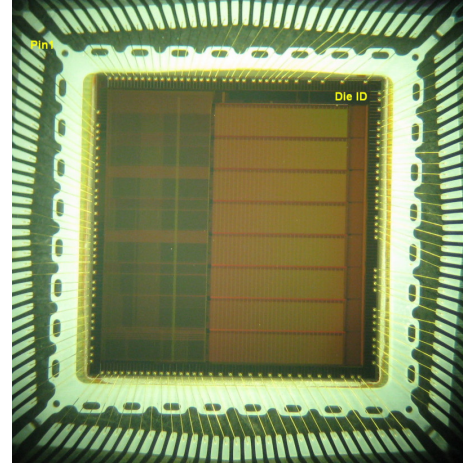
The LABrador (LAB) and Ice Radio Sampler (IRS) series of waveform sampling and digitizing ASICs were initially developed for an Antarctic balloon-borne neutrino / Ultra-High-Energy Cosmic Ray experiment.

This first series of ASICs did not have a built-in programmable timing generator and so performance depended heavily on PCB trace lengths and crosstalk as well as the ability of the FPGA to drive nearly-simultaneous signals with arbitrary (but crucial) relative delays.

3.2.7 IRSX waveform sampler + digitizer



(a) Simplified block diagram of IRSX



(b) Wirebonded IRSX (courtesy TSMC)

Figure 3.3: Block diagram and photograph of IRSX waveform sampling and digitizing ASIC

A timing generator (see Fig. 3.3a) was added to later ASIC revisions to greatly alleviate the burden on the controlling FPGA. Signals generated internal to the ASIC would now dictate precisely when capacitors would sample the incoming signal, when the values stored on the sampling bank of capacitors would be transferred to the storage bank, etc. Adjustment of these could be done in real-time by (re)programming a set of registers within the ASIC (see Fig. A.1 in the appendix).

Each channel of the ASIC also has a comparator, along with a Digital to Analog Converter (DAC) to set the threshold. These “trigger bits” are sent to the controlling FPGA and stored in a digital ring buffer until the Global Decision Logic (GDL) sends a signal to digitize all Regions of Interest (RoI) which in this case means regions where the trigger bits fired. It is in this way that a system with 8,192 channels all sampling at 2.714 GSa/s continuously (for a potential raw data rate of ≈ 33.3 TB/sec) can be made to only send a small $< \mathcal{O}(0.024\%)$ fraction to the DAQ.

CHAPTER 4

FIRST GENERATION OF TOP READOUT

The first generation of the TOP detector system was used as a proof-of-concept in the research and development phase. At this early stage of the project, demonstration of a working prototype was a prerequisite to obtaining funding agency authorization for the construction of the full TOP detector system, including that for polishing the quartz (which was a schedule driver). So it was imperative to read out a prototype quartz bar and successfully reconstruct folded Cherenkov cones from a test beam. This chapter describes the initial versions of the TOP detector system readout electronics.

4.1 Readout for KLM and TOP

Under the guidance of Gary Varner, the Instrumentation Development Lab (IDLAB) at the University of Hawaii was responsible for the readout electronics for the KLM and TOP.

Both subdetectors needed an FPGA to manage configuration and readout of the waveform sampling and digitizing ASICs. We chose the Spartan6 lx150t from Xilinx for both subdetectors because it has multi-gigabit transceivers (a requirement to communicate with the Belle II DAQ) and contains the most configurable logic resources available in the Spartan6 series. Choosing a component with the most resources available was a precautionary move, as none of the firmware had been written yet to talk to the timing, trigger or data acquisition systems of Belle II. Similarly, no firmware had yet been written for the simultaneous control and readout of multiple waveform sampling and digitization ASICs.

4.1.1 Scintillating KLM readout

Each scintillating KLM readout services 150 channels and the ASIC used was in the TARGET-series [11]. The TARGET-series of waveform sampling and digitization ASICs is similar in function to the IRS-series, but has 16 channels (instead of 8), operates at a lower sampling rate, and has a different trigger bit interface. Belle II needs 18,560 channels of scintillating KLM readout, which corresponds to about 1,240 TARGET daughtercards distributed across 136 SCROD + MotherBoard (MB) + Ribbon Header Interface Card (RHIC) assemblies.

In addition to the waveform sampling and digitizing ASIC, each TARGET daughtercard has amplifiers for the signal path and to monitor SiPM leakage current. Each RHIC board has an array of DACs to trim SiPM overvoltages as well as an array of connectors to interface with the incoming signals. The KLM motherboard houses 10 TARGET daughtercards and a SCROD and a RHIC and draws power from a custom 9U VME crate.

4.1.2 TOP readout

The TOP readout needs to read signals from an array of MCP-PMTs coupled to a quartz bar. Each PMT has 16 anodes and the dimensions of the quartz expansion bar fit two rows of 16 PMTs for a total of 512 channels. After some consideration of data volume through each multi-gigabit link and heat load from each additional FPGA, it was decided that each TOP readout would service 128 channels (4 to a quartz bar). The ASIC used was an 8-channel IRS-series, which meant that each TOP boardstack would need to operate 16 ASICs. In order to instrument all 16 quartz bars, Belle II would require 64 TOP boardstacks.

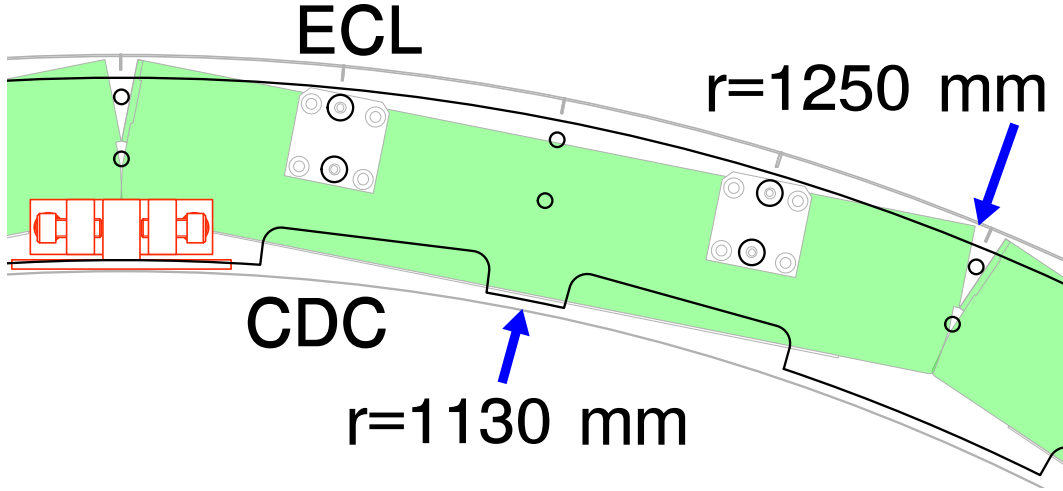


Figure 4.1: A tight fit (radially) for the TOP (in green) between the (new) CDC and the (existing) ECL. The small distance between the TOP and the ECL helps with detection efficiency in the ECL. The larger outer radius of the new CDC for Belle II was necessary to maintain performance compared to the CDC of Belle. (courtesy Belle II group)

The width and height of each boardstack was set by the width of the quartz bar and the available radial space fitting a rectangle between two circles (the inside diameter of the existing ECL and the outside diameter of the planned CDC; see Fig. 4.1). The length of each boardstack was set by the distance between the quartz bar and the backward ECL (see Fig. 4.2).

The 120 mm available space between the CDC and the ECL also includes the QBB which is responsible for keeping the quartz bars from flexing more than $100 \mu\text{m}$ and holding the PMTs tight up against the quartz to avoid losing photons to poor optical coupling.

With these constraints in mind, we set about planning a stack of PCBs that contained 16 ASICs and 1 FPGA, along with the needed amplifiers and voltage regulators and other support electronics.

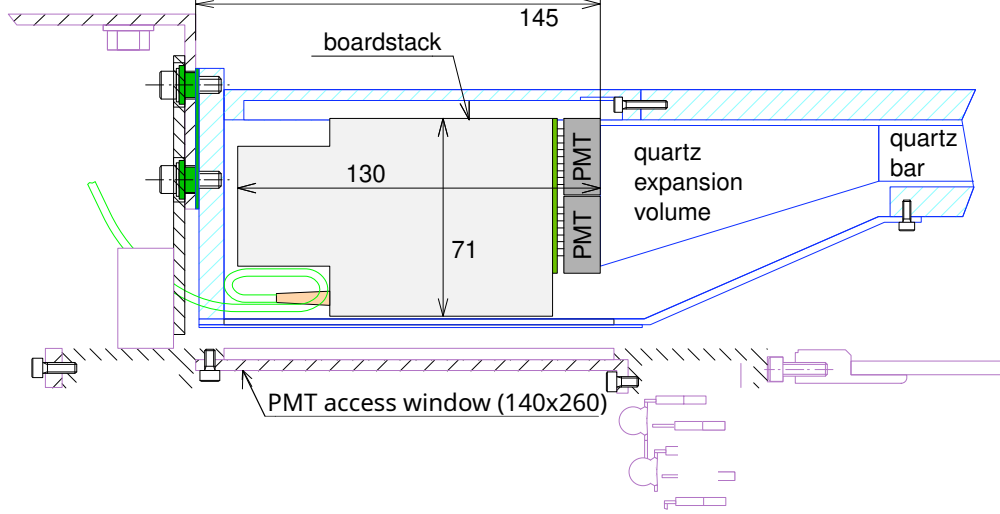


Figure 4.2: Increasing the axial dimension of the readout reduced the length available for quartz (courtesy T. Kohriki; dimensions in mm)

4.2 Standard Control ReadOut Data (SCROD) revA (KLM/TOP)

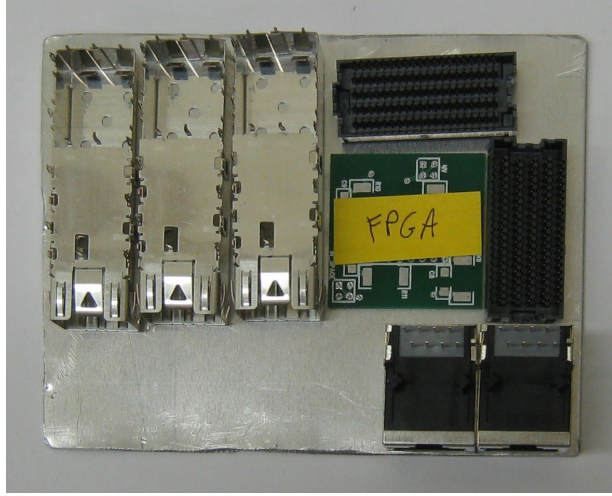
From the pinout of the chosen FPGA and knowledge of the mechanical constraints, we undertook a campaign to design a controller board to be used for the TOP and KLM in Belle II. The tighter mechanical constraint was by far the TOP so we endeavored to make that fit.

Both subdetectors needed at least two multi-gigabit fiber optic uplinks, one to stream raw trigger data to the GDL and another for streaming data to the DAQ system. The Belle II DAQ group designed and commissioned a tree of Front-end Timing SWitch (FTSW) modules that are capable of disseminating a submultiple of the accelerator RF clock, a stream of trigger and run control data as well as programming facilities for each subdetector module via a Joint Test Action Group (JTAG) link. We planned to use Small Form Pluggable (SFP) fiber modules and RJ45 connectors for the timing and JTAG links. This choice, along with the physical size of the FPGA and the number of connections we needed to make to the boards carrying the ASICs, set the rough size of the Standard Control ReadOut Data (SCROD) (see Fig. 4.3 and Fig. 4.4a).

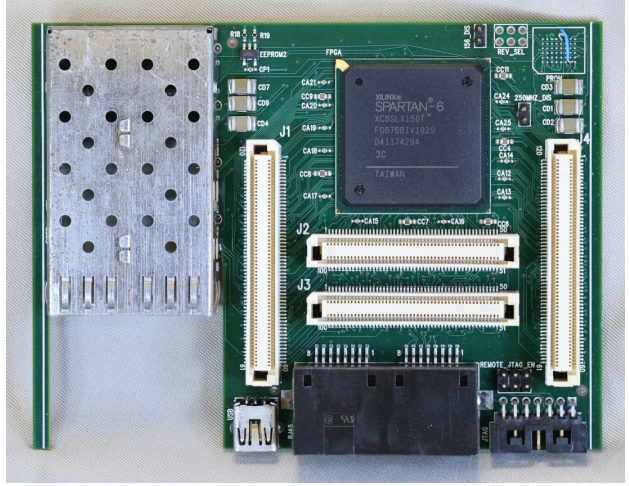
After further developing these ideas, the prototype SCROD was manufactured and assembled and tested successfully on the prototype KLM motherboard.

4.3 TOP carrier boards and daughtercards

The width of the packaged ASICs (TQFP-128A) set the number of ASICs per carrier board at 4, which implied that there would need to be 4 carrier boards stacked up on top of each SCROD to meet the channel density requirement (128 channels per boardstack). In order to accommodate single-ASIC failures, we chose to design a carrier board that had connectors in 4 locations for daugh-



(a) initial mockup of controller board

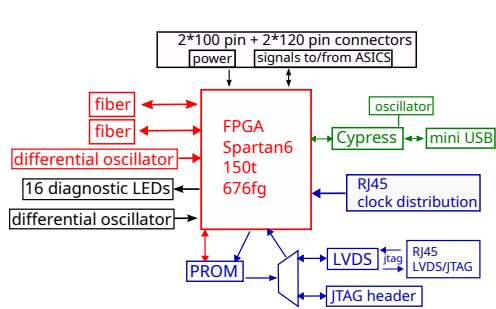


(b) Populated SCROD revA (100 mm x 75 mm)

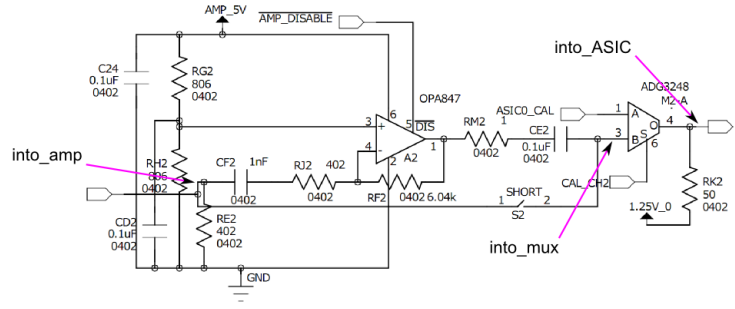
Figure 4.3: Initial development of SCROD revA-series

tercards that would each house a single 8-channel IRS-series ASIC (see Fig. 4.5). With 32 channels per carrier board, we picked a 2 mm rectangular connector and devised an electromechanical scheme to collect signals from a board that would constrain the PMTs.

Each daughtercard had 8 amplifier channels, a bus transceiver and two DACs to control various biases for the ASIC. The first daughtercard versions used a Monolithic Microwave Integrated Circuit (MMIC) amplifier (Broadcom ABA-31563) with 3.5 GHz of bandwidth. This bandwidth did not match the input characteristics of the ASIC, so we placed a lowpass filter in the signal path to attenuate unwanted higher frequency signal content.



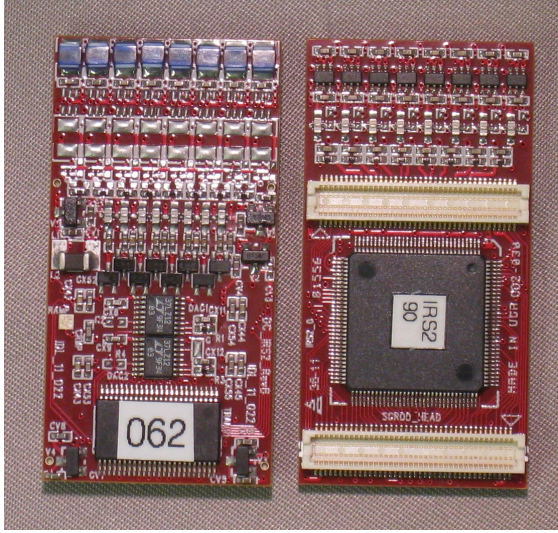
(a) SCROD revA block diagram



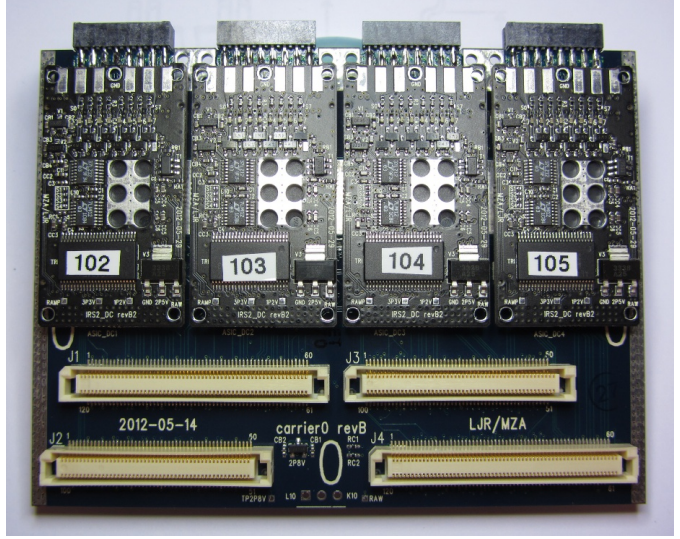
(b) Single-stage amplifier, showing AC coupling, DC biasing and calibration signal multiplexer

Figure 4.4: Planning the first generation of the TOP detector system

The amplifier circuit was developed over the course of several generations of daughtercard and carrier board. The second amplifier circuit (see Fig. 4.4b) used the Texas Instruments (TI) OPA846, which performed well (see Fig. 4.10a).



(a) Daughtercard with one IRS2 ASIC



(b) Carrier board with 4 daughtercards populated

Figure 4.5: The first generation of carrier boards had ASICs on individual daughtercards

4.4 High Voltage (HV), front-front, front-back

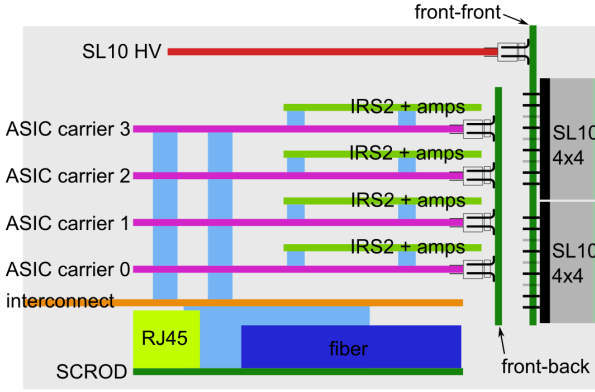
The HV board sits above the SCROD and carriers and provides each PMT with 5 distinct HVs via resistive dividers. Each divider is a passive string of $\mathcal{O}(10\text{ M}\Omega)$ resistors (to roughly match the resistances of the MCPs inside the PMT). To hold the PMTs mechanically, provide the HV biases and read out the signals from the anodes, we designed a sandwich of two boards, called front-front and front-back (see Fig. 4.6 and Fig. 4.7). The front-back was only responsible for routing signals to the carrier boards; no HV was present. The front-front routed HV to the PMTs and anode signals to the front-back.

4.5 Beamtest: Fermilab MTEST

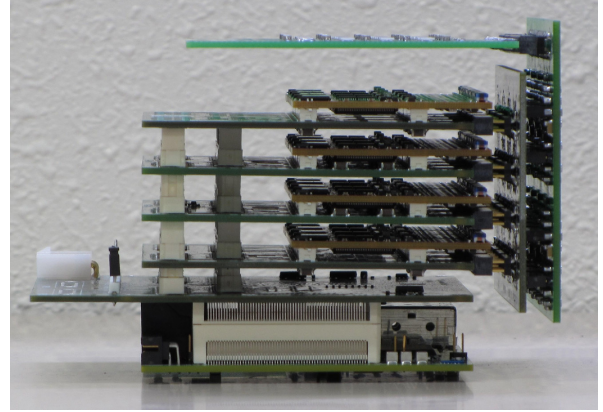
In late 2011, we brought the first prototype of this system to a beam test at Fermilab. The data acquisition system performed well; we were able to see Cherenkov photons in individual channels. Systematic issues in the collected dataset indicated the need for improvements in the ASIC and PCB connections between the FPGA and ASICs.

4.6 Further development

After some introspection, we had another round of board and ASIC designs to consider. First, we abandoned the daughtercard concept and placed the ASICs directly on the carrier boards. We then realized that with a judicious use of crossover wiring, we would require only two distinct carrier



(a) Scale drawing of side-view of boardstack



(b) Boardstack (112 mm x 110 mm x 80 mm)

Figure 4.6: Boardstack used for Fermilab beamtest

designs to serve the 4 carrier locations in the boardstack (see Fig. 4.8). After another Multi-Project Wafer (MPW) run with Taiwan Semiconductor Manufacturing Company (TSMC) and some PCB fabrication and assembly, we had another prototype to test.

4.7 Beamtest: SPring8-LEPS

The result of that development effort was the first successful test of the whole system in mid-2013 (see Fig. 4.9). An analysis of the data from the SPring8-LEPS beamtest [15] showed that the system worked well enough to act as the barrel PID for Belle II. Compare Data (Fig. 4.10a) with Monte Carlo (Fig. 4.10b).

4.8 Post-beamtest

Simultaneous with development of a fully functional TOP readout that performed well at a beamtest, we kept pushing on using more effective concepts.

The idea for two such improvements came from G. Visser. One was the addition of thermal walls to more effectively conductively cool the boardstack (see Fig. 4.12b and Fig. 4.11b). The clamping force can be increased to draw heat away from the electronics and dump it into a cold plate.

Another concept from G. Visser was to use pogo pins to mechanically decouple the PMTs from the readout. This is primarily to allow replacing/upgrading the boardstack without needing to decouple the PMTs from the quartz (see Fig. 4.12b).

We settled on using the TI LMH6629 amplifier which worked best in simulations (when compared to the OPA846 and OPA847).

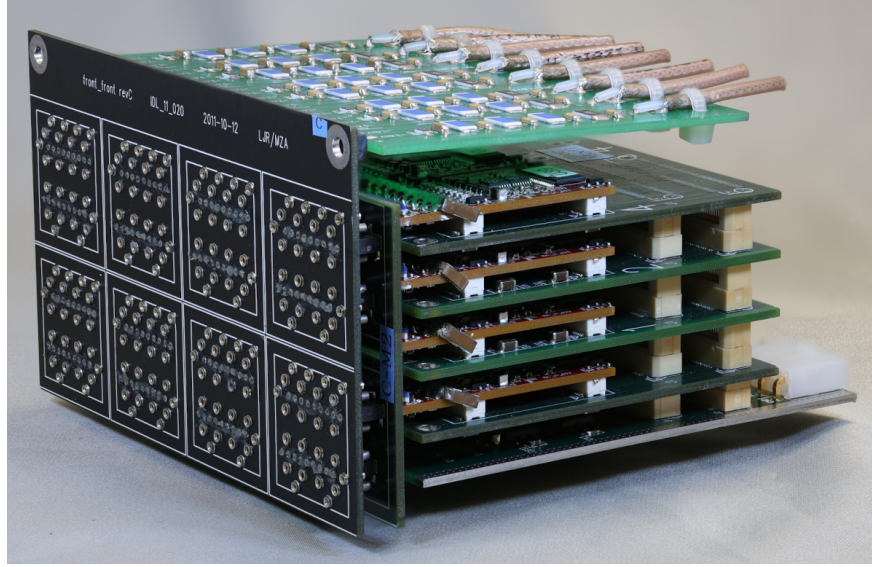
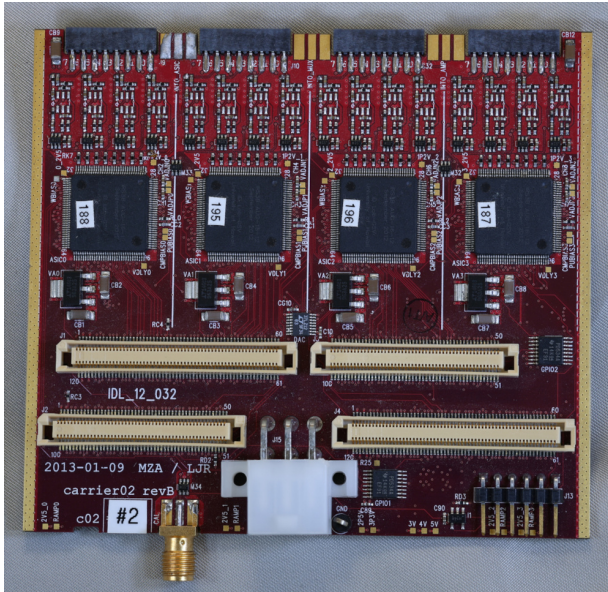


Figure 4.7: Boardstack from the Fermilab beamtest, showing front-front and HV board detail

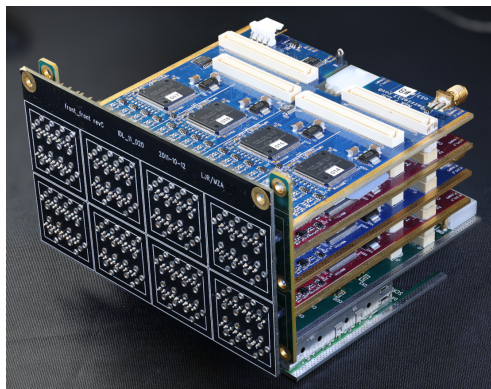


(a) Populated carrier02 revB

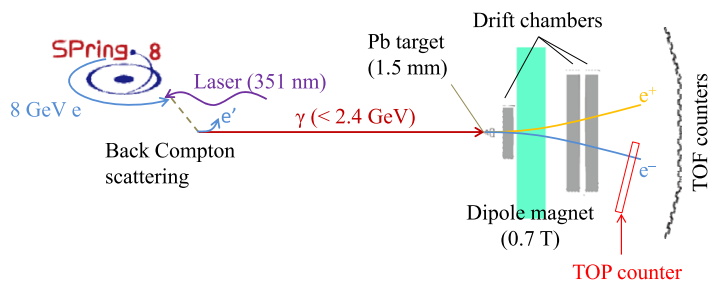


(b) Populated carrier13 revB

Figure 4.8: ASICs placed directly on carrier boards; now just two distinct designs are necessary

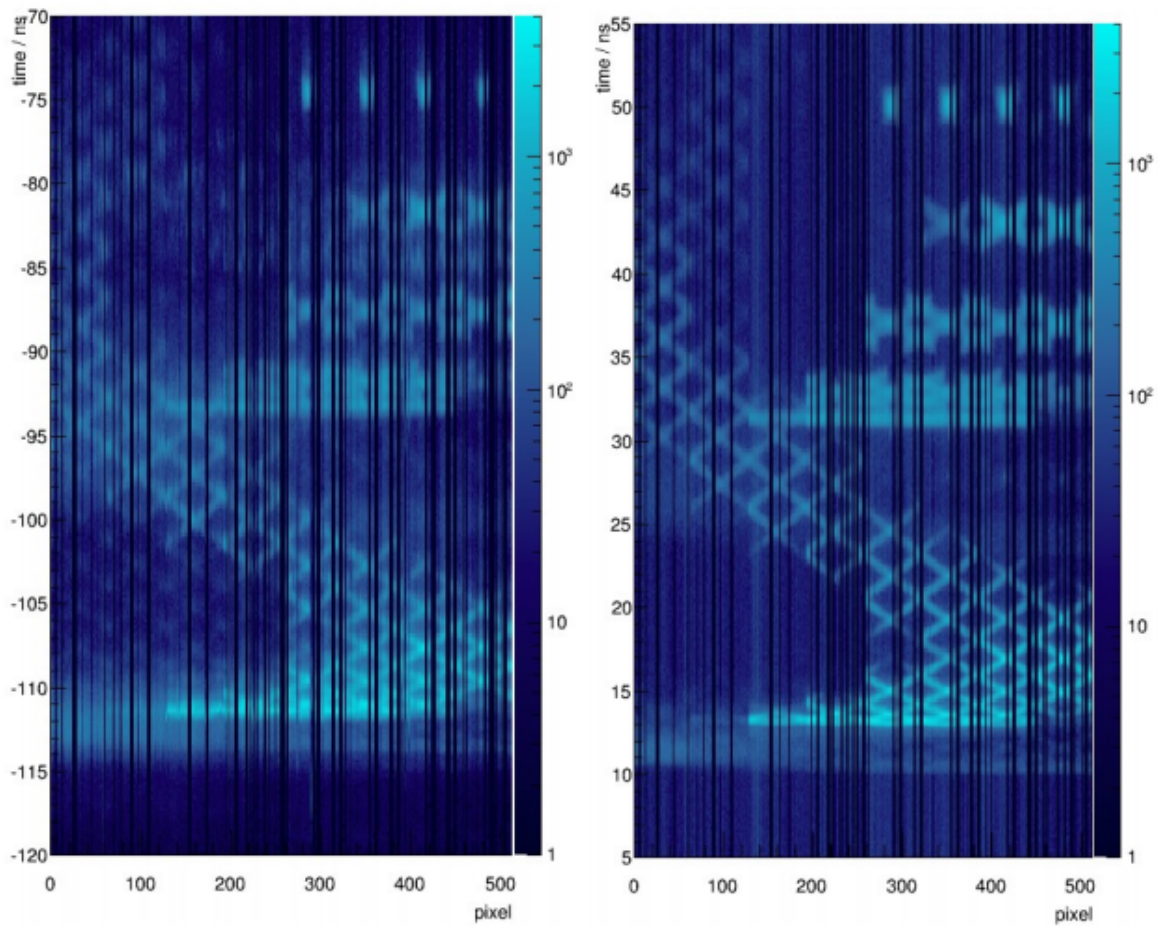


(a) Updated boardstack



(b) Beamtest setup (courtesy K. Matsuoka)

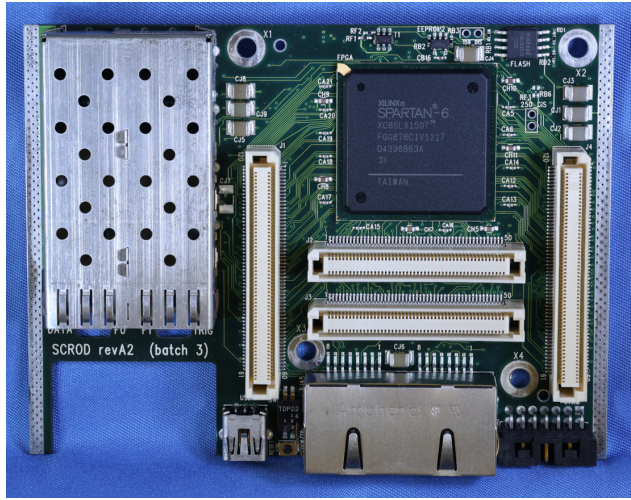
Figure 4.9: SPring8-LEPS beamtest



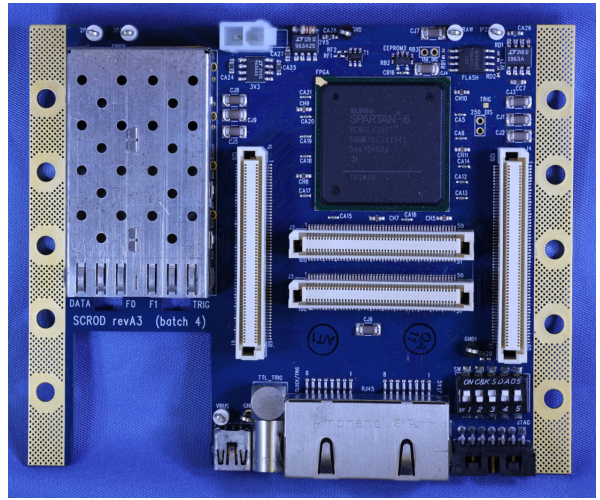
(a) Data

(b) Simulation

Figure 4.10: Folded Cherenkov images for beam incidence perpendicular to quartz bar from SPring8/LEPS beamtest (vertical bands are from inactive channels). The pattern unfurls over time (courtesy M. Barrett).

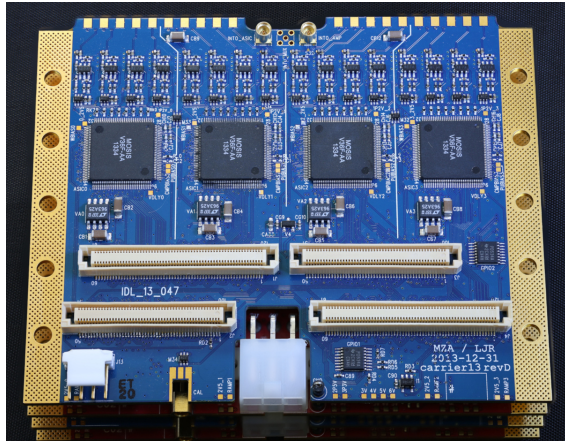


(a) Populated SCROD revA2

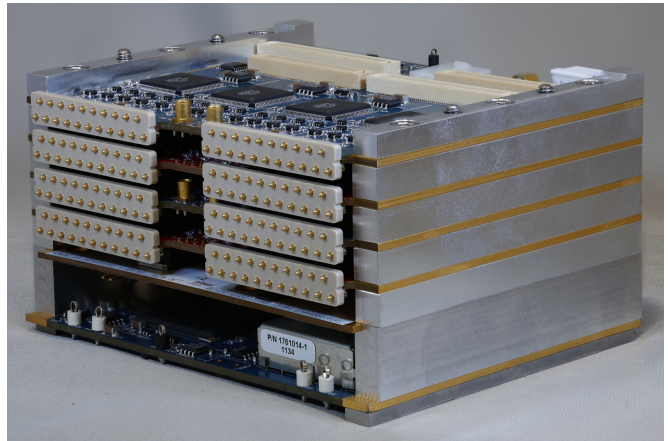


(b) Populated SCROD revA3, showing thermal wall (110 mm x 90 mm)

Figure 4.11: Further Development of SCROD revA-series



(a) Pogo pin pads at top and thermal wall concept on left and right



(b) Assembled into a module with conduction cooling and pogo pins installed

Figure 4.12: Last revision of the first generation

CHAPTER 5

SECOND GENERATION OF TOP READOUT

After the SPring8-LEPS beamtest where we showed our electronics could distinguish particle species by difference in opening angle of Cherenkov light, we set out to finalize the design for the production run to be integrated into Belle II. One of the needed improvements was to reduce the burden on the single FPGA controlling the boardstack.

This chapter describes the development of the second generation of the TOP detector system readout electronics, which were used in Belle II.

5.1 Readout for TOP detector system

Because we found that the TOP firmware was nearly impossible to fit in a single Spartan6, we decided to bifurcate the design paths for the TOP and KLM. The KLM would retain the Spartan6 part and the TOP would adopt a newer part from the Zynq series.

The Zynq series has the familiar Programmable Logic (PL) from an FPGA but additionally adds a Processing System (PS). The PS is a pair of Acorn RISC Machines (ARM) cores that can run embedded software, complementing the abilities of PL where appropriate. The second generation of the TOP consists of a set of five Zynq parts spread across five PCBs (see Fig. 5.1a). Partly, this is to separate distinct functionality and partly to reduce localized heat load.

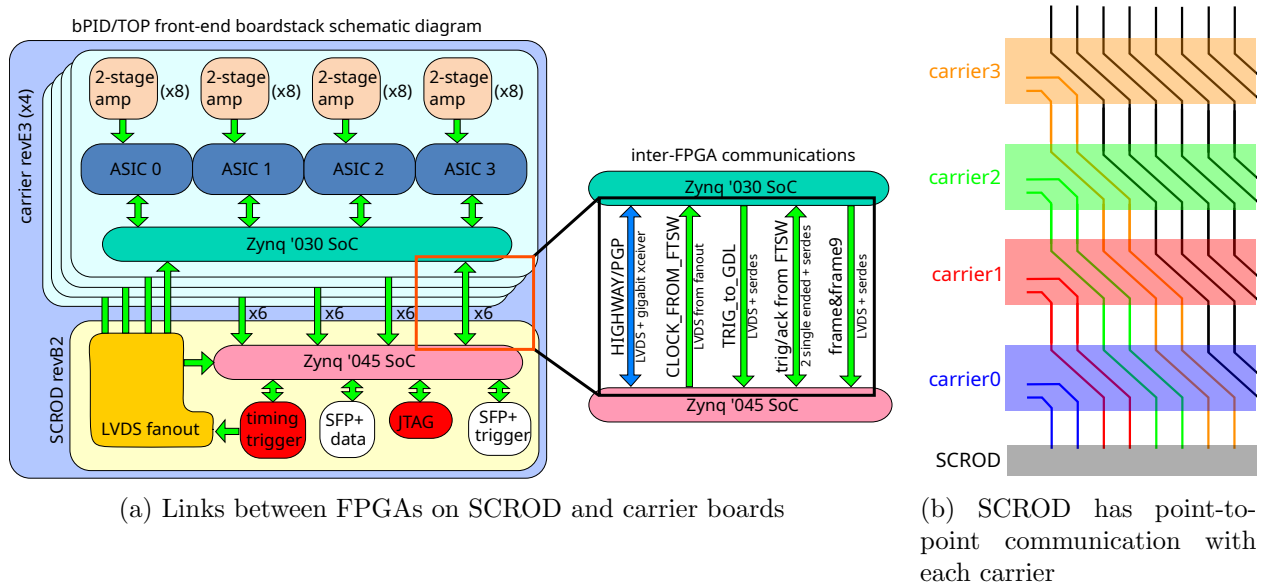


Figure 5.1: Planning the second generation of the TOP detector system

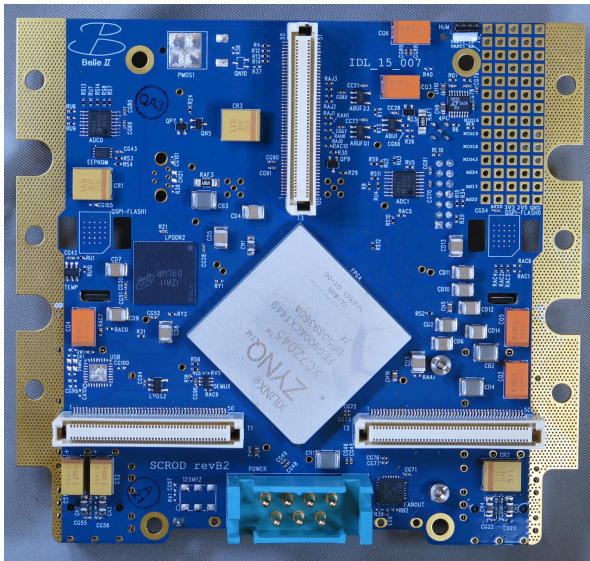
5.2 Standard Control ReadOut Data (SCROD) revB-series

As the main controller of each boardstack, SCROD has several tasks. The first is sending raw trigger information upstream to the trigger decision logic, as well as receiving a trigger decision and acting on it. The second task is consolidation, feature-extraction and streaming out of data [16]. The remaining tasks are handing off configuration register values to the carrier boards and collecting data to monitor the operating conditions for each boardstack.

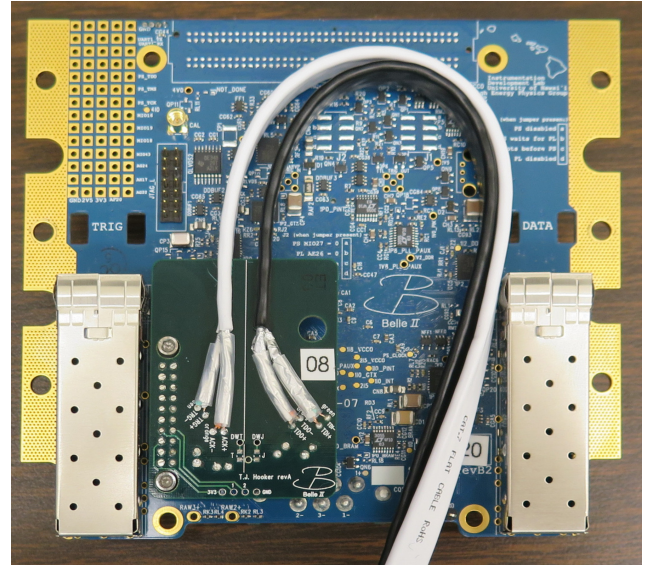
5.2.1 SCROD revB

To avoid wasting power unnecessarily, the boardstack accepts 3 distinct raw voltages. Each is tuned to be only slightly above the dropout of the Low Dropout Regulators (LDOs) for each voltage required on the board (see Tab. 5.1 for details).

To limit the inrush current, we employ a cascade of LDOs where the power good signal for the n^{th} regulator drives the enable of the $(n + 1)^{th}$ regulator. The goal of limiting the inrush current is multifold: (1) It puts less of a strain on the power supply system; (2) It suppresses some ElectroMagnetic Compatibility (EMC) issues; (3) And it avoids transient currents dropping so much voltage that regulators would no longer be regulating properly, leading to potential glitches in state machines and registers.



(a) Top



(b) Bottom with attached Timing and JTAG (TJ) assembly

Figure 5.2: Populated SCROD revB2

In order to assure that the distributed RF clock submultiple arrives at the same time for each carrier, we use trace length matching on SCROD.

The calibration distribution circuit takes a signal from the CAL input on SCROD, AC-couples it, then buffers it and delivers it to all 16 ASICs on the boardstack (see Fig. C.9 in the appendix).

SCROD revB worked well as a proof-of-concept for using a Zynq in the second generation of TOP readout. The difficulty of connecting power and timing/JTAG needed to be addressed, as well as a some multi-gigabit transceiver clocking issues.

5.2.2 SCROD revB2

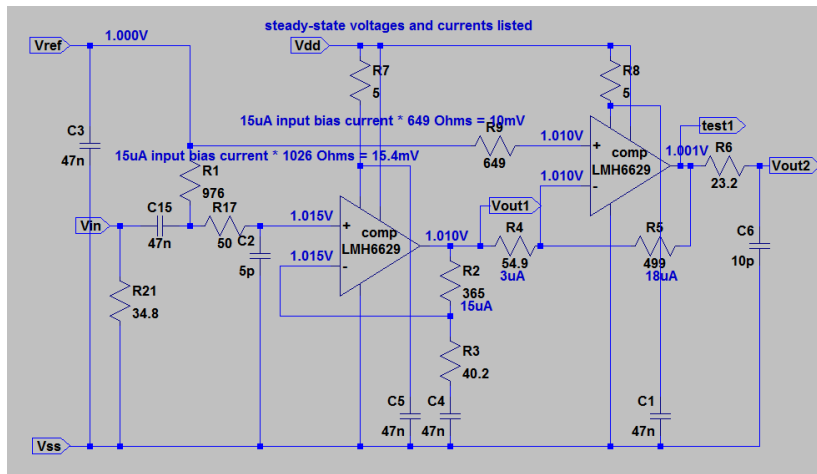
The major change from SCROD revB to SCROD revB2 is the addition of a power connector (see Fig. 5.2a) and a connectorized link to the timing/trigger system (see Fig. 5.2b).

5.3 Carrier revE-series

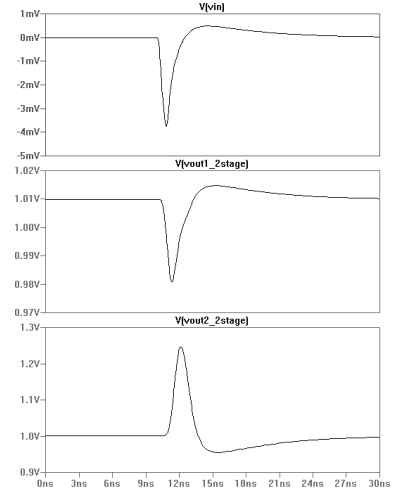
The carrier board is responsible for real-time control of waveform sampling and digitization, output trigger data pass-through to SCROD, dissemination of input trigger from the GDL to all ASICs, zero-suppression of data as well as housekeeping control and monitoring tasks.

5.3.1 Carrier revE

Compared to the carriers of the first generation of TOP boardstack, this generation also includes an FPGA on each board (see Fig. 5.4). With a slight extension of the first generation's crossover wiring, the second generation boardstack was able to use a single board *design* for all 4 carriers in the boardstack (see Fig. 5.1b and Fig. D.4 in the appendix).



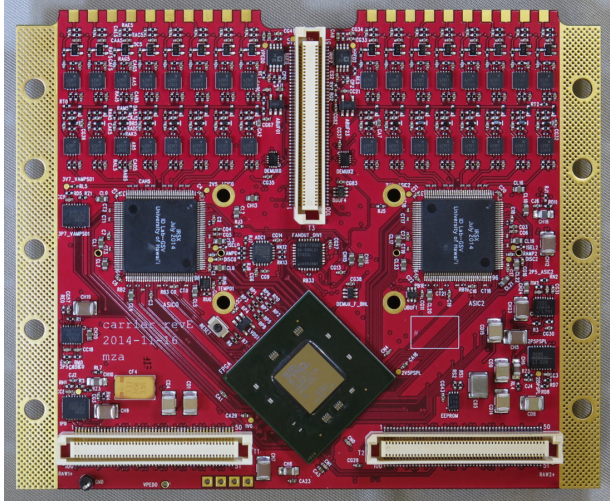
(a) Schematic of two-stage amplifier



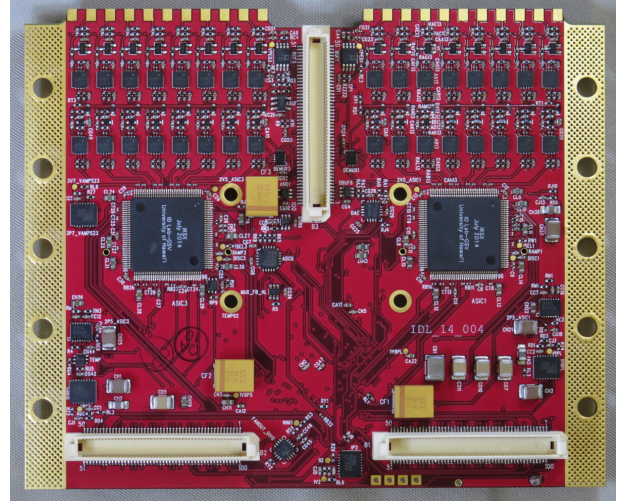
(b) Simulation result showing gain

Figure 5.3: Amplifier circuit used on carrier revE

The second generation of carrier board kept the discrete operational amplifier choice (LMH6629), but used a two stage configuration (one stage non-inverting and another stage inverting; see Fig. 5.3) and changed packages to one that allowed for lower unwanted parasitic capacitance.



(a) Top

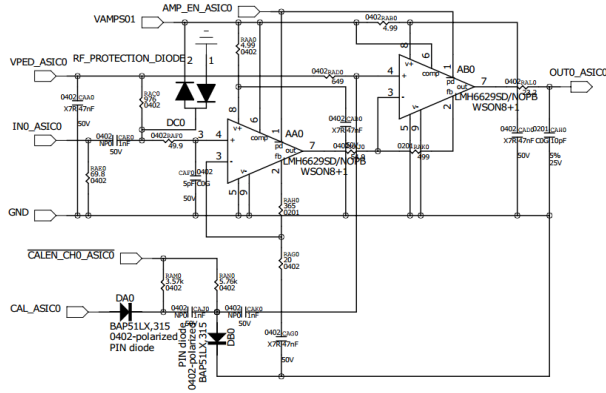


(b) Bottom

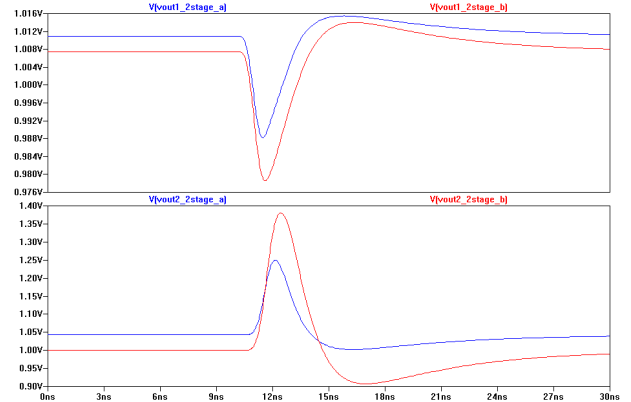
Figure 5.4: Populated carrier revE, showing two-stage amplifier

5.3.2 Carrier revE2

The major change between carrier revE and carrier revE2 is the amplification factor for the two-stage amp (see Fig. 5.5). This was deemed necessary as the estimation of the arrival time of the photon has a smaller error bar when the slope of the PMT pulse is steeper.



(a) Amplifier circuit used on production carrier boards



(b) Increase in gain from carrier revE (blue) to revE2 (red)

Figure 5.5: Production carrier board amplifier circuit

5.4 Ancillary boards

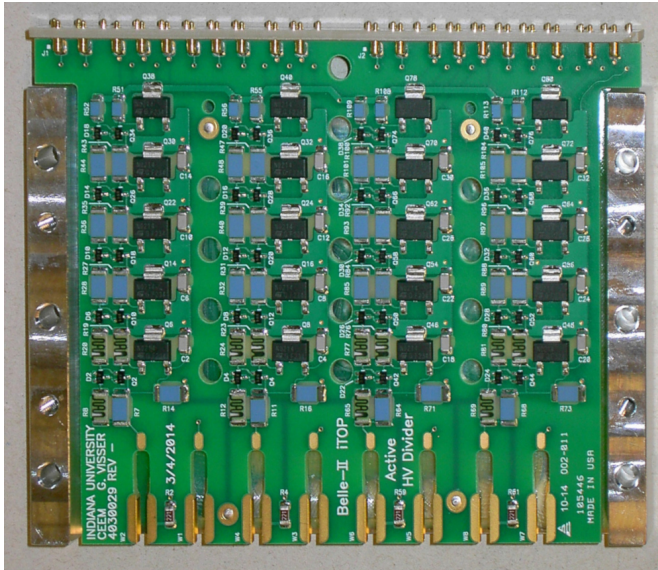
5.4.1 High Voltage (HV) board

The updated HV board (developed by G. Visser; see Fig. 5.6a) has the same function as the one from the first generation boardstack; namely to divide 8 High Voltage feeds for the 8 PMTs in each boardstack into individual biases for the photocathode and two sides of each of two MCP structures inside the PMT.

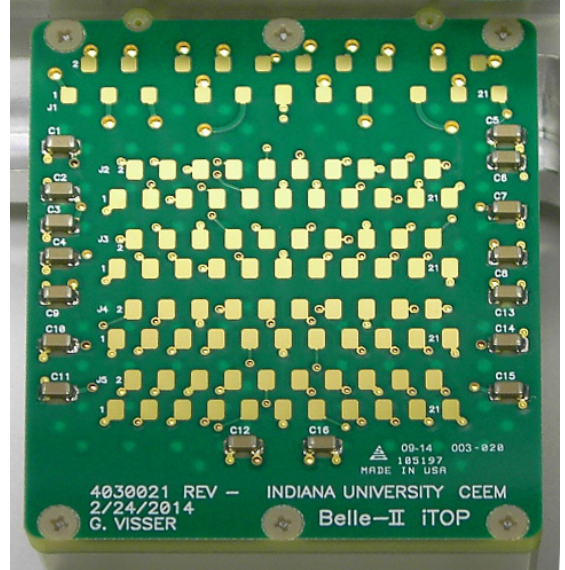
In this generation, the divider is instead a string of $\mathcal{O}(100\text{ M}\Omega)$ resistors that bias HV transistors so that the output impedances remain comparable to the MCP resistances. This has the effect of wasting much less power. The connection is now made with pogo pins on the HV board and Electroless Nickel Immersion Gold (ENIG) pads on the front board (see next subsection).

5.4.2 Front board

The new front board (developed by G. Visser) combines the functionality of the front-front and front-back from the first generation of boardstack, namely to mechanically hold the PMTs in place, deliver HV biases to the PMTs and collect and distribute anode signals to the carrier boards. The anode signals are now delivered to the carrier boards via pogo pins on the carrier boards and pogo landing pads on the front board (see Fig. 5.6b).



(a) HV board



(b) Front board

Figure 5.6: HV and front boards (courtesy G. Visser)

5.4.3 Bicentennial board

The cable length between the LV power supply in the E-Hut and each boardstack is $\mathcal{O}(40\text{ m})$. Wire cross-sectional area, length and current draw are listed in Tab. 5.1.

name	V	function	$length_{max}$	area	I_{max}	IR_{max}
RAW1	1.715 V	FPGA/LPDDR2	36.7 m	6.7 mm ² (10 AWG)	10.9 A	2.6 V
RAW2	3.049 V	ASIC	36.7 m	6.7 mm ² (10 AWG)	13.6 A	3.2 V
RAW3	4.374 V	amplifiers/CAL	36.7 m	2.7 mm ² (14 AWG)	4.4 A	2.7 V

Table 5.1: RAW voltages delivered to each boardstack for LV power

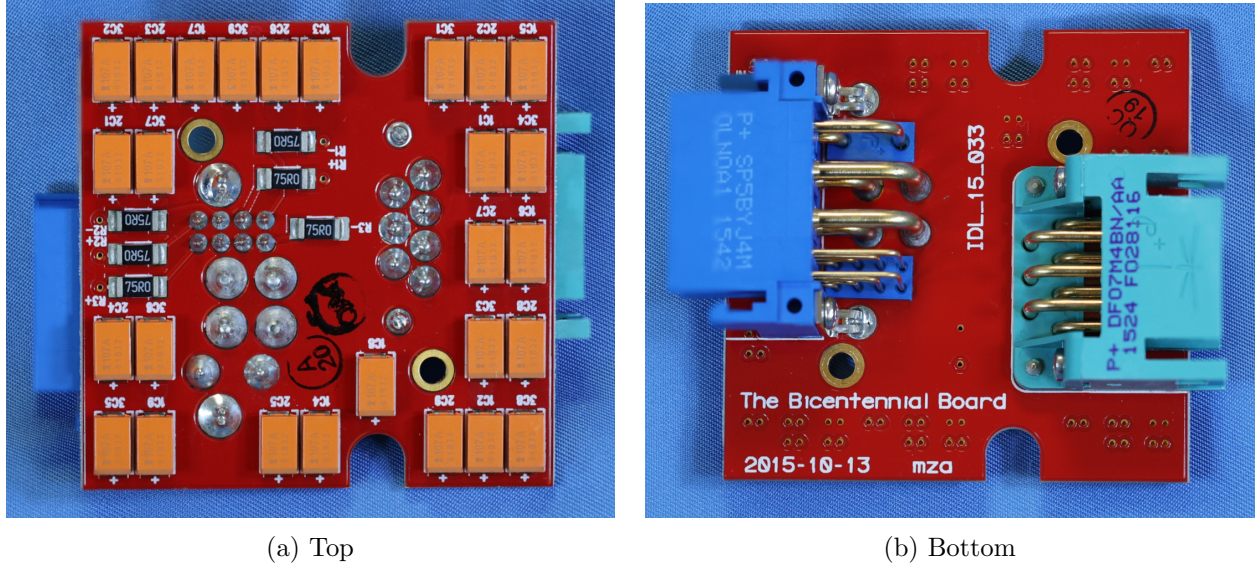


Figure 5.7: Populated bicentennial board

The LV power supply was chosen partly because it has a Kelvin sense feature whereby the power supply regulates on the remotely sensed voltage rather than the voltage measured at the power supply output terminals. This is crucial because the IR drops are comparable with the voltage input needed on the boardstack (roughly half the power is lost in the cables; see Tab. 5.1). To this end, we developed a PCB called the bicentennial board that made this sense connection at the end of the long cables. The voltage drop on the remaining 1.2 m cable between this board and the boardstack is considered manageable. The bicentennial board also provided bulk capacitance on the 3 RAW voltages to help with transient loads (see Fig. 5.7a).

5.5 Mechanical and thermal

Simple conservation of energy (or its time derivative) dictates that the power delivered to the readout electronics is all dissipated as heat and must be removed so the boardstacks are not subject

to thermal runaway. C. Ketter developed the heatsink / thermal wall combination in response to the high power draw of the ASICs, amplifiers and FPGAs. That, combined with the fact that there is no net airflow in Belle II, means that conduction cooling is the only option for heat removal (see Fig. 5.8).

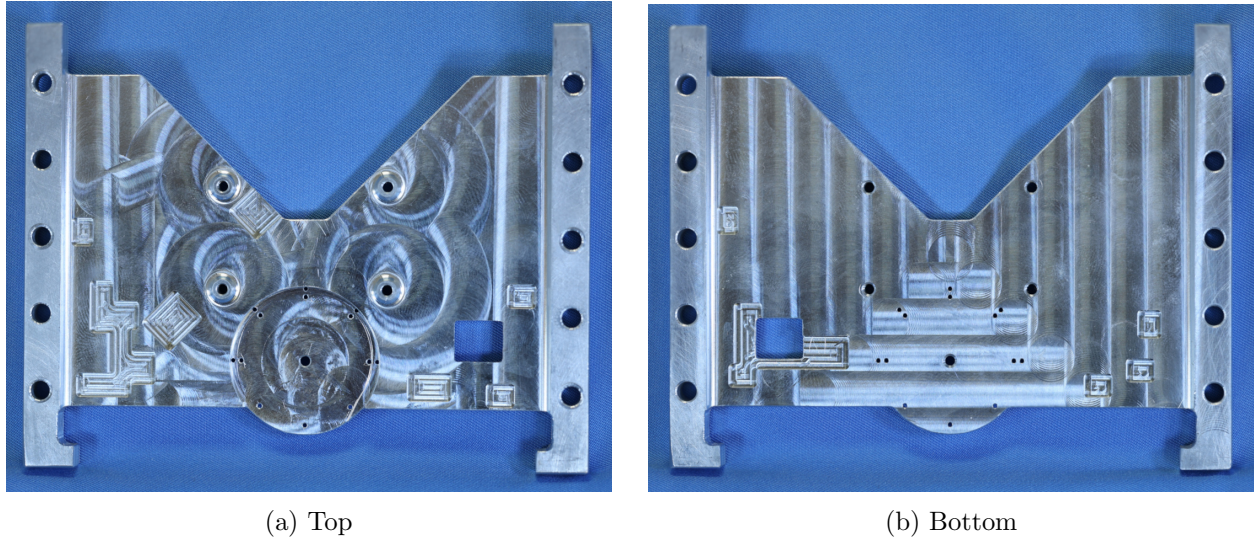


Figure 5.8: Heatsinks for conduction cooling of carrier board (courtesy C. Ketter)

Each QBB has a “cold plate” that couples to all 4 boardstacks and has a cooling channel through which chilled water is forced. Chilled water is circulated through all 4 quadrants separately and comes from a two-phase refrigeration system above the Electronics Hut (E-Hut).

5.6 Installed version of boardstack

The final revision of the TOP readout takes up almost the entire available space (110 mm x 102 mm x 72 mm) inside the QBB (see Fig. 5.9) [17].

5.7 Testing

5.7.1 Individual boards

Before being considered complete, the FPGA on each SCROD and carrier needed to be well coupled to its heatsink. Thermal gap filler was applied between each FPGA and the heatsink/thermal wall combo (see inspection holes in the circular recess of Fig. 5.8a).

Individual carrier and SCROD assemblies were tested at collaborating universities in Pittsburgh and South Carolina.

5.7.2 Boardstack assembly

Final boardstack assembly and testing was performed at the University of Hawaii. Thermal paste was applied between each PCB and thermal wall to improve thermal conductivity of the conduction cooling scheme.

5.7.3 Laser scan

Since the CAL input is only able to test the second stage of amplification and the waveform sampling and digitization ASICs, we needed an additional step to ensure the boardstacks were fully functional. To this end, we developed an XY stage that delivered pulses from a picosecond laser into any desired anode of 8 PMTs connected to a boardstack. We developed software to steer the laser pulses to successive anodes so the entire boardstack could be easily checked for dead/hot channels. Because of the pogo pin scheme, we were able to leave the PMTs in place and swap boardstacks quickly.

5.8 Integration into Quartz Bar Boxes (QBBs)

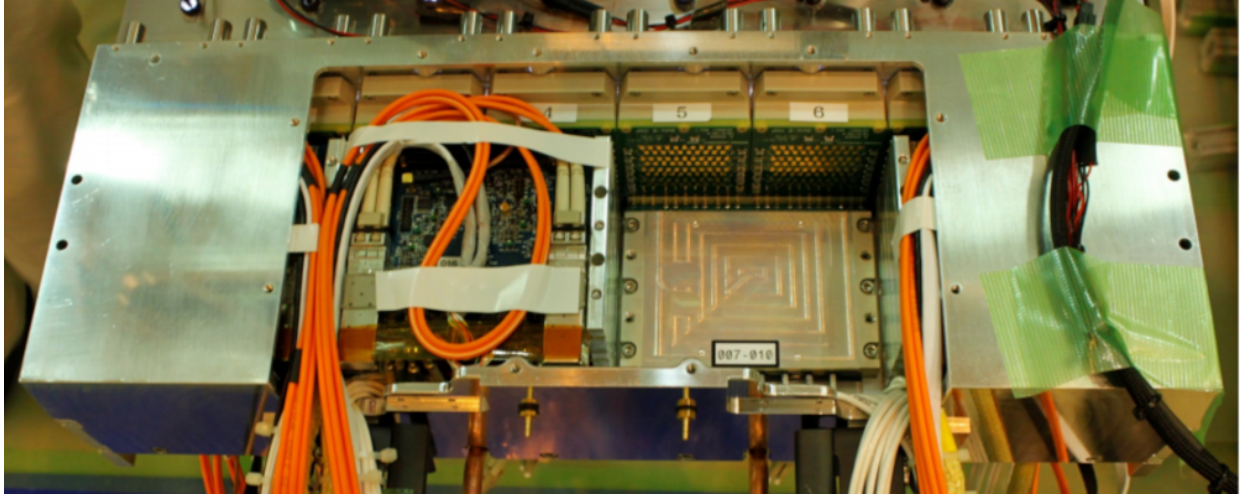


Figure 5.9: 3 of 4 boardstacks installed in the QBB of a TOP module (courtesy Belle II TOP group)

The boardstacks were delivered to KEK in batches of 4 (corresponding to 1 QBB) as they were completed and passed all the tests. A cleanroom at Fuji Hall (opposite side of the accelerator ring from Tsukuba Hall where the interaction region is) was set up to glue quartz bars together and perform metrology on them. While still in the cleanroom, the PMT modules were attached and later boardstacks were installed (see Fig. 5.9). After completion, strongbacks were added to the finished QBBs to prevent flex or damage, which were then moved to Tsukuba Hall where they

were operated for $\mathcal{O}(\text{month})$ collecting data from cosmic ray muons as a last functional test before installation.

5.9 Installation in Belle II

A crane lifted the QBB+strongback combinations up to a platform where a cantilevered installation jig was used to position each TOP module in the detector. After installation, datasets were collected from a large number of cosmic ray muons passing through the bars. With these datasets, the precise location and alignment of each bar was determined and is used during subsequent analyses.

CHAPTER 6

FIRMWARE, SOFTWARE, ETC

6.1 Firmware

The Programmable Logic (PL) of the FPGAs is reconfigurable and the hardware description is written in Very High-speed integrated circuit Hardware Description Language (VHDL) and Verilog.

6.1.1 First generation

Through the onboard multi-gigabit transceivers, the first generation of boardstack used the open-source Aurora protocol to transmit data from the Spartan6 on SCROD to the Spartan6 on a DSP_cPCI board, which was installed in a readout PC (cPCI crate).

Register reads/writes were handled with a custom built command interpreter within the firmware (initially VHDL but later a soft-core (PicoBlaze) microprocessor implemented within the FPGA).

The early IRS-series waveform sampling and digitization ASICs were tested on various incarnations of the TOP boardstack. Feedback from these campaigns informed each next ASIC revision. In total, there were about a dozen ASIC revisions that ultimately led to the IRSX used in the TOP detector system.

Firmware to control a bevy of waveform sampling and digitizing ASICs must perform a variety of tasks. Two sampling clocks must be distributed to all 16 ASICs and these clocks determines precisely when the analog switches are open and closed to the incoming PMT signals. Those samples must then be transferred to deep storage within the ASIC which requires a set of row/column address pins and strobes be asserted in concert. After a trigger decision is made, a region of the deep analog memory in the ASIC must be selected by the FPGA with row/column address pins. Once that is done, a ramp signal must be asserted to initiate a linear voltage ramp via accumulation of charge in the Wilkinson capacitor (external to the ASIC) simultaneous with an Wilkinson clock that increments an internal 12 bit counter that feeds a corresponding counter register for each analog storage cell. Finally, data must be collected by asserting a sample address and capturing the 12-bit data from the ASIC and then incrementing through all the sample address until the whole digitized waveform is transferred to the FPGA.

6.1.2 Second generation

The second generation of boardstack used the multi-gigabit transceivers with the gigabit Ethernet protocol to transmit data from SCROD to a readout PC (via a media converter or PCIe SFP board).

After development had stabilized, the transition was made to use the Belle2Link (B2L) protocol to transmit data to the Virtex5 on a High Speed Link Board (HSLB) which was connected to a readout PC (via FINESSE/COPPER and a PrPMC CPU).

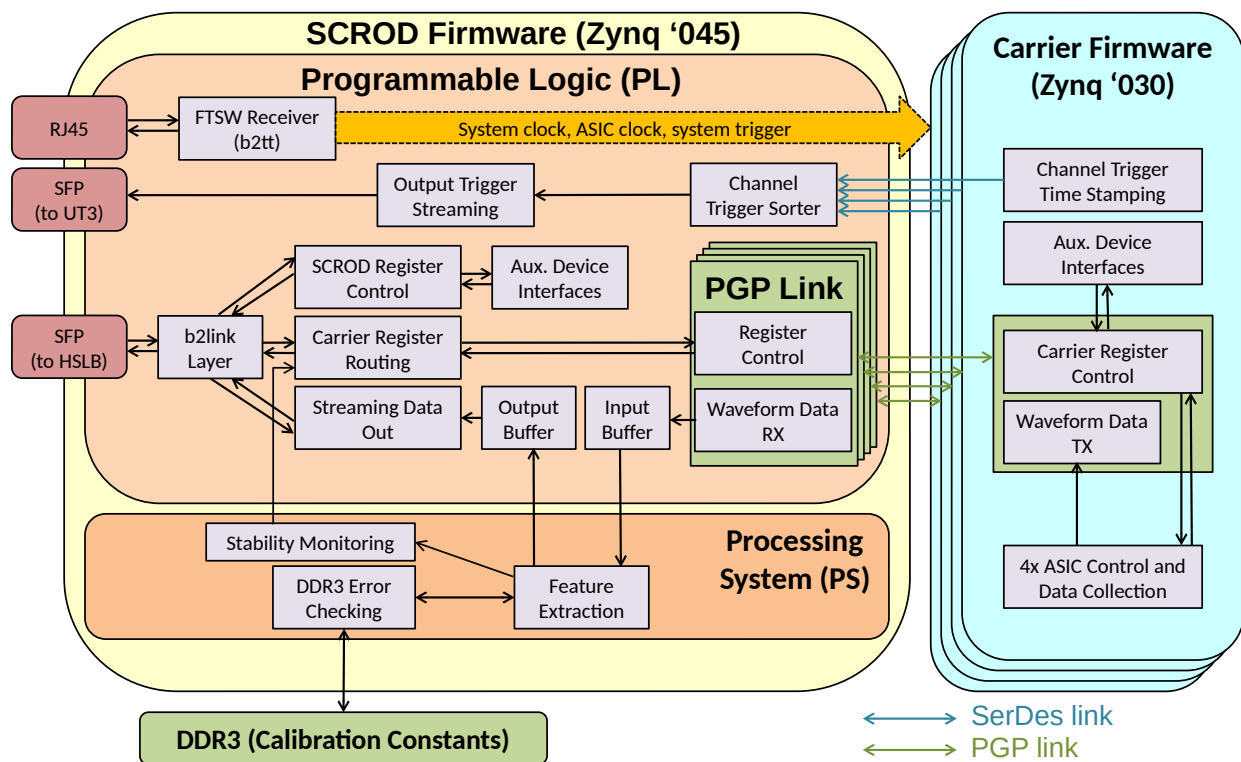


Figure 6.1: Firmware block diagram for second generation (courtesy K. Nishimura)

The 5 Zynq components on the 5 PCBs talk to each other over a custom protocol built on top of multi-gigabit transceivers (see Fig. 6.1).

The production ASIC (IRSX) avoided many of the issues with the first generation of TOP readout because much of the functionality of choosing the precise timing of analog sampling (opening and closing) and selecting rows/columns and sample addresses was now internal to the ASIC or available to be set over a high-speed serial link. Now all that is needed is a (slow) serial interface for configuration register writes, and a handful of differential pairs: A *single* sampling clock (a submultiple of the accelerator clock); A write clock (for transfer to storage array); A Wilkinson clock (dictates the TDC least count); And system-synchronous data output (with associated clock).

6.2 Embedded software

6.2.1 First generation

The embedded software of the first generation was the picoblaze command interpreter. It was programmed in assembly language and accepted simple read (and write) commands from (and to) a bank of registers.

6.2.2 Second generation

The embedded ARM processors PS of the Zynq have a high-speed link to the PL, so raw waveform data from the ASICs is transferred from PL to PS, where it is processed and then sent back to the PL for packaging and transmission. The processing includes pedestal subtraction, pulse finding, hit time estimation and deposited charge estimation.

The other task for the PS is monitoring voltages, currents, temperatures and humidity.

6.3 Readout software

6.3.1 First generation

DSP_cPCI: The C readout software for the first generation boardstack prototype was written in tandem with the customization of the Aurora firmware. This readout software interfaced with a linux kernel driver developed in concert with the firmware on the DSP_cPCI board. This is the version that was used at the Fermilab beamtest in 2011.

DSP_FIN: A second version of the readout software was written in Python which interfaced with the DSP_FIN board installed as a FINESSE board on a COPPER motherboard controlled by a PrPMC CPU. This version was used at the SPring8-LEPS beamtest in 2013.

6.3.2 Second generation

gigE: The readout software for the prototypes of the second generation was done with a C++ gui provided by a collaborating group at SLAC. This version was used 2014-2015.

HSLB: After boardstack mass production and testing were done, we switched to using Belle2Link. Readout control software was written in Python and called a small C executable that actually exchanged data with the HSLB. That version was used during commissioning and operation of Belle II from 2016 to 2021.

PCIe40: The current version of the TOP is connected to a PCIe40 backend, and the readout software is based on the HSLB version and now includes a gui.

6.4 Storage and analysis

6.4.1 First generation

For the Fermilab beamtest, we archived the data from the cPCI crate on other PCs (via Ethernet) and sent copies to analysis farms at Nagoya and Hawaii.

The SPring8-LEPS beamtest used a similar strategy. The readout PC (DSP_FIN / COPPER / PrPMC) was connected to an Ethernet network with some other PCs capable of storing all the data where it was analyzed (see Fig. 4.10a).

6.4.2 Second generation

Because Ethernet is available on most computers (unlike cPCI or FINESSE), the initial readout and analysis for the second generation of TOP boardstack was done with each developer's PC. This parallelized development, which had the effect of shortening the development cycle.

Once the TOP modules were at KEK, the data was streamed from the COPPER / HSLB / PrPMC computer and kept locally on ROPCs for analysis until the rest of Belle II had been commissioned.

Additional steps occur now after acquisition to merge the TOP data with that from the rest of Belle II. Data are streamed from the ROPCs to an Event Builder and High-Level Trigger (HLT) farm. The HLT makes a quick determination of whether the event was interesting from a physics standpoint and either discards it or passes it on downstream. Events that make it through are stored long-term for later analysis by collaboration members using the Belle II Analysis Software Framework (BASF2).

CHAPTER 7

OTHER APPLICATIONS

7.1 From one, many

The same 128-channel waveform sampling and digitizing readout that we developed for the TOP detector system is useful in myriad other situations. Most scientific experiments need some kind of readout electronics to collect data, and as channel counts increase to meet requirements to do more precise measurements, it becomes a challenge to find off-the-shelf data acquisition systems that match. Commercial solutions for the readout to such experiments are too big, too power hungry or too expensive. Four examples follow where we applied our “boardstack” as the readout electronics to other projects [18].

7.2 FDIRC @ SuperB

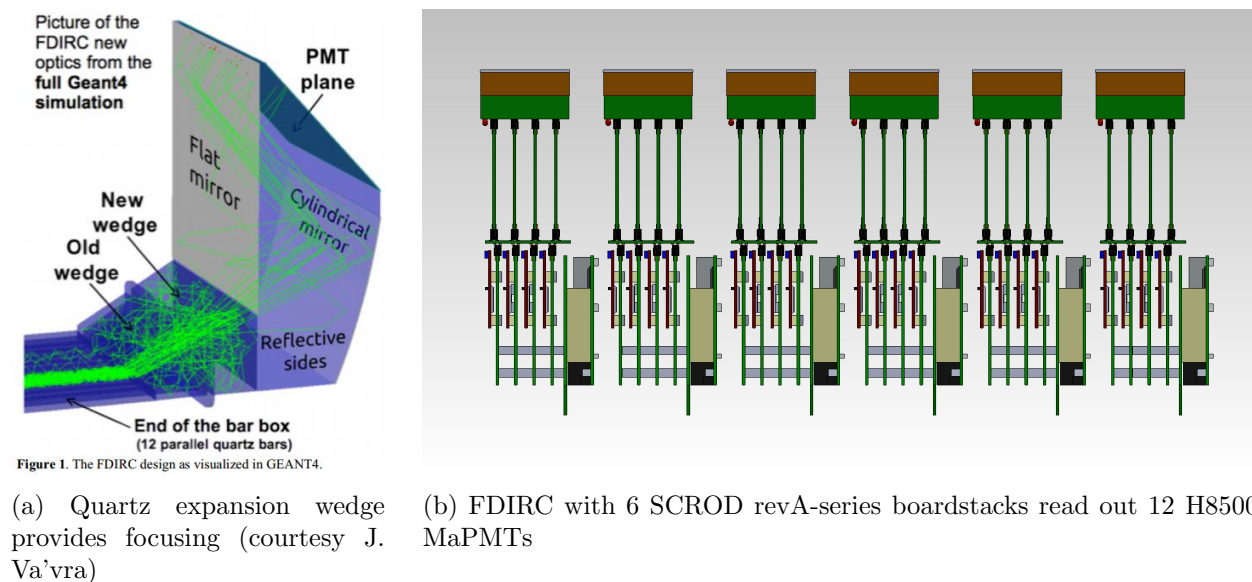
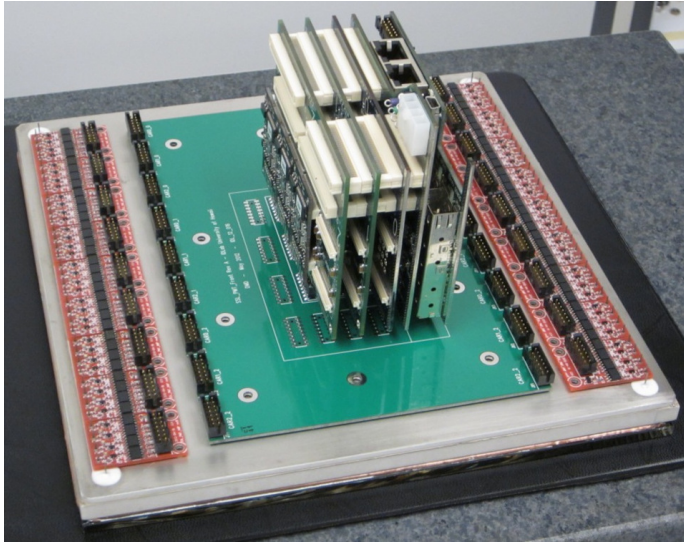
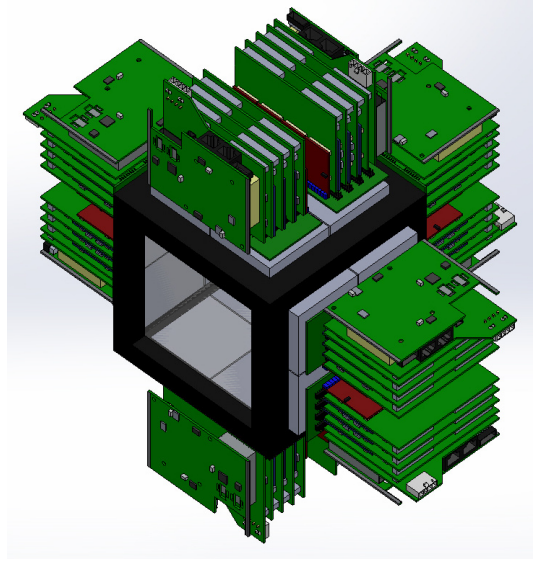


Figure 7.1: Focusing DIRC prototype for SuperB

There was a plan to build a e^+e^- collider detector experiment in Italy called SuperB. The PID component of that was to be a Focusing Detection of Internally Reflected Cherenkov (FDIRC) detector. With Jerry Va'vra (SLAC), we prototyped this using some leftover components from the BaBar DIRC and some new quartz pieces (see Fig. 7.1a) along with 6 of our first-generation SCROD revA-series boardstacks (see Fig. 7.1b). It ran successfully for over a year in a hodoscope at SLAC and showed good performance [19].



(a) SCROD revA-series boardstack attached to the back of a LAPPD ceramic tile (courtesy LAPPD group)



(b) Plastic scintillator cube cutaway showing PMTs and readout electronics on 5 of 6 sides (courtesy mTC group)

Figure 7.2: LAPPD and mTC

7.3 LAPPD

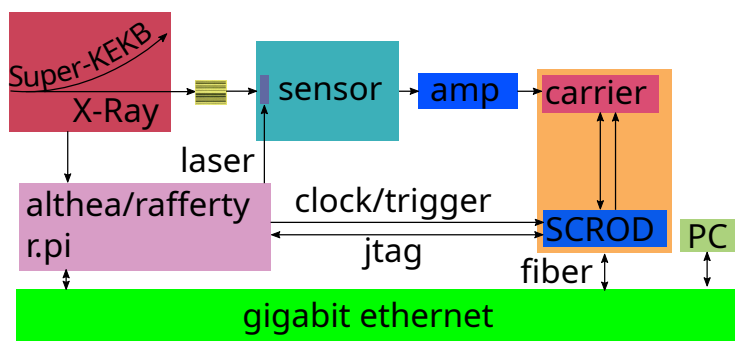
As a model readout for the Large Area Picosecond PhotoDetector (LAPPD) project, we used one of our first-generation SCROD revA-series boardstacks to instrument a prototype 20 cm x 20 cm ceramic tile with stripline anodes (see Fig. 7.2a) [20].

7.4 mTC

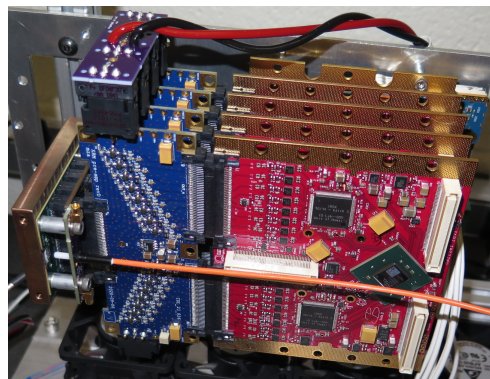
We instrumented a 10 cm cube of plastic scintillator with 24 Multi-anode Photomultiplier (MaPMT) tubes read out by 12 first-generation SCROD-revA series boardstacks (see Fig. 7.2b). When placed near a neutrino source, this type of tabletop detector is capable of doing *directional* neutrino detection.

7.5 SuperKEKB X-Ray Monitor (XRM)

To measure the vertical beam size for the electron and positron beams at SuperKEKB, we took synchrotron light from an upstream bend magnet, let it expand geometrically 10 m, passed it through a Uniform Redundant Mask (URM) coded aperture and then let it expand geometrically for another 30 m. After that, the size had expanded to 6 mm and we used a single-sided silicon strip sensor fabricated at the Stanford NanoFab to absorb the X-Rays. The sensor had 128 anodes



(a) Synchrotron radiation passes through URM and into the sensor



(b) Sensor, amplifiers and boardstack

Figure 7.3: XRM for SuperKEKB

with a $50\ \mu\text{m}$ pitch, and was $75\ \mu\text{m}$ thick. We mounted it with anodes parallel to the synchrotron light so that it presented 2 mm of active sensor to the beam (see Fig. 7.3a).

We instrumented the XRM with one of our second-generation TOP boardstacks modified to have a different first-stage amplifier and connector (see Fig. 7.3b). A raspberry pi co-located in the SuperKEKB tunnel was used to program the boardstack. We developed a timing distribution module to send the boardstack a submultiple of the accelerator clock. The backend was gigabit ethernet and readout was done with a PC.

With this setup, it is possible to determine the vertical beam size on a bunch-by-bunch basis. It operated successfully (see Fig. 7.4) for several months from late 2019 to early 2020.

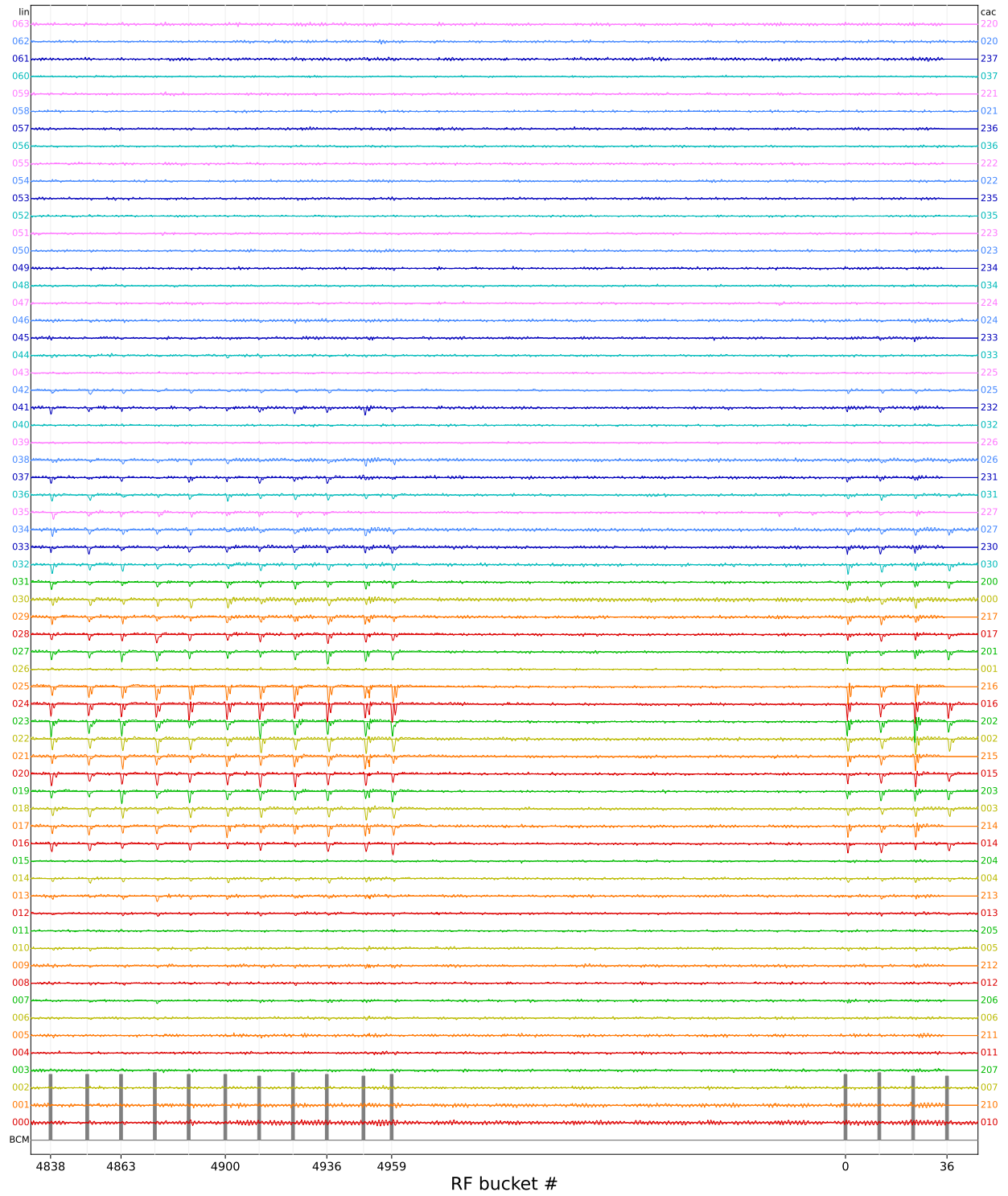


Figure 7.4: Subset of coded aperture data from synchrotron X-Rays in the SuperKEKB tunnel captured with the XRM in 2019 (channels are staggered for clarity and vertical scale is arbitrary units) showing one of the abort gaps and a comparison against the Bunch Current Monitor (BCM)

CHAPTER 8

CONCLUSION

Over the course of 6 years, we developed the readout electronics for the TOP detector system for barrel particle identification. All specifications (see Fig. 8.1 and Tab. 2.1) have been met.

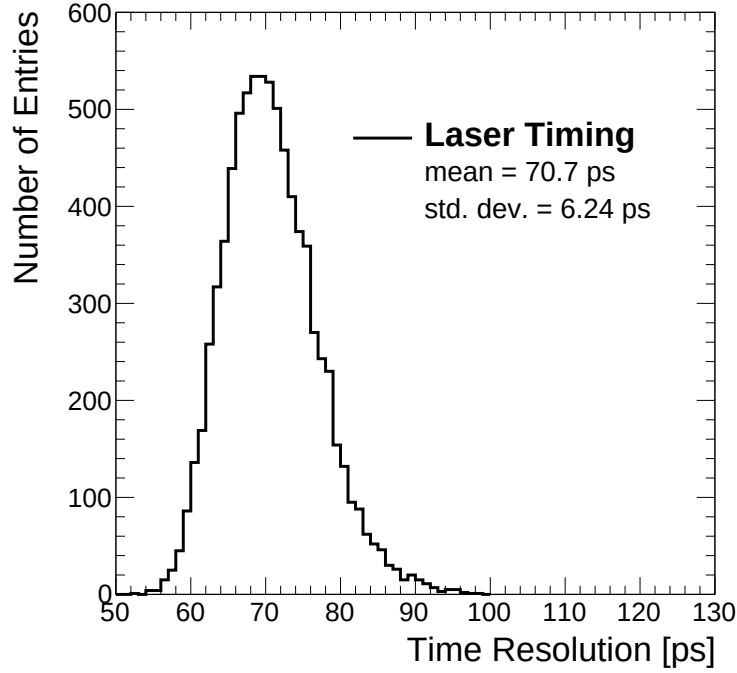
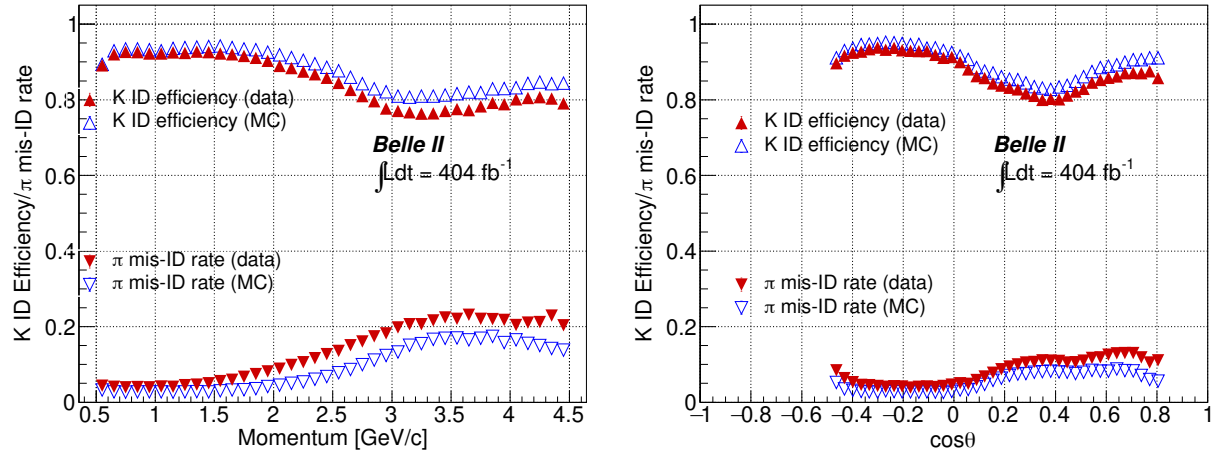


Figure 8.1: Distribution of timing resolutions for all 8,192 channels installed in the detector in 2016 (courtesy Belle II TOP group)

The TOP is now installed in the Belle II detector located at the interaction point of the SuperKEKB electron-positron collider and has been included in physics runs since 2018.

Because of the presence of the TOP detector system, Belle II can distinguish well between kaons and pions (see Fig. 8.2), which means each flavor tag is more accurate than it would otherwise have been. This keeps analysis results from being shifted from their true values and reduces associated error bars on analysis results [21].

This helps continue to uncover the underlying physics at work in the universe, whether it be to precisely confirm the Standard Model's predictions or to provide concrete evidence of something beyond.



(a) Kaon efficiency and pion misidentification rate as a function of track momentum (b) Kaon efficiency and pion misidentification rate as a function of polar angle

Figure 8.2: Ability of TOP detector system to distinguish kaons from pions (courtesy Belle II TOP group)

CHAPTER 9

FUTURE

9.1 B physics and the Standard Model

A major goal of running SuperKEKB and Belle II is to shrink the uncertainties on various components of the unitarity triangles that correspond to the CKM matrix elements. This is shown graphically in Fig. 9.1 to have improved greatly after inclusion of the data from Belle and BaBar. Belle II has contributed further to this and currently shows a tension with the standard model (see Fig. 9.2a) that will need to be resolved.

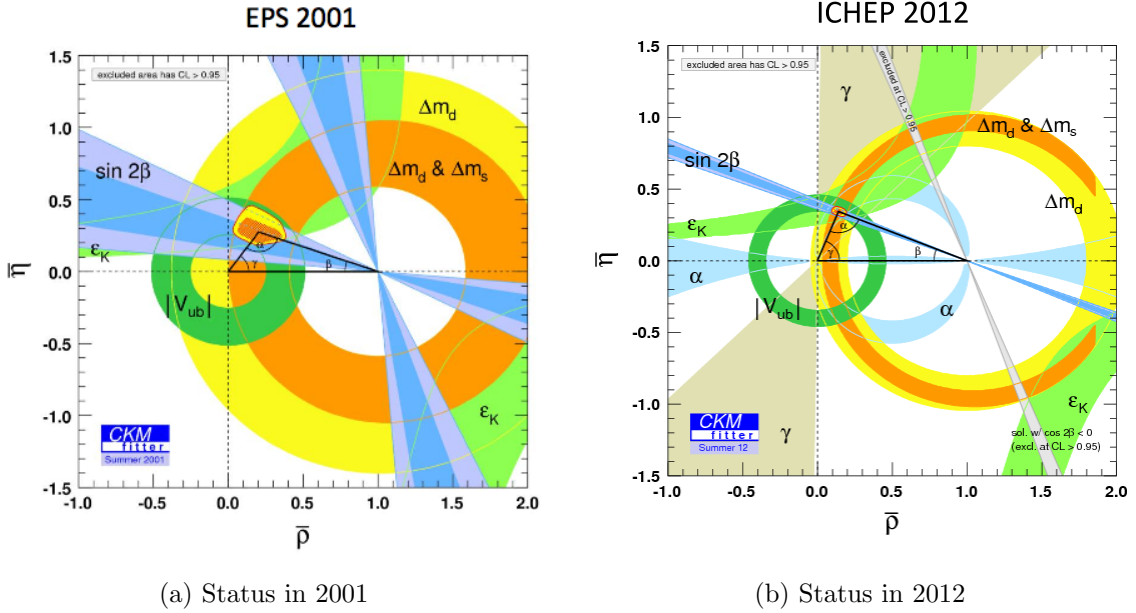
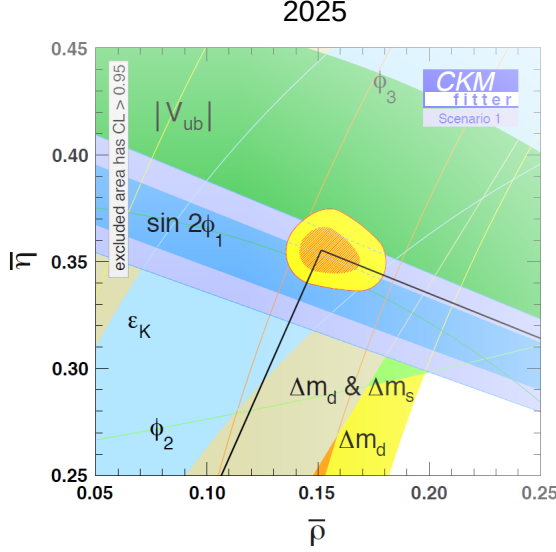


Figure 9.1: How the fits of data to theory have changed since the start of operation of the B -factories (courtesy ckmfitter group)

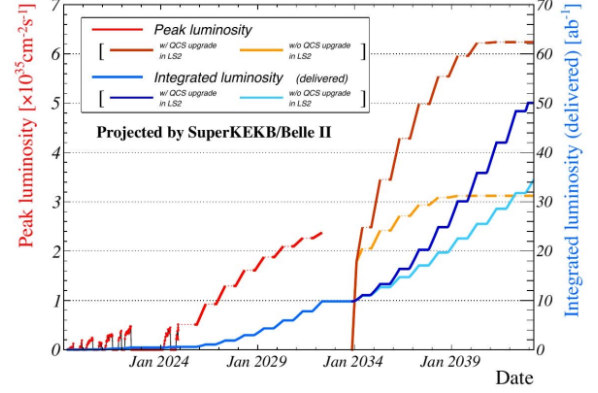
9.2 Belle II and SuperKEKB

The peak instantaneous luminosity reached so far is $L_{\text{peak}} = 5.1 \times 10^{34} \text{ cm}^2 \text{ s}$ which is the world record for any accelerator.

In 5 years of operation, Belle II has accumulated 505 fb^{-1} at the $\Upsilon(4S)$ resonance, already rivaling that of BaBar and Belle. By the time of the next long shutdown (for detector and accelerator upgrades) it is estimated that the data collected will be over $10x$ ($10\,000 \text{ fb}^{-1}$ or 10 ab^{-1}) what was collected with Belle. The goal for SuperKEKB and Belle II is to accumulate 50 ab^{-1} (see Fig. 9.2b).



(a) Zoomed-in status of the tension in the fit to the unitarity triangle vertex in 2025 (courtesy C. Kiesling)



(b) Projected L (red/yellow/orange) and L_{int} (blue/purple/light blue) (courtesy Belle II group)

Figure 9.2: Each increase in L_{int} reveals more of the underlying puzzle

9.3 TOP upgrades

The Belle II (and SuperKEKB) collaborations are constantly pursuing research and development on potential improvements to subdetectors, data acquisition systems, magnet systems, the trigger system and accelerator components. There is a plan for a “long shutdown” of Belle II in a few years to repair or replace subdetector components that have failed by that time (or will not survive much longer).

Several concepts to improve the TOP detector system have been proposed. A few of these ideas are discussed in the following sections. If we can show these are worthwhile improvements, they may be installed as upgrades.

9.3.1 Silicon PhotoMultipliers (SiPMs)

One of these proposals is to replace the MCP-PMTs with Silicon PhotoMultipliers (SiPMs) which are semiconductors that operate as Geiger-mode Avalanche PhotoDetectors (APDs). These do not suffer from the same photocathode damage from accumulated charge that PMTs do, but SiPMs are susceptible to neutron damage that lowers their effective gain.

The main drawback is the dark count rate (number of pulses per second that are not from light) which is *significantly* higher for SiPMs compared to PMTs. One solution for this is to operate them

at -30°C which partially alleviates the dark count rate problem [22]. The challenge then is to operate Peltier coolers (or a complete two-phase cooling system) and a new readout in the same limited space the existing readout is currently occupying.

9.3.2 Higher gain discrete amplifier circuit

To ensure the PMTs last as long as possible in the high radiation environment of Belle II, one avenue to pursue is to reduce the bias voltage (and gain) of the PMTs. This would reduce the rate of photocathode charge accumulation and prolong the life of the PMTs.

To compensate for this, we would need to redesign the amplifier circuit to provide more gain. Care would have to be taken to increase gain without addition of noise so as not to reduce the efficiency of the TOP to trigger on the PMT pulses.

9.3.3 Other carrier changes

Some of the issues we discovered during or since the carrier production campaign could also be addressed at the same time.

Since the PS is currently underutilized on each carrier, changing the design to use a Kintex FPGA instead of a Zynq SoC would provide some combination of power savings and increased PL resources.

Adding a deep memory to each carrier would allow us to do pedestal subtraction on each carrier before sending the data to the SCROD. This would alleviate the burden on the PS on SCROD, freeing it up for further processing throughput.

IRS3B block diagram

2012-10-23

register load interface
selectable pulse control

38 PCLK / bus & register latch
36 Sin / serial_data_in
37 SCLK / serial_shift_clock
39 RegClr / clear_all_registers

shift register
shift register
address decoder

SHout / serial_data_out 40

trigger control

29,25,21,17,13,9,5,1

TRGthresref / trigger_test_channel_threshold
TRGin / trigger_test_channel input
TRGbias2 / trigger_comparator_bias
TRGbias / trigger_comparator_bias
trig_thres [7:0] / trigger_threshold

monostable multivibrator

TrigMon / trigger_test_channel_output 119
TRG [7:0] / trigger_outputs 45,44,43,42,113,114,115,116

timing generator

VadP / sampling_rate_adjustment_PPFET
VadN / sampling_rate_adjustment_NPFET
SST_IN / sampling_hold_mode

RF inputs

31,27,23,19,15,11,7,3
32,28,24,20,16,12,8,4
30,26,22,18,14,10,6,2

RFin [7:0] / RF analog voltage input
1k Ohm / pedestal voltage
Vbias / buffer amplifier bias 1st to 2nd
Vbias2 / buffer amplifier bias 2nd to 3rd

buffer amplifiers

53,52,51,50,49,48
98,99,100

WR_ColSel [8:0] / sampling_to_storage_column_address
WR_RowSel [3:1] / sampling_to_storage_row_address

address decoding for sampling to storage transfer

storage array (256x128 samples)

address decoding for Wilkinson conversion comparator outputs

Wilkinson TDC counters (513 channels)

RD_clr / clear_read_address_counter
RD_en / storage_to_wilkinson_enable
RD Dir / storage_to_wilkinson_address_mode
RD SCLK / storage_to_wilkinson_address_clock
RD_Sin / storage_to_wilkinson_address_data_in
RD_Shout / storage_to_wilkinson_address_data_out

Wilkinson ramp buffers
Wilkinson ramp generation

Vrampref
200pF
NPO or COG

key:

- LIGHT BLUE = Serial / Parallel register loading / pulse interface
- BLUE = Trigger control and output
- ORANGE = RF inputs
- PURPLE = Serial analog transfer from sampling array -> storage array
- RED = "read" (analog to digital conversion directly from storage array)
- GREEN = Readout (data transfer after conversion)

Readout of data to external bus

74 SAMPLESEL_ANY / enable_sample_select_control_logic
68 DO_SCLK / data_out_address_serial_clock
69 DO_Sin / data_out_address_serial_data_in
70 DO_Dir / data_out_address_mode
71 DOE / data_out_enable
77,78,79,80,82,83,85,86,88,89,90,91 DO [11:0] / data_bus
DO_SHout / data_out_address_serial_data_out 71

TST_BoiCLR / Wilkinson_test_counter_reset
TST_Start / Wilkinson_test_counter_start
TSTOut / Wilkinson_test_counter_divided_output 94

cLR / Wilkinson_counter_rate
START / Wilkinson_counter_start 97

"read" Wilkinson conversion of samples in storage array

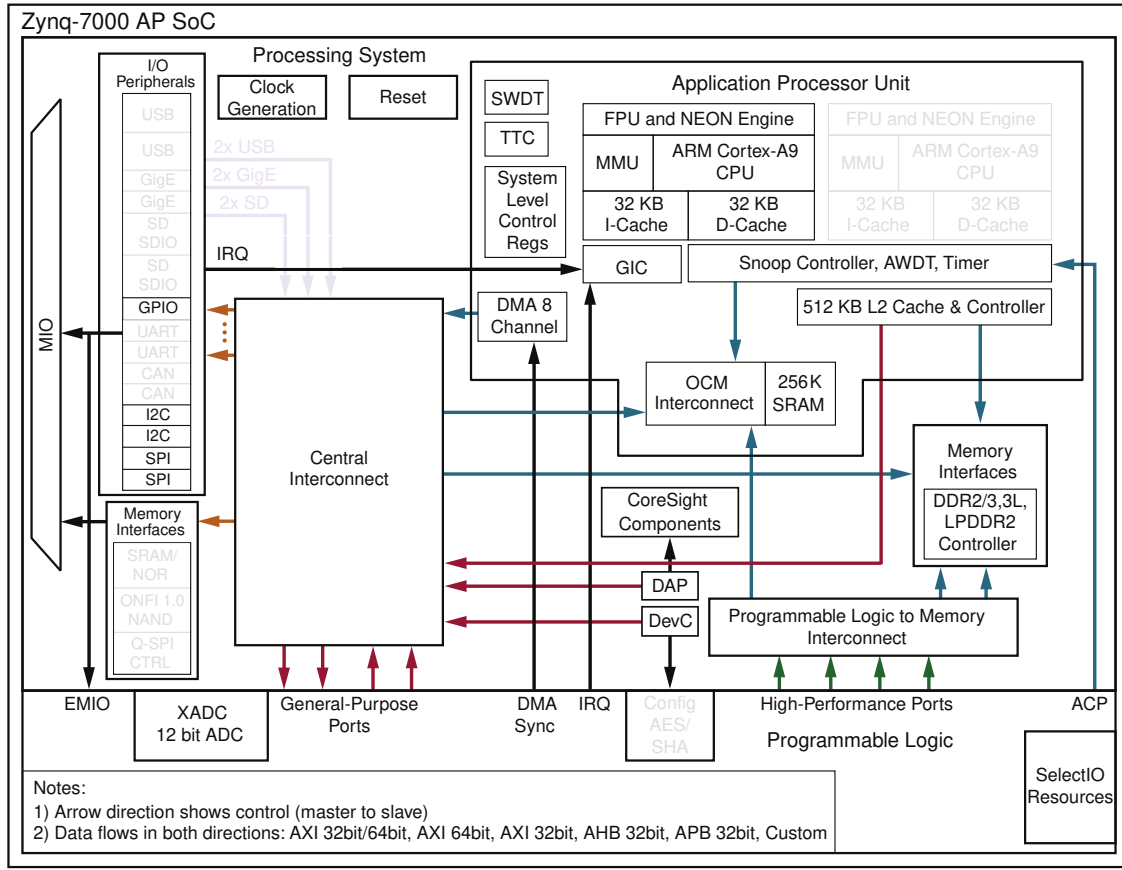
for addressing a window in the storage array to Wilkinson TDCs

83 RD Dir / storage_to_wilkinson_enable
85 RD Dir / storage_to_wilkinson_address_mode
86 RD SCLK / storage_to_wilkinson_address_clock
87 RD_Sin / storage_to_wilkinson_address_data_in
88 RD_Shout / storage_to_wilkinson_address_data_out

49

APPENDIX B

SCROD REVB-SERIES PLANNING



DS190_01_030713

Figure B.1: Block diagram for the PS inside SCROD revB-series (unmodified diagram courtesy Xilinx)

[illegible]

51

APPENDIX C

SCROD REVB2 BLOCK DIAGRAM AND SCHEMATIC

The full SCROD schematics are posted here: <https://www.phys.hawaii.edu/~mza/PCB/SCROD/index.html>.

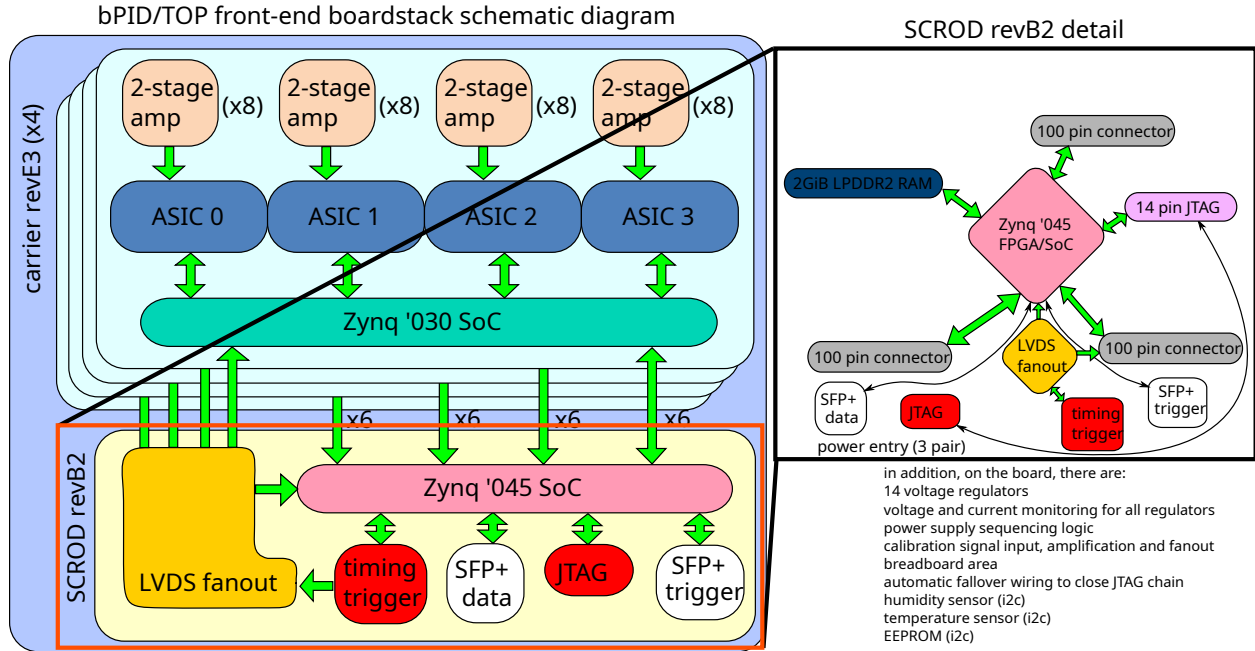


Figure C.1: SCROD revB2 block diagram (inset at right)

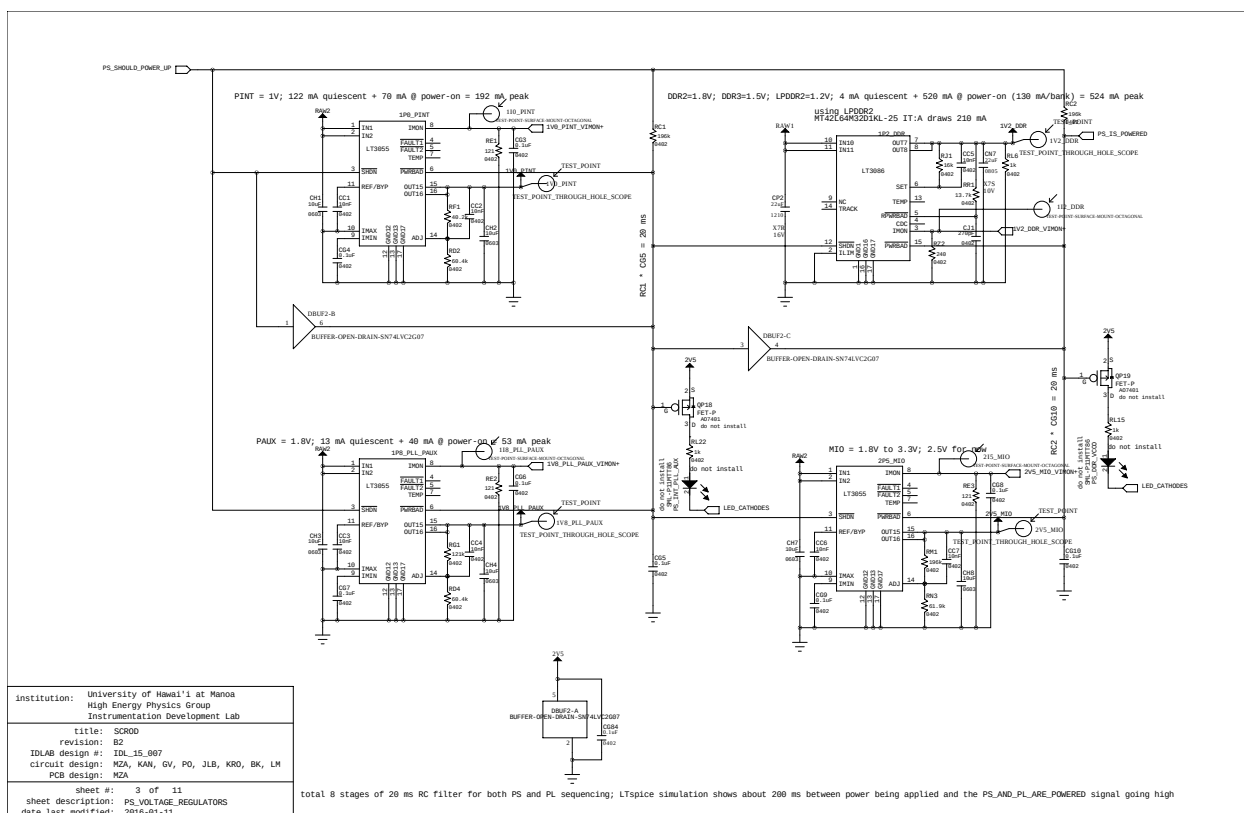


Figure C.3: Cascade of Low-Dropout Regulators (LDOs) (sheet 2 of 3)

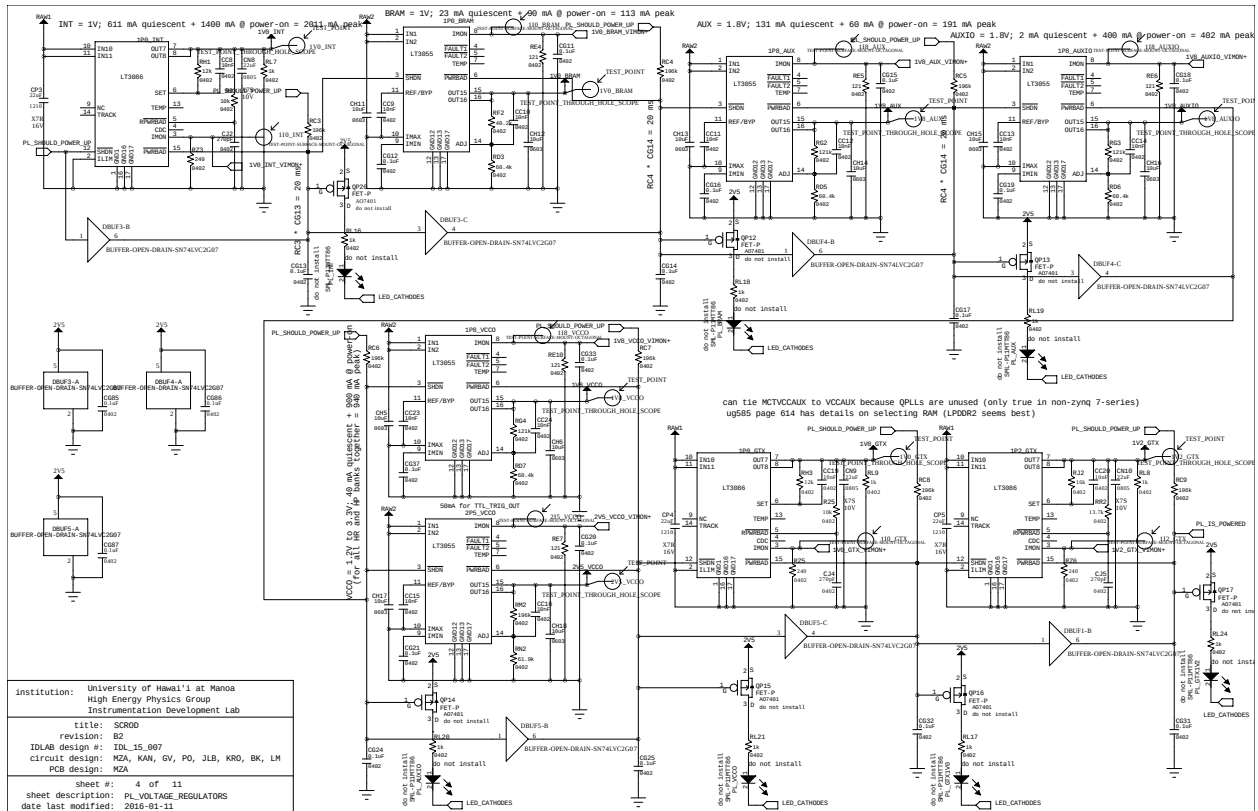


Figure C.4: Cascade of Low-Dropout Regulators (LDOs) (sheet 3 of 3)

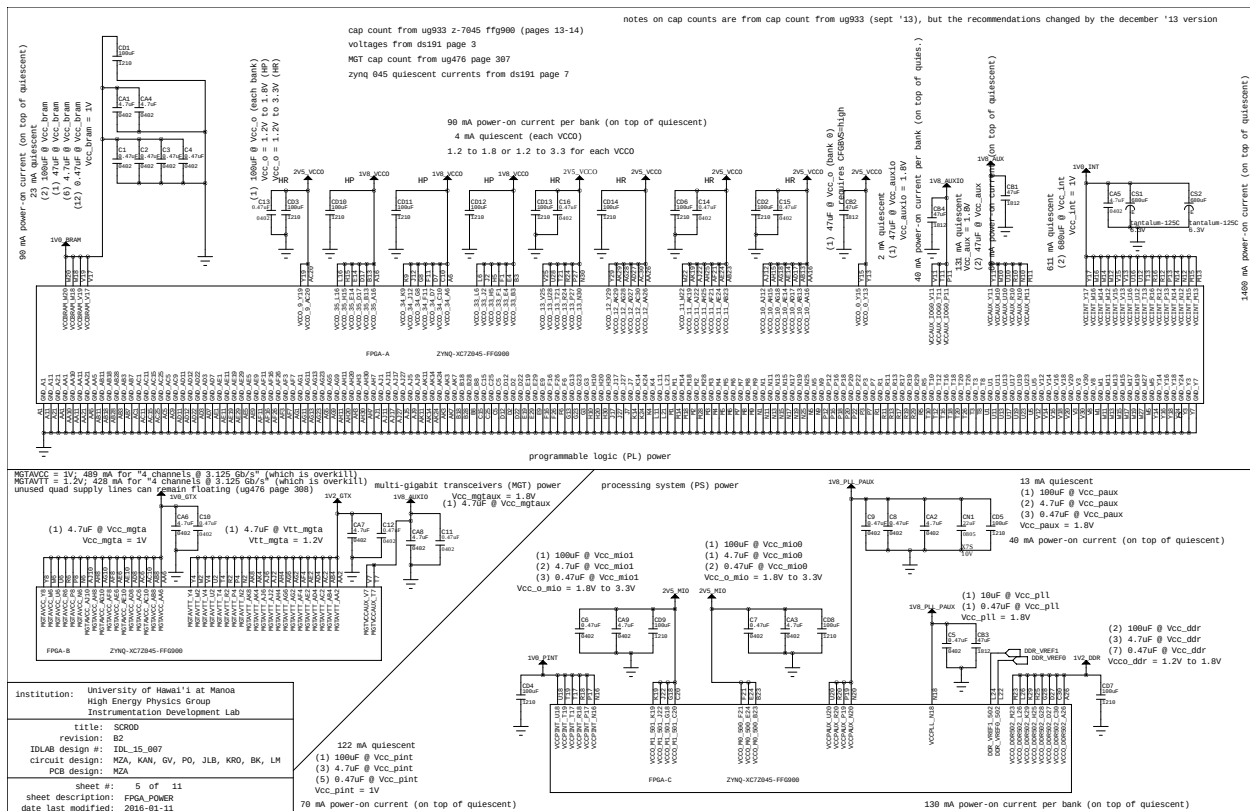


Figure C.5: Power-supply decoupling

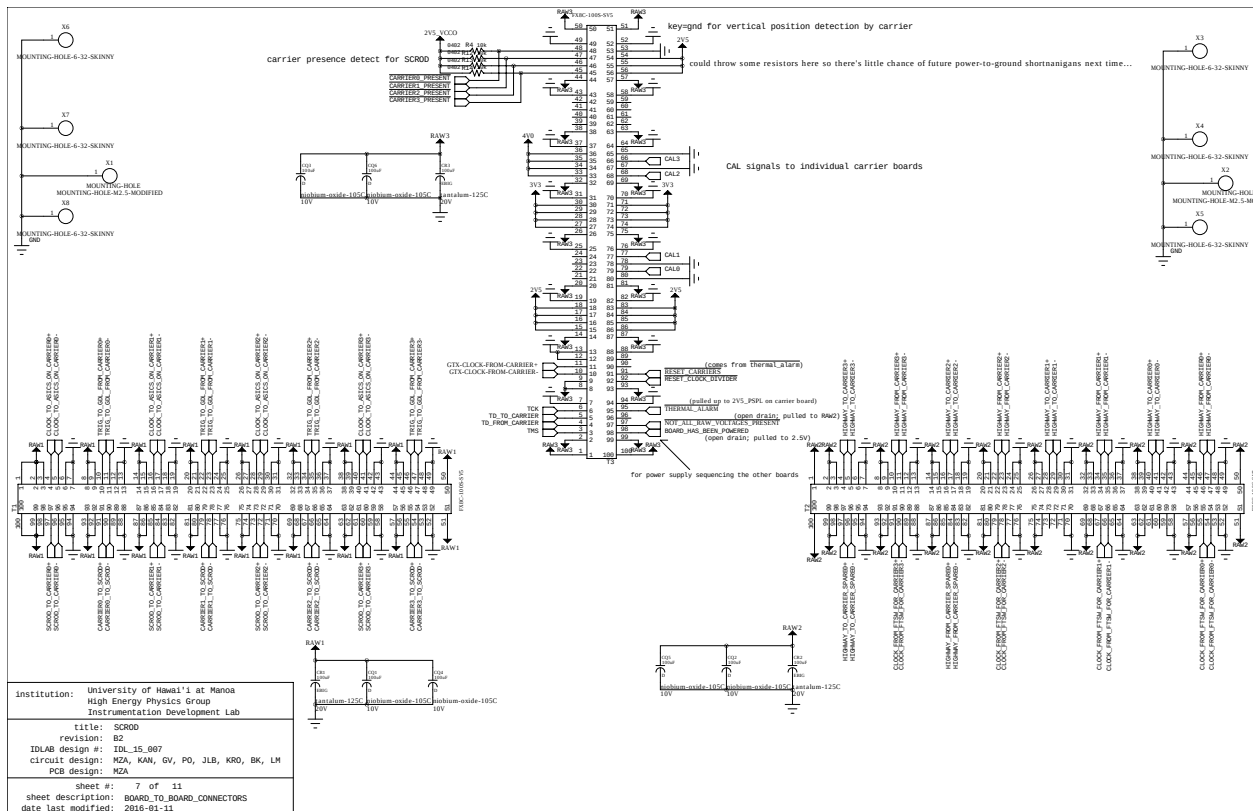


Figure C.7: Connection to carrier boards, bulk capacitance

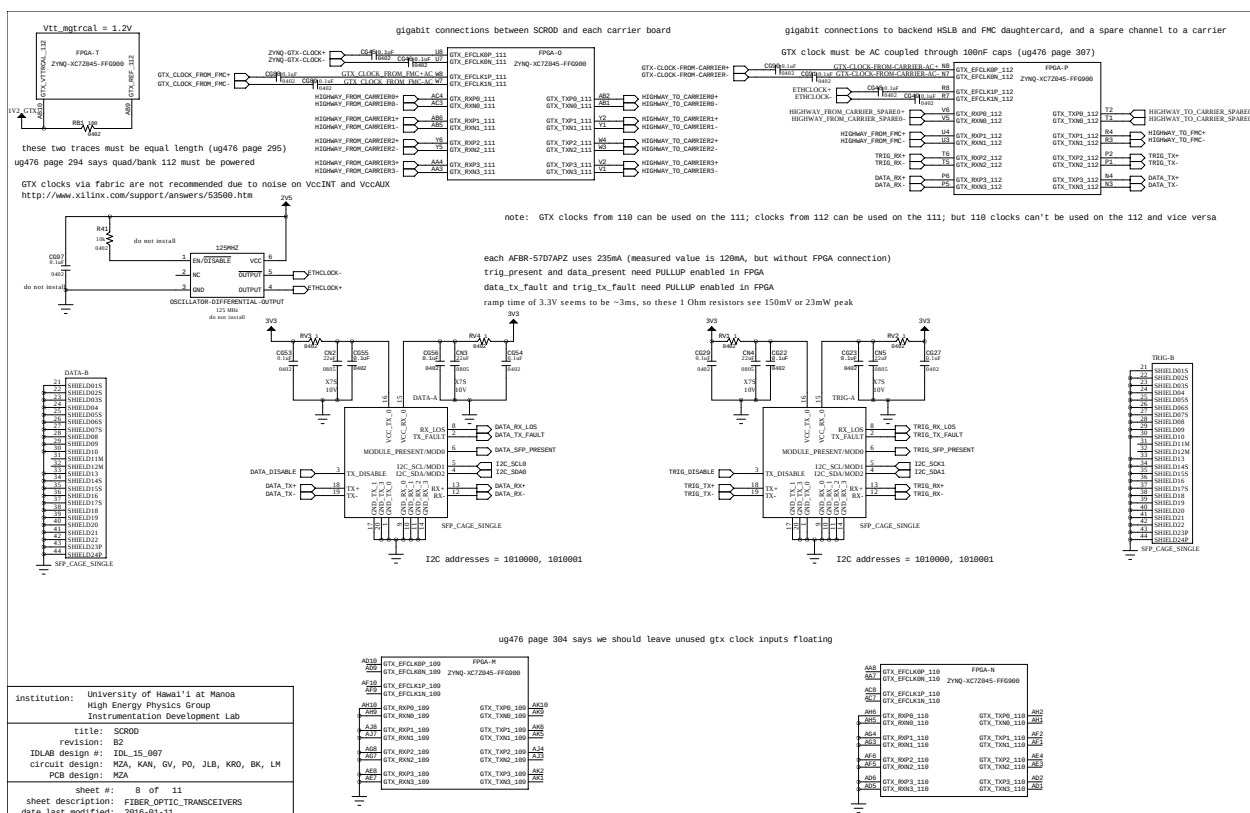


Figure C.8: Multi-gigabit transceivers, SFP ports, oscillator

APPENDIX D

CARRIER REVE3 BLOCK DIAGRAM AND SCHEMATIC

The full carrier board schematics are posted here: <https://www.phys.hawaii.edu/~mza/PCB/TOP/carriers/index.html>.

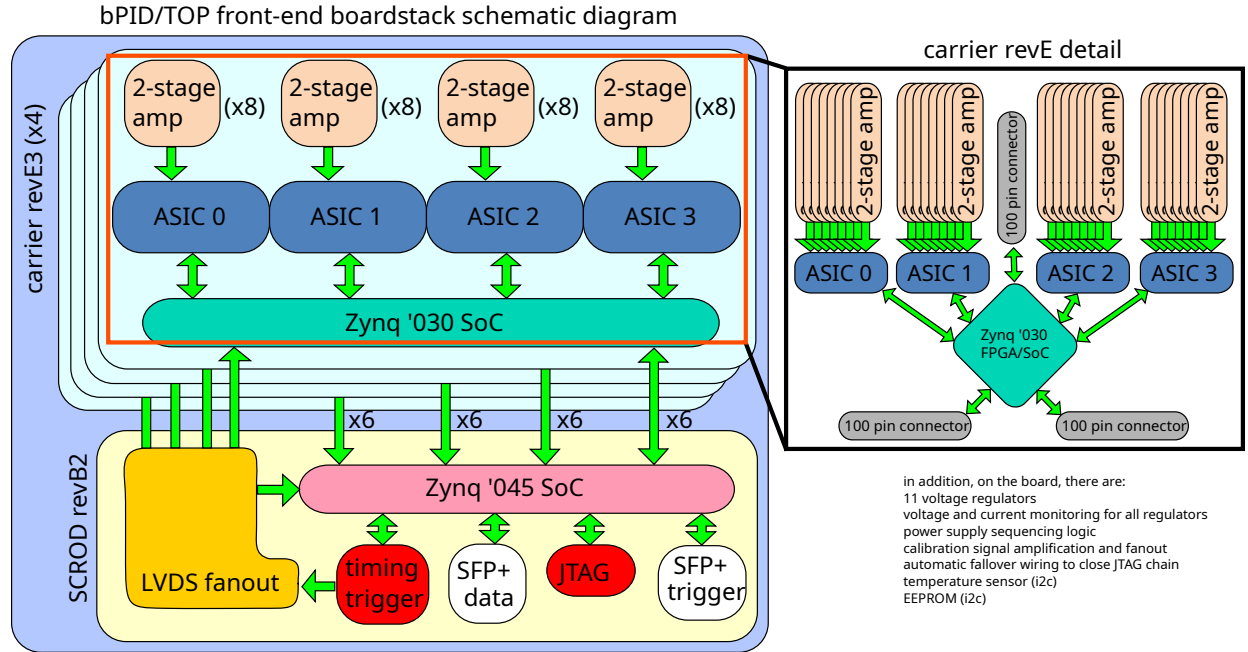


Figure D.1: Carrier revE3 block diagram (inset at right)

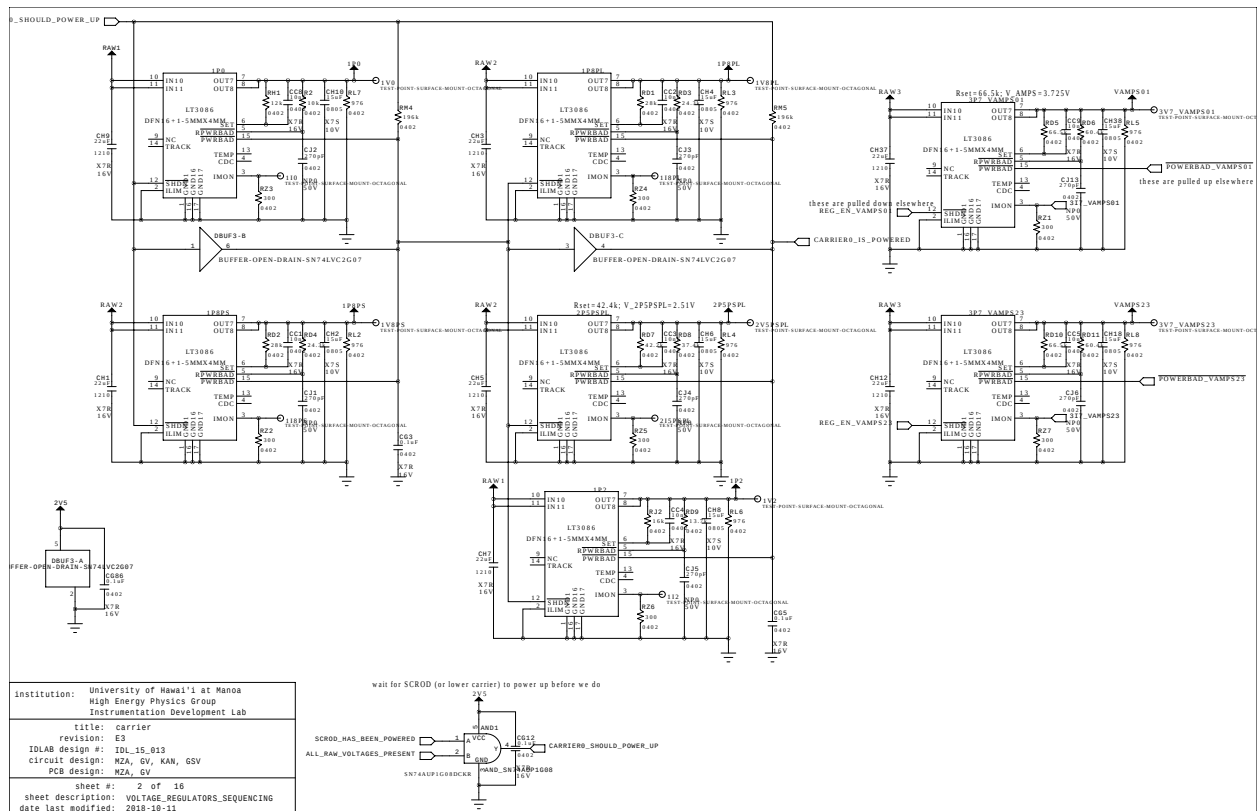
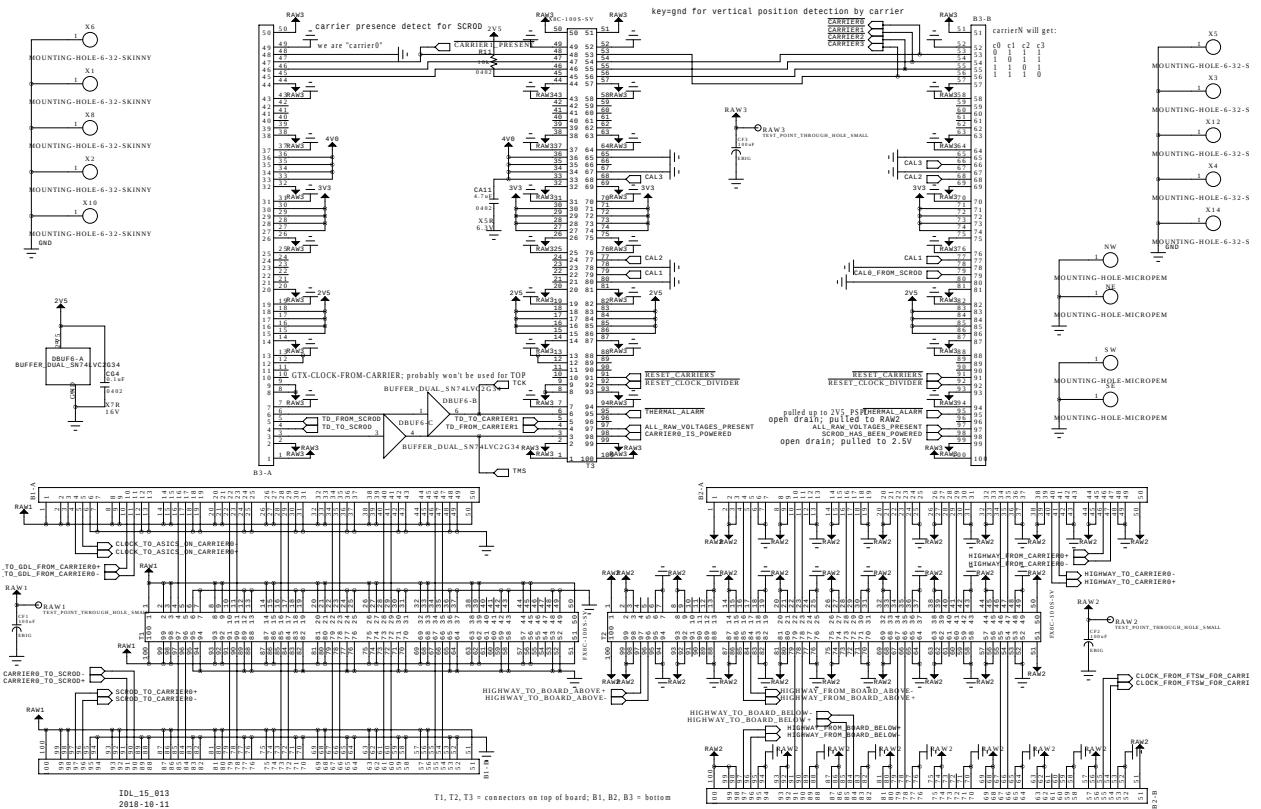


Figure D.2: Cascade of Low-Dropout Regulators (LDOs)



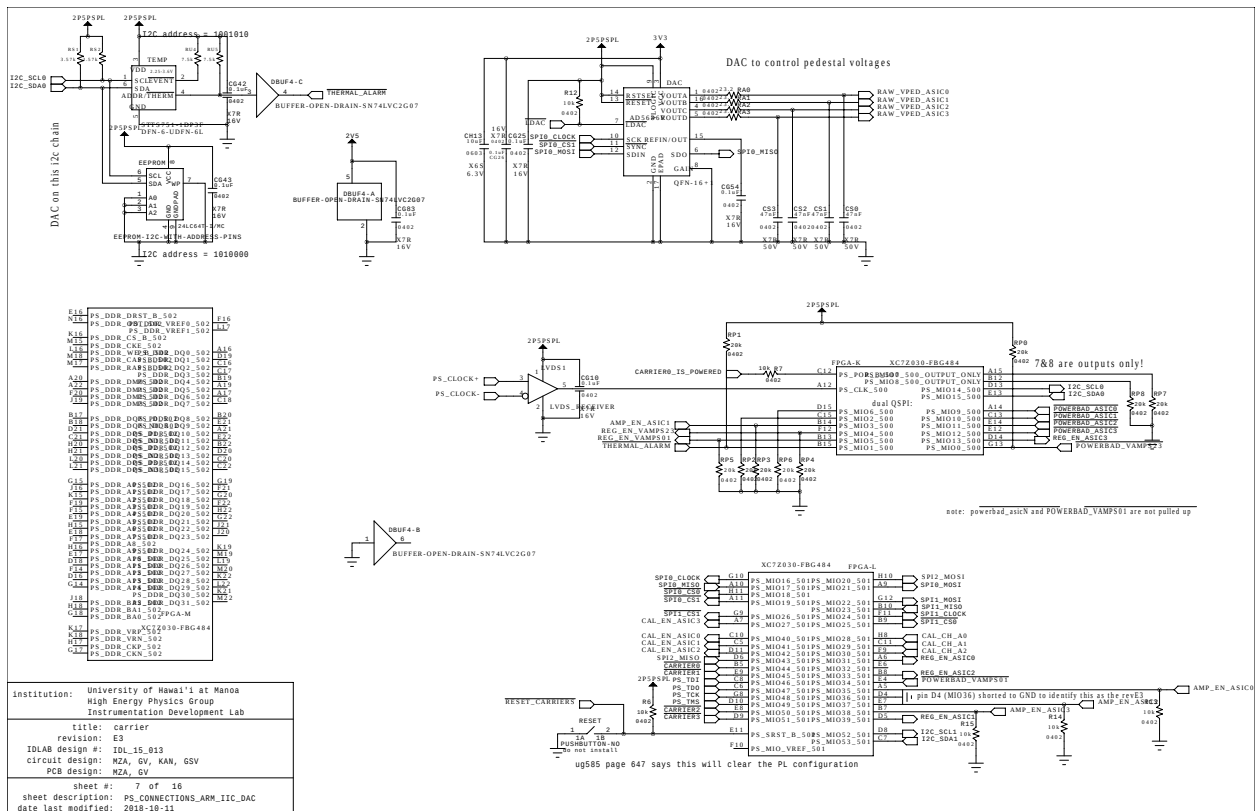


Figure D.7: PS connections, DAC control, temperature monitoring



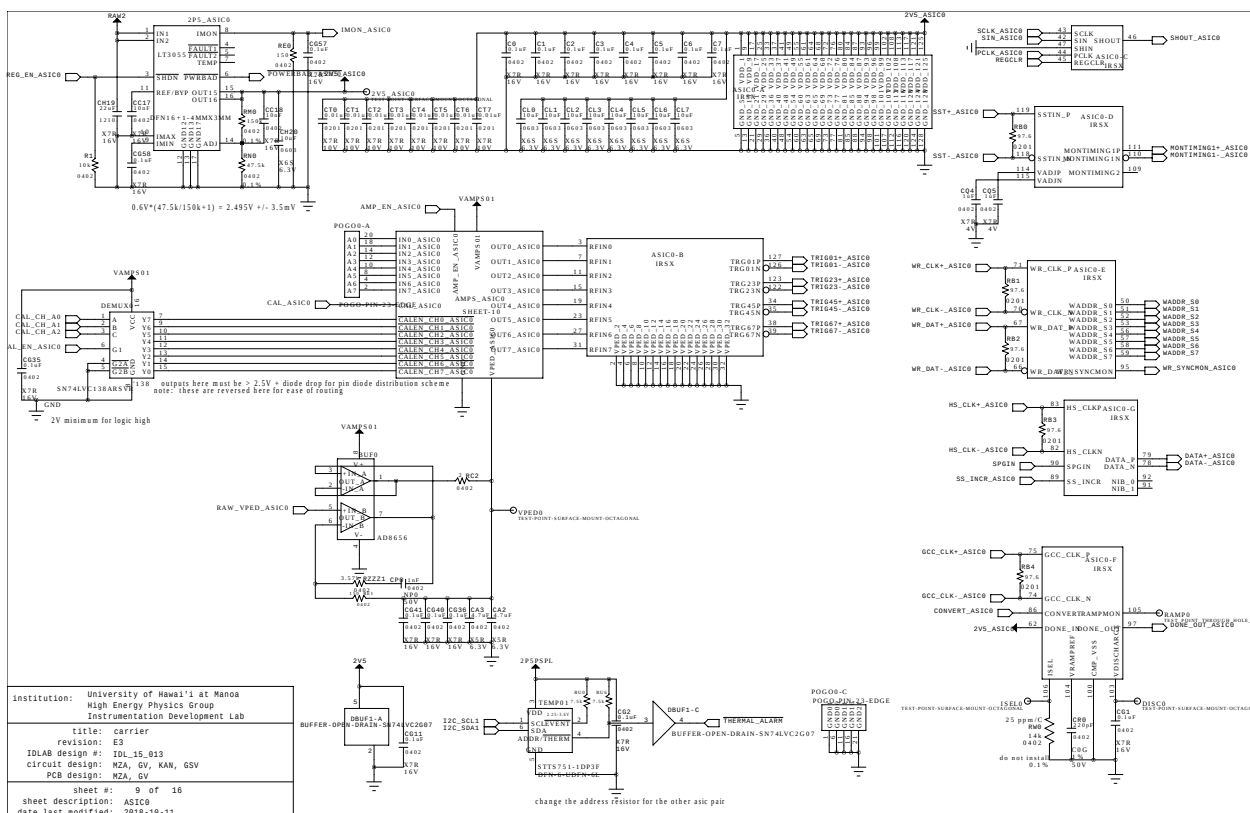


Figure D.9: IRSX waveform sampling and digitization ASIC (only first one shown)

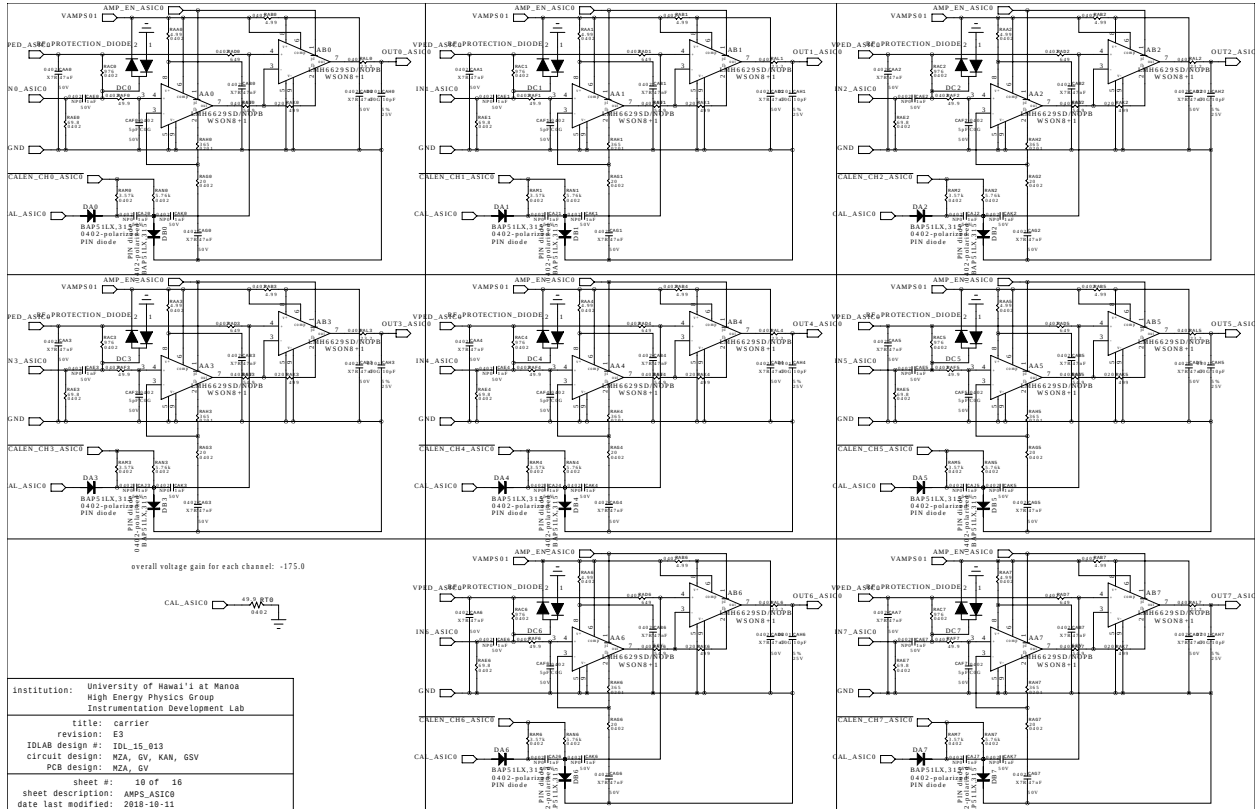


Figure D.10: Amplifier channels (only first 8 shown)

APPENDIX E BLOCK DIAGRAMS OF SECOND GENERATION OF TOP READOUT

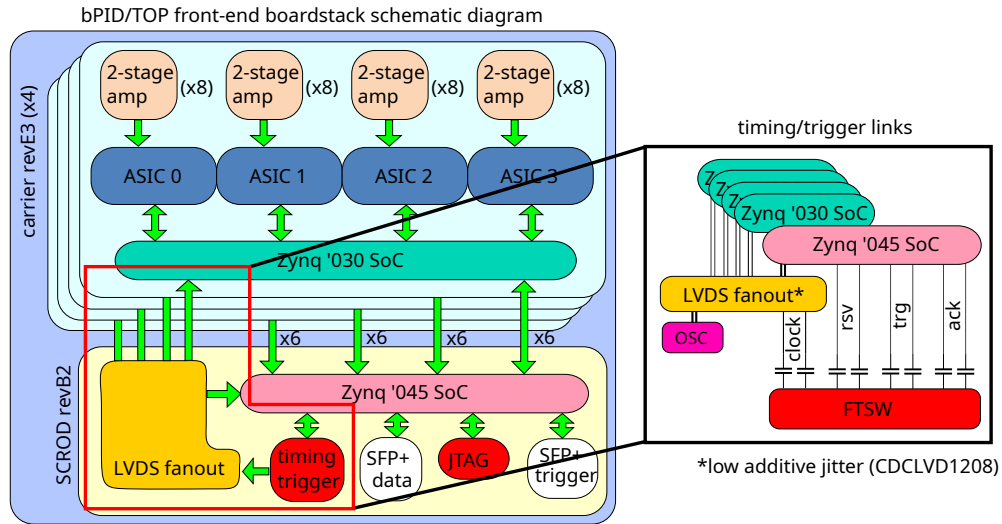


Figure E.1: Distribution of timing and trigger signals (inset at right)

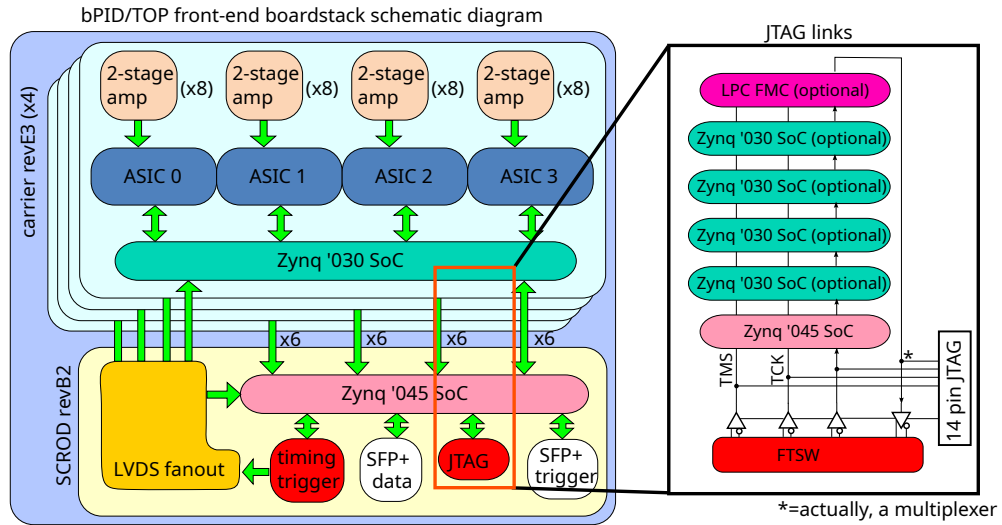


Figure E.2: JTAG (programming) loop traverses 5 PCBs (inset at right)

APPENDIX F CHANNEL MAPPING

bPID/TOP 2015 PMT-to-ASIC channel/row/column hardware mapping

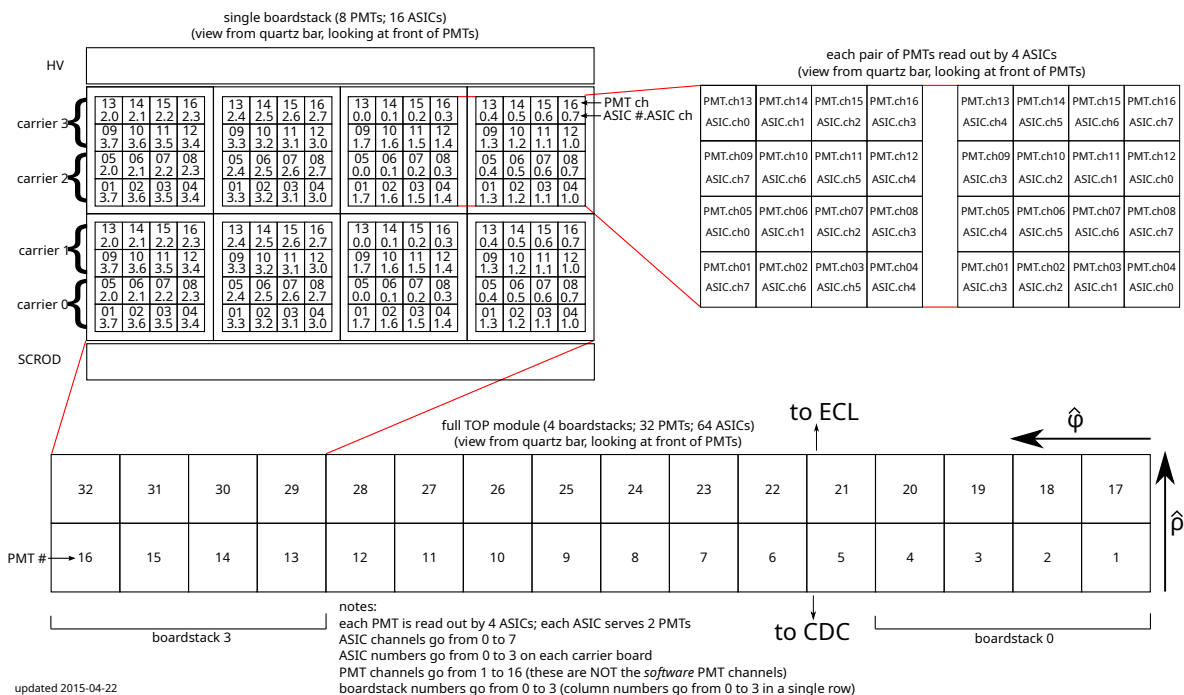


Figure F.1: Channel mapping with respect to Belle II coordinate system

APPENDIX G

FIRMWARE MAP

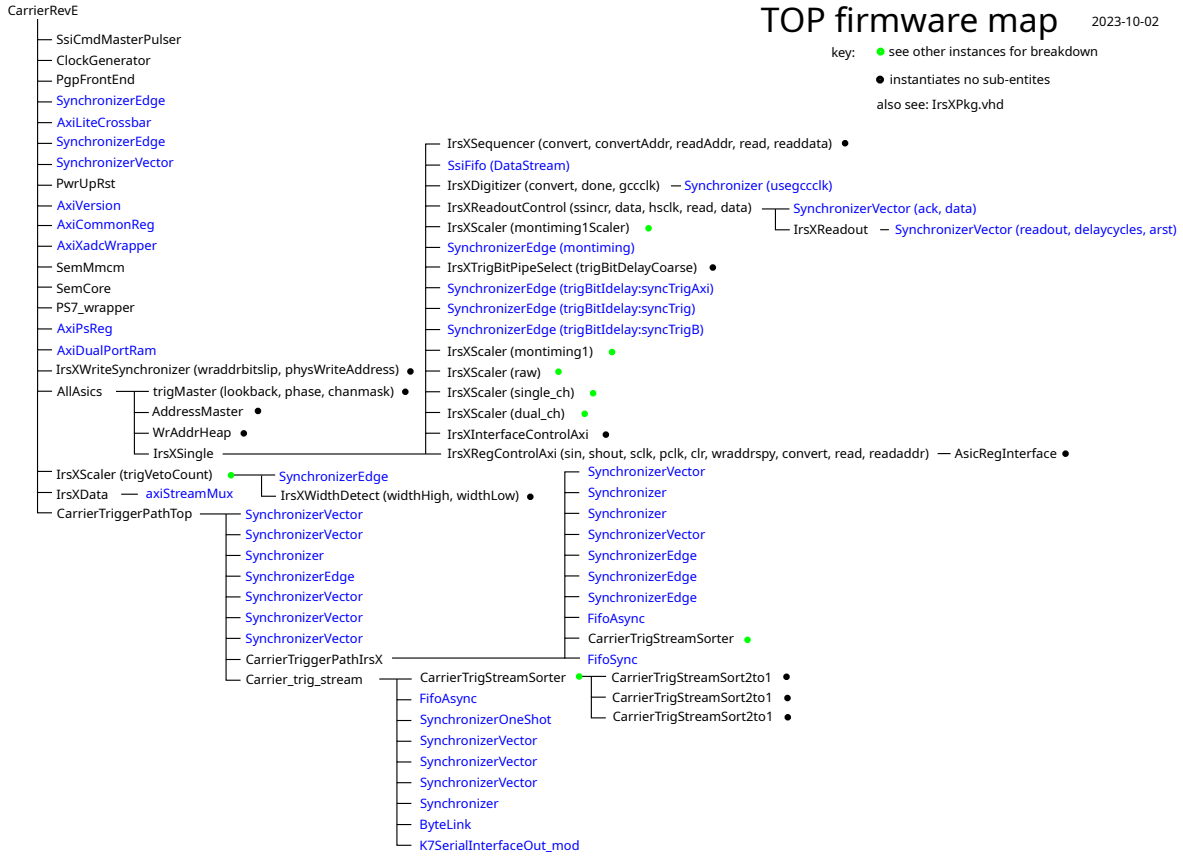


Figure G.1: Map of how individual firmware blocks are connected (carrier)

APPENDIX H POSTED INFO

H.1 Firmware and readout software

The custom firmware and readout software for this project are posted in a git repository here: <https://github.com/mzandrew/BelleII-TOP-firmware>. One major library used is the SLAC Ultimate RTL Framework (SURF), posted here: <https://github.com/slaclab/surf>.

H.2 G. Visser board designs and other information

Front and HV board designs, LVPS and other TOP-related information is posted here: <http://npvm.ceem.indiana.edu/~gvisser/BelleII/iTOP/>.

H.3 IRSX schematic and register definitions

The IRSX schematics and other information are posted here: https://www.phys.hawaii.edu/~idlab/taskAndSchedule/ASIC/IRXS/IRXS_homepage.html.

H.4 Other board design files

Other TOP-related board design files are posted here: <https://www.phys.hawaii.edu/~mza/PCB/TOP/index.html>.

H.5 Source for this document

L^AT_EX source for this document is posted here: <https://www.phys.hawaii.edu/~mza/presentations/thesis.tar>

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