B-Factory Programme Advisory Committee
Focused Review on Vertex Detector System
Full Report

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1 Executive Summary

A focused review meeting by the Belle Programme Advisory Committee (BPAC) for the Belle II vertex detector system (VXD) was held on the 24th and 25th of October at KEK and on the 26th at IPMU. The VXD consists of a two layer pixel detector system (PXD) immediately outside the beam pipe at the interaction point and a four layer silicon micro-strip detector system (SVD). At KEK, general VXD issues and particular items for the PXD were discussed. In addition, a visit to the VXD and SVD assembly areas and to the machine interaction point took place. Discussion on the 26th at IPMU was focused on the SVD issues, and the committee members also visited the clean room for SVD ladder production at IPMU. This section is an executive summary describing only the most essential conclusions of the review and more comprehensive reports are given in the remainder of the document. The BPAC was very impressed by the overall achievements, not only in the detector construction, but also in the area of data acquisition, detector control and software.

VXD

The revised project schedule shows that the assembly of the VXD system will be completed just in time for installation before the start of physics run without any contingency. A detailed integration procedure for the PXD and SVD is still to be developed. The committee recommends the Belle II management to carefully monitor the progress of the VXD construction and to direct effort towards generating contingencies wherever possible.

The work on the thermal mockup shows good progress. However this must be continued with further studies with both simulation and mockup measurements. The changes to the ASICs, in particular the Switcher, could have an impact on the power consumption. This needs to be understood and verified when the new devices are available. The design of the cooling system must take into account all operational scenarios, ensuring that the system is protected against thermal shocks and that operation remains above the dew point for any of the structures.

In the current plan, detector halves for the PXD and SVD will be separately assembled, and then mounted together on the beam pipe. Although the procedure presented appears to be feasible, the committee feels that not enough attention is paid to protect the beryllium section of the beam pipe from possible mechanical stresses or some objects accidentally falling during the assembly operation. A detailed step by step assembly procedure is urgently needed in order to avoid last minute modifications of the support mechanics.

For protecting the beryllium part of the beam pipe, bellows connecting both sides of the VXD beam pipe to the beam pipes of the final focus Super Conducting Quadrupole magnets (QCSs) are crucial. Their design and fabrication should proceed as soon as possible so that enough time will be left for the safety verification.

A serious concern for the Remote Vacuum Coupling device (RVC), that the connection mechanism between the QCS and the VXD vacuum pipes might get stuck, is largely mitigated by the introduction of the Emergency De-installation (EDI) procedure by releasing of hooks, which make solid connection between VXD and RVC. However, the process must be thoroughly tested in all possible conditions.

The committee learned that the machine group has recently discovered a small QCS design problem during the production of the first QCS. Design changes which should also speed up the production are being discussed for the second QCS. Such changes may modify the mechanical strength of the QCS. Furthermore, the machine background may also be affected due to the changes in the cryostat design. Although it is not within its competence, the BPAC thinks that advice from external experts would be useful and that Belle II should be consulted in the decision process.

Safety is a paramount issue. The Belle II interlock and safety system should prevent any accident which endangers human life, environment, infrastructure and the detector itself. The committee heard good progress made by the VXD group on their interlock system. The BPAC thinks that the Belle II collaboration should soon establish a global guideline for the interlock and safety system of the whole experiment to ensure that all subsystems follow the same safety standard for safe operation.

Many items in the VXD project are relevant for both PXD and SVD and must be treated globally. Successful installation and operation of the VXD system requires good coordination between the two systems. In order to ensure that those aspects will be properly addressed, the committee suggests the Belle II management to strengthen the overall coordination role of the VXD project.

PXD

The committee applauds the successful production of the first functioning pixel sensor ladder with electronics by the PXD group. This is a substantial step for the success of the project. On the other hand, the committee noted with concern that communication between two of the necessary ASICs did not perform as expected and revised designs have been submitted for production. Even if the corrected version of ASICs perform as expected, the new PXD production schedule looks very tight with little contingency for the planned date of the VXD installation. The PXD group should be prepared well in advance so that ASIC chip functionalities can be immediately verified upon delivery.

Only conceptual ideas have been developed for the PXD assembly. It should be noted that the PXD is the closest detector to the beryllium beam pipe section, which is a part of the mechanical structure of the VXD. The PXD assembly procedure must be rapidly developed with great care together with all necessary tools and infrastructure so that it can be practiced well. The idea to assemble and test the PXD system at MPI, where necessary expertise and resources are readily available, is well motivated and supported. However, the BPAC stresses that when the completed PXD is shipped to KEK, all the tools and infrastructure for the assembly must also be transported to KEK. It is essential that the PXD can be disassembled and reassembled at KEK for rapid intervention during initial VXD assembly or after data taking commences, if necessary.

SVD

The committee notes with great pleasure the progress made by the SVD group in improving its organisation, particularly the introduction of: a project leader who oversees the overall status of the project; a quality control and assurance group that ensures the production of high quality ladders with a uniform specification among all the production sites; and a common database where all SVD production information is stored.

Development of the detector mechanics and assembly procedure together with necessary tools is advancing well. Some of the procedures have already been rehearsed. Tight communication between the PXD and SVD groups is important in this area, which could be helped by introducing an overall VXD coordination level, which has been mentioned before.

Critically low availability of human resources at the IPMU production site is a concern. Since this site is responsible for producing the ladders for the outermost layer, which are the largest in both size and number, the problem must be solved with the highest priority.

BEAST Phase 2 Detector

During the second machine commissioning phase, the outer part of the Belle II detector and the QCSs will be in place, without the VXD. This is an essential period to understand the sources of machine background and to tune the machine parameters for the later physics run with the VXD. In place of the VXD, the BEAST Phase 2 detector will be installed in order to perform measurements needed for the Phase-2 commissioning. Detector components currently considered for the BEAST Phase 2 detector were presented during the review meeting. However, it appears that not all of those detectors are well motivated for the goals of the Phase-2. The BPAC recommends that the Belle II collaboration, in collaboration with the machine group, should establish a list of required measurements first, then work out which detector components are needed for those measurements. It is also recommended that an overall coordinator be appointed for all BEAST Phase 2 activities

Miscellaneous Observation

The BPAC committee noticed lack of engineering and infrastructure support by the host laboratory. Supports for the construction of subsystems are largely provided by the laboratories and institutes who are responsible for those components. However, for large structures and those items closely related to the accelerator components and safety issues, major support from the host laboratory is required. The work in the experimental area is also where support from the host laboratory is needed, primarily for safety. Some basic software and hardware computing needs, including database and communication infrastructure, require additional support. This support will benefit other experiments at KEK, as well as Belle II.

2 Machine Related Issues

2.1 Interaction Region

2.1.1 Status

Design effort for the Interaction Region is now concentrating on the integration of the Vertex Detector system (VXD) with the beam pipe. The inner detector assembly integrates the beam pipe section at the interaction point, heavy metal shieldings and the VXD. While the assembly is fixed to the inner support ring of the Central Drift Chamber (CDC), the beam pipes are connected to the sections inside of the final focus Super Conducting Quadrupole magnets (QCSs) with bellows in order to protect the beryllium part of the beam pipe.

Excellent progress is being made in the final positioning of the detector and cable routing. The background detectors for beam abort have been designed and first prototypes have been built. They will be used in Phase 1 of beam commissioning. Space for the background detectors that will be used in the Phase 2 commissioning has been allocated in the region near the beam pipe.

A serious concern for the Remote Vacuum Coupling device (RVC), that this connection mechanism between the QCS and the VXD vacuum pipes might get stuck, is largely mitigated by the introduction of the Emergency De-Installation (EDI) procedure by releasing of hooks, which make solid connection between VXD and RVC.

The committee learned that, during the production of the first QCS, the machine group discovered a small design problem that led to damage electric insulation of the superconducting wires. Design changes, which should also speed up the production, are being discussed for the second QCS.

2.1.2 Concerns

The interface between the inner detector assembly and the QCS, including the bellows, is not yet well defined. An issue was raised regarding the transverse stiffness of the beam pipe bellows. That issue must be understood. The committee suggests that reference information on the bellows transverse stiffness is directly applicable to the bellows in a fully compressed condition (when transverse deflection is dominated by shear), but that bending deflection of the bellows would reduce the effective transverse stiffness as the bellows are extended, thereby alleviating concerns.

Changes in the QCS design may modify the mechanical strength of the QCS. Furthermore, the machine background may also be affected due to the changes in the cryostat design. Any relative motion between the inner detector assembly and the QCS will affect luminosity performance as well as the collision spot location.

2.1.3 Recommendations

1. The Emergency Decoupling Insertion device of the RVC should be thoroughly tested in all possible conditions.

2. The interface between the inner detector assembly and QCSs, including bellows, needs to be defined as soon as possible to complete integration work of the interaction region. The committee recommends that the transverse stiffness of bellow assemblies be evaluated over the range of lengths that may occur. If that evaluation leads to a concern, the bellow's transverse stiffness should be determined by direct measurements and compared with the stiffness that is acceptable.

3. Although redesign of the QCS is not within its competence, the committee thinks that advice from external experts would be useful and that Belle II should be consulted in the decision process.

4. It is worth considering the installation of motion sensors between the inner beam pipe assembly and the cryostats. A possible motion detector design could be small capacitive readouts at strategic locations with respect to the VXD endplates and the cryostat inner faces.

2.2 Commissioning and BEAST

2.2.1 Status

In addition to the presentation, the committee also received additional information from the Belle II management on the BEAST Phase 2 of commissioning. This shows a plan for the commissioning and measurement of the backgrounds during the BEAST Phase 2. The plan is quite comprehensive and presents a very impressive list of goals and detectors to achieve these goals.

The primary goal is to measure all of the backgrounds from separate sources and to compare the measured rates with the background simulation. The six separate background sources are: Touschek, beam-gas, radiative Bhabha, two-photon (4-Fermion), synchrotron radiation and injection background.

Several groups have expressed interest in measuring these backgrounds and several detectors (a total of nine) are planned in order to measure all of these backgrounds. Several of these are specialised detectors and will have stand alone readout systems and other detectors (i.e., the PXD and SVD ladders) will be linked to the main detector readout system.

The first impression from the new information is that this BEAST Phase 2 plan is laudable and ambitious.

2.2.2 Concerns

The BEAST Phase 2 plan is quite ambitious and there are a lot of people involved either directly or peripherally. The committee has some concern that, without close coordination, the various groups will be struggling to use the same resources and sometimes even the same space and time for the installation of the detectors and readout systems.

Some of the detectors will be in nearly a final design state being prepared as a part of the Belle II experiment (e.g., diamond and some of the neutron detectors) and these detectors can be operational even before needed for the BEAST Phase 2 run. However, other detectors may require some attention in order to achieve the required performance.

About three weeks of dedicated runs seems to be short to get all of the necessary measurements, since some of these runs require specific beam parameters that may take time to achieve. In addition, many data runs never work the first time and need to be repeated to get the correct results. Although all of the measurements in the current plan are desired, it may become necessary to make sure particular critical measurements are made at the expense of other measurements if running time becomes insufficient.

The committee did not see any mention of background detectors located outside of the main detector. In particular, detectors along the incoming beam lines that could check for neutron fluxes or other backgrounds coming from origins possibly tens of meters away from the main detector. These backgrounds, due to Touschek, beam-gas and some other sources, might be present and should be looked for during BEAST Phase 2.

2.2.3 Recommendations

1. The committee thinks that coordination of the BEAST Phase 2 activity should be strengthened by introducing a dedicated BEAST coordinator. This coordinator makes sure that the various groups are ready in time to install their detectors and to make the measurements they are responsible for. A coordinator is also needed to communicate with the machine group.

2. The committee encourages the development of a plan which sets a priority for each measurement. This plan would be the starting point for discussions if choices among different running conditions are required.

3. The BEAST coordinator should be in close contact with the machine group and understand the goals of the machine group so that goals of the two groups (machine and background) for the Phase 2 commissioning run can be well integrated.

4. If it is not already planed, the committee encourages the installation of background detectors along the incoming beam lines outboard of the main detector.

3 Vertex Detector System (VXD) General Issues

A general remark concerns the fact that, approaching the VXD integration and installation phase, closer connection with the PXD group is needed, both to assure a complete information exchange and to provide synergies on common topics like software.

3.1 Cooling and Infrastructure

3.1.1 Status

The overall cooling system is complex, comprising separate dry volumes and interfaces with adjacent units to be held at different temperatures, for instance $\sim 23°$C for the CDC and $\sim 15°$C for the beam pipe. The combined support and cooling block (SCB) for the PXD is manufactured in 3D printing technology and combines CO_2 and N_2 channels. The block also functions as a local ground connected to a single point common return to the SVD, then to the Belle structure. The SVD is cooled with the Origami cooling pipes attached by dedicated clips. The main cooling requirements are that the PXD sensors must be maintained below 25°C and the ASICs below 50^{o}C. The SVD APV25 chips are preferentially maintained below 0°C to improve the signal-to-noise ratio. The total cooling capacity which must be provided by the cooling plant is 2-3 kW.

The concept for the cooling plant servicing the VXD (IBBelle) has evolved from a system with built-in redundancy via two independent cooling units into a system with one unit. The change is motivated by a lack of space in the Tsukuba hall to incorporate a double system, and the single unit will allow a more straightforward shipping as well as installation in the hall. This concept relies on the fact that reverse annealing is very modest when the sensors are not cooled hence a 100% up time is not essential, and leaves provision for a second unit to be added at a later stage. The IBBelle will be used to service BEAST Phase 2, while commissioning of the VXD will continue in parallel with the use of the upgraded prototype cooling system (MARCO). The components of IBBelle are all in hand, and assembly is expected by December 2015, with safety certification by June 2016. Good progress was shown on the frame, junction box and manifold, and there is provision for a dummy load which will be essential for the commissioning. The committee is pleased to see that the experience accumulated at Max Plank Institute for Physics (MPP) while building components for a similar cooling system for ATLAS will contribute to the assembly process of IBBelle. The cooling related services to be supplied by KEK, such as chilled water, gas, transfer lines and installation crane have been clearly defined.

There has been impressive progress on the thermal mockup, using MARCO, including routing of cables through the QCS region and diagnostics with Fibre Optical Sensors (FOS) and a thermal camera. The mockup has been sufficiently detailed to include beam pipe heating and paraffin cooling, and most components are ready, with the principal missing parts, the SVD ladder components, close to completion. Critical measurements of the pressure drop vs mass flow have been performed, allowing the characterisation of the system and the requirements for the cooling plant to be confirmed. The pressure drop in the SCB is according to expectation, however the principal pressure drop occurs over the flexible transfer lines. The SVD dry-out behaviour has been characterised for the full ladder length, and the MARCO system will need to be upgraded with a new pump to provide sufficient flow capacity for the full VXD test, which is planned for November. With the power off, the mockup shows an even distribution of the temperature of the cold N_2, with a small difference due to gravity between the top and the bottom layers. With power on, the measurements are within the acceptable range, but there is a discrepancy between the thermal camera and PT100 measurements, and between the top and bottom PT100 measurements. This discrepancy is potentially worrying due to the large difference ($\sim 7°$) and the asymmetry along the direction of the beam. The measurements have been made as a function of nitrogen flow showing that the operational conditions are in a stable region, and the behaviour as a function of CO_2 temperature is as expected. Excellent progress has been made in the understanding of the FOS behaviour as a function of temperature and humidity. Following these studies the cable routing has been optimised to allow delivery of N_2 to the PXD at a lower temperature. The mockup tests have demonstrated the critical importance of providing sufficient N_2 cooling.

There has been excellent progress on the interlock system. The system components include the beam abort system, temperature monitoring, humidity monitoring and the Interlock PLC. The beam abort section of the interlock system measures radiation dose rates and integrated doses using sCVD diamond sensors, with both fast and slow beam aborts implemented in the case of unacceptably high rates. The sensors have been tested for charge collection efficiency and uniformity and the related electronics designs are well under way. The packaged sCVD sensors are small but are still a challenge to fit into the limited PXD space including the cable routing. A special path for the radiation monitoring sensors has been included in mechanical design. The prototype sensors will be installed in BEAST Phase 1 and the final ones in BEAST Phase 2. The final electronics version will be decided after the BEAST Phase 1 tests in Q3 2016 with production completed by the beginning of 2017. The temperature interlock monitoring is based on Fibre Bragg Grating (FBG) sensors on optical fibres, together with negative temperature coefficient (NTC) thermistors, with hardware interlock capability. The FBG overall design is completed and the calibrations and final construction is planned for Q1 - Q3 2016 with installation on SVD ladders in Q4 2016. The NTC thermistors and readout electronics are prepared with a plan to make system tests in the DESY thermal mockup in 2016 and to install in the SVD at KEK in Q4 2016. A humidity interlock prototype, based on dew point sensors, is under preparation. The overall system will function in a Schneider PLC with EPICs drivers, able to combine a variety of inputs from the PXD/SVD system together with environmental information from the hall and control of the power supplies.

The overall monitoring and slow controls development has seen tremendous progress. The software interlocks have been implemented in the EPICS database and is already being exercised daily. Alarms are being tested during the current hardware development. The performance of the archiver and the whole database functionality will be tested during the upcoming beam tests at DESY in April 2016.

The ambitious VXD beam test scheduled for April 2016 at DESY is an important milestone for the VXD project. The test with two PXD layers and two SVD layers will exercise the complete system, i.e. detectors, readout electronics, cooling system, DAQ, slow controls, and tracking software.

3.1.2 Concerns

It was highlighted at the review that the chiller unit relies on the use of R404a, which has been under restriction within the EU following new legislation and will be banned from 2020 onwards. Care must be taken to follow the possible implementation of similar legislation in Japan with a backup plan in place.

During the accumulator production, corrosion was discovered in the the welding lines requiring cleaning and chemical treatment. Whereas not directly a part of the IBBelle local construction, this highlights the need for a careful control of every component in the cooling chain to be free of potential corrosive elements (in particular flux) and dust, and the appropriate vacuum to be applied before filling during all test phases to avoid humidity in the system.

The review highlighted expected changes in the PXD ASIC power consumption from the initial estimates. The cooling design must carefully follow all such changes and ensure that the total power consumption is respected.

The temperature measurements during the thermal mockup tests are impressive, however due to the large temperature gradients across the system there is margin for error.

The interlock system has shown very impressive progress with a global plan including communication with the machine. However, a detailed overview of all failure scenarios is still needed.

3.1.3 Recommendations

1. It is recommended that a list of the failure scenarios for the cooling and interlock system be compiled, taking into account the correct interplay between N_2 and CO_2 cooling systems and the possibility of different components of the system working fully or partially at any time, under different powering states. This list may cover the following points:

- In case of reduced power operation (e.g. part of the detector operational) verify that sufficient preheating power is applied to remove superheated CO_2 flow in the capillaries.
- Check that the cooling system is operational at all ranges of temperatures which may be required in case of reduced detector operation.
- In case of a leak, verify the procedure to identify the responsible CO_2 branch within the manifold and determine the procedure to connect/disconnect this branch without risk of contamination or humidity entering other parts of the system.
- Ensure relevant pressure tests are performed on all individual components in the system, and put in place a procedure to (re)qualify connectors which may have been reconnected after a repair.
- Identify the consequence of a leak, in terms of possible damage to system components.
- Define common rules for the failsafe mode of the interlock (HV/LV on/off).
- Compile a list of the reaction of the interlock system to failure scenarios including cooling system or water leaks, rack environmental conditions, power supply failure to LV/HV and cooling system, etc.
- Define the Interface of the interlock system to the Human Safety system and define boundaries for communication with the machine.

2. The continuation of the thermal mockup studies are strongly encouraged. The exact placement of the sensors should be verified, and the measurements of the complete system and comparison to expectation is important.

3. The committee notes and strongly endorses the plan to test failure scenarios during BEAST Phase 1 and Phase 2. The collaboration is urged to test thoroughly the slow controls software and interlock protocols during the DESY beam tests.

4. The committee recommends that the operational experience of the ATLAS IBL cooling system will be fully taken into account in the IBBelle project.

3.2 Assembly and Installation

3.2.1 Status

Steady progress has been made to test the parts, fixtures, and assembly procedures of the SVD mount structure. All end-rings are in hand, arrangements have been made for brazing the CO_2 cooling pipes to the end rings, and end-flanges are expected to be produced this Japanese Fiscal Year (JFY). Mock-ups are in hand to study assembly of the end flanges and end rings. Brazing of Streuli connectors will be tested. A 20 MPa pressure test will be performed on the cooling tubes/connectors after brazing them to the end rings. Isolation connectors with ceramic inserts are to be provided by DESY. Sampling of prototype assemblies is expected during 2015 with brazing cooling tubes to end rings and pressure testing them in January 2016. The tolerance for relative radial positions of end ring and end flange assembly after assembly is ± 100 μm. This tolerance is intended to take into account the thermal shrinkage associated with CO_2 cooling. The adhesive for gluing the end rings to the CFRP support cone has been selected and radiation tested. Two trials have been made of the assembly and gluing procedure, where FWD and BWD half mount structures have been produced, and the procedure has been demonstrated to be successful. The azimuthal alignment of FWD and BWD assemblies is determined by a support bar. Improvements in tooling and the alignment scheme have been made in the latest jigs. A trial gluing of the outer cover assembly using Araldite2015 showed lack of adhesion in some areas. Another test will be made with Stycast2850FT to see if it eliminates the gaps.

The final assembly and installation of the vertex detector (VXD) occurs in multiple steps:

1. Shipment of the assembled and tested pixel detector (PXD) from MPI to KEK
2. Verification at KEK that the PXD remains in good electrical and mechanical condition
3. Integration of the central portion of the beam pipe, the PXD, the silicon strip detector (SVD), and the diamond radiation sensors
4. Cosmic ray test of the VXD assembly
5. Transport of the VXD to Belle II
6. Installation of the VXD into Belle II.

At this review, the PXD group proposed to fully assemble and test the PXD system at MPI, where necessary expertise and resources are readily available. This results in the PXD being shipped to KEK in September 2017 and being available at KEK starting October 2017. Step 2 and 3 of the assembly would occur in November and December of 2017 and January of 2018, followed by Step 4 in February and March of 2018. Development of the detector mechanics and assembly procedure together with necessary tools is advancing well. Some of the procedures have already been rehearsed. The PXD and SVD are assembled and tested independently, the PXD on the beam pipe, the SVD as two separate halves. The VXD is then assembled by bringing the SVD halves to the PXD–beam pipe assembly without uncabling the PXD. The protocol for VXD installation is being developed together with an Alternative Installation Method (AIM). This will be exercised with dummy parts but with complete cabling during BEAST Phase 2.

Proposals for other tooling and procedures associated with transport and installation are being developed. They need to be completed in greater detail, tested, and agreement needs to be reached on the final procedures. Mock-ups have been prepared to check the forward and backward space allocations for VXD services. The space for cables and piping is tight, but an arrangement has been found which allows the machine group imposed “7 mm” rule, that is the clearance between the QCS outer envelope and the cables, to be satisfied.

3.2.2 Concerns

The revised project schedule shows that the assembly of the VXD system will be completed just in time for installation before the start of physics run without any contingency. A detailed integration procedure for the PXD and SVD is still to be developed. In the current plan, detector halves for the PXD and SVD will be separately assembled, and then mounted together on the beam pipe. Although the procedure presented appears to be feasible, the committee feels that not enough attention is paid to protect the beryllium section of the beam pipe from possible mechanical stresses or some objects accidentally falling during the assembly operation.

Clearances from the VXD to the CDC are tight in both forward and backward regions. Testing of installation procedures should be performed with equally tight clearances.

Though many successful tests have been completed, it is not clear whether no torque will be applied to the VXD and beam pipe as the RVC is closed/opened. It is not clear whether a mechanism is needed to maintain the relative azimuthal alignment of flange pairs as they are mated.

The committee is not aware of the fiducial details which would allow the positions and orientations of the VXD and its sub-detectors to be set and known relative to the rest of the Belle-II detectors. Cable and piping paths appear to have been specified, which satisfy spatial constraints. It is not certain whether those paths lead to any issues with unintended or excessive heat transfer.

The committee noticed a lack of engineering and infrastructure support by the host laboratory. Supports for the construction of subsystems are largely provided by the laboratories and institutes who are responsible for those components. However, for large structures and those items closely related to the accelerator components and safety issues, major support from the host laboratory is required. The work in the experimental area is also where support from the host laboratory is needed, primarily for safety. Some basic software and hardware computing needs, including database and communication infrastructure, require additional support. This support will benefit other experiments at KEK, as well as Belle-II.

3.2.3 Recommendations

1. The committee recommends that the Belle II management carefully monitors the progress of the VXD construction and direct effort towards generating contingencies wherever possible.

2. A detailed step by step assembly procedure for the VXD is urgently needed in order to avoid last minute modifications of the support mechanics and it is strongly recommended that the assembly procedure be developed in full detail as quickly as possible.

3. Successful installation and operation of the VXD system requires good coordination between the two systems. In order to ensure that those aspects will be properly addressed, the committee suggests that the Belle II management strengthens the overall coordination role of the VXD project.

4. A mock-up should be prepared to allow installation tooling and procedures to be practiced. A kit should be prepared with all tooling and instruments necessary during installation. The adequacy of that kit should be tested during trials of the procedures.

5. Training of specific personnel (as well as back-up personnel) to carry out each step of the procedure would help ensure that the people who perform final installation are properly trained.

6. At this review, the PXD group proposed to fully assemble and test the PXD system at MPI, where necessary expertise and resources are readily available. This change

is well motivated and supported. However, the committee stresses that when the completed PXD is shipped to KEK, all the tools and infrastructure for the assembly must also be transported to KEK. It is essential that the PXD can be disassembled and reassembled at KEK for rapid intervention during initial VXD assembly or after data taking commences, if necessary. The committee also notes that the decision to fully assemble and test the PXD system at MPI might shift the focus of attention to MPI rather than KEK. There is concern that the overall coordination of the VXD integration will be adversely affected. It is recommended that a tight contact with KEK is kept during the PXD assembly process.

7. For the piping and cable paths chosen, an evaluation of heat transfer to and from surrounding structures should be made. If necessary, cable and piping paths should be adjusted to address any issues.

3.3 Recommendation for Software

Software work related to detector simulation, alignment and track reconstruction was presented during the SVD session and steady progress has been made. It is also appreciated that PXD and SVD are sharing the same production database
http://www.hephy.at/hephydb
and have a common slow control framework.

1. Work should start to integrate the PXD and SVD software with the general Belle II reconstruction software. The committee welcomes presentation of a work plan which includes a list of task along with responsibilities and milestones.

4 Pixel Detector (PXD)

4.1 Sensors and ASICs

4.1.1 Status

At the February 2015 Belle PAC meeting, the pixel group introduced a pilot run for module production in response to the new Belle II schedule. A few wafers would be processed for pre-qualification of all production steps and provide for a check of the correctness of the latest layout changes, and permit testing of the ASICs with real detectors. The consequence of this pilot run was that the PXD would be delivered to KEK in March 2017 rather than August 2016. The committee thought the introduction of the pilot run was was a good tactical move, but remained concerned about the overall sensor production schedule.

The pilot run has finished successfully and the committee congratulates the collaboration on achieving this significant milestone. Many production steps have been optimised and many lessons have been learned. The production consists of three phases. The first phase includes all processing steps up to the deposition of the two aluminium layers, which happens in the second phase. The third phase encompasses the thinning and copper deposition. Three production and five dummy wafers were included in the pilot run. Each wafer contains six sensors, two for the inner layer and four for the outer layer. Optical inspection is carried out after Phase I. A yield estimate was obtained from the optical inspection, but was found to be too conservative. After the Phase II processing the full DEPFET matrix can be qualified and the defects quantified. After the deposition of the first aluminium layer in Phase I, it was found that 3 out of 18 half-ladders are affected by shorts between n^+ and p^+ implants, which result in a loss of the module. Also, 3 out of 18 modules have no shorts between poly-silicon layers 1 and 2. This defect results in a loss of a gate row. The maximum number of shorts observed in a module was 5, whereas it should be noted that there are 384,000 crossings of the two poly-layers in a module. After the deposition of the second aluminium layer, it was found that 13 out of the 18 modules have no shorts or opens in the drain lines. These defects would result in a loss of a pair of drain columns or a partial loss of one readout column, respectively. Some modules were affected by human error and some defects were a consequence of existing defects. Otherwise, there was not much correlation between the defects that were observed.

The pilot run provided good feedback and the processing will be adapted to further minimise defects. The first test results of the DEPFET matrix showed good performance. Overall, the pilot run had a yield of 77.8% of working sensors and 56% of prime grade sensors, which is defined as $> 99\%$ of working pixels. These are very promising yield numbers for the final production.

Electrical tests show lingering issues in the readout. Cross-talk between the data lines between the DCD to DHP is observed, which can be addressed by changing the line spacing of the data lines. Also common mode noise is not fully understood yet. The full speed operation of the modules is compromised due to bit errors in the data transmission. It is expected that some of these issues will be ameliorated with the next version of ASICs.

The PXD project uses three key ASICs for the readout: the data handling processor (DHP), the drain current digitiser (DCD) and the Switcher chip. The DCD chip receives and digitises the DEPFET signals. Each chip has 256 channels with a current receiver and an 8-bit ADC. Together with a 2-bit offset correction DAC it has 10-bit resolution with a dynamic range up to 90 μA. The 32-channel switcher chip generates the fast high-voltage pulses (up to 20 V) to activate the gate rows and to clear the internal DEPFET gates.

Various platforms for testing the ASICs exist either as system or as stand-alone. The main vehicle for testing the ASIC chain has been the Electrical Multi-Chip Module (EMCM). Now the full PXD9 pilot modules are also available for testing the readout chain. It is noted from the onset that there are many inter-dependent parameters in the chain of readout chips that have to be optimised for proper performance.

An internal review of the ASICs took place in July of 2015, at which the following status of the chips was presented. The DCD displayed “missing codes”, which is a feature of the ADC that can be eliminated with no impact on the physics performance. There are also “stuck” or “toggling” bits in the DCD-DHP chain, which is caused by the digital transmission between the two ASICs. The root cause of this effect has been understood and has been attributed to an asymmetry in the inverters used, which causes a distortion of the duty cycle. The drive current will be increased on the DCD side to add a larger safety margin and the logic sampling window increased by a factor of three. A new version of the chip is expected back in the middle of January 2016.

A new version of the DHP chip has been submitted at the end of August to address some significant errors. The serialiser had a timing error, which has been corrected and verified in simulations, with all corners of phase-space simulated. Parasitic resistances have been reduced in the new design and the duty cycle distortion addressed. On the date receiver end, its robustness has been increased by reducing input pad capacitance, adding symmetric delay line elements and removing the hysteresis. The new chip is expected to arrive at the end of November.

Safe operation of the DEPFET matrix requires almost complete clearing of the internal gate after read-out. The specification for the Switcher chip calls for a CLEAR signal with 10 ns rise time to 20 V with a 150 pF load. The time for this step of the read-out cycle should be as short as possible to allow settling of the drain current before it is read out by the DCD. A new Switcher chip has been submitted that will decrease the rise time of the CLEAR pulse to meet specifications, with little safety margin. There is a remaining concern that the rise and fall time will be slower in the final device given the large current draw and parasitic resistances and capacitances. The new version of the Switcher chip will also exclude the serial input from the switching scheme for safer operation and a change in pad layout to accommodate the changes in the bumping technology. The new chips are expected for the end of December 2015. When the new versions of all the chips have been received they need to be bump-bonded to a module before extensive testing can begin.

The modified version of the DHP chip was deemed to be ready for submission by the review panel. As for the Switcher chip, actual layout changes of the design were not presented during the internal review but a follow-up review addressed many of the issues to some degree. The collaboration decided to proceed with the submission given the schedule risk, though it presents a significant risk for the correct performance of the pixel detector. The DCD was in a similar status as the Switcher chip, that is, design changes had to be implemented after the internal review but given the schedule risks the collaboration proceeded with its submission.

4.1.2 Concerns

The margin for the operating parameters of the modules is very narrow. Moreover, unexpected behaviour of the readout chain is still being uncovered. Although it is expected that the overall performance will improve with the next version of the ASICs, the narrow operating margin of the many parameters for proper readout remains an area of concern.

Although the pilot run has been a great success and has provided very valuable feedback for the sensor production and maximises confidence in proper operation of the detector, sensor production remains a critical step in the overall process and is a key schedule driver. Modified versions of the readout ASICs have been submitted partly to maintain the schedule. In the absence of schedule constraints more tests, simulations and verifications would have been carried out before submission. There remain significant concerns regarding their final performance, both as stand-alone as well as integrated in a full readout system.

It is noted that the pressures on the PXD group will not relent over the coming months. To name a few; module production with exacting attention to detail will commence in earnest; new versions of the readout ASICs will be forthcoming, which have to be submitted to thorough testing; beam tests at DESY, integrated with the SVD, need to be prepared for and will divert effort and attention from other areas; module assembly, ladder production and its associated quality assurance needs to be put in place; PXD assembly, integration and installation plans need to be fully worked out, to name a few. This is a massive set of tasks to be completed with limited human resources. The committee is concerned that effort will diffuse and key priority tasks may get shortchanged.

4.1.3 Recommendations

1. Continued rigorous testing of the ASICs, EMCMs and modules to characterise all corners of parameter space is highly encouraged.
2. Attention should be given to the human resources needed for the parallel development of the electronics test system, the ladders assembly, and the preparation for the DESY combined test beam.
3. New production versions of all three readout ASICs will soon be forthcoming. It is very strongly recommended that the PXD group be fully prepared well in advance of the arrival of the first chips to test the full functionality of all ASICs and determine the operation margin of each both as stand-alone, in the full readout chain and, if possible, in system tests.
4. As noted before, with the increasing pressures on the PXD team, which seems already overextended, it is highly recommended that new human resources be identified to look after the overall PXD system, its performance and its integration with the rest of the detector.

4.2 Ladder Production

4.2.1 Status

The PXD surrounds the 10 mm outer radius beam pipe and consists of an inner layer with 8 ladders at a sensor radius of 14 mm and an outer layer with 12 ladders at a sensor radius of 22 mm. Ladders are designed to be self-supporting when held from a support and cooling block (SCB) at each end, with thicker portions of silicon (nominal thickness 0.525 mm) around the periphery of the sensors providing the required mechanical stiffness. The nominal thickness of silicon within the sensor active region is 75 μm. Each ladder consists of two sensors with readout at both outer ends. Ceramic reinforcement is added to the longitudinal joint between sensors to provide adequate mechanical strength and stiffness. Readout electronics are located at the outer end and one long edge of each sensor, with cables extending from each end of a ladder. The backward SCB is fixed relative to the beam pipe. The forward SCB slides on pins embedded in a structure which is fixed with respect to the beam pipe.

The first of four batches of sensors is expected in June 2016. Fixtures to assemble ladders are in-hand. The ladder production and mounting procedures, and associated quality assurance procedures are being developed. The module (or ladder) production involves several institutions: IZM Berlin for flip-chip bonding, surface mount device (SMD) at HLL, with backup at IFIC, and MPP Munich for Kapton attachment and wire bonding, which requires very tight coordinations between institutions to facilitate smooth ladder productions. The first PXD module (half ladder) with electronics was successfully produced and some tests are performed.

Quality assurance involves probe card tests at HLL after ASIC and SMD mounting to check the quality of the bumps, and required hardware and software have been developed and demonstrated. Repairs may be possible at this stage. After the half-ladders are produced, functionality tests and calibrations are performed at MPP and HLL. Some tests involve exposure to radioactive sources, laser tests and homogeneous illumination with light. It appears that complete ladder tests are not fully established and exercised.

The conceptual procedures and schedule for the ladder mounting have been developed and were presented during the meeting. Most parts necessary for mechanical fabrication and assembly are expected in spring 2016. Given the small number of ladders and the limited number of sensors, the number and variety of parts and fixtures for fabrication and assembly appears to be manageable.

Design and production of passive components are ongoing. Notably, one out of four Kapton cables are produced; the design of the other two cables needed is completed, and the design of the fourth cable is in progress. All four types of cable will be delivered by spring of 2016.

4.2.2 Concerns

The committee is concerned that most of the ladder production and mounting procedures have not been exercised except for production of one module, and details of the quality assurance procedure have not been established yet. Ladder production involves many institutions and tight coordination is critical to ensure timely completion. Ladder mounting requires special care since it takes place very close to the Be beam pipe which is one of the most delicate component in Belle-II.

Given that part failures have occurred in the sliding joints of SVD prototypes due to thermal contraction, the possibility of failures due to binding of the pin and socket assemblies of the PXD ladder mounts is a worry.

The committee notes also in this area that too little time contingency remains should problems develop during fabrication and assembly of the PXD. Personnel contributing to the PXD are doing very well but, as noted before, already appear to be overextended.

4.2.3 Recommendations

1. The committee strongly recommends performing end-to-end pilot production with all ladder components earlier rather than later using active components with a production-like schedule and ironing out any issues that could slow down the production. In this pilot production, all QA procedures should be exercised as well.

2. Likewise, ladder mounting procedure should be exercised using mechanical dummies as soon as possible in order to avoid any issue later and written procedures should be established.

3. Belle II management should monitor progress and seek additional resources should problems or delays be noticed.

4.3 Data Acquisition, Electronics Environment and Control

4.3.1 Status

The PXD data acquisition is characterised by the comparatively high data-rate out of the detector, which is more than $10\times$ the aggregated anticipated Belle-II event-size excluding the PXD. The strategy to reduce this is by using a region-of-interests (ROIs) provided by the High Level Trigger (HLT) based on the SVD information in a two stage-readout. The HLT needs about 5 s to decide and requires 128 GB of buffer memory. The maximum rate of incoming events can reach 30 kHz which sets a lower limit for the speed of the internal data-handling.

The selection is implemented in the ONSEN modules, which consist of an xTCA carrier and AMC functional cards. The AMC card v4 is ready and boards are being produced both for the PXD and SVD data-concentrator in two incompatible variants.

About a third of the required boards will be produced by the end of 2015. The DATCON functionality to concentrate incoming data requires two more auxiliary boards, the tracking card and the extension card.

The test results presented for the ONSEN and DATCON system are very encouraging showing no reason for concern regarding achieving the required performance. The DATCON system has moreover been used successfully in the DESY test-beam.

In the control of the readout-system good progress has been made in integrating the control with EPICS based software. Two more boards are required to interface all units with Intelligent Platform Management Interface (IPMI).

The status of the slow control is described in the SVD section.

4.3.2 Concerns

For the DAQ there are no concerns regarding the viability of the system. The committee just notes that a wide variety of boards and associated with them firmwares are being used in this system. The number of units for the various boards are small. Nevertheless an adequate number of spares should be ready, ideally no less than a minimum of two for each type. Some thought should be given on how hardware and firmware will be maintained over an expected 10 year life-span. In particular the FPGAs will likely be very difficult to obtain in case a spare-board beyond the available spares will be needed. Similarly, firmware expertise must be kept in the collaboration and the tool-flows to create revisions must be kept in working state and documented.

4.3.3 Recommendations

1. A strategy to deal with spares, firmware updates and component obsolescence for a ten-year life-span should be prepared.

5 Strip Detector (SVD)

The committee commends the large effort exerted by the collaboration to address the concerns expressed in the November 2014 focused review and in the February 2015 general review. In particular the BPAC congratulates the SVD collaboration for the successful implementation of the Quality Control Group (QCG) which defines the specifications in a sign-off process and reviews/qualifies site procedures. The group collects all documentation and stimulates the production of proper documentation and serves as an information exchange platform for the module production. The QCG is starting to cover on QC/QA for the SVD ladder mount, SVD commissioning and installation.

A revised project schedule has been presented. Major milestones are the completion of origami flex hybrids and pitch adapter in March 2016, end of ladder mounts in October 2016 and full SVD assembly in September 2017, so that integration in the VXD can start on November 2017. This schedule shows delays up to 7 months with respect to the February 2015 BPAC versions but it reflects the progresses achieved and the experience gained in the past year. Given that most critical issues in the ladder production are now solved and full qualification of all assembly sites is expected by January 2016, it appears realistic, provided adequate human resources are available for L6 ladder production.

More specific reports on the ladder production, mechanics and electronics and readout are presented in the following subsections.

5.1 Ladder Production

5.1.1 Status

During the meeting a detailed report of the achievements since the February 2015 BPAC meeting were presented and a new schedule outlined.

The Pisa production site was already qualified for production in May 2015 and has 20% of the FWD and BWD module production completed. At the time of the October BPAC meeting the status of the other sites was: Melbourne (L3) was under review for production readiness with the aim to start production in November, TIFR Mumbai (L4) was in the process to build a pre-production ladder to obtain production readiness in December and build ladders from January 2016 on, HEPHY Vienna (L5) obtained qualification for production in August with the aim to start production in November. At Kavli IPMU (L6), a shortage in human resources delayed pre-production which is now aimed for December with the goal to start full production in January 2016.

In February 2015, the BPAC recommended the purchase of additional DSSD sensors to reach at least 20% of spare sensors. The Melbourne site has purchased 5 additional HPK DSSD sensors to be delivered in December 2015 bringing the safety factor for all sensor types above 20%. The quality of the existing sensors has been validated. Except for fully equipped origami hybrids which are expected to be delivered in three batches, the first of which in December 2015, all ladder parts are now in the hands of the production sites.

The test procedures to be followed by all production sites were presented. Following the committee recommendations, the usage of the central construction database is required as a mandatory part of the site qualification process. The common database, which will be also used for PXD construction, is hosted on a server at HEPHY in Vienna and regular backups are performed.

The pitch adapter 0 (PA0) problem was completely solved by a re-design of the origami hybrid. A batch0 production of the newly designed hybrids, started in February 2015, revealed several problems in the origami production procedures identified by careful QA tests after each production step: (a) glue residuals were scattered by the laser cut on the PA0 pad, (b) solder drops were found on the PA0 pad after reflow, (c) dirty APV chip surfaces were found. As a result, the end of batch0 production shifted from April 2015 to July 2015. The sources of these problems were all identified and the production procedures adapted and documented accordingly so that they are avoided in the mass production. A full ladder assembly with a batch0 origami flex was made at HEPHY in Vienna and its performance was verified in a source and beam test and after thermal cycling. It was then further found that the pad for the grounding wire was damaged by the soldering procedure due to application of too high temperature. This will be avoided by letting the company (REPIC) to perform the ground wire soldering under well defined soldering conditions.

The new schedule foresees the start of the ladder mount in October 2016, the end of ladder production in May 2017, defined by the schedule of the L6 ladder production at IPMU, and the end of ladder mount in September 2017, two months before the now scheduled start of VXD integration.

5.1.2 Concerns

The revised time schedule still contains some contingency. However, procedures and corresponding documentation of the SVD ladder mount, commissioning and installation are still to be fully developed and therefore there might be less contingency than currently thought.

In general, the ladder production is on a good track thanks to the implementation of a well-working management structure and the QCG. However, the committee is worried by the fact that only recently it has been fully realised that the Kavli IPMU site, responsible for the most demanding L6 production, suffers from a shortage in human resources. At this point, the site is not completely ready for production. A significant delay in start of Ladder 6 production might remove the contingency of the SVD ladder production before the start of the VXD integration.

5.1.3 Recommendations

1. The committee urges Belle II management to give highest priority to a pertinent solution for the shortage in human resources for L6 production that not only guarantees more manpower but also the necessary long-term expertise over the whole production period. Ideally, such a sustainable solution should be put in place before the sign-off for qualification in order to guarantee that the whole production team is well trained right from the beginning of production.

2. The committee supports the plan of the QCG to work out procedures and corresponding documentation of the SVD ladder mount, commissioning and installation as soon as possible.

3. The inclusion of manpower evaluation in the examination of the site production readiness should be considered.

4. The committee is pleased to see the usage of the centralised database hosted on a server at Vienna. Given the importance of the database content the committee recommends the implementation of an additional backup which is geographically well separated from the database server and its backup.

5.2 Mechanics

5.2.1 Status

The committee is pleased with the substantial progress reported in the development of the SVD mechanics and assembly procedures. Since the focused review in November 2014 and the 9th BPAC meeting in January 2015 many design alternatives have been explored and design questions have been resolved. Furthermore, crucial tests of components have led to some new design features.

Approval of Revision 2.4 of the SVD mechanics has enabled commencement of ladder production. This revision includes final designs of the ladders, cooling pipe routings, and isolating connections of the pipes to the outside. Further design of services is now concentrated on the volume outside of the SVD.

Thermal cycling tests of the behaviour of an L5 ladder revealed issues with gluing the sensors to the ribs and with friction in the sliding swallow-tail mechanism that provides longitudinal compliance for L4, L5, and L6 ladders. During thermal cycling, sensors became detached from the ribs. This issue was corrected with a revised gluing procedure. Furthermore, an endoscope was purchased to enable immediate inspection of the glue joints. Adjustment of the sliding mechanism reduced the friction to a tolerable level. The resulting ladder performed well under thermal cycling with differential expansions that are thought to be larger than those likely to be encountered in Belle II. To maintain quality control of the sliding mechanisms, all will be assembled and adjusted under supervision of the designer and the resulting devices will be approved by him.

Vibration tests of a nonfunctional but mechanically precise L5 ladder revealed no resonances below 100 Hz.

Studies revealed two potential points of collision between ladders. The L6 rib comes uncomfortably close to a L5 cooling tube clamp. This issue was addressed by a small notch in the L6 rib. Finite element analyses reveal that this notch does not have a significant impact on ladder stiffness. Also, two cooling tube clamps in adjacent L4 layers are too close. This potential problem was addressed by a modest reduction in the thickness of one of the clamps.

With cooling pipe routing and isolating connections fixed, two remaining cooling pipe issues were discovered:

(a) Inserting the cooling pipes into the plastic clamps required enough force to result in an uncomfortable ladder deformation of about 0.5 mm. This problem was solved by a cleverly-designed tool that holds the clamp while pressing the tube into the clamp. Hence, all forces are local to the cooling tube and the clamp, so the ladder does not need to provide any force to oppose the insertion force.

(b) The cooling pipe routing requires 3D bends, with U turns to route the pipes back and forth along the lengths of the ladders and bending the U turns in the third dimension to enable the pipes to lie on an approximately cylindrical surface to match the patterns of the ladders in the x-y plane. The first 3D bending attempts were not entirely satisfactory. Two options are being considered to address this issue.

On the other hand, a pressure test confirmed that U turns do not compromise the structural integrity of the cooling pipes; a L6 cooling pipe with 7 U turns survived a water pressure test at 300 bar with no ill effects.

The design of the SVD mounting structure is now essentially final and many crucial aspects of the design have been verified in test assemblies. Three end rings (for L3 and L4 combined, L5, and L6) and end flanges to secure the carbon fibre cones to the CDC will be glued to carbon fibre support cones. A system of precision jigs is used to align the end rings and end flange when they are being glued to a carbon fibre cone. A carefully chosen glue is used to fill the gaps between rings and the cone to accommodate precision alignment of the rings and flange to the cone which is manufactured with less precision. This system has already been tested successfully on two half-ring, half-cone assemblies and the lessons learned will be applied to the construction of final full-ring, full-cone assemblies. Carbon fibre half-cylinders glued to aluminium half-rings will provide the mechanical connection between the forward and backward support cone assemblies and seal the VXD volume from the atmosphere.

Special jigs are being designed to mount the ladders to the end cone assemblies. A prototype jig for L6 has been produced and utilised in test assemblies. Experience with this jig has provided information for a detailed plan with milestones for assembly of the SVD when components become available.

5.2.2 Concerns

Tight communication with the PXD group in finalising assembly procedures is essential, but from the discussion at the meeting it appeared there is no formal body responsible for the PXD-SVD interface.

The half-shell test will be the first time that ladder performance will be evaluated with the final cooling pipe and high-pressure evaporative cooling. This is a critical test before the integration, but no detailed plan for the tests nor the equipment was discussed during the meeting.

5.2.3 Recommendations

1. As already mentioned previously, Item 3 of Section 3.2.3 Recommendations in Page 11, a very useful step forward would be the introduction of a VXD coordinator to ensure communication between the SVD and PXD groups in finalising assembly procedures and in the actual assembly.

2. The setup for the half-shell test before integration should be designed taking into account all aspects of detector safety, in particular implementation of dew-point control and appropriate interlocks.

5.3 Readout and Control

5.3.1 Status

The full readout chain of the SVD system, from the front-end hybrid to the central DAQ system, has been working and was tested for the test-beam at CERN in 2014.

Recently two major modifications were applied to the system:

(a) The Flash-ADC (FADC) board was redesigned from V2 to V3. There are two Altera FPGA chips on the FADC board: Stratix FPGA as a core FPGA and Cyclone FPGA as a VME interface. The Stratix FPGA is configured from the VME bus via the Cyclone FPGA. Independent watchdog programs are running on both FPGAs and require asynchronous VME access. The firmware on both FPGAs was also unnecessarily complicated, leading to redesign of the new FADC V3. The only function of Cyclone FPGA is to configure Stratix FPGA and all the other functions are implemented to be performed from VME bus to Stratix FPGA directly.

(b) To improve reliability and long-term stability of the FADC board, daughter boards for the signal level transition and one for the Stratix FPGA are removed and soldered directly on the main board.

Careful tests for Electromagnetic Compatibility (EMC) was performed in a dedicated laboratory in ITA Spain (May 2015). The full readout chain including a Layer-5 ladder, copper cables, FADC and power supplies were placed and responses of the chain to the induced noise on the power line was monitored by the data taken by the FADC system. As a result, a noise vulnerability was found and two actions were taken. The former was to introduce a noise filter to the CAEN power supply and it has already been implemented. The latter is the change of one of the capacitors from 10 nF to 100 nF to mitigate the induced noise. This resulted in sizeable improvements and the modification of all existing PCB hybrids is foreseen.

For slow-control, the SVD is adopting a common framework with the PXD, which is largely based on EPICS on the software side. Given the many similarities in the software and monitoring tasks, this is a very reasonable and effective approach. Other general comments relevant also for the SVD are made in Section 3.3 and Section 4.3.

5.3.2 Concerns

The schedule for the mass-production of the FADC system is summarised as follows. The first important milestone is the test-beam at DESY with the redesigned FADC system V3 in April 2016. Manufacturing of the last prototype V4 is planned to be in May. After the final test of V4 in June, mass production of the FADC (V4.1) will follow for three months starting in July. The schedule towards final production looks reasonable but tight.

During the meeting it was mentioned that, in case of problems, a fall back on V2 is still possible. Given the kind of improvements foreseen in the new versions and the decision to upgrade the software for the board design this solution is not desirable. This adds pressure on the schedule for completion and on the need to have a complete qualification of the new version.

On the slow control the only concern is the careful validation of all communication channels between the EPICS framework of the SVD and external (SuperKEKB and Belle II NSM) systems. The team is of course well aware of this, but this should be a main concern during commissioning.

5.3.3 Recommendations

1. Detailed test items and procedures as well as software and hardware used for the tests need to be developed well in advance for testing the FADC boards.

2. A test and debugging system able to qualify the electronics should be built, in parallel with the system test with test beam.

3. Attention should be given to the manpower needed for the parallel development of the electronics test system, the ladders assembly, and the preparation for the DESY combined test beam.

4. Replacing the decoupling capacitors of the PCB hybrids should be performed with high priority, in collaboration with the QCG.