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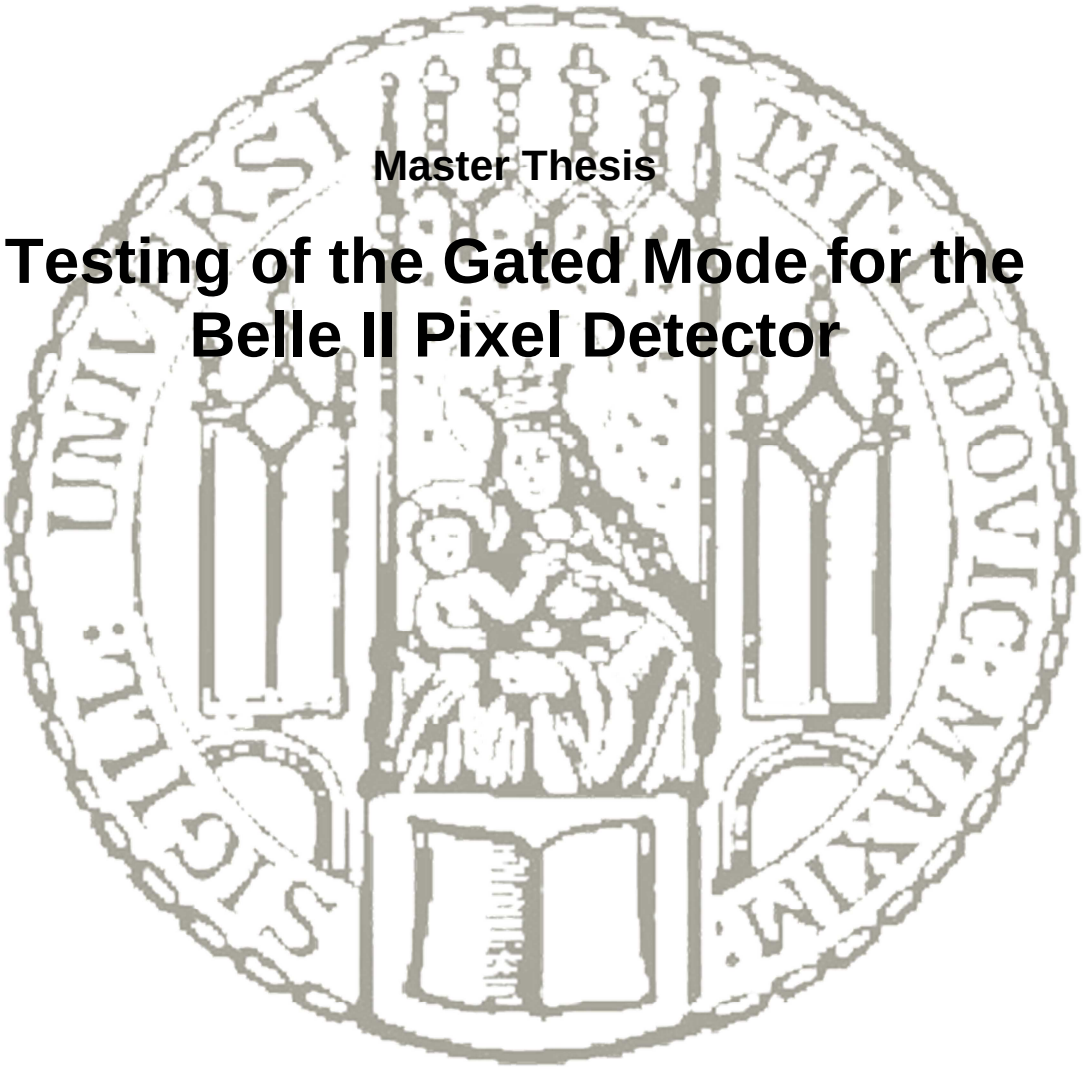

Master Thesis

Testing of the Gated Mode for the Belle II Pixel Detector

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Abstract

DEPFET pixel sensors offer intrinsic amplification, low mass and a very high signal to noise ratio. They form an integral building block for the vertex detector system of the Belle II experiment, which will start data taking in the year 2017 at the new SuperKEKB electron-positron collider in Japan. The particle bunch currents have a rather short lifetime in the order of 10 minutes. To keep the significantly increased luminosity of the collider constant over time, the bunch currents have to be topped off by injecting daughter bunches at a rate of 50 Hz. The particles in the daughter bunches produce a high rate of background ("noisy bunches") for a short period of time, saturating the occupancy of the sensor. Operating the DEPFET sensor in a so far unexplored new mode ("Gated Mode") allows preserving the signals from collisions of normal bunches while protecting the pixels from background signals of the passing noisy bunches. A special test board (Hybrid 4.1) is used, which contains a small version of the DEPFET sensor with a read-out (DCDB) and a steering chip (SwitcherB) attached, both controlled by a field-programmable gate array (FPGA) as the central interface to the computer. Experimental results presented in this thesis demonstrate that the Gated Mode can be efficiently operated at full target operation speed of 320 MHz.

Zusammenfassung

DEPFET Pixelsensoren zeichnen sich insbesondere durch ihre geringe Masse und ein hohes Signal/Rausch-Verhältnis aus. Sie bilden einen integralen Bestandteil des Belle II Vertex-Detektor-Systems am SuperKEKB Elektron-Positron-Beschleuniger in Japan, dessen Fertigstellung für 2017 geplant ist. Um die vorhandene, stark gestiegene Luminosität des Beschleunigers aufrechtzuerhalten, müssen die Teilchenpakete, deren durchschnittliche Lebensdauer ungefähr 10 Minuten beträgt, regelmäßig erneuert werden. Konkret werden alle 20 Millisekunden zwei zusätzliche Teilchenpakete in den Beschleuniger eingespeist. Die neu injizierten Teilchen verursachen zwischenzeitlich ein hohes Hintergrundrauschen. Dadurch stellen sich die Detektoraufzeichnungen als stark verzerrt und somit unbrauchbar dar. Eine spezielle Betriebsweise des DEPFET Sensors, der sogenannte „Gated Mode" ermöglicht es, dass bereits aufgezeichnete Signale erhalten bleiben und keine kontaminierte Ladung die Detektoreffizienz beeinträchtigt. Der Testaufbau umfasst eine spezielle Leiterplatte (Hybrid 4.1). Darauf sind alle wesentlichen Elemente des Belle II Pixeldetektors wie DEPFET Sensor, Auslesechip (DCDB) und Steuerungschip (SwitcherB) installiert. Ein zwischengeschalteter Field Programmable Gate Array (FPGA) – ein programmierbarer Schaltkreis der Digitaltechnik – dient als Verbindung zum Computer. Experimentelle Ergebnisse dieser Masterarbeit lassen darauf schließen, dass der Gated-Mode-Betrieb auch bei der geplanten Zielfrequenz von 320 MHz ausgezeichnet funktioniert.

Contents

1 Introduction

Citius, altius, fortius, this principle not only governs the Olympic spirit but can also serve as a guideline for particle colliders. In spring 2015 after a two years break the LHC was upgraded to almost its full specified center of mass energy at 14 TeV. The electron positron community on the precision frontier will answer in 2017 with an upgrade of the KEKB collider ("Super-KEKB") at the KEK laboratory in Tsukuba (Japan).[1] This collider will deliver an unprecedented luminosity of almost $10^{36}/cm^2$ and feature highly innovative technologies. Besides the revolutionary nano beam scheme a new ingenious DEPFET pixel detector ("PXD"), characterized by very low mass and internal amplification, will be inserted into the upgraded version of the Belle detector ("Belle II"), fitting perfectly the increased challenges. However, the thin DEPFET pixel sensors have to be read out sequentially row by row, resulting in a readout time of 20 µs, which corresponds to two full turns of the particle bunches in the SuperKEKB rings. The continuous beam injection scheme of SuperKEKB implies for the PXD, that about 20% of all recordings should be spoiled by the huge background originating from the "cool down" of the injected daughter bunches ("noisy bunches"). This would mean a high waste of time and resources. Various scientific studies proved that DEPFET detectors are in principle capable of shielding or gating the sensor during the passage of the daughter bunches. The objective of this thesis is to optimize the Gated Mode operation so that it can be used at the full target frequency of 320 MHz.

Chapter 2 gives an overview of the physics pursued at "B-Factories" and motivates their benefits. Also the Belle II detector system and some beam peculiarities of SuperKEKB are briefly explained. Chapter 3 introduces the DEPFET detector together with its connected electronics and explains its working principles and special features including the Gated Mode. Chapter 4 describes the necessary components for the test setup whereas chapter 5 outlines a detailed test plan for the Gated Mode operation. Without properly operating electronics there is no way of getting meaningful findings. Therefore chapter 6 deals with the characterization of the readout chip and the determination of the optimal settings. Additionally, the conversion algorithm is explained and several potential error sources are investigated. Chapter 7 describes the data acquisition system and the programming of the test sequences in conjunction with a discussion to shed some light on the understanding of the digital strobe logic. Next the calibration method for the detector's output is illustrated and different Gated Mode sequences are evaluated. The results and conclusions are included in chapter 8 and 9, respectively. In order to facilitate the fluency of reading some terms marked in **bold** are not explained in the text but in the glossary at the end of this thesis.

[1] and yet there are ongoing discussions for two Future Circular Colliders (FCCs), a proton-proton collider with a center of mass energy of 100 TeV and 80-100 km circular tunnel, as well as a >350 GeV high luminosity e^+e^- machine [116], besides two possible linear colliders, the ILC (at 500 GeV) [117] and CLIC (up to 3 TeV) [118]

2 Physics at Belle II

2.1 Basic Motivation: benefit of a Super Flavor Factory (SFF)

In 1972 Makoto Kobayashi and Toshihide Maskawa, two Japanese physicists, proposed a new scheme of the weak interaction of quarks, explaining the CP violation observed in the quark sector by Cronin and Fitch in 1964 [1]. This scheme postulates a CP violating phase and requires three families of quarks in the quark mixing matrix although at this time only three quarks (u, d and s) were known. The observed presence of CP violation in the B-meson system, detected by the BaBar[2] and Belle experiments, was an important confirmation of this hypothesis, awarding Kobayashi/Maskawa the Nobel Prize in Physics in 2008.

The name “Belle” stands for both an experiment in **flavor physics** conducted by the Belle collaboration and a detector system located at the collision point of the e^+e^- asymmetric energy collider, known as KEKB, in Tsukuba (Japan). The confirmation of the Kobayashi-Maskawa mechanism now widely accepted as the dominant source of CP violation in the Standard Model of particle physics (SM) was not the only outcome of the successful Belle experiment. Especially worth mentioning is the unprecedented precision with which the magnitudes of the CKM matrix elements and the angles of the unitarity triangle were extracted [2].

Nevertheless several fundamental questions in particle physics remain unanswered. Let me shortly describe a few of them: From the hot Big Bang model [3] one might expect that the universe consists of equal parts of matter and antimatter. However, the observed baryon asymmetry in the universe is by order of 10^8 higher than predicted by SM. While CP violation is an integral part of the SM framework and one of the so-called **Sakharov conditions** for a matter dominated universe, the magnitude of the asymmetry cannot be explained. A further mystery remains the cosmic observation of dark matter inferred from gravitational effects[3] on visible matter, cosmic microwave background analysis and the large-scale structure of the universe.

The recent discovery of a new particle with properties consistent with the SM Higgs boson at LHC was accommodated with great relief and big celebrations. Nevertheless the Higgs boson’s mass is expected to be much heavier near the Planck scale [4]. Since the Higgs potential contains a term in the SM Lagrangian with quadratic mass divergence this means that the Higgs mass of $\mathcal{O}$(100 GeV) materializes only after a huge cancellation between the bare Higgs mass and the quadratic divergent mass renormalization [5]. This is often called the hierarchy problem occurring when funda-

[2] BaBar represents an international collaboration of physicists located at SLAC National Accelerator Laboratory, operated by Stanford University for the Department of Energy in California

[3] evidenced by galactic angular velocity distributions, gravitational lensing and galactic collisions

mental parameters of some Lagrangian are vastly different than the parameters measured by the experiment, in other words: the Higgs boson is much too light. One would expect that the large quantum contributions to the Higgs boson mass would inevitably make the mass huge, comparable to the scale at which new physics appears, unless there is an incredible fine-tuning cancellation between the quadratic radiative corrections and the bare mass. As an example let us use a top quark fermion loop for calculating the Higgs boson mass [6]:

$$m_H^2 = m_0^2 - \frac{|\lambda_t|^2}{8\pi^2}\Lambda^2 + \mathcal{O}\left(ln\frac{\Lambda^2}{m_t^2}\right)$$

mass Higgs boson	*Higgs mass in 1st term of Lagrangian*	*λ_t t-quark Yukawa coupling*	*scale up to which SM is valid (e.g. GUT-scale≈10^{15} GeV)*	*m_t mass of t-quark*
what we measure	***free parameter***		***theory cutoff***	***much smaller than Λ^2***

Contributions from other fermions can be neglected. If we take for Λ^2 the GUT scale then m_0, the uncorrected mass of the Higgs boson has to be determined with an accuracy of 24 digits in order to calculate a Higgs mass of 100 GeV associated with the first and second term from the SM Lagrangian (right part of the equation). It's hard to believe that such a fine-tuning is provided by nature.

A further phenomenon currently not fully understood is related to the hierarchy of the CKM and the neutrino/lepton mixing matrix (PMNS) elements as shown in Figure 2-1. This again puzzles many physicists and points to some yet undiscovered mechanism existing at higher energy scales.

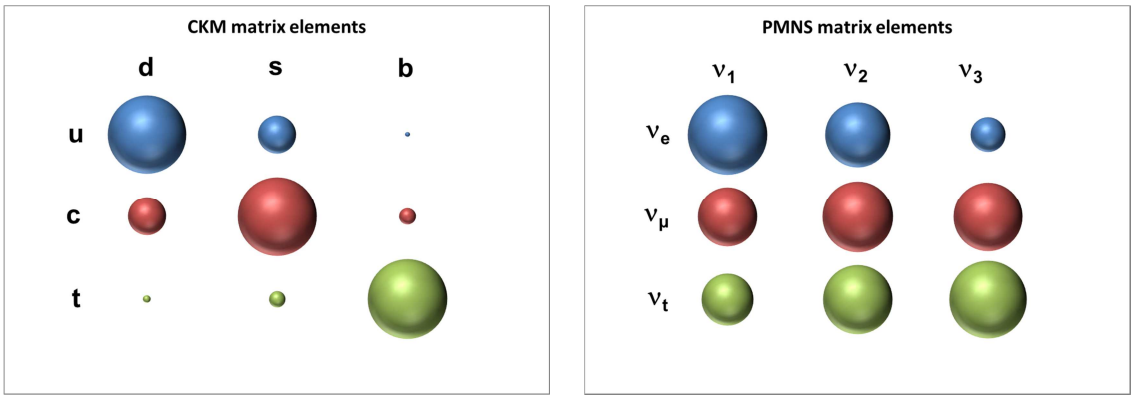


Figure 2-1: different weightings of CKM & PMNS matrix elements [7, 8]

In order to make considerable progress the Belle II collaboration is planning an upgrade for both the detector system and the collider[4] going live in 2017. With the emergence of the LHC operating at the TeV energy scale one might question the benefit of such Super Flavor Factories (SFF) [5] with energies still well below 100 GeV reaching not

[4] now called SuperKEKB

[5] often also referred to as B-Factories

even the mass of the Higgs particle quite recently detected. Moreover since the LHCb experiment is also studying flavor physics at much higher b-cross sections, it is understandable that for laymen in particle physics there are at least some doubts about the effectiveness of such enterprises. To answer these apparent inconsistencies one has to consider the goals pursued by the different approaches. The LHC is looking for new physics (NP) particles in high energy experiments by increasing the available center-of-mass energy whereas Belle II rather operating on the precision frontier would provide complementary constraints on the combination of couplings, mixing angles and NP masses [9].

If direct searches for NP are successful (e.g. Supersymmetry) flavor experiments will deliver essential information to identify the kind of NP sensitive physics [10]. One of the most efficient ways achieving this goal is the comparison of the determined CKM parameters with SM predictions. This can be achieved by putting all experimentally obtained data together and applying a best-fit-algorithm[6]. Again one can imagine that these fits depend heavily on detailed calculations of the effects of radiative corrections. The main radiative effects arise from the influence of loop diagrams involving virtual heavy particle exchanges. Most of the performed measurements are related to specific regions in the $\overline{\rho} - \overline{\eta}$ plane as shown in Figure 2-2.

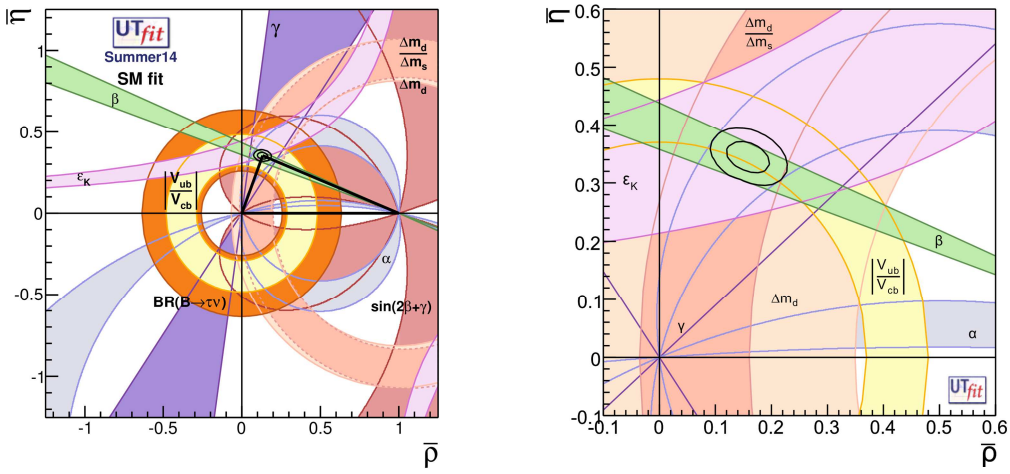


Figure 2-2: Left: Regions corresponding to 95% probability for the CKM parameters $\overline{\rho} - \overline{\eta}$ selected by different constraints, assuming present central values (summer 2014) with present errors. Right: zoomed in diagram representing 2007 fitting results.

Note that from the right plot of Figure 2-2 one can infer, that the uncertainty area was already small and a bold step towards increased integrated luminosity is needed to detect small deviations from the SM. This would dramatically change by placing a SFF into operation. In Figure 2-3 (left) based on 2007 data the validity of the SM is assumed applying the expected precision of a SFF. Going one step further and taking the current

[6] currently two organizations take care of that: UTfit and CKMfitter with different statistical approaches (bayesian vs. frequentist approach) but there are also other methodologies like the Scan-Method [93]

world averages for all parameters with the expected precision of a SFF this diagram would have transformed to a paradigm of NP.

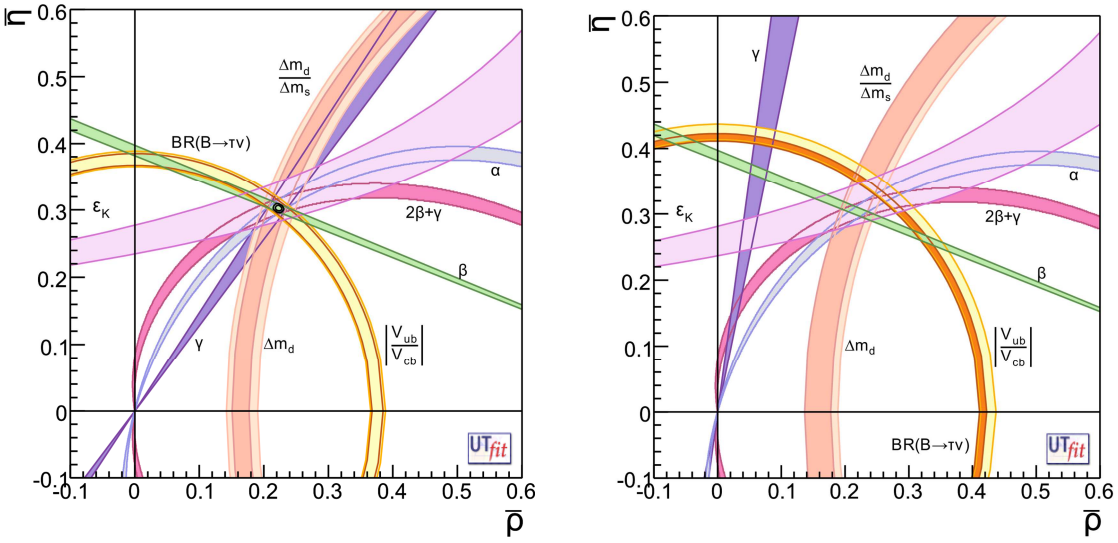


Figure 2-3: Left: Regions corresponding to 95% probability for the CKM parameters $\bar{\rho} - \bar{\eta}$ selected by different constraints, assuming 2007 central values with errors expected at a SFF tuning central values to have compatible constraints. Right: assuming present central values with the precision of a SFF [11].

As an important tool for finding physics beyond the SM, flavor physics probes large mass scales via virtual quantum loops. FCNC, neutral meson-antimeson mixing and CP violation typically occur at the loop level in the SM. Precise measurements could potentially induce small NP virtual corrections. Hence this approach is also called indirect search for it infers NP through virtual contributions of new particles in processes involving only standard particles. It is based on high-statistics muon, kaon, tau, charm and B-meson production as well as precise measurements of SM parameters providing different constraints to individual processes. Experiments always measure the sum of SM and NP contributions. In order to set limits or to extract signals from NP it is indispensable to fully understand the underlying SM contribution. A widely accepted paradigm is that tree-level diagrams are dominated by SM processes, whereas loop diagrams can be strongly influenced by NP [12]. An example is given in Figure 2-4.

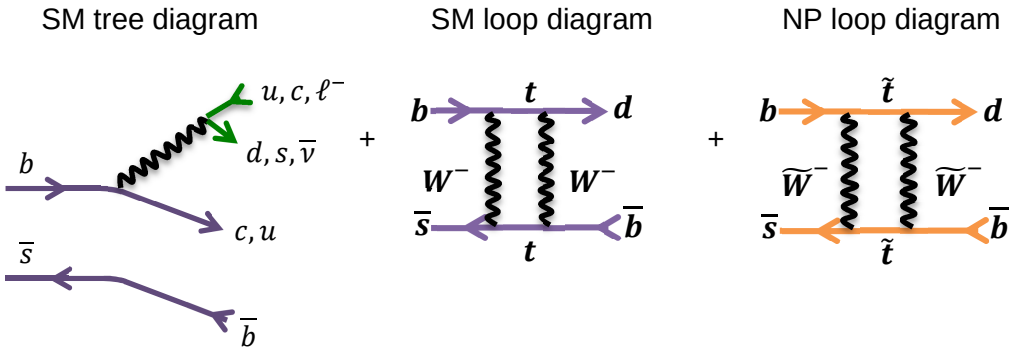


Figure 2-4: Example of an SM standard process and 1st order loop corrections

Both loop diagrams would add in the amplitude and hence interfere. The inclusion of NP particles with mass exchanged at the tree level with $\mathcal{O}(1)$ coupling constants g_{NP}/g would go well beyond the LHC energy scale [9]. Even if NP particles are exchanged only at 1-loop order the mass reach can be as high as $\mathcal{O}(1\text{TeV}/c^2)$ if **minimal flavor violation** (MFV) is assumed [13], and up to $\mathcal{O}(100\text{TeV}/c^2)$ if flavor violation couplings are enhanced compared to the SM [11]. The scope of the two approaches in searching for NP is depicted in Figure 2-5.

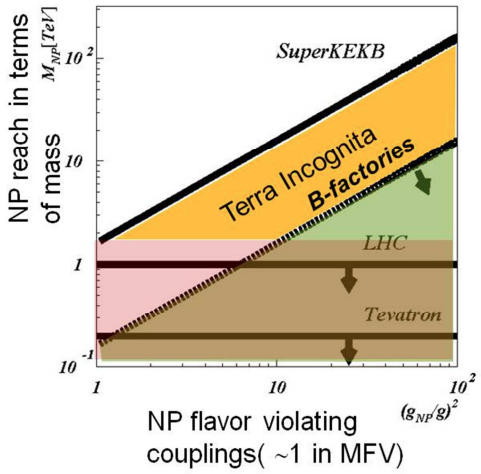


Figure 2-5: Sensitivity to New Physics as a function of the flavor violating couplings relative to the SM in the indirect searches at KEKB/SuperKEKB and direct searches at LHC/Tevatron [14].

In general if NP appears at the TeV scale in LHC experiments, SuperKEKB could measure its flavor- and CP-violating couplings or set independent constraints on the NP Lagrangian [15]. A comparison of SuperKEKB with **LHCb** unveils that the strengths of the two experiments are largely complementary [9]. At LHCb the expected yield for decay processes like $B \rightarrow K^*\mu\mu$, $B_s \rightarrow \phi\phi$ and $B \rightarrow \phi K_s$ should be substantially higher [16] because of the very large production cross section for b-quarks. This allows for example, extensive studies on B_s meson oscillations. On the other hand SuperKEKB provides a much cleaner environment which is essential for the exact measurement of CKM matrix elements, rare decay modes with missing energy as well as other searches for possible NP effects [2].

Colliders at Super Flavor Factories can form specific particles or their excitations without any associated particles in the form of resonances. As an example at the $\Upsilon(4S)$ resonance $B\overline{B}$-pairs are generated. This allows the full reconstruction of a B meson from its daughter particles. By this means one can infer the missing momentum attributed to the other B meson, which in turn is essential for the measurement of channels including neutrinos in the final state.

2.2 BELLE II Detector System

Detectors employed in high energy physics experiments normally incorporate several types of detection techniques into one single detector system [17]. The Belle II detector system in Figure 2-6 shows also a general purpose spectrometer consisting of layers of sub-detector components, each designed to look for particular properties or specific types of particles, arranged in the typical “onion shell”-fashion [18, 19]:

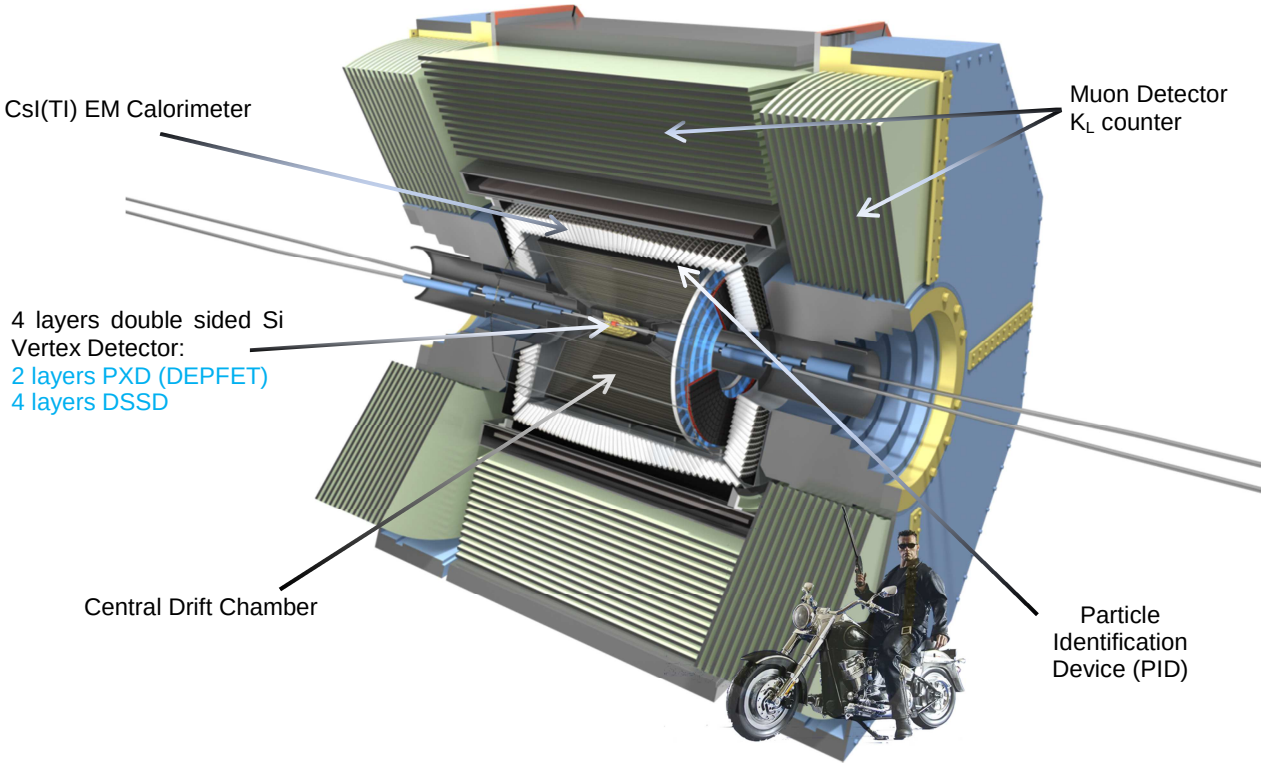


Figure 2-6: Belle II Detector System

There are tracking devices recording position, arrival time and path of a particle, calorimeters that measure a particle’s energy, and particle-identification detectors using a range of techniques to pin down a particle's identity.

- *VerteX Detector (VXD):* positioned most closely to the beam pipe there are two layers of Pixelated Silicon Sensors (PXD) adjacently followed by four layers of double-sided Silicon Strip Sensors (SVD). Together this sub-system measures decay vertex positions with a combined impact parameter resolution of σ_{z_0} ~ 20µm [19]. The precise evaluation of position coordinates is necessary for the determination of the particle’s trajectory origin. These tracking detectors register tiny electrical signals that particles create traversing the detector. From the deflection in a magnetic field the particle’s momentum can be derived. One of the main concerns for the Belle II collaboration is the detector performance in an environment with considerable higher background levels. Conservative estimates assume that the background hit rate will increase by a factor of 20 whereas the physical event rate will be about 50 times higher. In this respect

the addition of a pixel detector is essential since results from current flavor factories have proven high precision vertex reconstruction as a powerful tool to measure CP violation observables [20].

- *Central drift chamber (CDC):* the VXD is surrounded by a small-cell drift chamber (r = 16 – 112 cm) which measures trajectories, momenta and dE/dx information of charged particles. Additionally, it is used as trigger source and as a particle identification device for low momentum tracks.

- *Particle Identification Device (PID):* located just outside of the CDC in the barrel and end cap regions and principally[7] designed to improve the K/π separation capability of the detector [10]. They are of the **Cherenkov** type with very fast read-out electronics. In the barrel region the formerly used ARICH counters are replaced by Time-Of-Propagation (TOP) counters allowing to measure the propagation time of the Cherenkov light emitted from charged particles passing through quartz radiator bars. In order to identify charged particles over the full kinematic range this detector sub-system also includes a forward end cap RICH with an aerogel radiator.

- *Electromagnetic calorimeter (ECL):* photons generated by e^+e^- collisions at the $\Upsilon(nS)$ energy regime span a wide energy range from 20 MeV to 4 GeV, hence a high resolution electromagnetic calorimeter is essential for the precise determination of the photon energy and angular coordinates. It contains a total number of 8736 CsI(TI)-scintillator crystals with different shapes in the barrel and end cap region located inside a *Superconducting Solenoid Coil* that provides a 1.5 Tesla magnetic field.

- *K_L/Muon (KLM) Detector:* the outermost detector sub-system is instrumented to detect K_L^0 mesons and to identify muons. It consists of an alternating “sandwich” of 4.7-cm thick iron plates[8] and glass-electrode **Resistive Plate Chambers** (RPC) in between. Since RPCs in the innermost layers of the KLM detector show unsatisfactory performance in the end cap region because of the expected high background, they are replaced with scintillators.

There are many other factors influencing the performance of the Belle II detector system. Especially worth mentioning are a fast and reliable Triggering scheme (TRG), a Data Acquisition system (DAQ) recording collision events of interest upon trigger level-1 and a grid-based distributed computing facility for data processing, MC production and physics analysis.

[7] Providing also discrimination between pions, kaons and electrons below 1 GeV/c

[8] serving as stopping material and as the magnetic flux return for the solenoid

2.3 SuperKEKB injection scheme

2.3.1 Principles of particle acceleration

In order to accelerate particles in a synchrotron and to compensate for energy losses due to the emission of synchrotron radiation a longitudinal electric field is needed. Radiofrequency (RF) cavities[9] along the beam pipe use an oscillating voltage, so the particle senses an accelerating electrical field in the cavities. To ensure that a charged particle always receives an accelerating force within the cavity, the RF frequency must be an integer multiple of the particle's revolution frequency [21]:

$$h(integer) = harmonic\ number = \frac{RF\ frequency}{revolution\ frequency} \qquad (2\text{-}1)$$

At SuperKEKB the planned RF frequency basis clock is 508.89 MHz. With a circumference of 3 km the harmonic number for electrons at the speed of light gives about 5120 points.[10] The segments of the circumference centered on these points are called RF buckets. Electrons within the RF buckets get lumped into bunches.[11] Each bunch consists of 10^{11} positrons or electrons. The particle density within a bunch is not homogeneous but looks like a 3-dimensional Gaussian distribution.

The electrons in a bunch oscillate longitudinally around the equilibrium position, keeping the longitudinal size of the bunch stable. These oscillations are called synchrotron oscillations [18].

The electrons and positrons are guided in SuperKEKB by magnetic dipole fields around circular orbits, but move sinusoidally in both horizontal and vertical planes under focusing magnetic quadrupole fields around the design orbit. These periodic lateral movements are called **betatron** oscillations.

2.3.2 Beam Parameters increasing Luminosity

SuperKEKB is an asymmetric e^+e^- collider with a planned target luminosity of $\mathcal{L} = 8x10^{35}cm^{-2}s^{-1}$, about 40 times as high as its predecessor KEKB [22, 23]. The range of beam energy covers the $\Upsilon(1S)$ and $\Upsilon(6S)$ resonance states for the physics operation. By definition luminosity[12] is related to the rate of particle collisions, consequently it is crucial for the production of meaningful quantities of rare events. The number of detected events N depends on the process cross section σ usually measured in femto-

[9] metallic chambers containing an electrical field in order to accelerate charged particles

[10] with this number one can calculate the bucket length of ≈59 cm, which has to be compared with a bunch length of just 5-6 mm at SuperKEKB

[11] this represents also an upper limit for the number of bunches within the collider (at Belle II only every second bucket gets filled with electrons resulting in 2503 bunches altogether)

[12] luminosity can be interpreted as the beam focusing ability of the machine at the interaction point

barns[13] (fb) or picobarns (pb), the luminosity $\mathcal{L}$ controlled by the beam parameters of the collider and the detector efficiency ϵ including trigger efficiency:

$$\frac{dN}{dt} = \mathcal{L} \cdot \sigma \cdot \epsilon \tag{2-2}$$

The event rate N_{ev} of a specific process is given as:

$$\frac{dN_{ev}}{dt} = \mathcal{L} \cdot \sigma_{ev} \cdot Br \cdot \epsilon \tag{2-3}$$

where Br is the branching ratio, i.e. the fraction of events for a chosen particle measured to decay in a certain way[14] and σ_{ev} the cross-section dependent on the specific physics process only. Unfortunately with higher luminosity new phenomena emerge at the interaction point (IP) [24]: dynamic beta effects and disruption are just some of them and will not be further covered in this thesis.[15]

In common textbooks luminosity for two transverse Gaussian beam distributions colliding head-on with equal beam sizes is defined as

$$\mathcal{L} = \frac{f N_1 N_2}{4\pi \sigma_x^* \sigma_y^*} \tag{2-4}$$

where f is the bunch collision frequency, $N_{1,2}$ the number of particles per bunch in beam$_{1,2}$ and $\sigma_{x,y}^*$[16] is the beam size at the IP in the horizontal and vertical plane.

When the vertical **beta functions** of both beams are equal, the luminosity can be alternatively expressed by beam parameters (2-5) [25]:

$$\mathcal{L} = \frac{\gamma_\pm}{2er_e}\left(1 + \frac{\sigma_y^*}{\sigma_x^*}\right)\left(\frac{I_\pm \xi_{y\pm}}{\beta_y^*}\right)\left(\frac{R_L}{R_{\xi y\pm}}\right) \propto \frac{\boldsymbol{I_\pm \xi_{y\pm}}}{\boldsymbol{\beta_{y\pm}^*}} \tag{2-5}$$

where the subscript $\pm$ denotes positrons and electrons, $\gamma_\pm$ is the Lorentz factor, e is the elementary electric charge, r_e is the classical electron radius, I is the beam current, $\xi_\pm$ is the vertical beam-beam parameter, $\beta_{y\pm}^*$ is the vertical beta function, R_L and $R_{\xi y\pm}$ are geometrical reduction factors for the luminosity and the vertical beam-beam tune-shift parameter, respectively, owing to the finite crossing angle and the **hourglass effect**. Other factors like the horizontal beta function at the IP, the horizontal **emittance** ε_{xy}, the bunch length and the crossing angle between two beams not directly appearing in

[13] 1 barn = 10^{-28} m^2

[14] the sum of branching ratios for a particle is 1

[15] the high density of compressed particles provides strong electromagnetic fields viewed by the particles of the incoming beam and this would bend particle trajectories (disruption)

[16] the star indicates the minimum value

the formula are contributing to the luminosity through the beam-beam parameter [26]. Table 2-1 gives an overview of some key design parameters for KEKB/SuperKEKB.

	KEKB design	KEKB with crab	SuperKEKB[17]	Unit
Energy	3.5/8	3.5/8	4.0/7.0	GeV
β_y^*	10/10	5.9/5.9	**0.27/0.3**	mm
β_x^*	330/330	1200/1200	32/25	mm
ε_x	18/18	18/24	3.2/5.3	nm
σ_x^*	100		10	µm
σ_y^*	1.9	0.94	0.048/0.062	µm
ξ_y	0.052	0.129/0.090	**0.09/0.081**	
σ_z	4	6-7	6/5	mm
I	2.6/1.1	1.64/1.19	**3.6/2.6**	A
N_{bunch}	5000	1584	2503	
$\mathcal{L}uminosity$	1	2.11	80	$10^{34}cm^{-2}s^{-1}$

Table 2-1: Comparison of some of the key parameters of the SuperKEKB and KEKB designs [25]. Figures in bold red indicate three fundamental parameters determining luminosity.

2.3.3 Nano beam scheme

From equation (2-5) one can infer that the luminosity is sensitive to only three fundamental beam parameters:[18]

- increase the beam currents $(I_{\pm})$,
- make the electromagnetic beam-beam interactions small or equivalently increase the beam-beam parameter $(\xi_{y\pm})$ which is inversely proportional to the beam emittance [27] and
- reduce the vertical beta function $(\beta_{y\pm}^*)$ which addresses the focus of the beams at the interaction point [28].

Beam currents at SuperKEKB will be doubled in comparison with KEKB thus obtaining a luminosity gain by a factor of 2. Further current increases are not recommendable because of the electron cloud effect in the positron ring, high power costs and much higher detector backgrounds.

Regarding the beam-beam parameter, experiences from various colliders show that this value is limited to about 0.02-0.1. At SuperKEKB a maximum of 0.09 is assumed which has been already achieved at KEKB.

[17] as of 2013/July/29

[18] as an intermediate step KEKB scientists have installed crab cavities kicking the head and tail of each electron bunch so that the bunches made effective head-on collisions at the interaction point instead of crossing at an angle of 1.3 degrees (crab crossing improved the luminosity by 15%)

The most important luminosity increase will be achieved with a concept called “nano beam scheme” first proposed by scientists planning for the ILC [29]. The principal idea behind the nano beam scheme is to make the bunches very flat[19] in this way raising the collision probability. At SuperKEKB the vertical beta function β_y^* will be compressed by a factor of 1/20 of KEKB to just a few hundred microns at most. The new design will need strong final focusing quadrupole magnets placed closer to the interaction region to squeeze the beam into narrower bunches. However, this cannot be done arbitrarily small because of the **hourglass effect**. To minimize the hourglass effect for conventional head-on collisions the beta function has to be larger than the bunch length ~5mm $(\beta_y^* \geq \sigma_z)$. By contrast the nano beam scheme requires $\beta_y^* \geq \frac{2\sigma_x^*}{sin\ 2\phi}$ disclosing a proportional dependence on the horizontal spot size and an inverse dependence on the half crossing angle ϕ. Accordingly the crossing angles will be substantially enlarged from 22 mrad to 83 mrad and the bunches only intersect at the highly focused regions with effective bunch length $d = \frac{2\sigma_x^*}{sin\ 2\phi}$ shown in Figure 2-7.

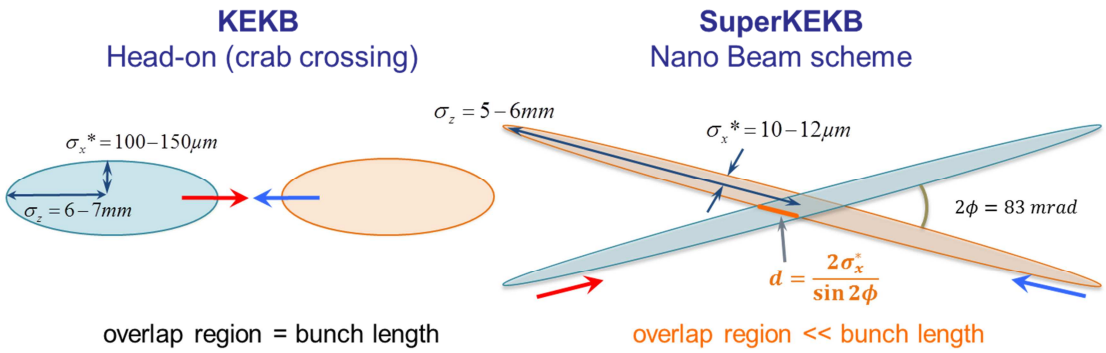


Figure 2-7: Comparison of different Collision Schemes (schematic view)

In order to implement the new scheme effectively a lot of former used items of the KEKB collider have to be upgraded [25]. First of all the lattice design, which represents the arrangement of the magnets along the beam path for guiding and focusing the electrons and positrons has to be updated. The magnet system in accelerators consists of various types like dipoles used for bending, quadrupoles used for focusing (focusing in one plane, and defocusing in the other) and sextupoles used for chromatic corrections. The combination of different magnets into building blocks constitute the lattice design resembling a complicated optical system with FODO cells (focusing & defocusing quadrupoles), double bend achromat (DBA), triple bend achromat (TBA) or other multi bend achromat types. For SuperKEKB the quadrupole magnets of KEKB will be reused as much as possible, the dipole magnets will be replaced by shorter ones and the period of the **wiggler magnets** will be reduced to half of that of KEKB by adding new ones. As already mentioned the final focus section was completely redesigned to achieve an extremely low beta function at the IP. By rearranging, replacing and adding magnets

[19] one might think of steamrolled spaghettis

the beta functions and dispersions will be modified. As a countermeasure against electron cloud issues the beam pipes in the LER arc section will be replaced with new aluminum-alloy pipes with antechambers. To reduce the emittance of the electron beam a photo-cathode RF low-emittance electron gun will be installed. The emittance of the positron beam will be minimized by a new damping ring. The overview of the upgrade to SuperKEKB is shown in Figure 2-8.

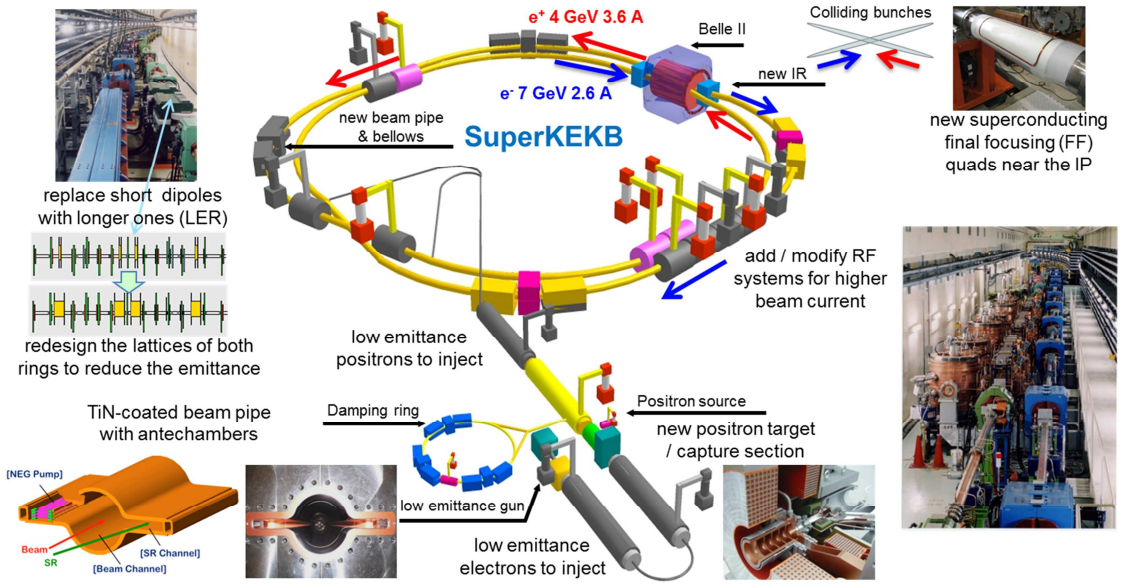


Figure 2-8: Overview of upgrade to SuperKEKB [25]

2.3.4 Beam life time and dead-time during injection

Due to various energy loss effects (see below), some of the particles deviate from the prescribed path along the vacuum tube and interact with the beam pipe thereby creating particle showers which may reach the detector. The number of particles lost in an accelerator is proportional to the number of beam particles [30]:

$$dN = -\alpha N(t)dt \tag{2-6}$$

where α is a constant. Defining the beam lifetime as $\tau = 1/\alpha$, then the beam current I decays as

$$I = I_0 \cdot e^{-t/\tau} \tag{2-7}$$

In general, beam losses mainly arise in the collimation area or on other aperture limits. Basically five beam loss processes are observable [31]: first, betatron or synchrotron oscillations intensify the quantum emission thereby increasing the tails of the bunch distribution. Next, the intra-beam scattering dominated by the **Touschek effect,** and the beam-beam background appearing at the IP when the colliding beam particles undergo scattering via radiative **Bhabha** processes. Finally, elastic and inelastic scattering with residual gas molecules in the vacuum tube.

The individual loss mechanisms contribute to the total beam lifetime as [32]:

$$\frac{1}{\tau} = \frac{1}{\tau_{quantum}} + \frac{1}{\tau_{Touschek}} + \frac{1}{\tau_{beam-beam}} + \frac{1}{\tau_{elastic}} + \frac{1}{\tau_{inelastic}} \tag{2-8}$$

As a result the total beam lifetime will always be less than the value of the smallest lifetime input. The most dominant beam loss contribution stems from the Touschek effect. The stability of the trajectories highly depends on the amplitudes of betatron and synchrotron oscillations. If these oscillations are outside the longitudinal or transverse acceptance of the storage ring the particles are lost. In this respect it is customary to define dynamic aperture as the maximum phase-space amplitude within which particles do not get lost after a certain amount of turns[20] [33]. In other words, dynamic aperture sets an amplitude threshold for the motion of charged particles. At SuperKEKB it is estimated numerically with six-dimensional tracking simulations using a specific program for optics design and particle tracking. As a result the dynamic aperture is rather small compared to KEKB inducing a larger background and consequently a shorter lifetime of the beam. The intra-beam scattering rate ("Touschek effect") per particle depends on the following parameters [34]:

$$(Rate) \propto \frac{N}{E^3 \cdot \sigma} \tag{2-9}$$

where N stands for the number of particles per bunch, E for the beam energy and σ represents the transverse beam size. As already mentioned most of the luminosity increase at SuperKEKB comes from a significant reduction of the beam size. A twenty-fold compression of the bunches significantly rises the likelihood of intra-bunch coulomb scattering. By implication this increases the amplitudes of particles that will be either absorbed at the collimation area or collide with the beam wall. Accordingly, the dominant particle loss mechanism[21] at Belle II will be the Touschek effect reducing the LER beam lifetime significantly from 150/200 min as in the KEKB case to just 10 min. As a consequence the bunches have to be replenished continuously. This is done by injecting two "daughter bunches" 100 ns apart into the LER and HER respectively at a total frequency of 50 Hz. The pair of daughter bunches are selected by bunch current monitors, and the pair with the smallest bunch current sum is chosen to be topped off in the next injection.

[20] 1000 turns at SuperKEKB with synchrotron oscillation but without **quantum excitation (radiation damping)**

[21] the loss rate due to scattering with gas molecules is lower by a factor of 3-4

Figure 2-9 and Figure 2-10 give an overview of the injection scheme for SuperKEKB with the septum magnets for bunch injection.

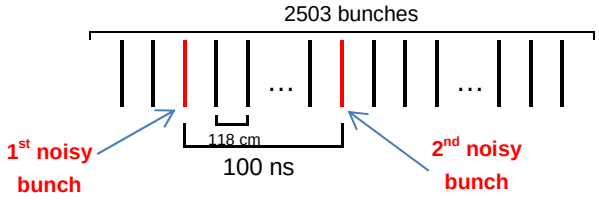
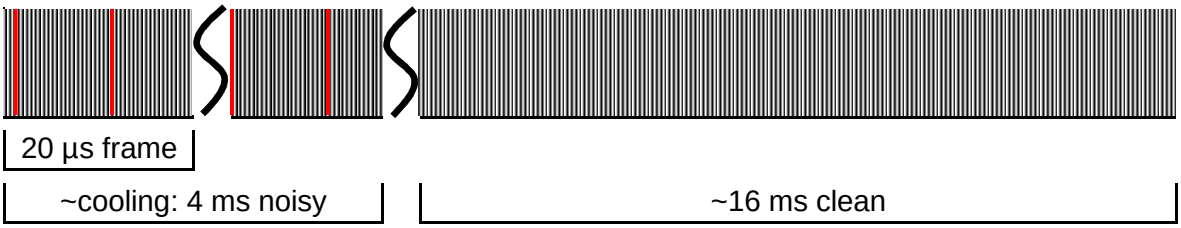


Figure 2-9: SuperKEKB bunch train.



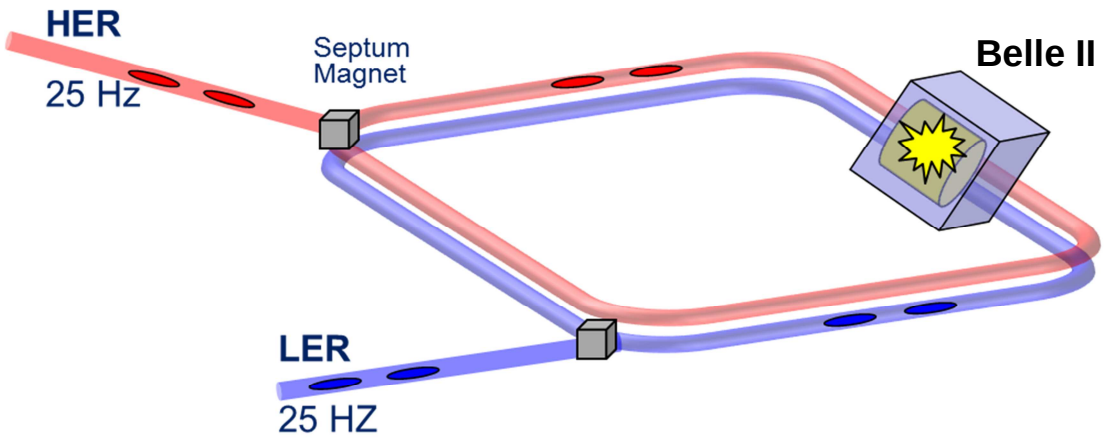


Figure 2-10: Injection Scheme of SuperKEKB

Now the problem emerges that these daughter bunches are located further away from the orbit of the corresponding main bunches and therefore are subject to large amplitudes in their betatron oscillations. They are naturally cooled down by synchrotron radiation within a certain damping time. During this time the particles in the daughter bunches are more likely to collide with the bream pipe in the vicinity of the interaction point, creating additional background. The daughter bunches are therefore often called "noisy bunches". At KEKB the damping time was 4 ms and this number will be also assumed for SuperKEKB. The noisy bunches will pass the detector every 10 µs. For the PXD (see chapter 3.5) the detector readout cycle was determined at 20 µs which means that all signals registered within the 20 µs between two readout cycles are

stored (integrated). As a worst case this would mean that all frames recorded during the cooling period have to be discarded. This would substantially raise the dead-time of the detector to 20% or in other words produce a loss of two years time assuming a typical operational period of 10 years. Many proposals have been made to overcome this problem, for example a faster read-out (4-fold ganging), decreasing the injection rate while injecting 4 bunches instead of 2, synchronize injections from LER and HER or reducing damping time. But these alternatives are either too costly or not feasible from the current technical status. Fortunately the PXD used at Belle II offers a lot of amazing features especially the possibility to gate the detector during the passage of the noisy bunches. Its modalities, operation principles and the design will be described in the next section.

3 DEPFET Sensors

Flavor physics sets high standards on precision measurements requiring a spatial resolution of a few ten of microns in order to measure the decay vertices of the two B mesons produced at the $\Upsilon(4S)$ resonance. At Belle II a specific condition for detector resolution is the measurement of the decay time difference of the B meson and its antiparticle, expressed in their mean flight distance of $\Delta z \approx 130\ \mu$. A derivation of this figure can be found in the Appendix A.

To safely distinguish two different vertices the vertex resolution has to be one order of magnitude better than the distance between the vertices [35]. Only silicon detectors can meet the challenge of acceptable resolution combined with a fast readout. However, the double sided silicon strip detector (DSSD) as innermost detector used for Belle cannot cope with the much higher event rate at SuperKEKB together with the higher background[22], which would lead to a large strip **occupancy** making vertex reconstruction of B-decays impossible. For that reason it was decided to upgrade the new Belle II detector system with a pixel detector. The combined PXD and SVD **impact parameter** resolution at Belle II will be at $\sigma_{z_0} \approx 20\ \mu m$.

There are fairly different pixel detector architectures under consideration all having advantages and drawbacks [36]. CCDs suffer from relatively slow read-out speed and continuous sensitivity distorting the measurements during the transfer cycle. In contrast hybrid pixels used for the ATLAS detector at CERN are very fast (25 ns read-out speed) but with their thick sensors and chip-integrated full read-out electronics they are too bulky for energy levels in the $\mathcal{O}(1GeV)$area (multiple scattering because of relatively low particle momentum). A very promising and highly innovative technology are monolithic active pixel sensors (MAPS) incorporating standard CMOS technology in a p-type epitaxial layer on a high resistive n-type substrate [37]. Because of their low intrinsic capacitances these devices have excellent signal to noise ratios. On the other hand the charge collection times are still too long. Nevertheless the idea of integrating readout electronics into a single monolithic device will influence the construction of detectors in future high energy experiments. In contrast DEPFET detectors seem to be actually best-suited for high precision vertex pixel detectors [38]. They avoid most of the above shortcomings having low mass and offering intrinsic amplification and adequately fast readout times. Furthermore power consumption can be kept very small saving additional cooling material.

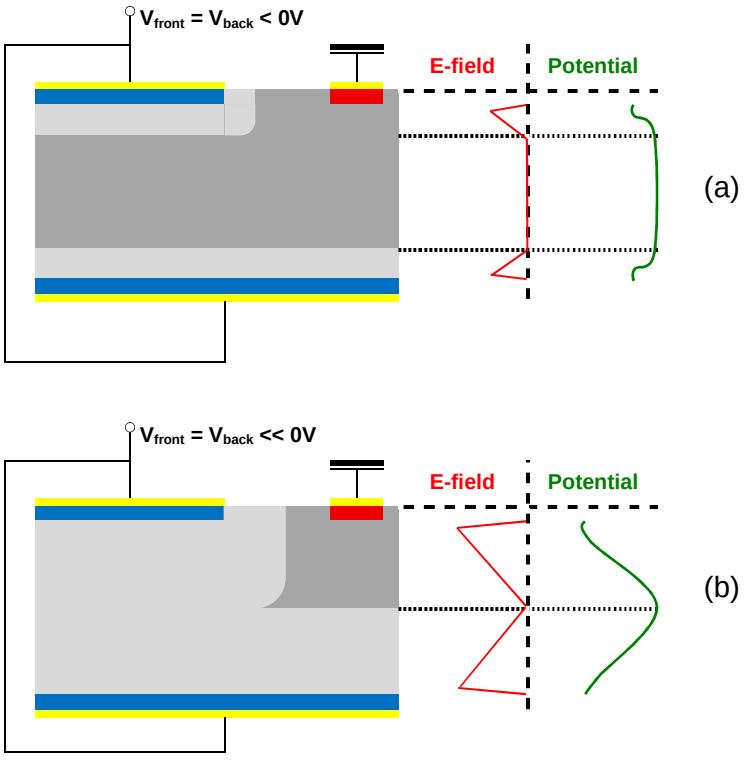
[22] the beam pipe radius shrinks to about 10 mm, so the detector can be put closer to the IR, which is good news for vertex reconstruction; on the other hand the background increases substantially since is proportional to the inverse square of the radius

3.1 DEPFET Operation

3.1.1 The DEPFET Principle

The idea for DEPFET detectors was proposed by two Munich scientists J. Kemmer and G. Lutz in 1987 [39]. The technology was developed by the Semiconductor Laboratory (HLL) of the Max Planck Society in Munich. DEPFET detectors integrate signal detection and first amplification in a single silicon pixel structure, so that the position measurement of traversing particles can be achieved with a minimum of material. The sensor consists of a depleted p-channel MOSFET implanted onto the surface of a high-resistive n-doped silicon substrate and a p^+ implant at the backside. More about semiconductor devices can be found in common textbooks like [40, 36], MOSFETs are comprehensively described in [41].

The substrate is fully depleted by means of sideward depletion as depicted in Figure 3-1. This is established by applying negative voltages to the source p^+ and back contact p^+ relative to the bulk potential n^+ (a). If the voltages applied on both p^+ contacts are sufficiently strong and equal, the depletion layers will meet in the center of the substrate (b) creating a potential minimum for the electrons. By relatively varying back and front side voltages, the minimum is shifted up vertically right below the top surface of the bulk substrate (c).



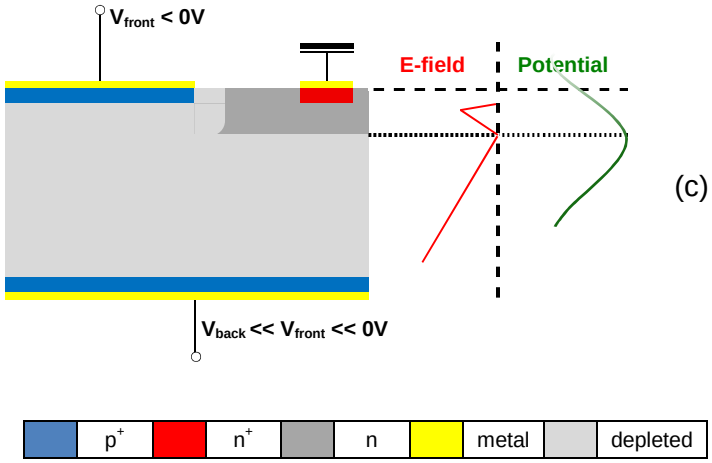


Figure 3-1: Concept of sideward depletion. Two p-n junctions share the same bulk contact. The n-bulk is grounded by means of a n^+ electrode. The electrical field and the parabolic potential curves for different voltage settings are displayed on the right.

The full depletion voltage V_{dep} of an n-type bulk together with a highly doped p^+ region is directly proportional to the quadratic sensor thickness d^2 [36]:

$$V_{dep} + V_{bi} = \frac{q}{2\varepsilon\varepsilon_0} d^2 \left| N_{eff} \right| \tag{3-1}$$

with V_{bi} the **built-in** voltage representing the potential difference across the p-n junction in equilibrium, q the elementary charge, ε the vacuum permittivity and ε_0 the relative permittivity of silicon and the effective doping concentration $N_{eff} = \frac{N_A \cdot N_D}{N_A + N_D}$ with N_A, N_D the acceptor and donor concentrations.

The position of the potential minimum z_{min} can be derived solving the one-dimensional Poisson equation with the given boundary conditions $\left(\varphi(0) = V_{front}, \varphi(d) = V_{back}\right)$ [42]:

$$z_{min} = \frac{d}{2} + \frac{\varepsilon\varepsilon_0}{q N_D d} \left(V_{back} - V_{front}\right) \tag{3-2}$$

where it was assumed that the acceptor concentration is much larger than the donor concentration $N_A \gg N_D$. $V_{back} - V_{front}$ label the voltages of the back and front side p^+ electrodes.

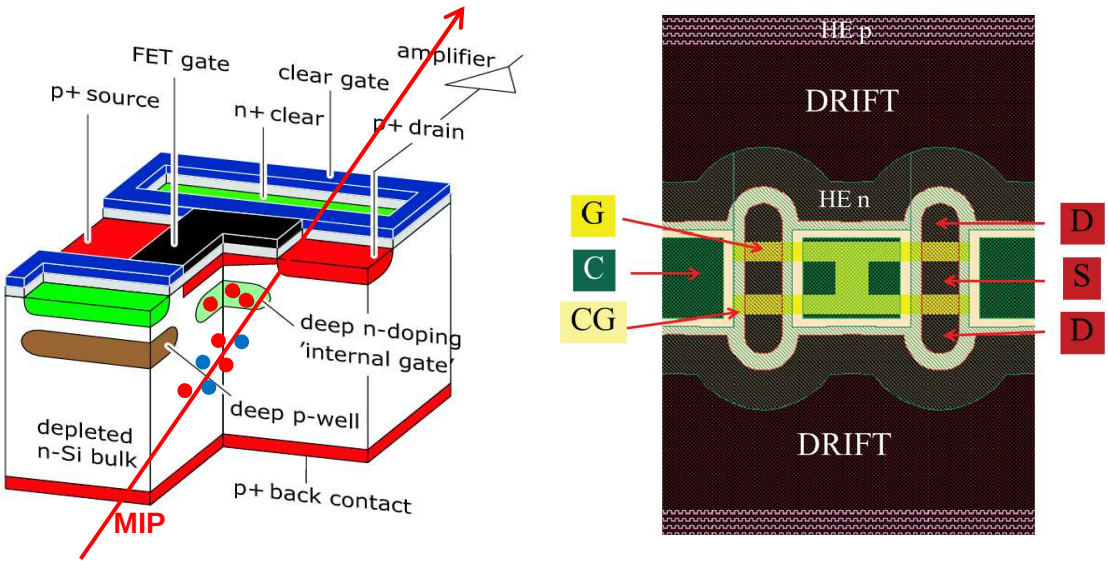


Figure 3-2: Left: cross section of DEPFET pixel with a minimum ionizing particle creating 80 electron hole pairs per µm for a 75 µm thick sensor. The electrons are attracted by the internal gate, the holes drift to the p^+ back contact. Right: PXD6 standard prototype design view on polysilicon and implanted layers (beige – first Poly (*Cleargate*), yellow – second Poly (*Gate*), brown – p-type implant (source, drain, drift), green – n-type implant (*Clear*). High Energy (HE) implants are used to increase the lateral drift field [43].

By an additional phosphorus n doping a potential minimum, called internal gate, is shaped at 0,65 µm below the *Gate* oxide of the transistor channel. This deep doping implant occupies only a tiny fraction of the pixel volume.[23] At depletion all free electrons are removed from this area leaving back a positive space charge remaining highly attractive for electrons. Now the detector volume is sensitive to incident radiation producing electron-hole pairs. Applying an electric field to the pixel separates the holes which drift to the negatively biased backplane whereas the electrons are collected in the potential minimum. High accumulated charges in the internal gate can neutralize the internal gate potential leading to an insensitive detector. To avoid this effect the electrons are regularly removed by applying a positive voltage to a *Clear* contact as explained in chapter 3.1.4

3.1.2 Electrical properties of DEPFET devices

The accumulated charge in the internal gate changes the potential and thus modulates the current[24] of the MOSFET channel if it is switched on. The source-drain current with empty internal gate is called pedestal current I_{ped}. If electrons are stored in the internal gate after an ionization event an additional signal current I_{sig} will be generated. To

among many other parameters on the external gate structure, doping concentration and varies its size dynamically with the amount of charged electrons

[24] in electrodynamic terms the charge stored induces mirror charges in the external transistor

measure the signal current the pedestal current has to be subtracted from the total transistor current.

$$I_{sig} = I_{sig+ped} - I_{ped} \tag{3-3}$$

This signal current represents the first amplification stage of the DEPFET sensor. Its amplitude is proportional to the number of collected electrons in the internal gate. The internal amplification g_q is defined as change of the transistor current ∂I_{DS} as a function of the internal gate charge ∂Q_{sig} at constant *Gate-Source* V_{GS} and *Source-Drain* voltages V_{DS} [43]:

$$g_q = \left.\frac{\partial I_{DS}}{\partial Q_{sig}}\right|_{V_{GS},V_{DS}} \tag{3-4}$$

typically given in pA/e^-. It is now possible to determine the amount of charges accumulated in the internal gate. The electrical characteristics of DEPFET transistors are very similar to that of standard MOSFETs. The main difference concerns the space charge region below the channel. In case of a standard MOSFET this region extends up to the undepleted bulk whereas for the DEPFET the region between channel and internal gate potential is relevant. The latter changes its potential depending on the amount of stored electrons. Due to parasitic couplings to other regions[25] [44] of the pixel structure not all but a fraction f of the charge will be induced in the channel. With the approximation that this induced charge is uniformly spread over the channel, an internal gate charge is equivalent to an external *Gate* voltage change by an amount of[26]

$$\partial V_{GS} = f \cdot \frac{\partial Q_{sig}}{C_G} \tag{3-5}$$

with $C_G = W \cdot L \cdot C_{ox}$ the *Gate*-channel capacitance, W and L denoting the width and length of the transistor and $C_{ox} = \frac{\varepsilon_{ox}\varepsilon_0}{d_{ox}}$ the oxide capacitance per unit area depending itself on the dielectric constant ε_{ox} and the width of the oxide d_{ox}. For a DEPFET device, which is operating in the saturation region under the condition $\frac{\partial I_{DS}}{\partial V_{DS}} = 0$, the current-voltage characteristics become:

$$V_{DS,sat} = f \cdot \frac{Q_{sig}}{C_G} + V_{GS,eff} \tag{3-6}$$

$$V_{GS,eff} = V_{GS} - V_{th} \tag{3-7}$$

[25] neighboring electrodes like backside contact, source and drain

[26] a derivation of the following formulas can be found in [32]

$$I_{DS,sat} = I_{DS}(V_{DS,sat}) = -\frac{W}{L}\mu_p C_{ox}\frac{V_{DS,sat}^2}{2} \tag{3-8}$$

$$g_{q,sat} = \frac{\partial I_{DS,sat}}{\partial Q_{sig}} = -\frac{W}{L}\mu_p f\frac{C_{ox}}{C_G}V_{DS,sat} = f\sqrt{\frac{2\mu_p}{WL^3C_{ox}}}\sqrt{-I_{DS,sat}} \tag{3-9}$$

with μ_p being the hole mobility and V_{th} the transistor threshold voltage expressing the minimum *Gate-Source* voltage needed to create a conducting path between source and drain terminals. From equation (3-9) one can easily derive the following dependencies of the internal amplification keeping all other parameters constant in each case:

$$g_q \sim \frac{1}{L^{3/2}}\ ,\ \frac{1}{W^{1/2}}\ ,\ \sqrt{d_{ox}}\ ,\ \sqrt{I_{DS,sat}} \tag{3-10}$$

For Belle II applications the internal gate can store about 40,000 electrons without any degradation of the linear response. Injecting more electrons could make the MOSFET channel conducting even when the *Gate* voltage is in off-state. This process saturates at about 60,000 electrons due to charge overflow [43]. The g_q-value for a *Gate* length of $L = 6\ \mu m$ and a $I_{DS} = 100\mu A$ used in this study is about $400\ pA/e^-$ [44].

3.1.3 Readout of DEPFET Pixel Matrices

The readout process of a single DEPFET pixel follows an iterative loop [37]:

a. *Sampling:* pixel is in off-state and remains sensitive to ionizing particles. The generated electrons will accumulate in the internal gate.
b. *Readout:* switching on the transistor by applying a voltage to the external *Gate*. The source-drain current, composed of $I_{sig+ped}$ is measured. The signal is calculated by subtracting a stored pedestal value, which was determined before during a dedicated pedestal measurement. This strategy is also referred to as single sampling. At an earlier stage a double correlated sampling was considered equivalent to an extra pedestal measurement directly after erasing the signal via a *Clear* process. However, balancing signal quality against readout speed the collaboration opted for the latter.
c. *Clear:* a voltage pulse is applied to the *Clear* contact, removing the collected charge completely from the internal gate.
d. *Reset:* set external *Gate* voltage in off position, which switches off the transistor. Sampling charge continues.

The whole matrix operation is characterized by low power consumption[27] as the transistors are turned off during charge collection.

The DEPFET pixels can be arranged in a two-dimensional matrix structure. All transistor drains of a column are connected in parallel to the amplifier nodes of the DCDB. The *Gate* and *Clear* contacts are connected row wise and steered by the SwitcherB. To increase readout speed, four pixel rows are connected together, so they are collectively switched on/off and erased at the same time. This in turn quadruples the drain lines: four drain lines for the readout of four rows of one pixel column are needed. As a result the pixels in the same column are read out sequentially, while pixels in the same row are read out in parallel. This is known as rolling shutter mode: one electrical row = 4 physical rows. The rows are switched on by applying the *GateOn* voltage and all pixels of that row are read employing the sample-clear-sample cycle described above. Then these four rows are switched off and the next four rows are turned on for readout until all rows have been read and the cycle starts again.

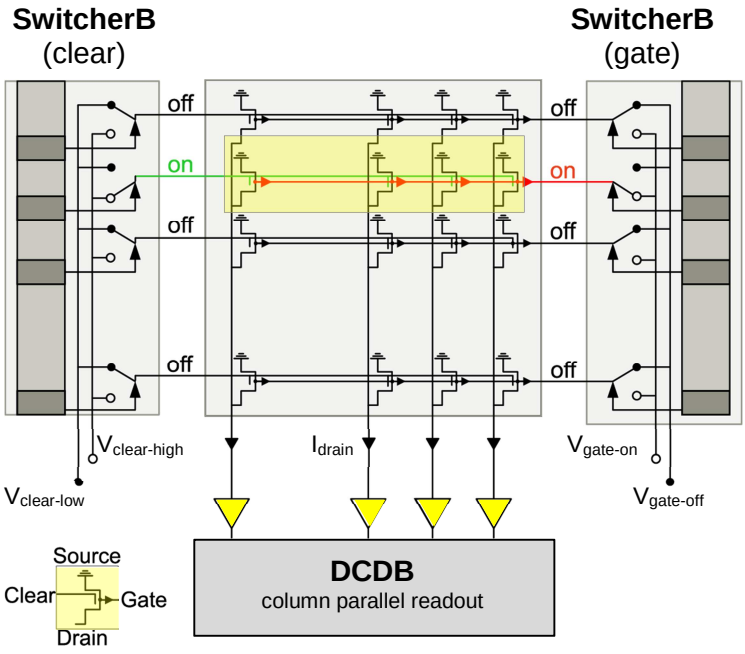


Figure 3-3: Schematics of DEPFET sensor operated in rolling shutter mode. The rows are activated sequentially by the SwitcherB chip. The drain currents are transmitted in parallel to the DCDB for further processing. Before switching to the next row (or set of rows) the *Clear* pulse is applied (*Gate* and *Clear* function are physically implemented into one chip).

The measurements for this thesis were performed with a rather small matrix structure consisting of 64 rows and 32 columns with a total of 2,048 pixels, each covering a sur-

[27] for an average current of 100 µA a DEPFET half ladder only consumes 0.5-1 W in the sensitive area and 9 W in total, mainly due to the readout electronics at the end of stave; accordingly air cooling is sufficient [38] [95]

face area of 50x75 μm^2. This has to be compared with a half ladder of the PXD composed of 768 rows and 250 rows with a total of 192,000 pixels.

3.1.4 *Clear* Process

In contrast to many other sensor concepts the collected charge will not be erased during the readout of the DEPFET pixels, so the measurement is non-destructive. This allows in principle multiple readouts for the same signal. However, leakage current and signal charges can quickly fill up the internal gate. We will see later that even a relatively weak laser pulse easily shifts the internal gate of many pixels into saturation, subsequently preventing further charge collection.

Without radiation damage[28] leakage currents will be negligible small for the BELLE II PXD. Former analysis on a 450 μm thick DEPFET sensor measured 600 electrons that accumulated in the internal gate within a time interval of 0.8 ms [45]. Taking into account the much shorter integration time of 20 μs this translates to only about a dozen leakage electrons, a factor of ten below the sensitivity threshold of the DCDB for 1 ADU (=73nA).[29]

To preserve the sensitivity of the sensor, the charge must be removed regularly from the internal gate. This process is called *Clear*. The *Clear* region is an n$^+$-implantation in the substrate shared by 4 DEPFET pixels. It is placed peripherally on both sides of the internal gate to facilitate a very fast *Clear* process. Applying a positive voltage to the *Clear* contact induces electrons to flow from the internal gate to the *Clear*. The entire charge of the internal gate can be removed with a sufficiently strong and long *Clear* pulse called “Complete *Clear*”. If a residual charge remains in the gate, this would represent an additional source of noise.

HLL together with the Weierstrass Institute have performed extensive 3D-simulation studies on how to structure the DEPFET pixel drift fields[30] in order guide the electrons directly to the internal gate. A special mechanism prevents a competition between internal gate and *Clear* in the course of the charge collection phase: during charge collection the *Clear* contact is put on negative potential compared to the substrate and a further deep boron p$^+$-implantation, called p-well, is introduced shielding the *Clear* contact from the internal gate. However, this implantation introduces a new potential barrier, making the process of clearing more difficult. To control the p-well and the potential of the substrate neighboring the internal gate, a *Cleargate* structure has been implemented [46]. Besides serving as a potential barrier the *Cleargate* supports the *Clear* process if the *Cleargate* voltage is raised during the *Clear* process.

---

[28] in case of radiation damages this is no longer true but can be kept under control via cooling

[29] 1 ADU corresponds to an internal gate charge of at least 180 electrons (assuming an internal amplification of $400\ pA/e^-$)

[30] vertically the electrons move within a few nanoseconds to the local potential minimum however, since the lateral drift fields are weaker the whole process takes between 50-60 ns depending on the drift voltage

3.1.5 Parasitic Capacitances of a DEPFET Matrix

The DEPFET operation mode is heavily influenced by parasitic couplings to neighboring regions. Simply because of their proximity to each other, implantation regions *(Source, Drain, Clear*), *Gate* contacts (external *Gate* and *Cleargate*) and their respective connection lines show intrinsic capacitive couplings and resistive components commonly referred to as parasitic capacitances [47].

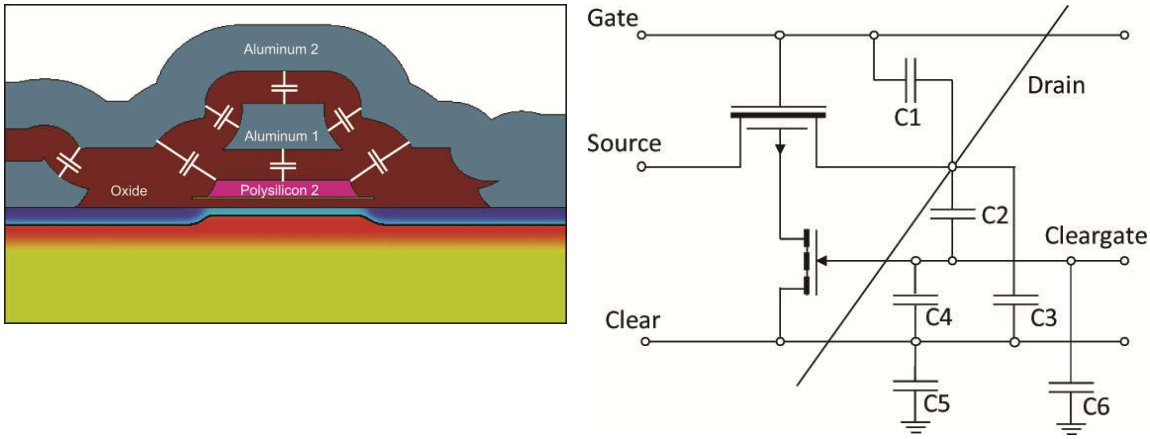


Figure 3-4: Left: Schematic cross-section view of a DEPFET pixel showing the parasitic capacitances between the connection lines. Right: equivalent circuit model [47]. Relevant quantities include the *Gate-Clear* capacitance, the *Gate-Cleargate* capacitance and the *Clear-Cleargate* capacitance.

As an example, the *Clear* capacitance of an electrical matrix row was measured at 135 pF. This is important for the rise time of the SwitcherB *Clear* signals which is 4,2 ns on 98 pF [48]. Since the RC time $\tau = RC$ is a constant, one can infer the rise time for enabling a full matrix row:

$$\frac{135\ pF}{98\ pF} \times 4.2\ ns \approx 5.8\ ns.$$

3.2 DEPFET Technology & Design

In order to keep multiple Coulomb scattering at an acceptable level, the material budget of the first silicon layers should be as small as possible [19]. This would be equivalent to a silicon thickness of 200 µm. The thinned DEPFET sensors give them a unique position in the field of silicon pixel detectors. Additional metal and polysilicon layers are needed for matrix readout and control, the sensors can be thinned down to 75 µm or below, only supported by a narrow silicon frame of 525 µm thickness around the sensitive bulk of the matrix. Various options have been investigated in order to optimize the final design. The prototype PXD6 used in this thesis mainly differs from BELLE II PXD9 in the thickness of the thinned sensor region (50 µm vs 75 µm). Normally the readout of a standard half ladder module requires 4 DCDB chips and 6 SwitcherB chips. In the

case of a PXD6 also smaller arrays were produced allowing to operate the readout with just one DCDB and one SwitcherB. These matrices are used as workhorses for a systematic characterization of the DEPFET operation.

The DEPFET pixel technology for BELLE II contains 25 photolithographic mask steps and 9 implantations [43]. It is a highly complex and custom-made using different technology aggregates and innovations like wafer bonding (SOI), double poly silicon, triple metal[31], back side thinning [49] and double sided wafer processing. To learn more about microtechnology and its processing steps one can refer to [50].

3.3 Biasing scheme

The powering of the PXD poses high challenges. 24 different voltages are needed for the operation of one half-ladder module. The operation voltages of the DEPFET matrix specifically influence the detector performance. As already mentioned, different voltage combinations can switch the detector into different operational modes. Furthermore there are constraints on each voltage applied. If these are surpassed this could severely deteriorate the detector performance or even damage the device. Applying parametric scans with a calibration source allows to optimize these settings.

All DEPFET voltages are typically referenced to the source of the transistor. The absolute value is derived from the DCDB analogue supply voltage AVDD (1.8V) and the necessary voltage for operating the DEPFET in saturation mode. An overview of all PXD6 test setup voltages can be found in Appendix D.

V_{Gate}: the applied *GateOn* and *GateOff* voltages directly affect the charge collection and the internal amplification. It is important that the *GateOff* voltage is never set below 0V. Otherwise all transistor channels would be switched on simultaneously and a high current would flow. This could potentially ruin the detector by damaging the readout chip or in an extreme case even causing the matrix drain lines to melt.

V_{Clear}: the *Clear* high voltage has to be determined in a particular trade-off: on the one hand a complete *Clear* should be guaranteed ($V_{Clear,high}$ ↑), on the other hand the *Clear* region should not become attractive during charge collection ($V_{Clear,high}$ ↓). If $V_{Clear,low}$ is chosen too negative, electrons could flow back from the *Clear* implantation to the internal gate.

V_{Drain}: the drain voltage is given by operating the DEPFET in saturation mode.

$V_{Cleargate}$: the *Cleargate* voltage has to be optimized together with the *Clear* voltage in order to find the optimal working point for an efficient *Clear*. The whole process capitalizes on a capacitive coupling between *Clear* and *Cleargate* of 0.3.

V_{Bulk}: the bulk contact (n^+-implant) serves as a counter-electrode to the punch-through electrode (p^+-implant). It drains leakage electrons from the non-pixelated zones and establishes a natural border between the outer pixels and the frame area. The bulk

[31] the metal system takes care for signal transfer, control and power lines

voltage should not be confused with the bulk voltage applied for standard **CMOS** processes where it is responsible for the “body-effect”. This effect describes the modulation of the threshold voltage by indirectly influencing the operating speed: if a standard p-channel MOSFET (pMOS) is tied to a positive potential, the source-body p-n junction would be reverse biased ($V_B > V_S$)[32]. Under reverse bias conditions the width of the depletion region increases corresponding to an increase in the ionic bulk charge. To maintain the charge balance, the mobile charge in the inversion layer decreases. Now the *Gate* voltage has to be increased to achieve a similar level of inversion as before.[33] A closer look reveals that the internal gate of the DEPFET is taking over this function in a similar way with one exception, that it is not fixed to a certain value but changes depending on the amount of stored electrons.

$V_{Punch\text{-}through}$: a special case is related to the biasing of the backside. Since sideward depletion is usually done from both sides of the detector, an additional wire bond and also an electrical link between module back side and front side are needed to route the correct bias voltage to the back side. Alternatively a punch-through[34] biasing scheme has been implemented for our test set-up. A punch-through occurs when the voltage difference across two p-type electrodes, separated by the depleted n-bulk of the detector, is high enough to enable a large hole current between the electrodes [51].

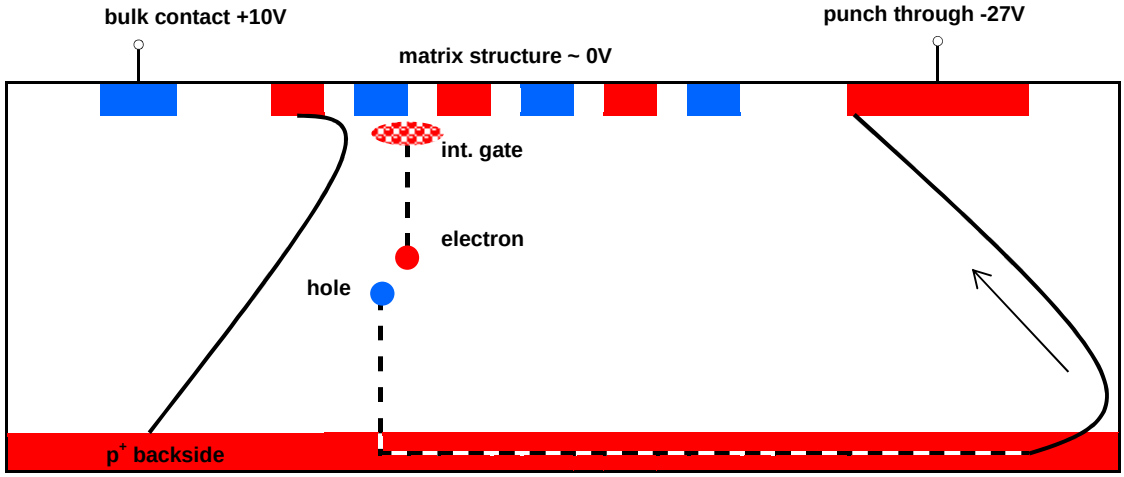


Figure 3-5: Schematics of the punch through biasing method on DEPFET matrices

To understand the punch-through process one should imagine an undepleted bulk with zero voltage applied to the punch through contact at the front side of the detector. Oppositely a floating p+ electrode exists covering almost the whole back side. It finds itself in equilibrium with the detector bulk being surrounded by a **built-in depletion region**. Now a slightly negative voltage is applied to the punch through electrode and a small region underneath depletes. The positively biased bulk contact acts as a counterelec-

[32] p-type region is connected to a negative voltage, n-type is connected with a positive voltage

[33] for forward biasing its exactly the other way around

[34] this should not be confused with the **punch-through** in a MOSFET or the lateral clearing mechanism between the internal gate and the clear contact which is also sometimes referred to as punch-through

trode. Further voltage reductions cause an expansion of the depletion region until it reaches the built-in depletion region at the back electrode. From this point on the region between these two electrodes becomes over-depleted and a hole current evolves from the back electrode to the fully depleted region toward the punch-through contact due to the punch-through effect (see Figure 3-5). Next the back potential begins to decrease controlled by the punch through voltage and the entire region of the detector from the back electrode upwards to the matrix becomes depleted. The biasing requires about $-2 \times V_{dep}$ which is in the range of -70V for the PXD9 sensors [43]. Since the depletion region scales with the squared bulk thickness d^2 a minimum punch-through voltage of -31V for PXD6 would be sufficient.[35] To learn more about this effect specifically for DEPFET detectors consult [52, 53].

V_{Drift}: outside of the transistor there are large drift areas which have to be negatively biased in order to route the electrons to the internal gate.

V_{Edge}: the voltage applied to the guard ring at the end of the sensitive area taking care together with V_{Bulk} that no electrons from the frame area drift into the pixel structure.

[35] $\frac{50^2}{70^2} \times -70$, in the test set-up it was -37V ($V_{Punch\text{-}through} - V_{Bulk}$)

3.4 The Gated Mode

As outlined at the end of chapter 2.3.4 DEPFET pixel detectors offer a very simple and elegant method to survive the noisy bunch phase of SuperKEKB. Providing a positive voltage to the *Clear* electrode while the *Gate* is held in off-position would switch off the signal collection for the entire matrix and preserve the information already stored in the pixel [43].In other words, the detector will be “gated” into an insensitive (blind) mode during the passage of noisy bunches.

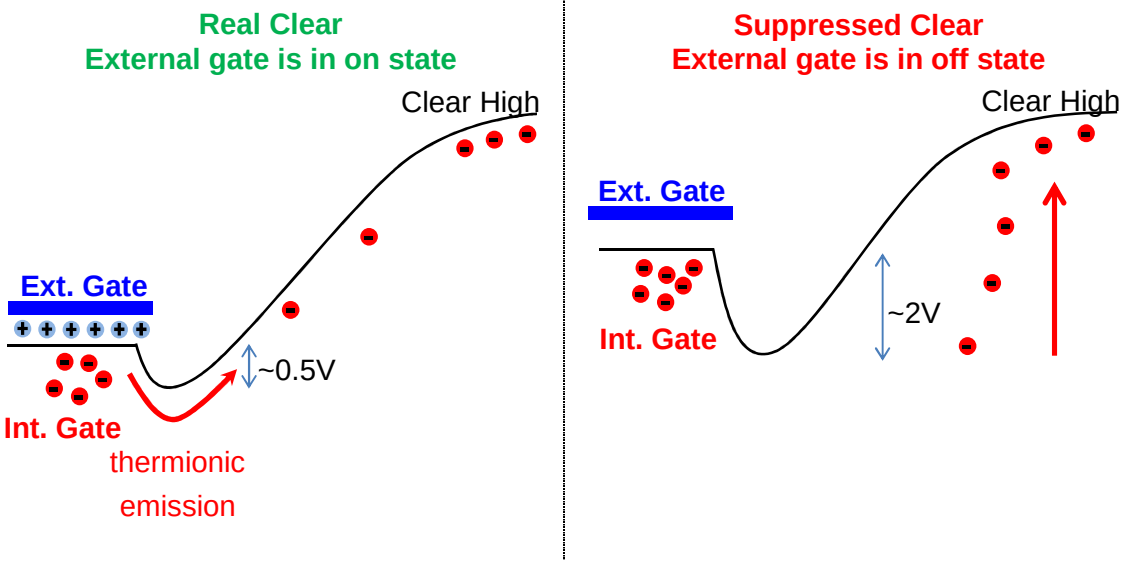


Figure 3-6: Selectivity of the *Clear* Process. Real *Clear*: The electrons in the internal gate can overcome the small potential barrier (<0.5V) by thermionic emission. Suppressed *Clear*: The external *Gate* shifts the potential of the internal gate by capacitive coupling → The electrons stay in the internal gate, the leakage electrons move directly to the *Clear* region.

The selectivity of the *Clear* process is controlled by the external *Gate* voltage as depicted in Figure 3-6. During real *Clear* operation the external *Gate* voltage is lowered in order to switch on the transistor hole current (pMOS). The holes in the channel shield the internal gate from being influenced by the external *Gate*. This effectively fixes the internal gate potential to the most negative one. Additionally, this results in the maximum possible difference between internal gate and *Clear* potential. The built-in potential barrier of around 2V decreases via capacitive coupling to just 0.5V, low enough for the stored electrons to leap over with thermal energy (punch-through). Switching into the Gated Mode (*GateOn* + *Clear* high voltage) turns off the hole channel and raises the internal gate potential via capacitive coupling. Consequently the potential barrier increases and the *Clear* process is suppressed.

3.5 PXD Detector

The PXD detector, shown in Figure 3-7, is placed closest to the IR and consists of two sensor layers, with radii at 14 mm and 22 mm. The barrel shape is approximated by a polyangular (“wind mill”) arrangement of planar modules, the so-called ladders.[36] All in all there are 20 ladders, 8 for the inner layer and 12 for the outer one. The sensitive part of the ladder is thinned to 75 µm, part of the read out electronics is directly mounted on the unthinned parts (“balcony”, 525 µm) also supporting the mechanical stability.

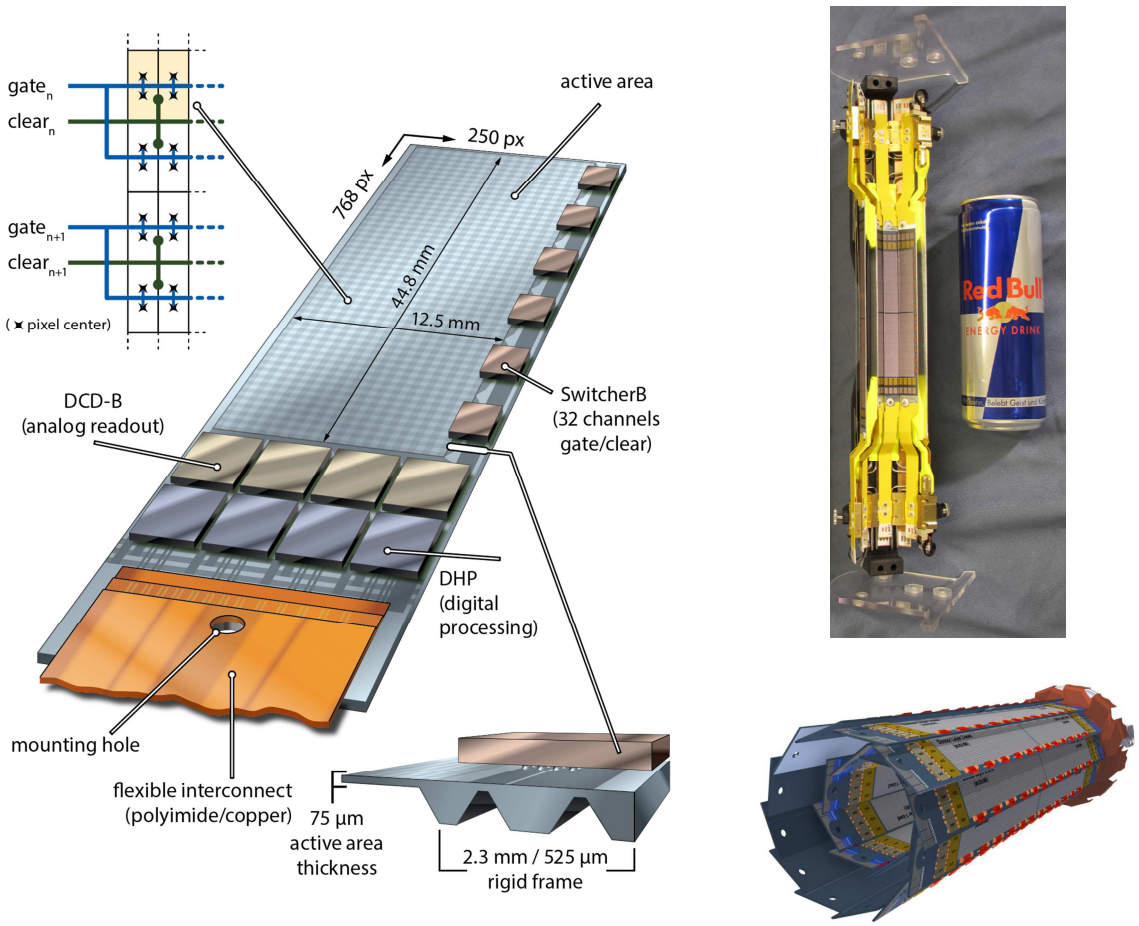


Figure 3-7: Belle II PXD vertex detector. Left: half-ladder module including steering and read out chips bump-bonded on the balcony or end-of-stave, respectively. Deep corner cubes are anisotropically[37] etched into the supporting frame in order to further reduce the material budget [54]. Right above: PXD detector proportions showing the ladders mounted on the mechanical support structure. Right below: schematic of the polyangular geometrical arrangement of the sensors for the PXD [55].

The sensor area of the half ladder consists of 768 rows and 250 columns (=matrix frame) with two different pixel geometries adjusted to the incidence angle of the collid-

[36] composed of two half-ladder modules glued together

[37] unequal physical properties along different axis

ing particles. 6 chips are responsible for clearing and enabling of the detector rows (in the following called SwitcherB), 4 chips are responsible for receiving and amplifying the drain currents (hereinafter called drain current digitizer - DCDB[38]) and 4 chips are used for early data analysis and data reduction (data handling processors - DHP).

Data reduction is essential since the total data rate for the complete PXD can be estimated at 409.6 GB/s[39]. This has to be compared with the peak traffic of the DE-CIX (German Commercial Internet Exchange) the largest internet exchange point worldwide with 384 GB/s[40] corresponding to memory requirements of 800 CD ROMs per second [56]. A common clock delivered from the data handling engine (DHE) should ensure a frequency of 320 MHz which translates into a read out speed of 20 µs per frame.

The data transmission system connects the DEPFET modules to the DAQ system [19] as shown in Figure 3-8. A multi-layer kapton cable connects the end of stave of the half-ladder to a patch panel (PP) responsible mainly as a cable adapter for the fast signals from the DHP and also for power filtering and impedance matching. An **infiniband cable** guides the data to the DHE which interconnects with the Data Handling Controller (DHC). Each DHC is responsible for controlling 5 DHEs and transmitting the data stream via optical fiber to the compute node (CN).

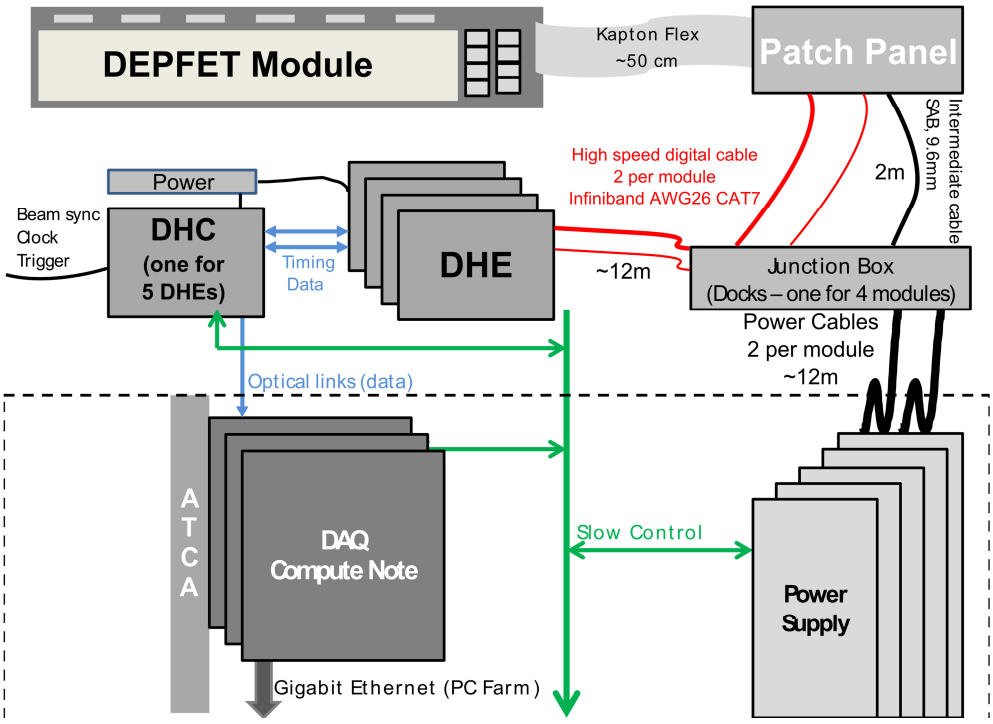


Figure 3-8: Elements of the PXD data transmission system [57]

[38] "B" stands here for "Belle" version

[39] DCDB digital serialization multiplexes the conversion results of the input channels onto eight output channels (8-bit wide); applying a clock rate of 320 MHz each of the 160 DCDB chips mounted on the PXD detector produces a data rate of 2.56 GB/s

[40] 1 Byte = 8 bit

The compute node represents the hardware platform designed as a 14-layer **printed circuit board** (PCB) of the Advanced Telecommunications Computing Architecture (ATCA) standard. Based on Monte Carlo Simulations (MC) and on past experiences the detector occupancy at the highest luminosity can be estimated to $8x10^4$ fired pixels per frame, which corresponds to an average occupancy of $\cong 1\%$ [43][41]. A safety margin with a factor of three accounts for possibly substantial contributions from the so far poorly known machine background (see chapter 2).

3.6 PXD Sensor Electronics

The following chapter will discuss the readout electronics of the PXD sensor subject to the several important limitations: by current standards of integrated circuit design the employed chips constitute a highly sophisticated custom-made solution. For that reason the layer of abstraction restricts itself to the block level explaining just the core functionalities and principal modes of operation. Furthermore many electrical terms will be introduced and it is not possible to explain everything in detail. The interested reader might consult existing standard literature, as for example [58, 59, 60, 61]. Finally only the DCDB and SwitcherB chip will be described since for the test setup no other electronics of the PXD sensor will be used.

The challenges of Belle II are reflected in a highly optimized application-specific integrated circuit (ASIC) design for DCDB and SwitcherB [62] :

- relatively weak signal currents of ~2-3 µA for a minimum ionizing particle (MIP)
- high expected occupancy of the Belle II detector necessitating a high frame readout speed of 20 µs which in turn requires short shaping times leading to increased noise
- large capacitances of the column lines of ~50 pF that load the analog inputs of the DCDB chips causing additional noise
- large pedestal dispersion of the DEPFET sensor up to 25 µA
- need for fast high-voltage signals to steer DEPFET rows of large capacitances within a short time (within 10ns into 100 pF)
- high radiation tolerance
- all-silicon module concept for BELLE II bonding chips directly onto the sensor

[41] 7.68×10^6 pixels in total

3.6.1 The DCDB pipeline

3.6.1.1 Overview

The DCDB was designed by I. Peric et al. [63] in order to readout and digitize the current signals generated by the DEPFET pixel sensors. It covers an area of $3240\,\mu m \times 4969 \mu m$ that is determined by the following two main building blocks:

- analog domain: 256 parallelly operating analog channels containing each a transimpedance amplifier and eight pipeline analog to digital converters (ADC)
- digital domain: separated fully **synthesized** digital readout and control block

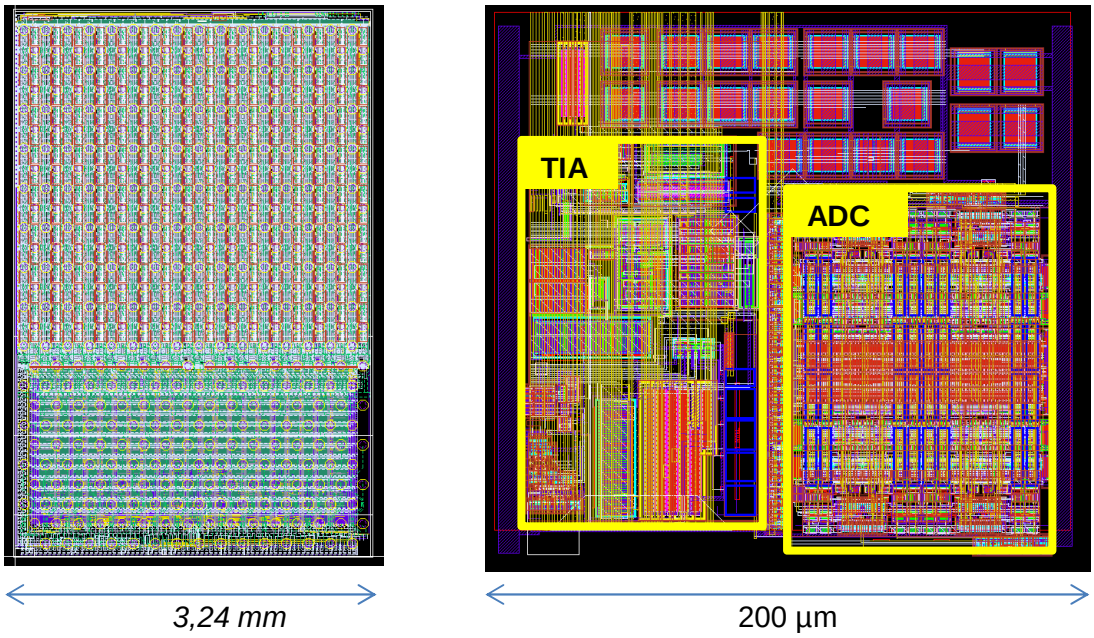


Figure 3-9: Left: Picture of the DCDB layout. The 256 ADC channels on top are arranged in a 16 x 16 matrix. The digital logic is located on the bottom side. Right: Floorplan layout of one DCDB pipeline channel [64].

Incorporating mixed analog and digital functions on a single chip poses special challenges to the designer and the simulation software. The block diagram of the analog channel is shown in Figure 3-10.

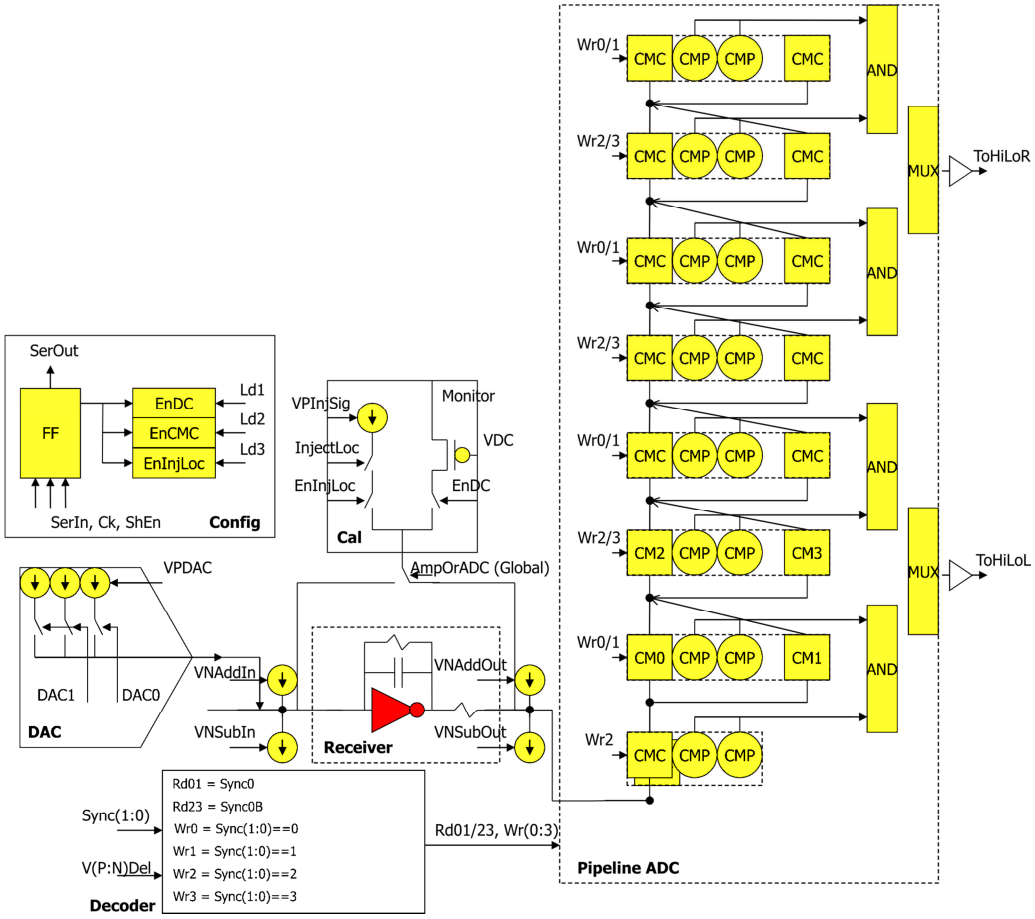


Figure 3-10: Block diagram of one DCDB pipeline analog channel with several building blocks explained in the text [63]

3.6.1.2 DCDB pipeline main circuits

Receiver

The Receiver consists of a transimpedance amplifier *(TIA)* with two feedback resistors R_f (each 30 kΩ) and two output resistors R_s(each 15 kΩ). The transimpedance amplifier converts the DEPFET current into voltage. The current gain or "transimpedance" without output resistor is equal to R_f: $V_{out} = -(I_{in} \times R_f)$. Including the output resistor the current gain G would become: $G \equiv R_f / R_s$ [63]. One of the output resistors can be switched allowing for high or low current gain with respect to the output signal. This possibility also exists for the feedback resistor $R_f$hence the nominal dynamic range of the ADCs can be adjusted to 4 different stages between 12 and 29 µA as shown in Figure 3-11. This is more than enough for measuring the signal current produced by one MIP (~2-3 µA), but at the borderline for the pedestal current fluctuations of the PXD9 matrix which can reach up to 25 µA. Accordingly for the next DCDB release it is planned to enlarge the total dynamic range.

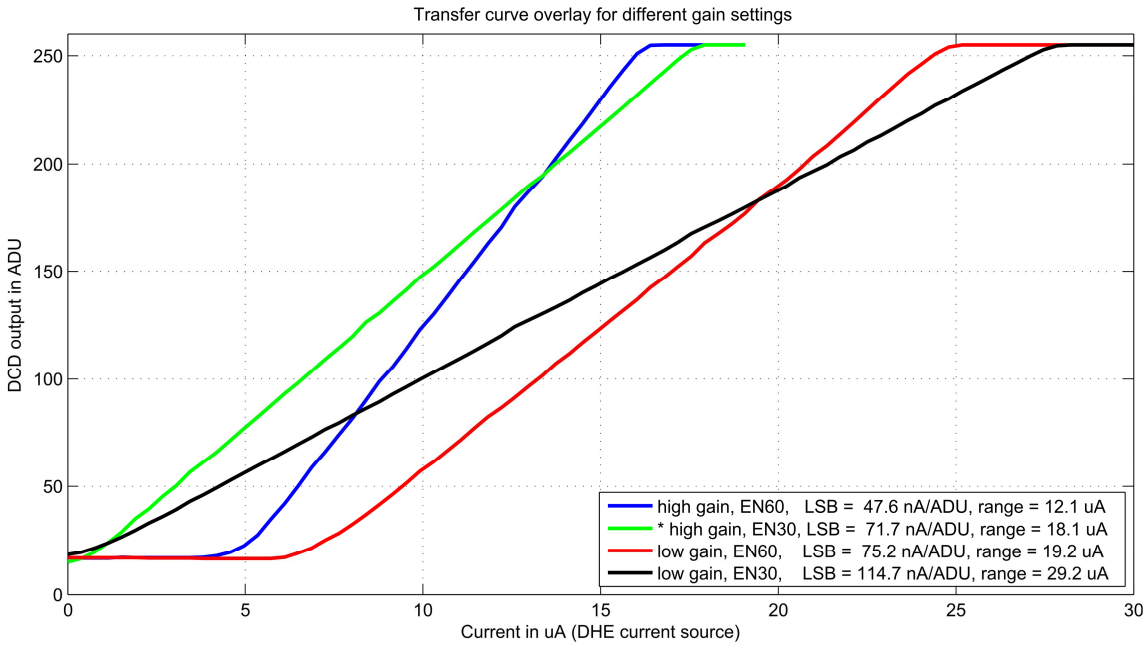


Figure 3-11: **Transfer curves/functions** for different resistor settings influencing the dynamic range of the ADC. The least significant bit (LSB) of the 8-bit output code expresses the gain per analog digital unit (ADU) and varies between 47.6 nA/ADU and 114.7 nA/ADU. The star marks the settings used for the testing of the Gated Mode.

Current mode pipeline analog to digital converter (ADC)

An analog to digital converter (ADC) takes an unknown continuous input signal (in this case an electric current) and converts it into an n-bit binary number corresponding to the ratio between unknown input current and the converter's full-scale current I_{FS}. The smallest current change occurs, when the least significant bit (LSB) in the digital word changes from a 0 to a 1 (or back). This also expresses the resolution of the detector given by [59]:

$$I_{LSB} = 2^{-n} I_{FS} \qquad (3\text{-}11)$$

The most significant bit (MSB) at the other extreme has a weight of one half I_{FS}. In between the digital output code stairsteps in case of a 4-bit converter from 0000 to 1111 as shown in Figure 3-12. The 1-LSB quantization interval is responsible for the quantization error. This is a typical property for all ADCs. While the input current increases in a continuous fashion, the output code's resolution first underestimates the input current and then overestimates the input current.

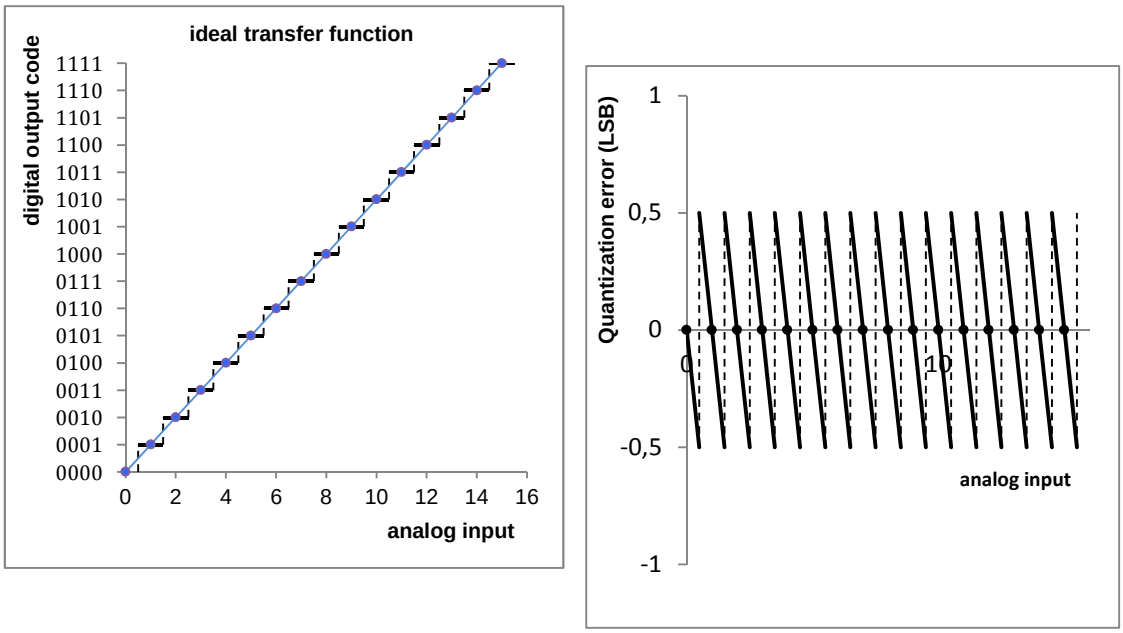


Figure 3-12: ideal 4-bit ADC: Left: Input-output relationship. Right: Quantization error.

In the DCDB pipeline the quantization is distributed along a series of 8 stages that are isolated by current memory cells (CMC[42]) also known as sample-and-hold buffers (S/H). The stages work concurrently, the first one operates on the most recent sample, while the following stages process the residual currents from previous samples. Each stage consists of a double cell block containing two current memory cells and two comparators (CMP). The main purpose of the $CMCs$ is to store a current into a capacitor (for the DCDB pipeline in the range of $\pm 16 \mu A$) and to keep the input node at a constant potential. The CMC input node's potential should not be affected if the input current lies within its dynamic range but should rise or fall instantaneously once the input current exceeds the dynamic range.

The comparators compare the input signal to two reference currents $\pm I_{ref}$, one positive and one negative. The result of the comparison is used to decide about adding, subtracting or disabling the reference currents according to the conversion algorithm described in chapter 6.3. The final result will be forwarded to a digital output pin via the **multiplexer** (MUX).

Steering and configuration blocks

The pedestal currents of the DEPFET pixels vary substantially. In order to adjust the pedestal current to the ADC's dynamic range a controllable compensation mechanism, steered by a Digital to Analog Converter (DAC), adds a certain current to the channel's input node. Precondition for setting the correct DAC values are dedicated pedestal measurements for every pixel of the DEPFET matrix.

[42] the elementary principles of current memory cells are explained in [97, 98]

For system calibrations, performance tests or debugging purposes a configuration *(Config)* and a calibration *(Cal)* circuitry are embedded in each channel. The calibration circuit allows for injecting test currents. Additionally, through its monitor line an external calibration current (via a Source Measurement Unit, SMU) or an internal global source called *ISigMirror*[43] can be sourced to the amplifier or directly to the ADC (*AmpOrADC* switch). By means of a pixel shift register the three local switches (*EnDC*, *EnCMC* and *EnInjLoc*[44]) can be configured for each pixel separately.

Based on the sequence stored in the digital block of the DCDB the Decoder generates write *(Wr)* and read *(Rd)* signals used to control the ADCs.

3.6.1.3 Pipelined ADC Realization

The pipeline architecture for the ADC was chosen for achieving a reasonable high conversion rate while avoiding excessive silicon area and power consumption like full parallel "flash" converters[45]. Indeed the covered area of the predecessor DCDB chip with cyclic ADC was even two times smaller (8 instead of 16 CMC cells) and consumed half of the power, whereas the pipelined solution is regarded as less noisy since it allows to operate with half of the clock speed[46].

3.6.2 Switcher-B

3.6.2.1 Overview

The SwitcherB steering chip shown in Figure 3-13 generates fast high-voltage pulses (10 ns into 100 pF[47]) of up to 20 V amplitude to enable the read out of the signal and to clear the stored charge of the internal DEPFET gates [65]. One SwitcherB consists of 32 different output channels each providing a *Clear*- and a *Gate*-driver. Within an output channel a transistor is configured as an electronic switch to act as a level shifter (or level converter) in order to switch between upper *(CHi, GHi)* and lower voltage levels *(CLo, GLo),* respectively [48].

[43] ISigMirror is common to all channels and consists of 3 switchable 128-bit pMOS current sources

[44] EnDC enables the common monitor bus individually for each pixel, EnInjLoc activates the switch for the VPInjSig common current source for test signal injection, EnCMC enables the **common mode noise** compensation mechanism

[45] a consequence of a pipelined concurrent operation is latency, meaning that the output code is not obtained until a number of clock cycles later

[46] 25ns clock for current memory cell making comparators working more precisely

[47] 10 ns into 100pF means that the combined transition time for the rising and falling edges of the gate or clear pulses is about 10ns

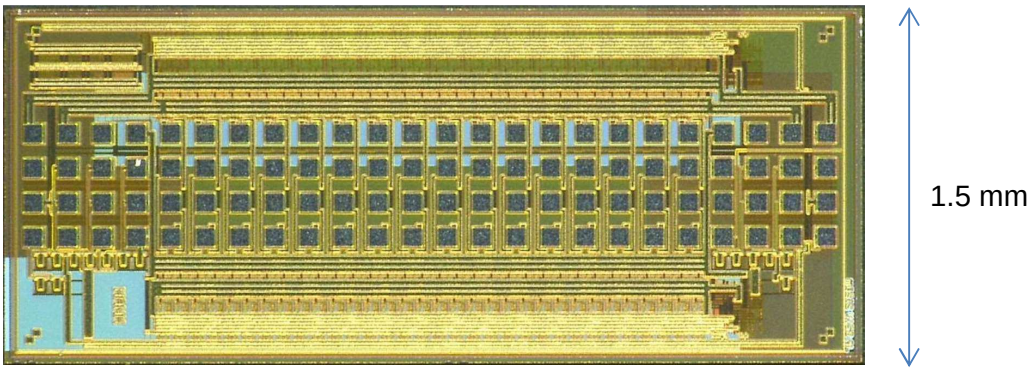


Figure 3-13: standard layout of the SwitcherB in 180nm AMS[48] CMOS technology with four rows of bump pads in the middle of the chip. Four bump columns are placed at both ends of the SwitcherB footprint for control signals and power supply. Additionally, this allows for a series connection of multiple SwitcherB chips along the balcony of the DEPFET module. The other 64 pads are for the *Clear* and *Gate* channels. The big output transistors are located at the top and the bottom of their corresponding output pad columns whereas **JTAG** and the digital logic are arranged at the corners of the chip [66].

3.6.2.2 SwitcherB operation mode

As shown in Figure 3-14 (bottom) the channels are sequentially addressed by means of a 32 bit deep shift register. An external "1" which initializes its serial input *(SerIn)* is clocked *(CLK)* through all the channels. Once a channel is enabled (e.g. $en\langle 0\rangle$ for selecting the first channel), a low voltage control block acting as level shifter unit transfers controlling information from the low voltage digital domain to the high voltage analog output stages [67]. Two fast common strobe signals *(StrG, StrC)* are activating the high voltage switches[49]. A voltage regulator *(Regulate)* generates four high voltage supplies out of two main ones. For more details about the high voltage channel of the SwitcherB see [68]. In this context one feature of the DEPFET matrix sometimes causes confusion. Since it consists of pMOS transistors a matrix row is regarded as *ON*, if the corresponding *Gate* signal is at *GLo* level whereas it is considered to be in *OFF* state if the *Gate* signal is at *GHi* potential. For the *Clear* channels, this is just the other way around.

The strobe digital logic block allows different operation modes depending on the relative position of the *Clear* or *Gate* strobe signals with respect to the shift register's clock signal. More information about the operation details can be found in 7.3. The **slow control** is based on a JTAG compatible interface mainly used for configuration of the chip's operation mode and debugging purposes (**boundary scan chain**).

[48] Austrian semiconductor manufacturer

[49] high voltage transistors distinguish themselves from standard transistors by a larger size and a much thicker oxide at the drain side; additionally these transistors use the **enclosed design** to reduce radiation induced leakage currents [48]

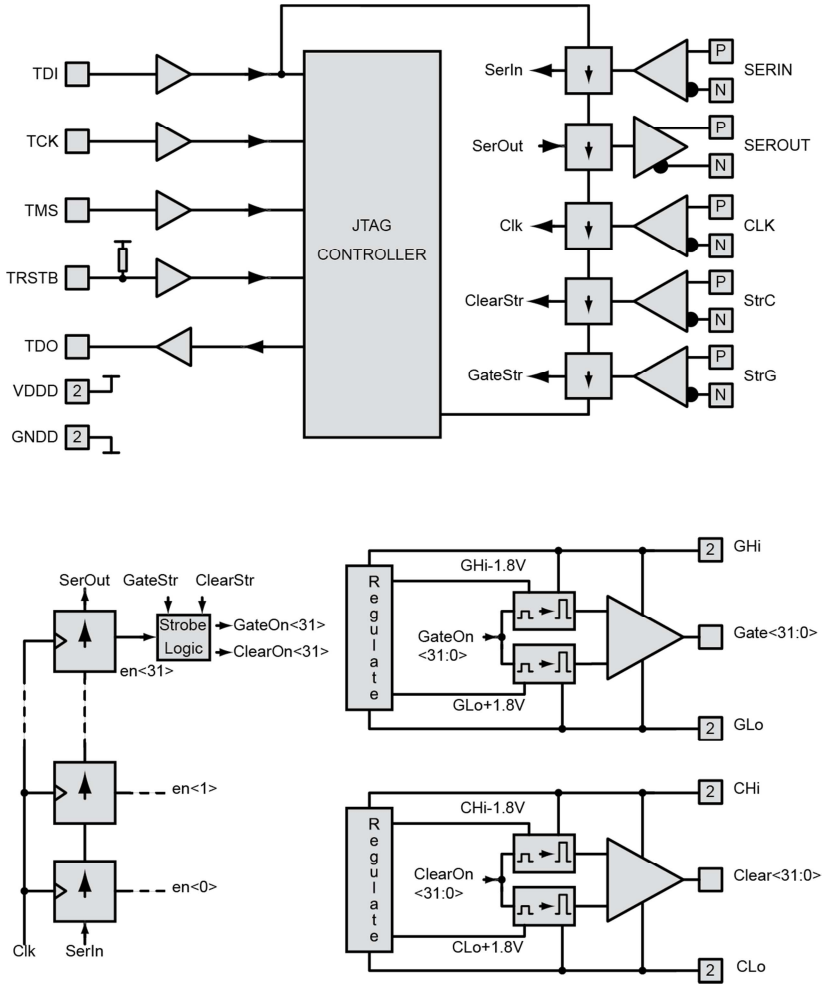


Figure 3-14: Top: SwitcherB block diagram of the JTAG controller and boundary scan chain. Bottom: One output channel containing a voltage regulator, a low voltage control block, a CMOS-to-differential-current voltage-to-current (U/I)-converter (triangle) with its *Clear*/*Gate* drivers and high voltage power transistors [48].

3.6.2.3 SwitcherB Biasing

The SwitcherB needs a 1.8 V supply voltage *(VDDD)* for the digital part and four analog voltages for the *Gate* and *Clear* operation. The high voltage power transistors can sustain high *Drain-Gate* and *Drain-Source* voltages. However, the voltage difference between analog high and low should be larger than 5 V and must not exceed 20 V. The chip substrate voltage *(sub)* is connected to the lowest of all supply voltages. A reference voltage *(Vref=VDDD)* at 1.8 V above *sub* serves as digital ground for the level shifters.

There are several rules for the power up sequence which have to be followed strictly otherwise the chip may be damaged. In general there must always be a current limit on the power supplies. Before starting operation the digital supply voltage has to be turned on. The next step the shift register gets cleared (filled with 0's) and finally the analog supply voltages are switched on.

4 Hybrid 4.1 Board and FPGA Board

4.1 Overview

For the characterization of the DEPFET sensors a special test system was developed [54]. It consists of two printed circuit boards (**PCB**) responsible for housing the chips and the required mainly passive components (e.g. capacitors, resistors and connectors ensuring signal and power integrity):

a) a hybrid board[50] which assembles a small PXD6 matrix (64 rows, 32 columns), one SwitcherB, one DCDB and one chip called DCDRO[51] responsible for reading out and multiplexing the digitized data from the DCDB.

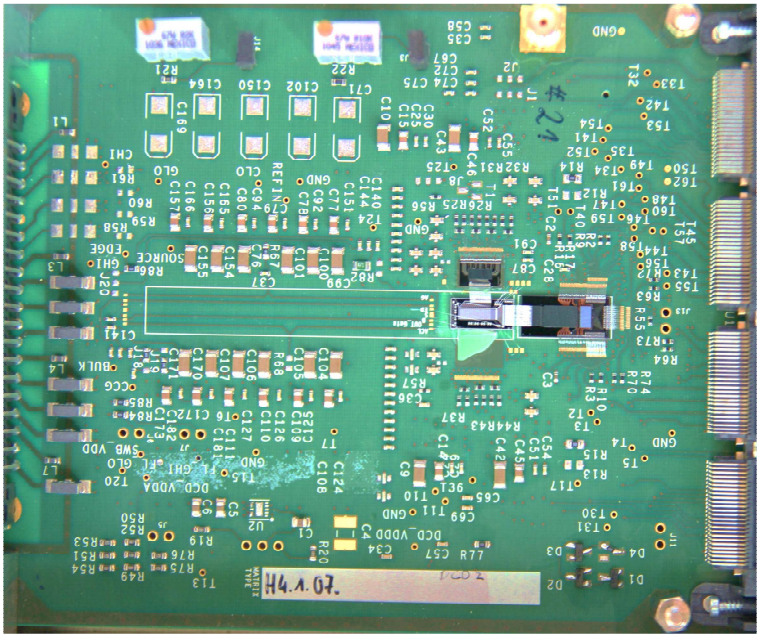


Figure 4-1: Hybrid 4.1.07 board

b) a general purpose field-programmable gate array (FPGA) board serving as a controlling unit. It acts as an interface between the hybrid board and the data acquisition system. On the one hand it configures, steers and reads the DCDB and SwitcherB and on the other hand it communicates via USB connection with the host PC where the data acquisition, processing and displaying is implemented [69].

[50] the PCB is called hybrid, since more than one distinctive device type is combined (silicon sensors, chips, active and passive mechanical components)

[51] RO stands for readout

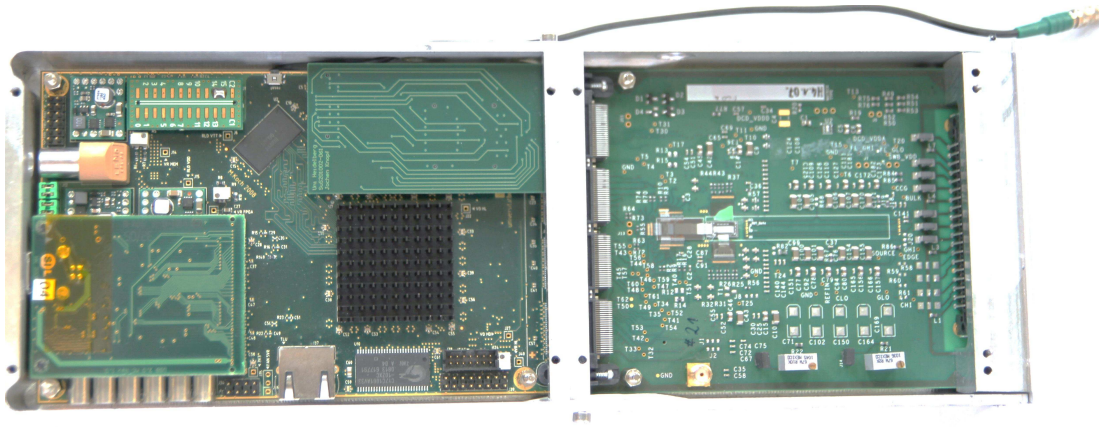


Figure 4-2: Aluminium box with FPGA board and connected hybrid board.

4.2 Hybrid 4.1 Board

All hybrid boards can be distinguished via their specific version number H4.1.x (H = hybrid board, 4.1 = design revision, x = individual identifier). For the PXD the chips will be mounted directly on the DEPFET sensor matrix using bump-bonding and flip-chip techniques due to the very tight space limitations. Unfortunately the DCDB bond pads are very narrow pitched and therefore cannot be directly connected to a standard PCB. This problem is solved by the wire bond adapter shown in Figure 4-3, developed and fabricated at the MPI Semiconductor Lab (HLL). It utilizes a one aluminium layer technology [43]: DCDB, DCDRO and SwitcherB are bump-bonded with gold studs and manually placed solderballs on these wirebond adapters, which in turn are glued onto the hybrid PCB and electrically connected using wirebonds. The matrix is also wirebonded to the different wirebond adapters and to the bond pads on the PCB.

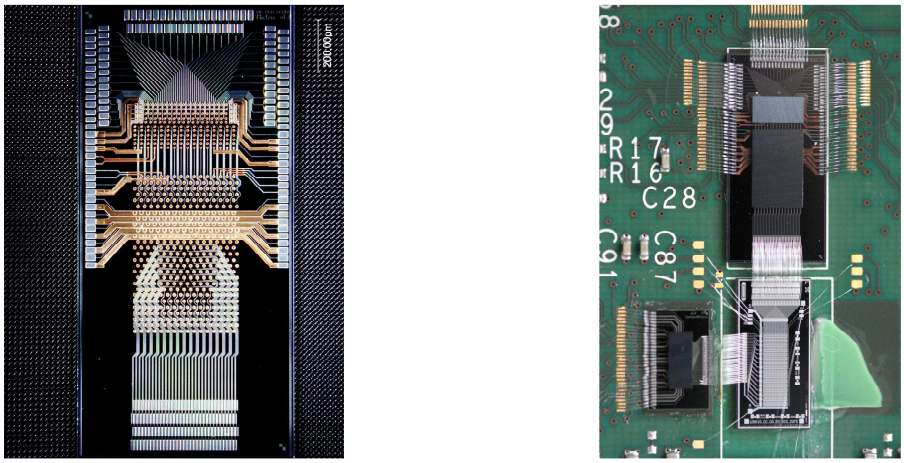


Figure 4-3: Left: DCDB wire bond adapter without assembled chips. The wire bond pads on the bottom establish a connection from the DCDB to the matrix. The pads to the left and to the right are for power and control signals. Right: small DCDRO chip on top followed by the DCDB; wire bonds to the columns of the matrix and also from the SwitcherB chip located on the bottom left.

The PCB implementation establishes a very flexible environment for testing purposes: it allows to send test input signals to the DCDB via its monitor bus or one of the input channels, which are accessible by means of **SMA** connectors [67]. For testing the DCDB chip one of these SMA connections will be linked to an external source measurement unit (**SMU**) in order to calibrate the internal current source of the DCDB. Additionally, a test board was wirebonded to the SwitcherB chip facilitating the measurement of the steering sequences with an oscilloscope. A small hole in the PCB directly underneath the detector permits irradiating the sensor on the backside. Finally the **vias** of the PCB provide for bias measuring or for probing digital signals sent from and to the DCDB.

4.3 FPGA Board

One of the fastest and most flexible solutions for testing the combined effectiveness of DCDB, SwitcherB and DEPFET matrix is to use a field-programmable gate array (FPGA). An FPGA is a reprogrammable silicon chip based on a matrix of **configurable digital logic blocks** (CLBs) connected through a massive fabric of programmable interconnects. FPGAs allow users to reprogram the chip to a desired task or functionality after fabrication. This feature distinguishes FPGAs from Application Specific Integrated Circuits (ASICs), which are custom manufactured for specific applications and are built on fixed digital logic. As an example, DCDB pipeline and SwitcherB fall into the ASIC category.

At the end the decision between ASIC or FPGA comes down to the question of scalability versus flexibility: ASICs are advantageous when it comes to high volume design (much lower unit costs) and full custom capability. FPGAs offer a faster time-to-market, much lower initial costs and the ability of reprogramming for special features. FPGAs use specific Hardware Description Languages (HDL) like verilog or VHDL. At first glance these look like normal programming languages such as C++. However, they differ significantly in the following aspects: first, HDLs explicitly include the notion of time and secondly, whereas a C++ program runs through a sequential series of instructions, HDLs describe concurrent circuits being able to model multiple parallel processes (such as flip-flops or adders). For the test setup the FPGA chip has to meet several criteria [54]:

- Flexibility: adapt to different test scenarios.
- Connectivity: connect to all relevant inputs and outputs of the device under test (DUT) and being able to communicate with a computer.
- Speed requirements: these are mainly driven by the target operation frequency for the DCDB of 320 MHz and requires a programmable, fine grained, clock management as well as high precision with respect to the time shifting of the SwitcherB signals.
- Memory: provide storage capacity for 8 consecutive small PXD6 matrix frames and internal memory space for different SwitcherB sequences.

- Safety, Stability and Testability: especially to mention are test points for all voltages and relevant signals and a monitoring system for controlled power up sequencing and voltage control.

The Virtex4 LX40[52] FFG1148[53] (Speed Grade -10)[54] FPGA from Xilinx Inc. [70] satisfies all of these requirements and forms the core of the FPGA board[55]. It offers 41,472 logic blocks, 1,728 Kb[56] block RAM and a total of 640 general purpose inputs and outputs. The digital clock managers (DCMs) deliver an adjustable output frequency derived from the input clock by simultaneous frequency division and multiplication [71]. The user may specify any integer multiplier (M between 2 and 32) and divisor (D between 1 and 32) under the constraint of a maximum clock frequency of 400 MHz. For example, M=16 and D=5 would multiply the input clock of 100 MHz by a factor of 3.2.

In addition to the FPGA chip several peripheral devices are available on the PCB. Of particular note is the USB 2.0 add-on card offering an interface to the computer. It consists of a microcontroller and a storage device for its program code. The microcontroller provides a USB 2.0 compliant PC connection. An 80 pin IEEE connector ensures the link to the FPGA [72]. The USB 2.0 interface manages a theoretical data throughput between FPGA and connected PC of 60 MB/s however, in reality a data rate of only about 12 MB/s was achieved [67]. The connection to the hybrid board is established with a 200 pin high speed connector. The FPGA is powered from a single input voltage in the range of 4.5 to 5.5 V generating a total of 10 internal voltages.

The DCDB chip digitizes the drain currents of the DEPFET matrix and multiplexes them onto an 8-bit wide parallel output. With an operating clock frequency of 320 MHz each row of the matrix is switched every 100ns. Hence it takes 1.6 µs in order to read out a single frame from our test setup. One single frame requires a memory space of $128\,columns \times 16\,rows = 2048\,Bytes$ (8-bit resolution). The total raw data rate will be around 1.28 GB/s which is huge compared to the 12 MB/s USB/PC-connection of the FPGA system. Since the storage capacities of the FPGA system are limited a triggered readout scheme is applied. By means of the block memory generator from XILINX a **ring buffer** within the block memory was created to store 8 subsequent frames (consumes 16.384 KB out of 216 KB available block RAM which is more than sufficient for the test purpose[57]). Accordingly the matrix readout rate can be decoupled from the available data transfer bandwidth of the DCDB.

[52] LX denotes the platform family (LX, FX and SX) offering multiple feature choices and combinations to address all complex applications, 40 denotes the rounded number of logic cells (in thousands)

[53] FFG denotes a lead free package type, 1148 the number of available pins: this relatively large number strongly simplified the routing during the PCB design [34]

[54] determines the reference clock range up to 400 MHz [100] and the chain delay resolution of 75 ps (chain delay elements are individual small buffers) an important number to keep in mind for the DCDB delay settings

[55] 12-layer 100 mm x 160 mm sized PCB

[56] kilobits

[57] the actual Xilinx Virtex7 series offers 30 times more logic cells and also 30 times higher block memory

5 Test Plan for the Gated Mode

5.1 Overview

Regarding the Gated Mode operation two basic strategies are under consideration:

- *Junk Charge Generation: how much additional charge is generated during the blind phase potentially distorting the signal?*

The applied method is emptying the internal gate with a normal readout sequence, switching the Gated Mode on, impinging a laser pulse on the backside of the DEPFET sensor, thereby creating electron/hole pairs in the bulk. Finally, switching the Gated Mode off and hopefully observing no signal charge collection in the internal gate if the external voltages are chosen correctly.

- *Signal Charge Restore: how much of the junk charge will arrive in the internal gate?*

Here the internal gate is not empty. The applied method is the creation of a known load quantity with the laser, impinging on the bulk in the sensitive mode. After switching on the Gated Mode and waiting some time (1-3 frames), the normal readout sequence sets in again. Ideally there should be no charge loss from the internal gate escaping to the *Clear* contact.

The whole schematics for the experimental set-up including power supply, laser driver and laser pulse generator is depicted in Figure 5-1.

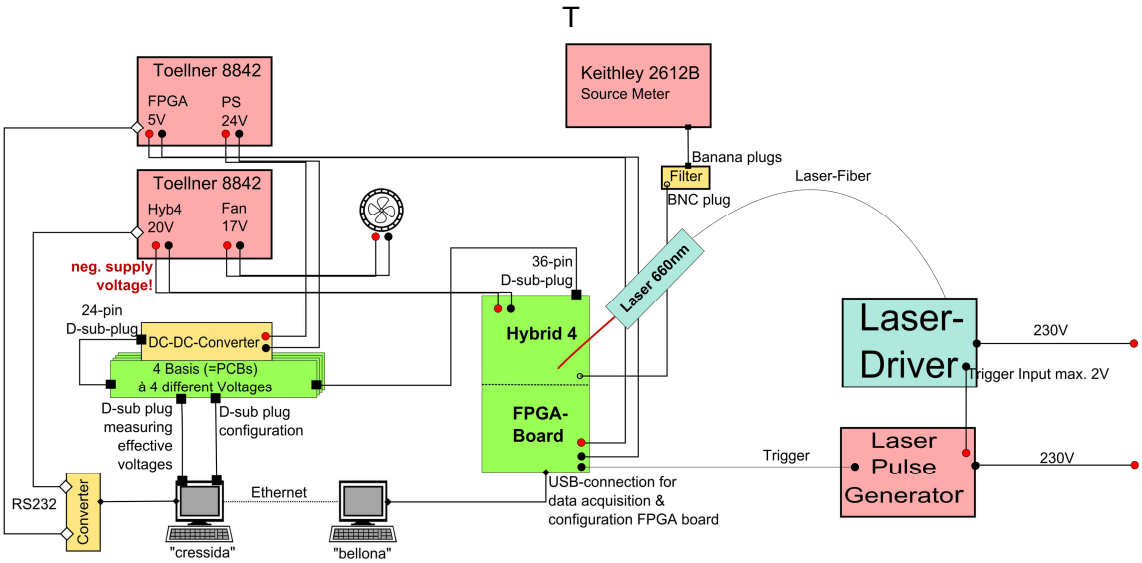


Figure 5-1: Experimental Set-Up for testing of the Gated Mode

5.2 Testing of Hybrid4 PCB components

Before starting with the Gated Mode analysis one has to ensure that the electronic read out system is working properly. First of all the matrix, the DCDB and SwitcherB chips have to be characterized individually before running the detector prototype operation.

5.2.1 PXD6-Matrix

The matrix was already tested on wafer-level showing no „shorts“ and no „opens“ (meaning: no interruption of conducting paths).

5.2.2 DCDB pipeline Characterization

The DCDB pipeline characterization starts with a digital functionality check in order to find the correct sample delay for the 8 DCDB columns[58]. The digital test injection comprises a particular pattern of constant input values. Next the transfer curves for each ADC channel are determined using a SMU for internal source calibration. The main task consists of determining the operational settings with respect to minimum noise. Ideal transfer curves should show smooth slopes within a certain bandwidth irrespective of a chosen ADC-channel.

5.2.3 SwitcherB Characterization

5.2.3.1 Programming of SwitcherB

As already mentioned, the SwitcherB offers different operation modes, which have to be programmed individually. The sequencer as part of the FPGA firmware is based on a RAM (“sequence-RAM”) that is sequentially reading out binary programmed sequences from a text file. In order to allow fast clocking the program sequence has to be arranged in 4 parallel sub-lines each containing 1 bit: one for the laser trigger, one for Strobe*Clear*, one for Strobe*Gate* und one for CLK. These 4 sub-lines are packed into one RAM-line accessible with a dedicated RAM address. The read-out time is inversely proportional to the frequency of the FPGA clock. In case of 320MHz one clock cycle corresponds to 3,125 ns. Accordingly one RAM-line is 16 bits wide and loaded every 12,5ns to the serializer (the serializer sends one sub-line every 3,125 ns to the SwitcherB inputs).

A second RAM (“address-RAM”), also 2 bytes wide and clocked with the same read clock as the “sequence-RAM”, allows to access specific addresses directly as well as programming loops and jumps in a very simple manner.

The read-out of one matrix row needs some time for various reasons: first a complete *Clear* requires at least 10ns to be finished [46]. Additionally, the *Gate* activation time, the reception of the drain currents and the rising and falling edges of the signals are putting constraints on the read-out speed. However, the main restriction comes from

[58] the DCDB pipeline is organized in 8 column groups (each containing 32 channels)

the DCDB since each of the 256 ADC pixels needs 32 clock cycles for generating a byte of data [63]. Hence at the compulsory frequency of 320 MHz the total read-out time sums up to 100ns for one row, resulting in 1,6 µs for one frame of the test setup. Selected rows will be turned on by changing voltage supplies from high voltage to low voltage (e.g. 3V to -2V vs source). The existing FPGA allows the storage of 8 subsequent frames.

5.2.3.2 SwitcherB oscilloscope measurements with test board

The bare SwitcherB chip in our experimental setup is embedded in a **ball grid array** (BGA)-substrate and connected with the mounting pads of a wire bond adapter. With a length of just 50µm the pads of this adapter are too small for the probe of the oscilloscope. Additionally, the matrix has to be protected from the sharp tip of the oscilloscope probe. Thus a test board must be mounted on the circuit, wiring the *Gates* and *Clears* of SwitcherB. This enables oscilloscope measurements of the self-programmed sequences of the Gated Mode for SwitcherB.

5.3 The Gated Mode Analysis

After insertion of the matrix on the Hybrid4 board a new analysis tool called “BonnDAQ” (see chapter 7.2.1) is used for various types of measurements. First, the correct mapping has to be determined with the help of digital test injections and thorough studies of the wirebonded connections between matrix and DCDB. Next, the pedestals of the drain currents have to be shifted to match the dynamic range of the DCDB. This is done by adjusting the current sources at the input or output node of the transimpedance amplifier *(VNSubIn* and *VNSubOut)*[59] as shown in Figure 3-10. An important issue will be the programming of the laser trigger in the FPGA verilog code. The next step is to calibrate the laser source. This is done in a two-fold way: by means of a radioactive source (Cd^{109}) and by measuring different pulse lengths and amplitudes directly with a laser power meter.

After the DCDB tests many additional voltages have to be adjusted. This again makes it necessary to find an optimal operation window. An automatic sweep tests different voltage combinations with respect to *ClearGate* and *ClearHigh/ClearLow* voltage. Additionally, the impact of different drain voltages (*GateOn/GateOff*) has to be investigated.

Special attention will be laid on pedestal analysis since it is essential for the PXD operation to find out, how long it takes to switch into the Gated Mode and return back to normal operation.

[59] *VNSubIn* is a much stronger current source than *VNSubOut* providing a coarse grain adjustment

6 DCDB pipeline Characterization

6.1 DCDB Test Software

Before starting with extensive test series a fundamental decision had to be made concerning the appropriate computer operating system. A natural and easy solution would maintain the existing openSuse[60] software: all needed programs and processes were up and running, in plain language at least at the beginning this would have saved a lot of time. Nevertheless the Belle II collaboration has decided to use Scientific Linux as target operating system and therefore it was advisable to pursue a more burdensome path at the start in exchange for hopefully fewer problems at the end.

The FPGA plays an important role as interface between DCDB and host computer. It delivers the steering signals *(CLK* and *SYNC_RESET*[61]*)* needed for synchronous data transfers, it facilitates the slow control and JTAG configuration of the ASICS, it decodes and filters the raw DCDB data and it temporarily stores the data for later transmission to permanent storage. Since the clock frequency between FPGA and USB microcontroller is by one order of magnitude lower than the envisaged target frequency of the DCDB, these functionalities have to be implemented directly in the FPGA firmware and not outside in a PC program code [67]. The ISE Design Suite from Xilinx enables the conversion of the verilog code into a *.bit*-file, a binary format which is required by Xilinx FPGAs containing all relevant configuration information for the circuit. For the testing of the DCDB a *top.bit* file already existed and it was not necessary to change anything in the firmware.

On the PC side a software suite developed at the university of Heidelberg establishes the connection to the FPGA and thus an indirect communication to the ASICs. It is compatible with all Linux operation systems adopting the C++ programming language and the Qt framework as graphical user interface. In principle, testing DCDB is nothing else than injecting some test sequences to the chip by varying the input signals and recording their output. Single channels can be analyzed via the integrated plot environment called *KUPE*, multiple channels are captured and analyzed with another program called *ADCAnalyzer*.

6.2 Digital functionality check

For debugging purposes and for finding the correct mapping of the matrix pixels the DCDB offers a very useful switch *TestInjEn* which injects a test pattern into the DCDB's digital logic block.

---

[60] openSuse belongs to the long list of Linux distributions

[61] the 320 MHz clock signal controls the serialization logic, whereas the *SYNC_RESET* signal is used as synchronous reset for the entire digital logic of the DCDB

A careful chip design ensures that the clock edge reaches all circuits of the DCDB chip simultaneously. Nevertheless any clock signal distribution structure introduces some signal delay, the so-called clock insertion delay which is approximately 2 ns for the DCDB [67]. This certainly causes problems for the synchronization of the data streams since it is in the order of the clock's period of 3.125 ns.[62] One method of circumventing this problem introduces some delay elements, extending the delay to exactly the next clock period. In this way the output signal can simply use the next edge of the same clock to sample the data signal. The FPGA program code already implements a fixed coarse grain adjustment to synchronize the inter-chip connection between FPGA and DCDB. However, some additional fine grain delay elements facilitate the fine-tuning of the valid sampling points.

The DCDB is organized in 8 columns each containing 32 channels.[63] Instead of a real analog to digital conversion an internal source injects a constant input value to the digital block. ADC channel 0[64] should show an output value of -127, channel 31 and 1 correspond to a value of 0 and all other channels of the digital test pattern should show an output value of $+127$. With the help of this pattern the sample delays for pairs of two columns were adjusted in ±75 ps steps and finally the exact position of the ADC channel "zero" in the byte stream was determined.

6.3 Conversion Algorithm

Analog to digital converters employ different coding techniques based on the same principle. The simplest method uses an iterative algorithm to determine the n-bit output of the ADC: as an example an 8-bit system digitizes the input range to 2^8 = 256 discrete measured values. The conversion process starts with the most significant bit (MSB). If the doubled input signal $2 \times I_{in}$ is larger than a specific threshold or reference current I_{ref}, the MSB is set to 1 and the threshold is subtracted, if it is lower, the MSB is set to 0. Next the residue signal I_{res} is multiplied by 2 and the same procedure is repeated in order to get the following bits until the operation is finished after 8 cycles. The reference current is set to the dynamic range of the ADC, which is defined as the difference between maximum and minimum input current $I_{ref} = I_{FS} = I_{max} - I_{min}$. Let us assume a threshold of 8µA and the detector measures a signal of 4.2 µA as illustrated in Table 6-1:

[62] assuming a frequency of 320 MHz

[63] in the DCDB reference manual the channels are referred to as pixels

[64] in electronics it is common to include the zero for counting purposes

Clock cycle	I_{res}	?	I_{ref}	Bit	Operation	I_{res}	?	$\tilde{I}_{ref}$	Bit	Operation
1	8.4	>	8	1	$(I_{in}-8)\times 2$	8.4	<	8.5	0	$I_{in}\times 2$
2	0.8	<	8	0	$I_{in}\times 2$	16.8	>	8.5	1	$(I_{in}-8)\times 2$
3	1.6	<	8	0	$I_{in}\times 2$	17.6	>	8.5	1	$(I_{in}-8)\times 2$
4	3.2	<	8	0	$I_{in}\times 2$	19.2	>	8.5	1	$(I_{in}-8)\times 2$
5	6.4	<	8	0	$I_{in}\times 2$	22.4	>	8.5	1	$(I_{in}-8)\times 2$
6	12.8	>	8	1	$(I_{in}-8)\times 2$	28.8	>	8.5	1	$(I_{in}-8)\times 2$
7	4.8	<	8	0	$I_{in}\times 2$	41.6	>	8.5	1	$(I_{in}-8)\times 2$
8	9.6	>	8	1		67.2	>	8.5	1	

Table 6-1: Example of a conventional converter with exact comparator (left) and with imprecise comparator (right in red) causing a reference current offset.

The resulting 8-bit code for 4.2 µA is 10000101.[65] Unfortunately the conventional conversion algorithm is very sensitive to the accuracy of the comparator. Small deviations causing the actual comparison level to exceed I_{ref} would expel the signal from the region of convergence. This type of error is called comparator offset.

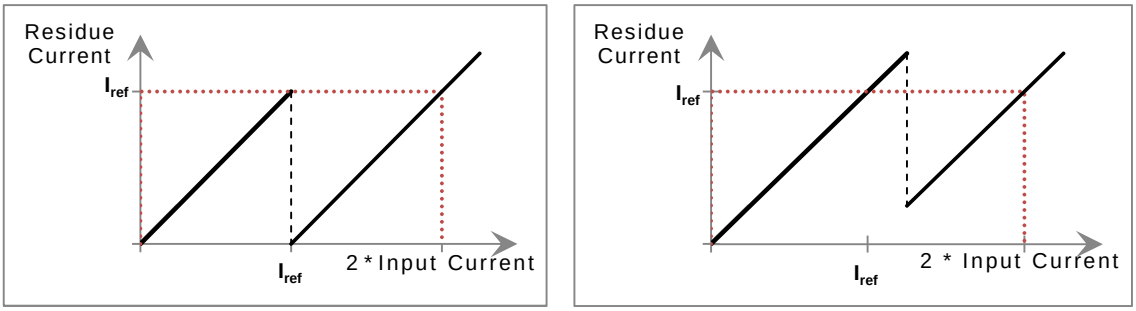


Figure 6-1: Robertson diagram [73] representing the transfer function of a conventional cyclic ADC. Left: precise ADC with no comparator offset. The horizontal axis plots twice the residual current being compared with the reference current. The vertical axis displays the updated residue current. Right: the ADC leaves the region of convergence contingent on a positive comparator offset where $\tilde{I}_{ref} > 2I_{res} > I_{ref}$. In contrast, if there is a negative comparator offset and $I_{ref} > 2I_{res} > \tilde{I}_{ref}$ the updated residual current could be less than zero.

Coming back to the above example, the actual comparison level of the ADC now should step up $+0.5\,\mu A$ to $\tilde{I}_{ref}$ instead of I_{ref}.[66] As soon as the residue drops out of the convergence region the result suffers from leaving the dynamic range with increasing

[65] this result looks sufficiently accurate since the whole input range of 8 µA is divided by 256 which gives a LSB value of 0.03125, consequently a digital value of 10000010 corresponds to an analog value of $(2^7+2^2+2^0)\times 0.03125 = 133\times 0.03125 = 4.1625$

[66] one reason for this offset might be some transistor mismatch in the comparator circuit

errors as can be seen in Table 6-1 (red). Only in cases where the comparator offset is less than ½ LSB the ADC residues would remain inside the convergence domain [74].

The DCDB pipeline digitizes the input currents with the more robust redundant signed digit (RSD) conversion algorithm [73]. Instead of one comparator level now two thresholds $\pm I_{th}$, symmetrically surrounding the old comparison level, are used. If the comparison takes place after the multiplication by two, I_{th} must lie between $[-I_{ref}, 0]$ and $[0, I_{ref}]$, respectively, and $2 \times I_{res} \in [-2 \times I_{ref}, 2 \times I_{ref}]$.[67] For the DCDB the comparison levels are set to $\pm I_{ref}/2$. If the input signal is larger than the upper threshold, the converter would produce an output code of 10 and the reference current is subtracted.[68] If the input signal is lower than the lower threshold, the output code is set to 01 and the reference current is added. If the input signal is in between the two thresholds, the bits are set to 00 and no arithmetical operation is carried out. Next the residue signal is multiplied[69] by two and the same procedure is repeated ,for 7 further conversions [63, 75].

$$I_{res_n} = \begin{cases} 2I_{res_{n-1}} - I_{ref} & if\ 2I_{res_{n-1}} > I_{ref}/2 \rightarrow 10 \\ 2I_{res_{n-1}} & if\ -I_{ref}/4 < 2I_{res_{n-1}} < I_{ref}/2 \rightarrow 00 \\ 2I_{res_{n-1}} + I_{ref} & if\ 2I_{res_{n-1}} < -I_{ref}/2 \rightarrow 01 \end{cases} \quad (6\text{-}1)$$

The comparator's accuracy or,, more precisely, the tolerance level for keeping the residue in the dynamic range has now increased to $\pm I_{ref}/2$.

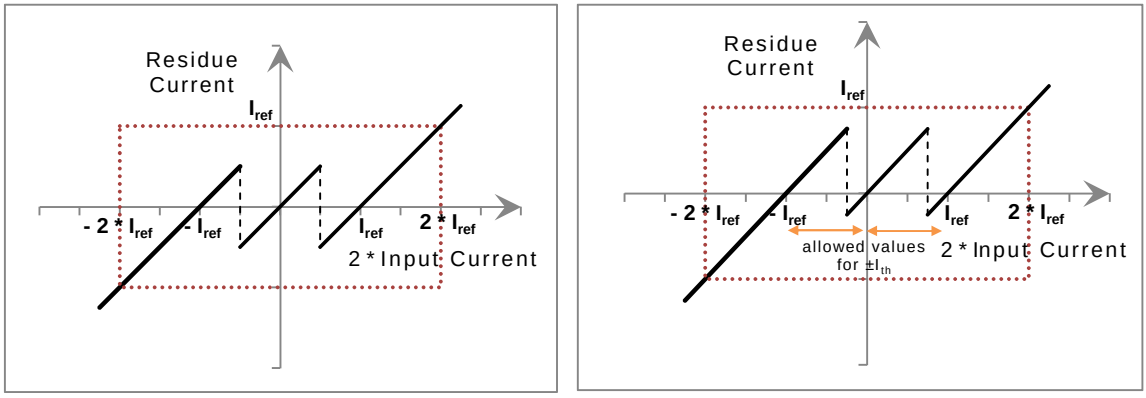


Figure 6-2: RSD converter with allowed values for the comparison current between $[0, \pm I_{ref}]$.

Before applying this approach to the example above several adjustments have to be made: the dynamic range changes from $[0\ \mu A, 8\ \mu A]$ to $[-4\ \mu A, +4\ \mu A]$, the input cur-

[67] the reference current is set to the difference between maximum and minimum input current divided by two $I_{ref} = I_{FS} = (I_{max} - I_{min})/2$

[68] the redundant signed digit algorithm is often referred to as 1.5-bit stage [99]

[69] effectively the residuals of the two current memory cells are summed up which is equivalent to a multiplication by two

rent changes from $4.2\ \mu A \rightarrow 0.2\ \mu A$ accordingly, and the comparison level is no longer $I_{ref}\ but\ I_{th} = I_{ref}/2$.

Clock cycle	I_{res}	?	I_{th}	Bit	Operation	I_{res}	?	$\tilde{I}_{th}$	Bit	Operation
1	0.4	in	±2	00	$I_{in} \times 2$	0.4	in	±3	00	$I_{in} \times 2$
2	0.8	in	±2	00	$I_{in} \times 2$	0.8	in	±3	00	$I_{in} \times 2$
3	1.6	in	±2	00	$I_{in} \times 2$	1.6	in	±3	00	$I_{in} \times 2$
4	3.2	out$_>$	±2	10	$(I_{in} - 4) \times 2$	3.2	out$_>$	±3	10	$(I_{in} - 4) \times 2$
5	-1.6	in	±2	00	$I_{in} \times 2$	-1.6	In	±3	00	$I_{in} \times 2$
6	-3.2	out$_<$	±2	01	$(I_{in} + 4) \times 2$	-3.2	out$_<$	±3	01	$(I_{in} + 4) \times 2$
7	1.6	in	±2	00	$I_{in} \times 2$	1.6	in	±3	00	$I_{in} \times 2$
8	3.2	out$_>$	±2	10		3.2	out$_>$	±3	10	

Table 6-2: Example of a RSD converter with exact comparators (left) and with comparators shifted by $\pm I_{ref}/4$ (right in red) still ensuring that current residues remain inside the convergence domain.

If the comparator offset level even rises by 1 from $2 \rightarrow 3$ as highlighted in Table 6-2, the 8-bit ADC delivers exactly the same result as an ideal converter. Note that this is not generally valid for all input currents, but the ADC at least remains in the region of convergence for comparison levels $I_{th} \in [0, \pm I_{ref}]$.

The last step is the conversion of the entire array containing the RSD code into standard binary code:

Starting with the MSB, a 10 is consistent with a binary 1, if the result is a 00 the MSB matches a binary 0 and if the first RSD code delivers 01, a zero is shifted to the left and the two's complement of one is added to it. For the remaining bits the following holds: a 10 is treated as a shift to the left and adding a one to the code (multiply by one and add one), a 00 corresponds to multiplying by two which means shifting to the left and adding 0 to the code, a 01 would multiply the code by two and subtract a 1, in other words decrement the binary code by one LSB.

RSD									
								0	
00							0	0	shift left, add 0
00						0	0	0	shift left, add 0
00					0	0	0	0	shift left, add 0
10				0	0	0	0	1	shift left, add 1
00			0	0	0	0	1	0	shift left, add 0
01		0	0	0	0	1	0	0	shift left
		1	1	1	1	1	1	1	add 2's compl.
		0	0	0	0	0	1	1	
00	0	0	0	0	0	1	1	0	shift left, add 0
10	0	0	0	0	0	1	1	0	1 shift left, add 1
	0	0	0	0	0	1	1	0	1 signed code
	1	0	0	0	0	1	1	0	1 unsigned code

The RSD algorithm implements the subtraction by adding the two's complement of 1 or equivalently inverting all the bits encountered before the first bit set to one, including

the present [73]. The described procedure delivers the signed[70] code. To obtain the unsigned code, I_{ref} corresponding to $MSB = 1$ has to be added. An 8-cycle quantization of the input signal produces 8 pairs of bits in redundant format which is equivalent to $8 + 1$ bits in standard binary format.[71] Compared to the conventional converter example the RSD conversion now turns over $100001101 = (2^8 + 2^3 + 2^2 + 2^0) \times \frac{8}{512} = 4.203125\mu A$ for both ADCs. The accuracy of the current duplication and reference subtraction/addition no longer depends on the threshold values, unless the threshold offsets are within $\pm I_{ref}/2$.

The logic implemented in the digital part of the DCDB follows a conceptually different method proposed by [76] for "on-the-fly" serial translation of redundant signed digits into two's complement binary format. However, the result should be exactly the same.

6.4 ADC Error Sources

As mentioned in chapter 3.6.1.2 even a perfect linear transfer function shows some error, resulting from the quantization of a continuous signal into a limited number of digital output codes. The deviation for an ideal ADC is $\pm 1/2$ LSB. The minimum quantization error can be calculated assuming an ideal converter with step width $q = 1\ LSB$ and uniformly distributed probabilities $p(\epsilon) = \frac{1}{q}\ for\ \left(-\frac{q}{2} \le \epsilon \le +\frac{q}{2}\right)\ otherwise\ p(\epsilon) = 0$ as

$$minimum\ quantization\ error = \sqrt{\frac{1}{q}\int_{-q/2}^{q/2} \epsilon^2 d\epsilon} = \sqrt{\frac{q^2}{12}} = \frac{LSB}{\sqrt{12}} \qquad (6\text{-}2)$$

The quality of an ADC can be assessed by static and dynamic performance parameters. The Gated Mode operation measures a relatively static, DC-like input signal, therefore the first category is considered the most important. Major static parameters include the offset error, gain error, nonlinearities and static noise. The offset error is defined as the difference between the ideal and actual output value when the digital output code is zero [77]. It will be treated analog to the DEPFET's pedestal currents described in 7.2.2.2 and corrected by the offline analysis software [54]. Similarly, gain variations representing a difference in the slope of the actual and ideal transfer function are corrected offline.

The differential nonlinearity (DNL) is defined as the difference between the actual step width and the ideal code bin width which is $1LSB$ divided by the ideal code bin width [78]:

[70] the signed binary code uses the MSB to discriminate whether the number is negative (MSB = 1) or positive (MSB = 0)

[71] for the DCDB the amount of digital output pads is limited, hence the least significant bit (LSB) conversion is omitted, implicitly accepting a reduced digital conversion accuracy by a factor of $1/n$ [49]

$$DNL_k = \frac{(T_{k+1} - T_k) - LSB}{LSB} = \frac{T_{k+1} - T_k}{LSB} - 1 \qquad (6\text{-}3)$$

with $T_{k+1} - T_k$ the width of code bin k. DNL characterizes the ADC's precision, in other words its ability to relate a small change of the input current to the correct change in the code conversion. Perfect differential nonlinearity coincides with $DNL = 0$. $DNL_k \leq -0.9$ indicates that the ADC has missing codes as shown in Figure 6-3: an infinitesimally small input current change between two adjacent digital codes causes an output change of at least two codes, with the intermediate code never being set. Additionally, if an ADC is giving a lower conversion result for a higher input stimulus the ADC is said being non-monotonic or inverting.

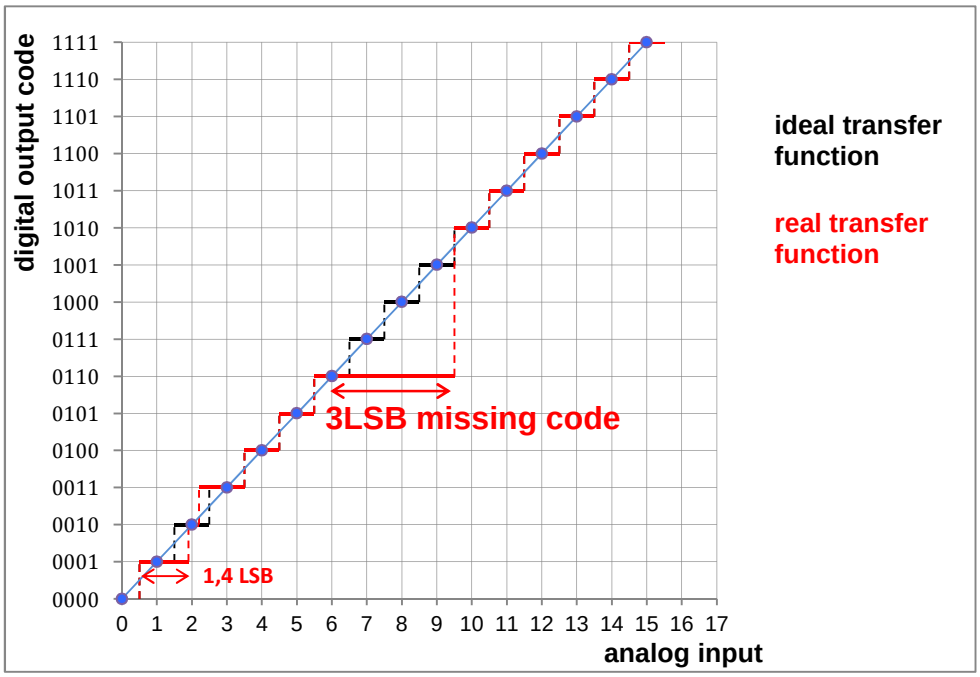


Figure 6-3: Differential Nonlinearity (DNL) with missing code

The integral nonlinearity (INL) is defined as the deviation, expressed as a percentage of the full scale range, or in units of LSBs, of the actual transfer function from a straight line. The DCDB test algorithm uses a straight-line fit as shown in Figure 6-4 in order to determine the closest approximation to the ADCs actual transfer function.

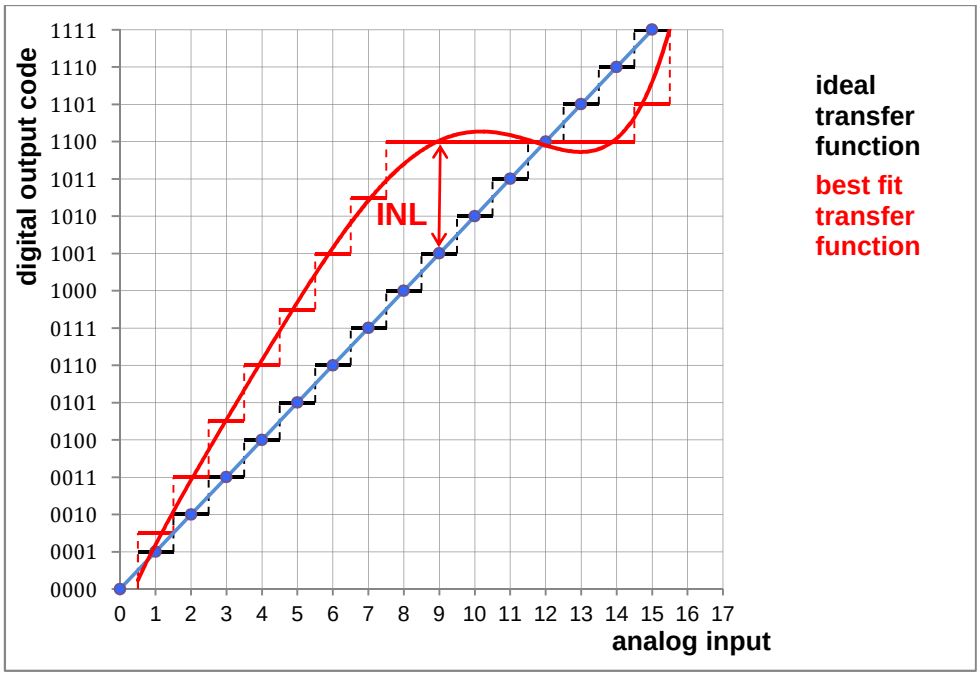


Figure 6-4: Integral Nonlinearity (INL) showing some curvature

In contrast to DNL the output code deviates from the ideal location instead of the ideal width. Both terms can be related by the following formula:

$$INL_m = \sum_{k=1}^{m} DNL_k \tag{6-4}$$

Fundamentally INL represents the curvature in the actual transfer function relative to the ideal transfer function.

RMS noise (including random noise and quantization error) is any deviation between the output and input signal except for deviations caused by linear time-invariant system responses or DC level shifts [78]:

$$RMS\ noise = \left[\frac{1}{n}\sum_{i=1}^{n}(y_i - \bar{y})^2\right]^{1/2} \tag{6-5}$$

with n the number of samples in the data record, y_i the sample data set and $\bar{y}$ its mean value.

6.5 ADC characterization

6.5.1 Optimize Settings

The determination of the correct settings to run DCDB pipeline properly is a very complex and time consuming task.[72] In theory all 25 **DAC settings** depicted in the input mask of Figure 6-5 permit an integer value[73] between 0 and 127. This alone would give 127^{25} different possibilities. Moreover including all other 40 configuration bits of the global shift register (most of them are illustrated as check-boxes in Figure 6-5) and adding the external power supply with 6 different DCDB voltages (see Table 6-3) one clearly realizes that a systematic scan would not be feasible in reasonable time[74]. Fortunately the designer building on his rich experience and detailed chip knowledge delivered an initial setting serving as an excellent starting point. Additionally, only DAC values marked as *Important!* in the DCD-Bv4-Pipeline Reference Manual [63] exert significant influence on the conversion result. Some of the important DACs are deliberately kept at 0 or at another fixed value, hence ultimately only the following 6 parameters were picked out for further optimization: *RefIn, DCDRO-VDD, DAC IFBPBias, DAC IPSource, DAC IPSource2, DAC IAmpPBias.*

Supply Voltage	Value
RefIn	0.9 V
DCD_AVDD	1.8 V
DCD_DVDD	1.8 V
AmpLow	0.4 V
DCDRO_VT	0.9 V
DCDRO_VDD	1.8 V

Table 6-3: Supply voltages for DCDB pipeline measurements

[72] the whole DCDB analysis was performed without any DEPFET sensor attached

[73] the full scale DAC current is 10 µA

[74] bearing in mind that one KUPE plot takes on average 30 seconds

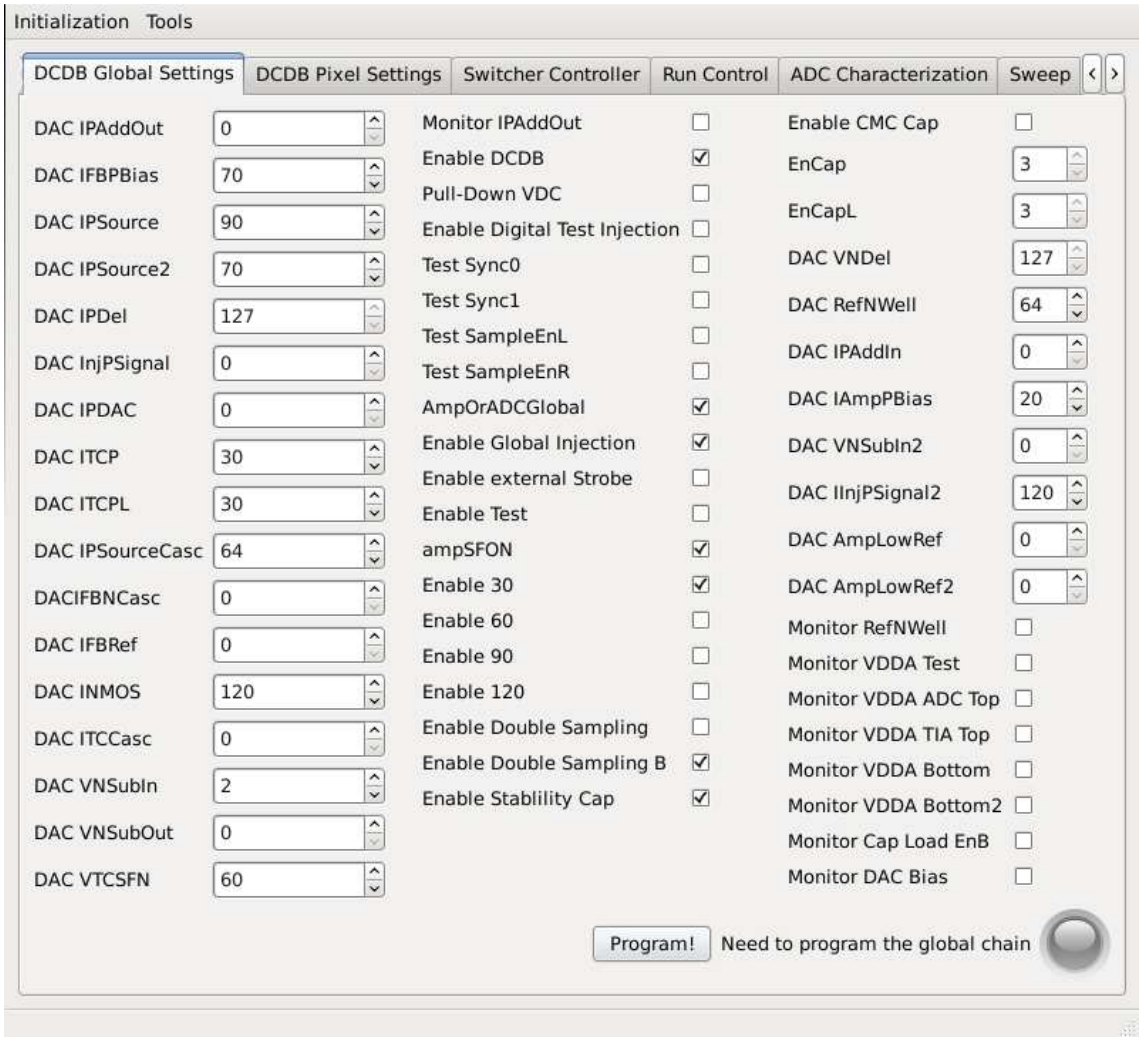


Figure 6-5: DCDB pipeline optimized settings

The next step is figuring out which error parameter should be minimized in order to avoid conflicting goals. For this analysis the signal noise measured in ADUs was chosen to be most important. It is calculated separately for every input signal by the standard deviation of all samples[75] relating to that particular signal. For the evaluation of the accuracy of a DCDB's ADC channel the signal noise should be kept well below 1 ADU.

In principle test input signals can be sent to the ADC channels from an internal current source via its monitor bus or from an external SMU to one of the wire bonded input channels. However, the internal source generates much faster and less noisy signals. Nevertheless a SMU is necessary for calibration purposes though the link must be decoupled after calibration in order to avoid interference noise. The following procedure proved to be very useful:

[75] for each ADU 100 measurements were performed, in more specific terms this means that each time the 3 internal sources increment the current by one DAC unit (until the maximum of 3x128=384 DACs corresponding to 30µA), 100 samples are taken out and get averaged

- Select a “bad” (=noisy) ADC channel using the KUPE plot program, which displays the transfer curve, INL and noise of the respective channel as shown in Figure 6-6.
- Try to change by ±10% every DAC setting as well as RefIn and DCDRO_VDD in 0.1V steps in an interval between, respectively, 0.8-1.2V and 1.8-2.2V.
- Take notes:
  - Are the characteristics improving/worsening (e.g. noise spikes, INL spikes missing codes, bumps etc.)?
  - Does the setting variation change the nonlinearity for negative values?
  - Is there any change in the minimum ADC code?
  - Is there any improvement/deterioration for some other channels?

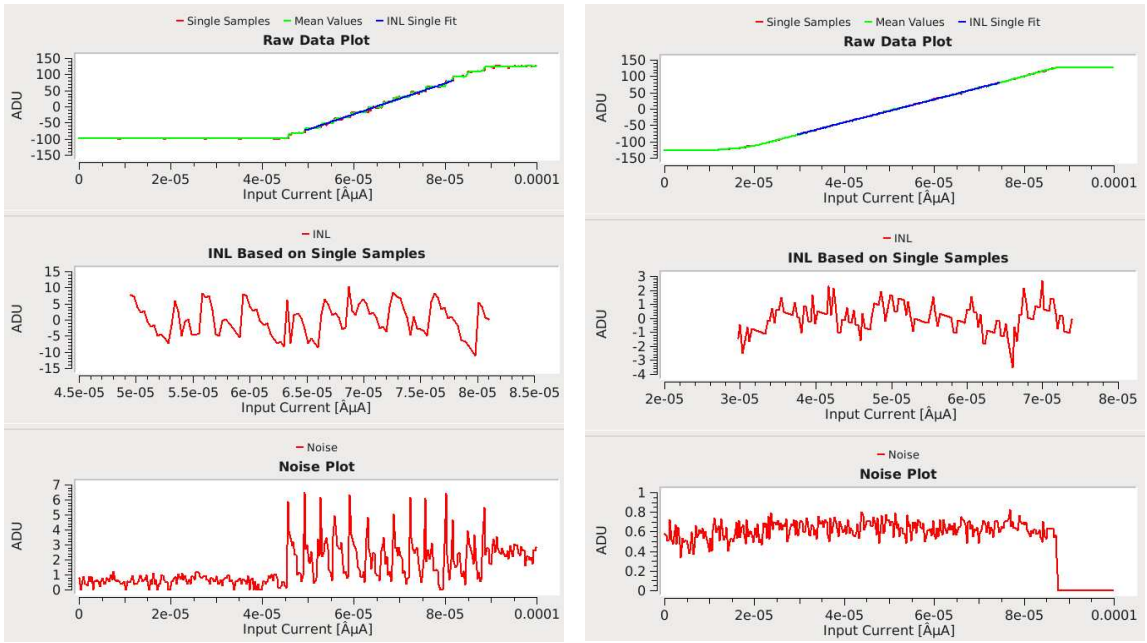


Figure 6-6: Left: Bad ADC channel with high INL and high noise. Right: Same ADC channel after settings optimization. The x-axis does not represent input currents as misleadingly shown in the diagram, but arbitrary units subdivided into 384 steps from $0\ to\ 100 \times 10^{-6}$. Since the whole internal current source adds up to 30 µA, one unit corresponds to about 78.125 nA. Accordingly, a x-value of 6×10^{-5} corresponds to an input current of 18 µA.

In total there are at least 2025 different settings (5 per each power supply parameter and 3 per each DAC value). Since even small DAC variations sometimes showed a strong impact on the transfer curve characteristics the optimization was performed also on intermediate values. The final settings are shown in Figure 6-5.

6.5.2 Analyzing the ADC Transfer Curves

When optimizing a certain ADC channel it was frequently observed that the ADC characteristics of other channels suddenly deteriorate. This is mainly due to statistical process variations within the ASIC, like different doping concentrations or transistor mismatches. Another reason for this observation might be a distinct voltage drop on the power support rail as shown in Figure 6-7. Since the DCDB channels are organized in a 16×16 matrix (as seen in Figure 3-9) and the support lines must be kept small because of area constraints the more distant channels get less power.[76]

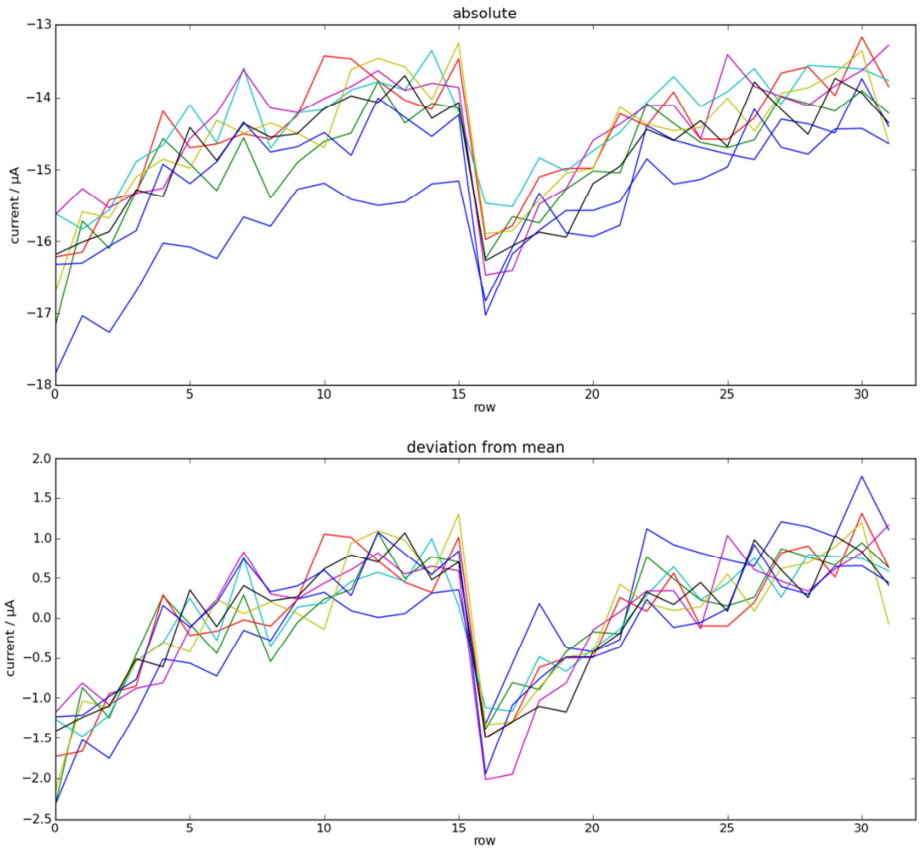


Figure 6-7: Current variations of DCDB channels. The lines represent the eight DCDB columns containing each 32 channels organized in a double row. Most distant channels (15 and 31 get the least power; note that these are negative currents)

[76] this problem should be fixed with the next DCDB version by connecting the gate of the nMOS sources in only one point [101]

Figure 6-8 shows the set of 256 transfer curves superimposed[77] on each other using the optimal settings as shown in Figure 6-5 and listed in Table 6-3. For an ideal ADC the parametric current sweeps should generate a straight line within its operational range. The offset variation can be estimated at ±1.5 µA around mid-range. This can be easily compensated by the current sources *VNSubIn/VNSubOut* as well as *VNAddIN/VNAddOut* and/or the 2-bit DAC shown in Figure 3-10. All parameters are expressed as a function of an arbitrary ADC channel index which are sorted by the respective position on the chip.

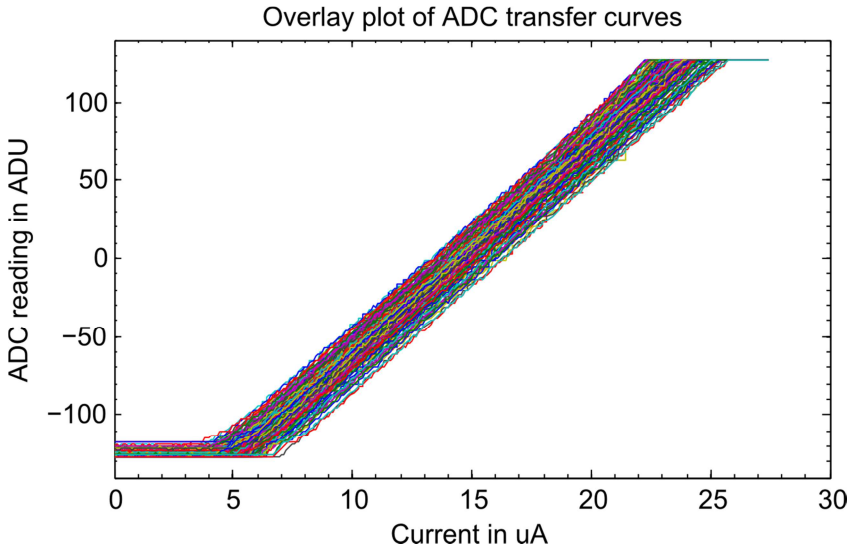


Figure 6-8: Multi-channel ADC Transfer Curves

The ADC gain as shown in Figure 6-9 is defined as the reciprocal of the slope of the transfer curve and expressed in *nA/ADU*. It is roughly in the range between 72 – 78 *nA/ADU*. The sawtooth shape might suggest a small gradient potentially caused by a voltage drop on the supply rails. The slope is taken from a straight line fit.

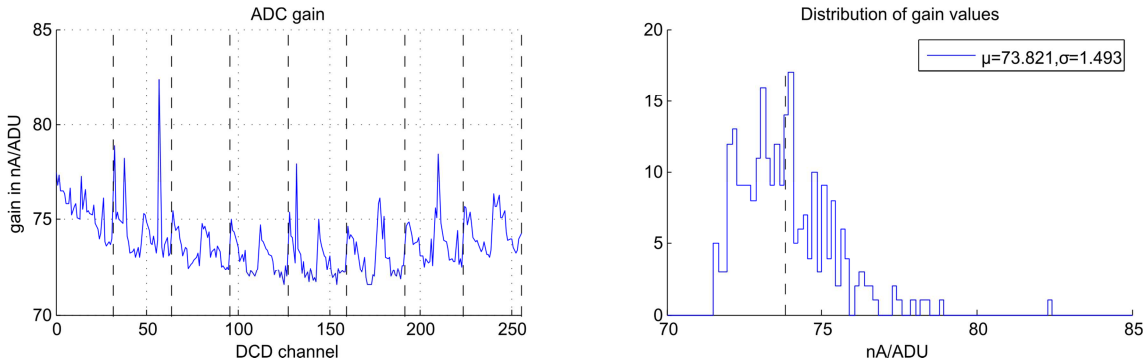


Figure 6-9: Gain of all ADC channels (left) and Distribution of gain values (right)

[77] the calibration current can only be fed into one selected channel

The mean noise shown in Figure 6-10 is well contained below 1 ADU with a few outliers reaching a maximum value of 1 ADU. The mean value is around 0.6 ADU.

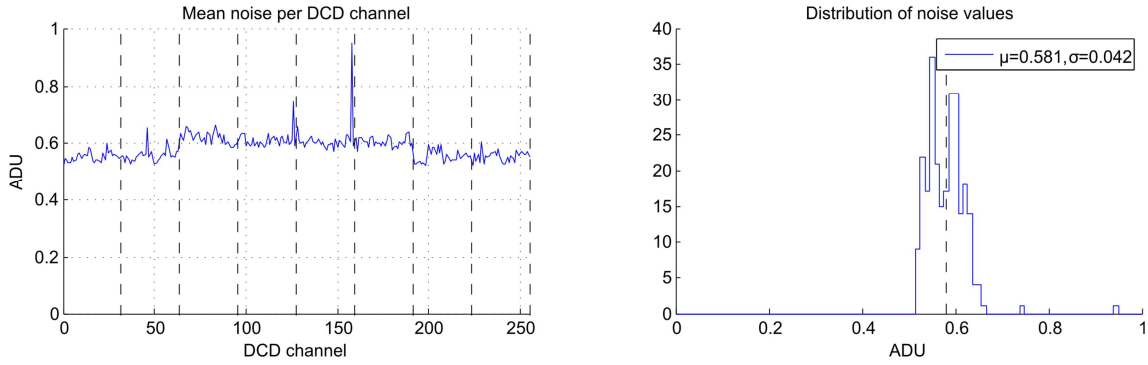


Figure 6-10: Mean noise of all ADC channels (left) and distribution of noise values (right)

A significant problem arises from the analysis of INL and DNL for some channels, although this is hardly recognizable in the transfer curve diagram because of the overlay by other channels. A closer look to the region with an input current at 21.5 µA and the output at +63 reveals a small bulge. This bulge is zoomed in for one channel in Figure 6-11.

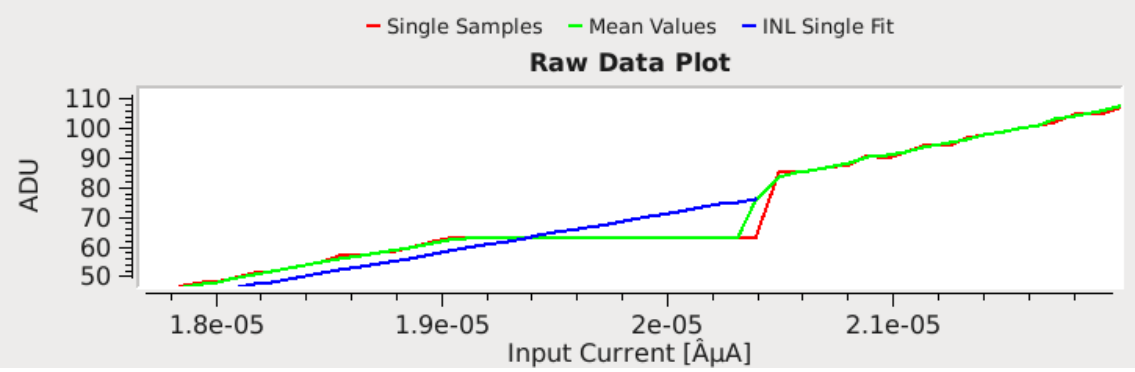


Figure 6-11: Large missing code for one ADC channel (zoomed KUPE plot)

A comprehensive DNL representation for the whole DCDB is shown in Figure 6-12. None of the ADC channels shows a DNL < 1 which strongly suggests the existence of missing codes. The question arises at which level a higher DNL would be considered as problematic. A DNL of 2 corresponds to 2 ADU or approximately 150nA which is equivalent to a signal of 375 electrons. On the other hand noise is about 110 electrons (0.6 ADU)[78] and 6 σ is equivalent to 660 electrons. In practice the threshold for detecting some signal will not be set below 1000 electrons so a reasonable estimate for problematic DNL would be in the range of 5 ADUs. Unfortunately almost 25% of all ADCs have INL and DNL equal to or well beyond 5 with a peak value 15.

[78] assuming a gain of 72 nA/ADU and an internal amplification of $400\ pA/e^-$

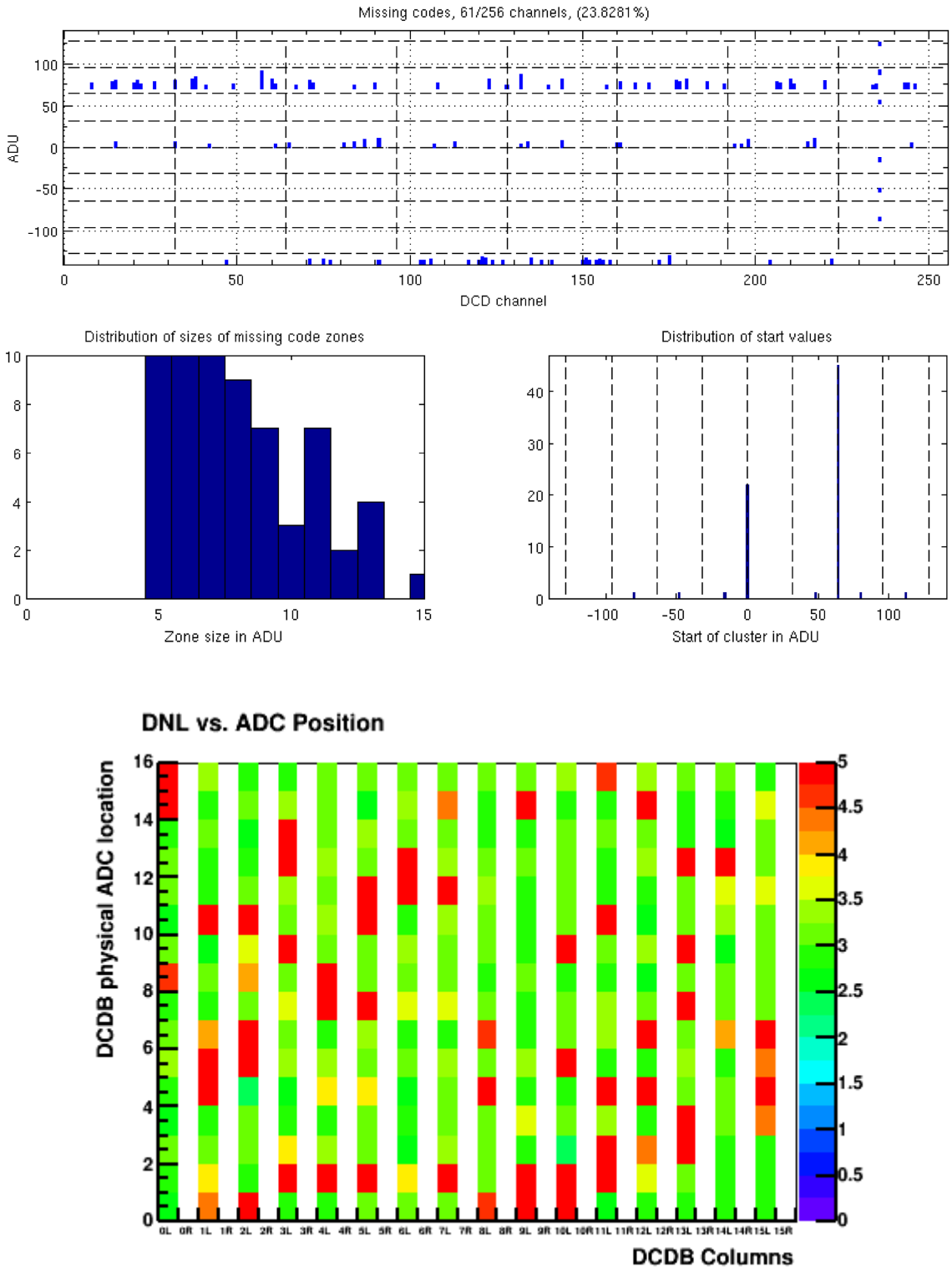


Figure 6-12: Top: Missing codes per channel and ADU area. Middle left: Distribution of the sizes of missing codes. Middle right: Clustering of missing codes at certain ADU values. Bottom: Distribution of missing code pixels over a full matrix.

Missing codes

The origin for this long missing code problem might be located in the ADC unit of the DCDB chip[79]. Each ADC unit consists of a double cell block containing two current memory cells and two comparators (CompLo, CompHi) [79, 80]. The comparators are only connected to the voltage output of the first memory cell. The second memory cell is used for copying the input current after the subtraction of a 12µA input offset. The current stored in the first memory cell will be copied to the comparators where a threshold current will be added (CompLo 14µA, CompHi 10µA). Taking into account the input offset the current flowing into CompLo/CompHi is, respectively, 2µA and -2µA. Depending on the input current size (too low or too high) the comparators generate a signal for adding, subtracting or disabling a reference current (4µA) to the input current of both memory cells. This procedure should ensure that the residue currents in cells 1 and 2 cover just half of the full signal range for an input signal within $\pm 2I_{ref}$.

As a consequence the residuals of both memory cells can be summed together which is equivalent to multiply the output current by two. The result is stored into subsequent cells as required by the conversion algorithm described in chapter 6.3. Hence the conversion result depends only on the precision of the multiplication and the precision of adding/subtracting I_{ref}. It does not rely on the accuracy of the comparator, provided its thresholds guarantee that the output residue currents occupy half the range after conversion.

Now let us assume that there is a larger mismatch between the original transconductor[80] in the first current-memory-cell and the copy transconductor of the comparator. Due to the complex design of the transconductor even a small mismatch between transistor NFB1 and NFB2 in the copy transconductor, shown in Figure 6-13, can cause a critical change of the threshold voltage. As an example a positive input current of 5u[81] should flow (notice that the reference current direction is out of the transconductor). The mismatch between NFB1 and NFB2 amounting to 3u would erroneously keep the comparator in idle state with $I_{comp} = 0$ although it should generate a TooHigh signal. The output current will no longer be within half of the input range, ultimately leading to missing codes.

[79] a DNL increase for shorter sampling times was already observed for older DCD versions [34]

[80] also called U-I converter responsible for converting a voltage into current

[81] u = unit (µA)

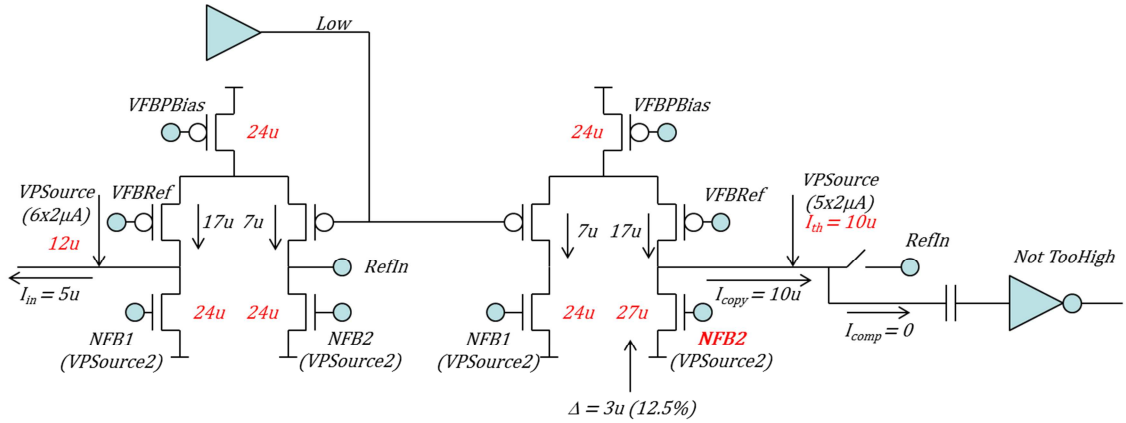


Figure 6-13: Transistor level schematics of the transconductor for one CMC and one Comparator. The devices are controlled by the bias voltages[82] *VFBPBias, VPSource, VPSource2, RefFB* and *RefIn* (fixed bias currents in red, variable signal currents in black). A nMOS transistor mismatch in the copy transconductor (NFB2) which is only in the order of $3/24 = 12.5\%$ can cause a critical change of the threshold voltage and lead to missing codes.

If the effective threshold for TooHigh is larger than 4u (in the above example at $5u = 2u + \Delta u$) and the input current is between 4u and the threshold one gets always the following result: MSB (TooHigh) would be 00 instead of 10. The current gets duplicated and in all further cycles a TooHigh is recorded. The bit sequence for TooHigh is 0111_1111 corresponding to a value of 63. There are some ways of mitigating this problem for individual channels by changing biasing parameters as, for example, increasing the *IPSource* current or decreasing *RefIn* (if missing codes are predominantly observed in the +63 ADU area) but this could also have a negative impact on other parameters like noise.[83] At the end this problem should be fixed with the next chip version, where among other things larger nMOS transistors NFB1 and NFB2 are planned. nMOS transistors which serve as a current sink are more difficult to design because they must be constructed radiation hard as **enclosed transistors**[84], and increasing the transistor size may be difficult because of constraints on the acceptable area of the chip.

[82] note that *VPSource* and *VFBPBias* are current sources, whereas *VPSource2* is a current sink

[83] especially for *RefIn* there is a tradeoff if there are missing codes on both +64 and -64 ADU

[84] in contrast pMOS transistors serve as current sources and are much easier to design radiation hard; as a rule of thumb for pMOS the source potential > drain potential whereas for nMOS ist exact the other way around

7 The Gated Mode Operation

7.1 Conceptual Approach for testing of the Gated Mode

The effectiveness of the Gated Mode operation can be tested by answering two questions:

A. Is it possible to preserve charge in the internal gate during the Gated Mode?
B. Does the Gated Mode effectively shield the internal gate from junk charge generated by noisy bunches?

Both questions will be answered separately with two different experiments labeled experiment A: Signal Charge Preservation (SCP) and experiment B: Junk Charge Prevention (JCP). As a condition for the delivery of meaningful results an optimized operation point for the matrix biasing has to be found. This is achieved via sweeping the following voltages: *GateOff*, *ClearHigh* and *Cleargate*. The optimization goal consists of minimizing the lost charge during the Gated Mode.

To evaluate if the Gated Mode works, a laser pulse is impinged on the backside of the DEPFET sensor and 8 DEPFET frames are consecutively read out, each with a particular sequence. The different sequences are abbreviated as follows: *Read & Clear* (C), *Read no Clear* (R) and *Read no Clear + Laser* (RL). Concerning the Gated Mode there are four possibilities: Gated Mode with readout (GR), Gated Mode without readout (G), Gated Mode with readout + Laser (GRL) and Gated Mode without readout + Laser (GL).To avoid *Clear* pulse toggling on drain currents during sampling, *StrC* sets in as late as possible and is kept very short[85] (12.5 ns). Previous studies on a predecessor readout chip provided some evidence that parasitic capacitances between *Drain*, *Gate* and *Clear* lines generate overshoots and undershoots directly after switching the steering signals [54]. Since the period of data sampling takes 30 ns (out of the 100 ns required to read out a full row) a too early *Clear* pulse could influence the data sampling and lead to wrong pedestal calculations.

Even if both experiments deliver satisfactory results there is another complication, since the Gated Mode operation is afflicted with a severe time constraint. As stated earlier the noisy bunches pass the detector every 10 µs. The whole cycle, switching into the Gated Mode → switching off the Gated Mode and return to normal operation must occur significantly below this limit, otherwise there is nothing won. In particular high pedestal variations immediately after returning to normal operation distort the signal data and must be studied carefully.

[85] theoretically the clear pulse can be shortened to 3.125, but then a very high clear pulse is required for a complete clear

7.2 Processing Chain

7.2.1 DEPFET Readout System

The data acquisition system (DAQ), internally referred to as “Bonn-DAQ” [81], integrates the whole detector prototype system to the PC. Its main components consist of

- a powering up/down sequence
- a LINUX based USB driver connecting to the FPGA board
- a DEPFET Producer responsible for the configuration of the DEPFET module (hybrid board and FPGA board) as well as steering and control of the data acquisition
- a USB readout client transferring the data to the *Event Builder*, which assembles complete matrix data and stores them into a shared memory buffer
- an event server sending the DEPFET data to consumers like the *Data Quality Monitor* (DQM) or to the *File Writer* (local disk).
- a *Run Control* server with GUI based *Run Control Client* executing different input commands (e.g. start/stop monitor, reload file settings, write to the file writer, exit program)

DQM is responsible for the online data processing on a graphical user interface with hit reconstruction, pedestal and noise analysis, common mode correction and cluster reconstruction. All these items are explained in the next chapter. Additionally, the DQM allows to find most of the DAQ and DEPFET matrix problems during the run.

The file writer will be used to record triggered frames from the ring buffer of the FPGA for further offline analysis: from a theoretical viewpoint the FPGA could immediately process all data transferred from the DCDB. However, the USB 2.0 interface for PC communication creates a bottleneck since the data throughput is around two orders of magnitude lower than the data production rate of the DCDB at target speed. For that reason a triggered readout scheme is applied implemented at FPGA level. If the trigger is activated the FPGA records 8 subsequent frames, then stops recording and transfers the raw data to the PC. This package is labelled as one *event*. After about 30 milliseconds the trigger is activated again and the whole process is repeated. The necessary off-line analysis is explained in the following chapter.

7.2.2 The Gated Mode Analysis Tool

7.2.2.1 Data Conversion

The data coming from the FPGA will be stored in a binary *.dat*-file to the computer. For further processing it must be transformed to a suitable file format. However, a self-programmed solution would be a waste of time. A much easier way to convert native

DEPFET data comprises the adaption and integration of parts of the **LCIO**[86] persistency framework and event data model to the Gated Mode analysis tool. Among many other things the LCIO framework defines a concrete file format (*.sclio*-file) to store the data more efficiently. Additionally, a C++ interface is provided to read and write LCIO data files [82]. Besides serving as a persistency framework for the next linear collider physics and detector response simulation the model has been extended to support test beam data, vertex reconstruction and many other applications [83]. A program called *Converter* integrates some useful functional blocks of the LCIO framework. Its only function is to convert the native binary *.dat*-file to a *.sclio*-file. The *.sclio*-file contains all ADC values of the 2048 matrix pixels delivered from the DCDB. Furthermore it also includes the name of the detector, the event and frame number and the size of the matrix in a run header.

7.2.2.2 Pedestals, Noise and Common Mode Correction

The next step in the process chain is performed by a program called *Data Processor* [84]. As the name implies this program unlocks the ADC values from the LCIO file and reassembles the pure charge signal to two-dimensional color plots and many useful histograms. It also connects to **ROOT** as a very powerful analysis tool for particle physics developed by CERN.

The measured signal S^{meas} of pixel ij (where i denotes the row and j denotes the column) is composed of four independent contributions: the pedestal value S_{ij}^{ped}, the input referred noise $N(\sigma_{ij},0)$[87], the common mode correction $N(\sigma_j,0)$ and the pure charge signal S_{ij}^{sig} [44]:

$$S_{ij}^{meas} = S_{ij}^{ped} + N(\sigma_{ij},0) + N(\sigma_j,0) + S_{ij}^{sig} \qquad (7\text{-}1)$$

Pedestals Calculation

It is not possible to construct all constituents of the DEPFET matrix exactly identical with respect to their geometrical dimensions, doping concentrations etc. Even small variations within these parameters can lead to considerable discrepancies between measured drain currents[88]. A recent study at HLL determined the range of pedestal spreads between 14 to 25 µA where, depending on the gain setting, the latter covers more than the full dynamic range of the DCDB chip [85]. Accordingly it must be adjusted with the 2-bit DAC of the DCDB for pedestal correction. For the calculation of the right pedestal value two conditions must hold: first the assumption that the pedestal offset is constant over many frames for each pixel and secondly the mean of the input noise and common mode noise should be normally distributed or, equivalently, inde-

[86] Linear Collider I/O

[87] $N(\sigma,0)$ are normal distributed random numbers with mean 0 and standard deviation σ with individual numbers for each pixel (or row) or equivalently the oscillation of the signal distribution around its baseline

[88] in addition to statistical process variations ionizing radiation damage can have a significant impact on pedestal currents [102]

pendent of each other with mean zero. Otherwise there is no chance to correctly resolve the influencing quantities. Taking into account the conditions above the pedestal value can be estimated averaging the measured signal over a number n[89] of so called dark frames[90], these are frames without signal:

$$S_{ij}^{ped} = \frac{1}{n}\sum_{k=1}^{n}\left(S_{ij}^{meas}\right)_k \tag{7-2}$$

The achievable precision in the estimate is given by [44]:

$$\sigma_{ped} = \sqrt{\frac{\sigma_{RMS}^2 + \sigma_{CM}^2}{n}} \tag{7-3}$$

Accordingly averaging over $n = 1000$ frames improves the precision by a factor of 33 compared to the combined common mode and input noise.

Common Mode Correction

The common mode correction adjusts for the row-wise correlated noise caused by the row-wise readout of the pixel matrix. In contrast to the pedestal noise, which is an intrinsic characteristic of silicon sensors, this is an external perturbation as for example rooted in the instabilities of the power supply or due to an electromagnetic pickup. As an example a sudden pickup current couples on the *Gates* which would lead to an increase of the current for the whole row. The common mode noise can fluctuate heavily from row to row and from event to event, but it is assumed to be totally correlated within a row for any given event. To perform the common mode correction the row-wise average is subtracted after the pedestal subtraction:

$$N(\sigma_j, 0) = \frac{1}{\#col}\sum_{j=1}^{\#col}\left(S_{ij}^{meas} - S_{ij}^{ped}\right) \tag{7-4}$$

The common mode and pedestal corrected raw signal finally gives the signal value. From a methodological point of view this approach might be questionable for a row containing just 128 pixels. As a more robust mean estimator one can alternatively use a truncated mean[91] or the median, which is resistant to outliers.

Input Noise

As a last step the input noise of the signal is determined. Even for DC input signals the internal circuitry of the ADC produces a certain amount of root-mean-square (RMS)

[89] 1000 frames as a standard for gated mode analysis

[90] in order to exclude the influence from daylight some opaque membrane was put over the hybrid4 board and the dark box encompassing the whole device was closed

[91] excludes values above a certain threshold (e.g. 2 to 4 % of the highest pixel measurements)

noise due to resistor noise and thermal noise also referred to as kT/C noise[92] [86]. The randomly distributed output codes are centered around the nominal DC input value and can be expressed in a histogram which is approximately Gaussian. The standard deviation of the histogram is calculated corresponding to the effective RMS noise.[93] This usually has an impact on the choice of the threshold, since the threshold has to be sufficiently above the noise in order to avoid large noise occupancy for the detection of a signal. Assuming that $S_{ij}^{ped,CMC}$ are common mode and pedestal corrected measurements:

$$Noise\ (i,j) = \sqrt{\frac{1}{n}\sum_{i=0}^{n}\left(S_{ij}^{ped,CMC} - \overline{S_{ij}^{ped,CMD}}\right)^2} \tag{7-5}$$

The individual noise of each pixel is not further reducible. If the pedestal value of a specific pixel exceeds some threshold value *(bright pixels)* this pixel gets masked from further analysis. Additionally, a further cut is introduced for pixels showing a significant RMS compared to the average *(hot pixels)*. The random noise of the analyzed pixels likewise follow a gaussian distribution with a root mean square standard value around 0.6 ADUs.

7.2.2.3 Data Assembling

To discriminate pixels with signal from those without a signal a threshold or cut must be applied. On the one hand the cut must be high enough that no noise would be erroneously counted as a hit. On the other hand it should be as small as possible that no signal is rejected. The chosen algorithm first finds the seed pixel, which is the pixel with the highest signal value. In a typical operation the level for this seed finding mechanism is dependent on the pursued purpose: if the PXD6 sensor should detect MIPs the threshold should be as low as 7 ADUs (seed-cut), if a laser beam is tested the threshold can be easily increased to much higher values depending on the beam intensity.

Another issue is related to the clustering mechanism around the seeds. Since particles hit the detector at different incident angles, neighboring pixels must be included to determine the total deposited signal charge. Accordingly the program code scans the surrounding area and compares it with a second limit, the so-called neighboring or zero suppression threshold. This process is repeated until no pixel neighbor is found exceeding this neighboring threshold. In this way also δ-electrons which sometimes can

[92] although the electronic part dominates by far

[93] since the output codes are randomly distributed with mean 0, the RMS exactly corresponds to the standard deviation $\sigma = \sqrt{\frac{1}{n}[(x_1-\mu)^2 + (x_2-\mu)^2 + \cdots + (x_n-\mu)^2]} = \sqrt{\frac{1}{n}(x_1^2 + x_2^2 + \cdots + x_n^2)} = x_{RMS}$
with mean value $\mu = \frac{1}{n}(x_1 + x_2 + \cdots + x_n) = 0$

move a long way parallel to the detector can be detected [87]. The compound value of the whole cluster area[94] gives the signal value.

All relevant settings for performing the analysis (e.g. defining thresholds, masking pixels, entering run number, file path etc.) are entered into a configuration ***.xml*-file**. Most of the offline data processing and correction steps like input noise, pedestals and common mode correction are performed by the *Data Processor*, whereas the charge signal is calculated by a program called *Cluster Processor*.

7.3 Programming Switcher Sequences

7.3.1 SwitcherB Strobe Logic

The *Clear* and *Gate* channels of the SwitcherB are each controlled by a particular logic block. The schematic of the strobe logic for one channel is depicted in Figure 7-1.

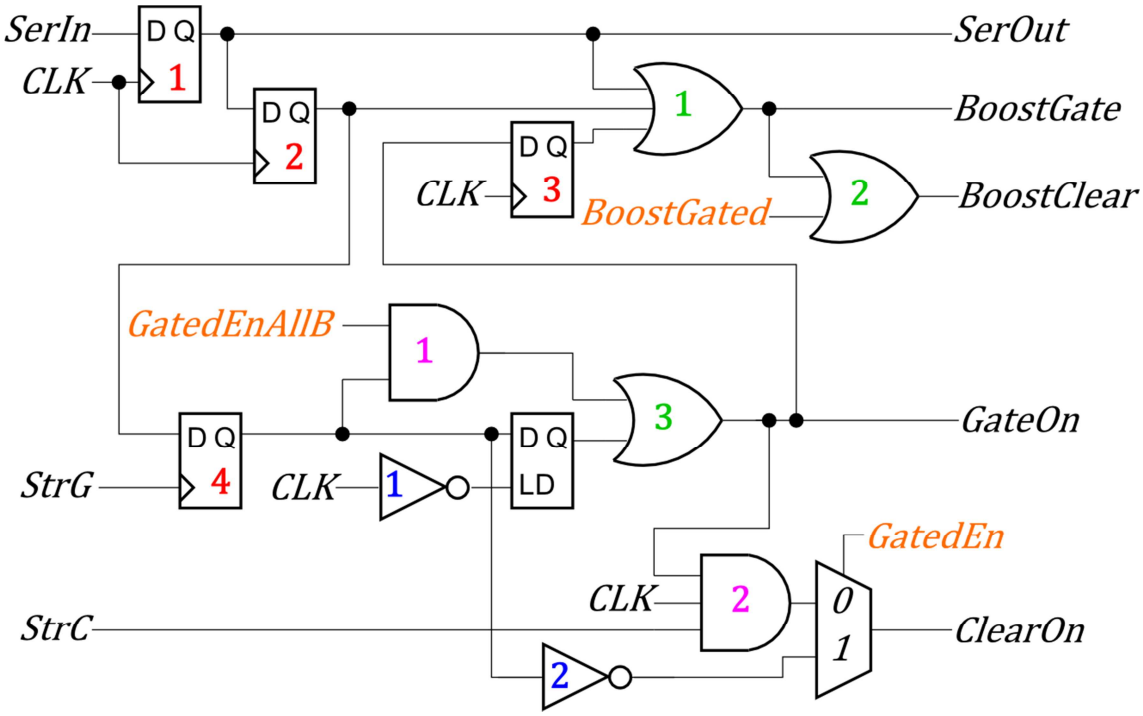
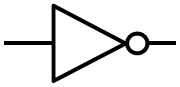
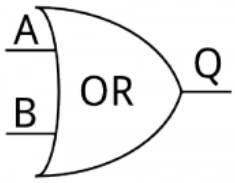
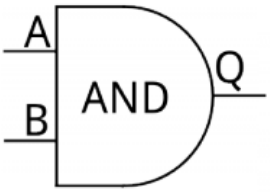
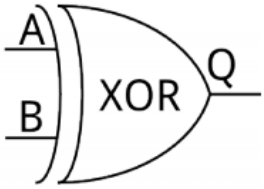
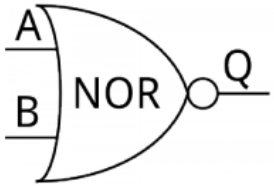


Figure 7-1: Schematic of the strobe logic for one SwitcherB channel. The numbers categorize logic elements referenced in the text.

The elements of the control logic block are described in the following [88]:

[94] the average cluster size at Belle II is expected to be 2 pixels [38]

<table>
<tr><th colspan="5">Combinational Digital Logic</th></tr>
<tr><td>  </td><td colspan="4">This symbol describes an inverter or NOT gate which implements logical negation</td></tr>
<tr><td rowspan="3">OR gates implement a logical disjunction. A high output results if one or both inputs are at high (see right the corresponding symbol with a truth table attached).</td><td rowspan="3">  </td><td colspan="2">A</td><td></td></tr>
<tr><td rowspan="2">B</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>1</td></tr>
<tr><td rowspan="3">AND gates also behave according to Boolean algebra. A high output results only if both inputs to the AND gate are high.</td><td rowspan="3">  </td><td colspan="2">A</td><td></td></tr>
<tr><td rowspan="2">B</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td rowspan="3">The output of the exclusive OR (XOR) gate is true only when the values of the input differ.</td><td rowspan="3">  </td><td colspan="2">A</td><td></td></tr>
<tr><td rowspan="2">B</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
<tr><td rowspan="3">NOR gates marked with a small circle at the output line negate the output of the OR operator. Together with NAND gates this is a universal gate since any Boolean function can be constructed using only NOR or NAND gates.</td><td rowspan="3">  </td><td colspan="2">A</td><td></td></tr>
<tr><td rowspan="2">B</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td></tr>
</table>

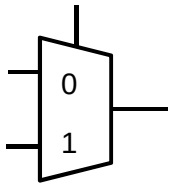
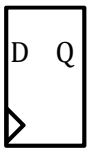
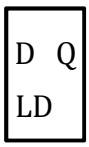
<table>
<tr><th colspan="4">Sequential Digital Logic[95]</th></tr>
<tr><td> 
</td><td colspan="3">This symbol characterizes a multiplexer which selects one or several digital input signals and forwards the selected input into a single line.</td></tr>
<tr><td rowspan="4">This symbol denotes a D flip-flop (D for “data” or “delay”). A flip-flop is a binary storage device consisting of 26 transistors in the SwitcherB to make it single event upset (SEU) tolerant. It remains in the memory state as long as it is directed by an input signal to switch over to the other state. A D type flip-flop has a single data input (D) and a clock input (>). It prevents the value of D from reaching the output (Q) until either a rising or falling clock pulse edge occurs. Subsequent changes of the D input will be ignored until the next clock event.</td><td colspan="2" rowspan="2"> 
</td><td>D</td><td></td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td rowspan="2">CLK</td><td>0</td><td>Q_{n-1}</td><td>Q_{n-1}</td></tr>
<tr><td>↑</td><td>0</td><td>1</td></tr>
<tr><td> 
</td><td colspan="3">In contrast to D flip-flops the output Q of a D latch always reflects the logic level present at the D input. If the data on the D line changes state while the clock pulse is high, then the output, Q, follows the input, D. When the CLK input falls to logic 0, the last state of the D input is trapped and held in the latch.</td></tr>
<tr><td>FF<X:Y></td><td colspan="3">Shift register based on a cascade of flip-flops sharing the same clock. At any clock cycle the content of a flip-flop is shifted into its output which is connected to the data input of the next flip-flop. In accordance with the FIFO principle (first in first out) the first bit reaching the last flip-flop in the bucket chain is shifted out and lost.</td></tr>
</table>

Table 7-1: Combinational and sequential logic elements of SwitcherB logic block.

The digital logic block is steered by 4 different input signals: *SerIn* activates a 32-bit deep shift register which interconnects the control blocks of all 32 channels of the SwitcherB chip. The input of the first as well as the output of the last flip-flop are linked to chip pads. Thus several SwitcherB chips can be chained together. The clock signal *CLK* coordinates and synchronizes the activity of the two strobe signals *StrG* and *StrC*, which in turn enable the *Gate* and the *Clear* output. The other input signals *(BoostGated*, *GatedEnAllB* and *GatedEn)* are only coming into play during the Gated Mode operation. The boost signals (*BoostGate* and *BoostClear*) directly activate the level shifter unit,

[95] in contrast to combinational logic the output of a sequential logic circuit depends not only on the present value of its input signal but on the sequence of past inputs; hence in order to determine the next state of an output the previous state must be stored in a memory (in some aspects a computer resembles an advanced sequential logic circuit)

which is used to transfer steering information from the low voltage digital domain to the high voltage analog output stages. A *Gate* is said to be in the *ON* state if the corresponding output driver reduces its potential to the *Gate*-low level. This is due to the fact, that DEPFET transistors possess a pMOS structure. For the *Clear* operation a positive voltage is needed in order to extinguish the internal gate.

The normal readout and *Clear* operation for a specific row is initiated by storing a logical *1* to the *SerIn*-flip-flop of the channel's logic block as shown in Figure 7-1 (*SerIn*-flip-flop labeled with number 1). At the rising edge of the clock the corresponding output drivers get boosted (enabled). The next clock[96] pulse transfers the logical *1* from flip-flop #1 to flip-flop #2. While keeping the output drivers in the boosted state the logic block is now sensitive to signals form *StrG*. A rising edge of *StrG* after the falling edge of *CLK* stores the logical *1* of flip-flop #2 into flip-flop #4. Since *GatedEnAllB* is always high during normal operation mode the output of AND gate #1 is high and *GateOn* of the specific channel is now enabled. The AND gate #2 ensures that the *Clear* pulse is only working when the *Gate* is switched on and the *CLK* is on high level too. The *Gate* returns to the idle potential as soon as the next *Gate* is switched on. A link from *OR* gate output #3 transfers the logical state of *GateOn* to flip-flop #3, which leads to a delay in releasing the boosted state by a single clock cycle. Consequently not only the activated channel gets boosted but also the previous and the following one [67].

In normal operation mode the controlling block also foresees the possibility of skipping rows or overlapping *Gates*. For skipping rows the *StrG* signal simply has to be omitted. The overlapping *Gate* feature generates an overlap of a few nanoseconds while switching rows. This may influence the readout frequency favorably. Additionally, a temporarily absent offset current potentially occurring between row switching can be avoided. It is enabled with a rising edge of *StrG* before the falling edge of *CLK* and implemented in the logic block as interplay between flip-flow #4 and the sole latch element. However, for the Gated Mode analysis both properties are not used.

In an ideal world all *Clear* outputs of SwitcherB would be simultaneously activated to shield the internal gate from noisy bunches. In reality the level shifters are boosted sequentially in groups of 8 channels to limit the high current supplies and to avoid damages to the chip. Two different operation modes can be selected: the Gated Mode with and the Gated Mode without readout. In the first case the Gated Mode is initiated by a high level on *CLK* or *StrC* at the falling edge of *StrG*. This would store a logical *1* into flip-flop *FF<0>* of FIFO register *FF<0:5>* depicted in Figure 7-2. The *Clear* changes to the high level immediately on non-active channels. Rows being enabled during the short readout time (100 ns) are sensitive to any irradiation but are not cleared. For a better understanding a closer look might focus on the operational details of the Gated Mode logic block:

[96] at 320 MHz a full clock cycle takes 3.125 ns

- During normal operation (non-overlapping *Gates*) the rising edge of *StrG* has to be after the falling edge of *CLK*. Accordingly the state of the logical *OR* input to the FIFO register would be on low level and a logical *0* would be stored into *FF<0>*. The rising edge of the *StrG* signal, in this case replacing the clock input, will be turned to a falling edge by the inverter. So no action takes place.
- The *Clear* during normal operation is similar: indeed the data line gets a high input from the logical *OR* but the rising *StrG* edge translates to a low input preventing the D-flip-flop shifting the stored data to the output.
- If now both inputs to *FF<0>* deliver a logical *1* which can be achieved by a high *CLK* or high *StrC* level together with a falling edge of *StrG,* register[97] #0 shifts its output to the next register. Simultaneously the *GatedEnAllB* signal gets deactivated and the *BoostGated* signal gets enabled for all channels by the *XOR* gate. The following *StrG* signal shifts the data input from *FF<0>* to *FF<1>* and again injects a logical *1* to *FF<0>*. This in turn enables the *GatedEn* input to the multiplexer which instantaneously switches the *Clear* pulse to high via its single output *ClearOn* signal for the first 8 channels. After three further *StrG* signals all channels are activated and the whole detector is in the gated or blind mode. *StrG* also enables the *Gates* one after the other like in normal rolling shutter mode, though inverter #2 prevents the multiplexer from sending the *Clear* signal for the active channel during readout.

The Gated Mode without readout is activated by stopping *CLK* while *StrC* is high (turning the *OR* gate permanently on high level) and *StrG* is running. Similar to the preceding situation the FIFO register gets activated and a minimum of 5 falling *StrG* is required for switching all channels into the Gated Mode. Since the *CLK* stops running no *Gate* will be enabled and SwitcherB will resume normal operation from the last active channel after turning into the Gated Mode.

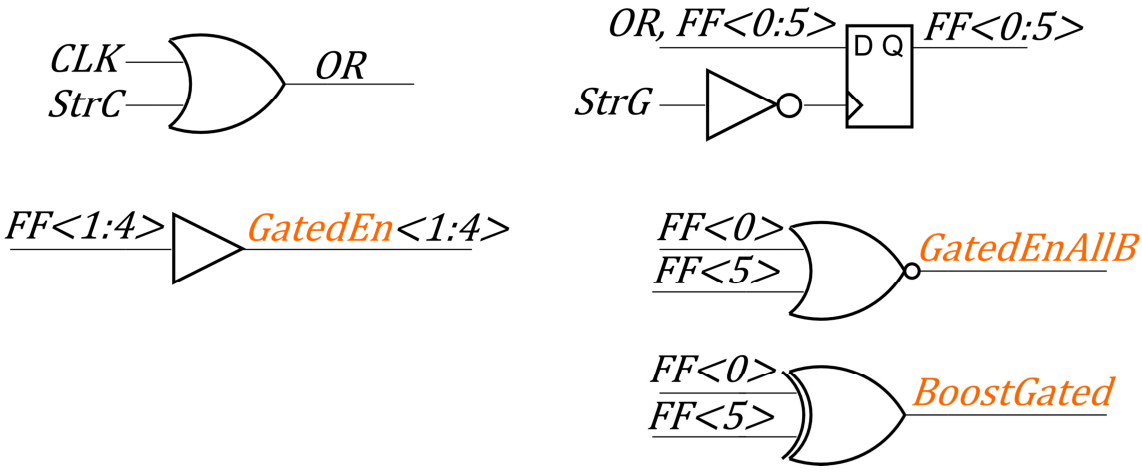


Figure 7-2: Schematic of SwitcherB Gated Mode logic controlling all channels

[97] the term register is sometimes synonymously used with the term flip-flop

7.3.2 SwitcherB Controller

The programmable sequencer responsible for steering the two SwitcherB chips is implemented in the FPGA firmware. The sequences, expressed by an ordinary bit-code, are sequentially read from a writable memory (RAM) and have to be translated into microcode for SwitcherB. The sequence RAM contains five modes of operation: *read & Clear*, *Read no Clear*, *Read no Clear* + Laser, Gated Mode and Gated Mode + Laser. These subsequences are organized in such a way that the memory readout logic is referenced to the same clock as used for the controlling of the DCDB. More concretely the code is entered in a csv[98] text file consisting of 4 sub-lines. Each sub-line of a sequence contains 4 bits, the first one (from right to left) for the clock, then Strobe*Gate*, Strobe*Clear* and the last one for the laser trigger:

Line	#3: laser, 2: clear, 1: gate, 0: clock	
1	0,0,1,0	#start frame read & clear, activate gate 0
2	0,0,1,0	
3	0,0,1,0	
4	0,0,1,0	
5	0,0,0,0	
	⋮	
25	0,0,0,1	#clock cycle for shifting to next row
26	0,0,0,1	
27	0,1,0,1	#clear row 0 while *CLK* is high
28	0,1,0,1	
29	0,1,0,1	
30	0,1,0,1	
31	0,0,0,1	
32	0,0,0,0	#end of row 0
	⋮	

Table 7-2: Small portion extracted from the sequence steering SwitcherB. The program code is easy to interpret, showing the implementation of the strobe logic described in chapter 7.3.1.

To allow fast clocking 4 subsequent sub-lines are merged into one 16-bit wide RAM line in the FPGA[99]. Every RAM-line can be accessed with a dedicated RAM address. At 320 MHz target speed the serializer sends one sub-line every 3.125 ns to the switcher inputs. After 32 steps one matrix row is activated sufficiently long for the readout and clearing process. This corresponds to 100 ns. Since the test matrix contains 16 rows a whole frame cycle takes 1.6 µs.

Of special concern is the start-up phase of the device: whereas the DCDB is starting its task immediately after activation, the shift register of SwitcherB must be reset by writing 16 zeros into it. This is implemented in the code by an extra start-up sequence of 512 sub-lines inhibiting the DCDB readout during this time.

Additionally, a much shorter frame RAM with a similar structure contains all the information in which order the different subsequences have to be run through:

[98] comma-separated values (csv)

[99] again starting always from right to left

address code	line number	subsequence
0000_0000_1000_0000	128	read & *Clear*
0000_0001_0000_0000	256	read no *Clear*
0000_0001_1000_0000	384	read no *Clear* + laser
0000_0010_0000_0000	512	Gated Mode
0000_0010_1000_0000	640	Gated Mode + laser

Table 7-3: Frame RAM pointing to the correct start address for running a subsequence

Each subsequence is homogenous in the sense that it takes exactly one frame to finish this sequence although in principle it is also possible to program a mixture e.g. Gated Mode and *Read no Clear* within one frame. In that way the program is very flexible and allows to run through all possible combinations of different operation modes. For the purpose of the Gated Mode analysis 8 frames are sufficient, thus only 8 16-bit addresses have to be stored into the frame RAM.

After resetting the FPGA the RAM-address is set to zero. The address counter will then increment with one clock delay, i.e. start-address minus one which is equivalent to perform the entire start-up sequence. Before stopping the sequences pass through an endless loop according to the stored sequences in the sequence RAM.

7.4 Calibration Measurement

7.4.1 Interaction of Photons with Silicon

The indirect band gap of silicon equals 1.12 eV at 300K. Increasing doping concentrations cause the band gap to shrink, since the wave functions of the electrons bound to the impurity atoms start to overlap. The p^+ layer on the backside of the PXD6 sensor is just 3 µm thick. Its doping density distribution is Gaussian-like with a peak of $10^{19}/cm^3$. According to equation (B-1) this has barely an impact on the band gap energy of the detector.

Upon light absorption two types of excitations are possible: lattice excitation with no formation of mobile charge carriers, and ionization processes with the formation of electron hole pairs. To conserve energy and momentum the electron hole generation is achieved by means of a two-step process. The photon vertically excites a valence band electron to the higher conduction band level. Then both, the electron and hole release their excessive kinetic energy by a process called thermalization in which their momentum is transferred to phonons (warming up the detector). If the photon energy is very

high, the primary electron transfers its energy to other electrons thereby generating multiple electron hole pairs[100] until it eventually stops.

The mean ionization energy $W(h\nu)$[101] required for producing a charge carrier pair is a basic material property and changes as a function of the photon energy [89]. The energy dependence turns out to be non-monotonous due to the silicon band structure: at the lower extreme a minimum energy is necessary for electron hole pair generation, corresponding to a wavelength of 1.1 µm in the infrared area, whereas beyond the silicon is said to be transparent. If the photon energy ranges between the band gap and twice its value (2.24 eV) it can create only one electron hole pair. Above this constant value the mean ionization energy increases strongly to a peak value of 3.8 eV at 4.5 eV photon energy [90], then decreases to a constant value of 3.66±0.03 eV for incident photon energies between 50 eV and 1.5 keV [91] and reaches its asymptotic value of 3.63 eV [92] for very high energies.

Not all incident photons generate electron hole pairs. The quantum efficiency of a detector characterizes its ability to absorb photons converted into detector current [93]:

$$\eta = (1 - R)\zeta[1 - exp(-\alpha d)] \tag{7-6}$$

where R is the reflectivity, ζ the probability that a single photon will generate an electron hole pair, α is the absorption coefficient and d the detector thickness. A photon can penetrate the sensor without any interaction or it can transfer part (Compton scattering depending on the wavelength) or all (Photoelectric effect) of its energy to a single electron. In general the photoelectric process is the predominant mode of interaction for photon energies below 50 keV in silicon (see Figure 7-6). The probability of photoelectric interactions is inversely proportional to the cube of the photon energy $\sim 1/E^3$. The National Institute of Standards and Technology (NIST) provides data tables for the resulting mass attenuation/absorption coefficients $\alpha = \mu/\rho\ [cm^2/g]$ for almost all elements and covers photon energies from 1 keV to 20 MeV [94]. The transmission rate is given by I/I_0:

$$I/I_0 = exp[-(\mu/\rho)x] \tag{7-7}$$

where I_o is the incident intensity penetrating a layer of material with mass thickness $x = \rho d$ which is obtained by multiplying the thickness d by the density $\rho\ [g/cm^2]$. $1 - I/I_0$ finally gives the interaction probability ζ.

7.4.2 Laser Intensity Measurements

It would be an attractive approach to measure the intensity of a laser pulse with an optical power meter and to convert the entire photon flux into electron hole pairs in the DEPFET sensor. The internal gain could then be easily derived from the induced de-

[100] this process is also called impact ionization

[101] h is the Planck constant, ν the frequency

tector current. As a caveat this method relies on a lot of estimated parameters which are prone to errors. Nevertheless Appendix B outlines a proposal how this could be carried out.

7.4.3 Radioactive Source Measurements

Cd-109 with half-life of 461.9 d decays by **electron capture** to the isomeric (88 keV) state of Ag*-109 [95]. The 88 keV level of Ag*-109 has a half-life of 40 s and decays mainly by the emission of conversion electrons to the ground state of Ag-109 (see Figure 7-3).

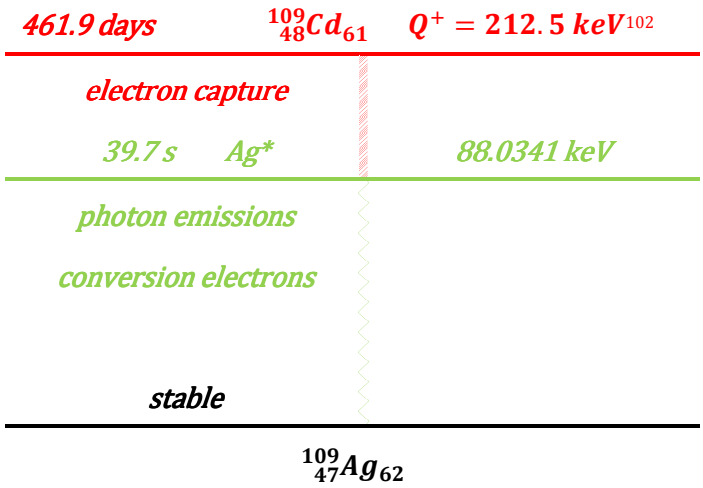


Figure 7-3: Nuclear level scheme of Cd-109 decay

Conversion electrons use the electromagnetic energy of the excited nucleus to be expelled from the atom. Following this internal conversion, outer orbital electrons will fill the vacancy in the electronic shell, producing an X-ray or an **Auger electron**. This process should not be confused with the photoelectric effect, where an external gamma ray ejects an electron form the atomic orbit or with beta decay, since the electron in beta decay comes directly from the nucleus induced by the decay of a neutron. Moreover beta decay generates a continuous energy spectrum, whereas conversion electrons only contribute to a single sharp peak. However, this peak is not detected in the DEPFET sensor, because the Cd-109 source is encapsulated in a 1.02 mm thick beryllium jacket with 0.127 mm silver coating and according to formula (C-1) 88 keV-electrons have a maximum range of just 68 µm in this material.

Consequently only photons can escape. Four peaks in the energy spectrum of the Cd-109 decay can be expected: one, due the 88 keV γ-radiation, which are rare, because only an amount of 3.9% of all Ag* transitions remain unconverted. The second and third peak at around 22 keV and 25 keV, respectively, due to the emission of Ag K-shell

[102] the Q value corresponds to the amount of energy released by that reaction

X-ray quanta following the emission of conversion electrons and the fourth peak at around 3 keV, due to Ag L-shell X-ray quanta.

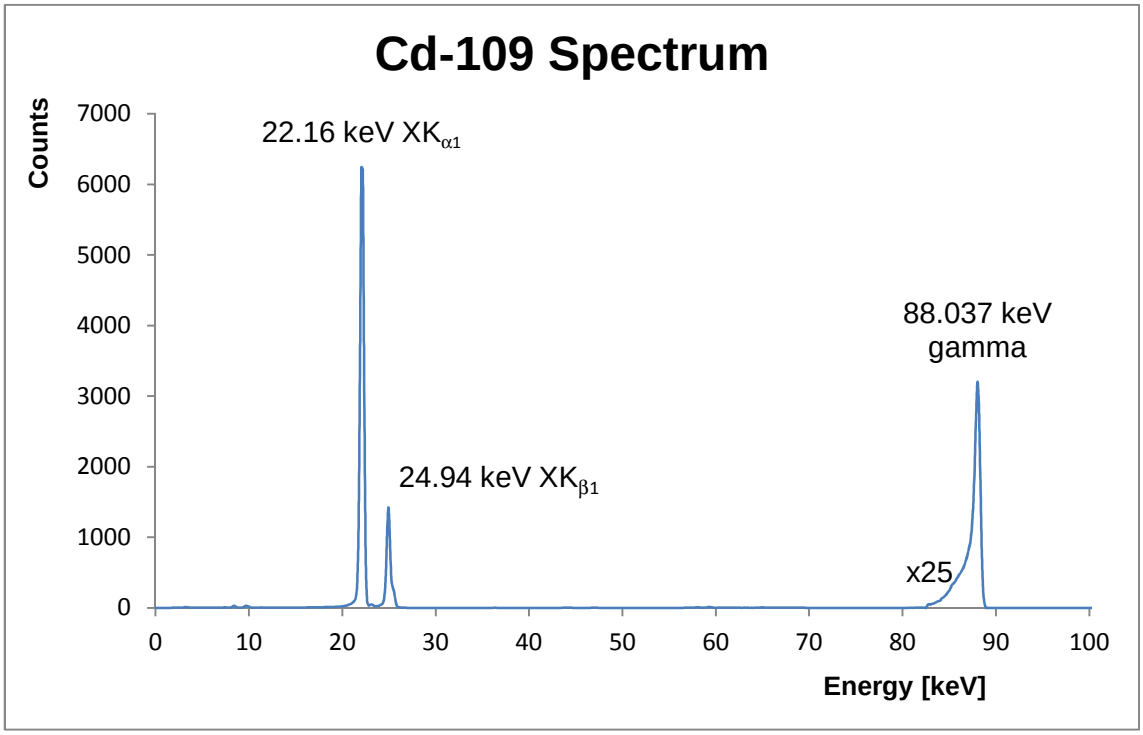


Figure 7-4: Spectrum of Cd-109 source measured with CdTe γ/X-ray detector (data series courtesy of AMPTEK Inc.). The 2.98 keV $XL_{\alpha1}$ peak is strongly suppressed as a result of the Be window on the detector. The 88 keV γ-peak is magnified by a factor of 25.

Figure 7-4 shows the X-ray and γ-ray spectrum of a Cd-109 source measured with a CdTe-detector. Cd-109 is a very well suited calibration source by virtue of its characteristic **photopeak** at around 22 keV which corresponds to about 6,000 electron-hole pairs in silicon. This is identical to the amount of electrons generated by a MIP in a 75 µm thick silicon sensor. If a gamma ray deposits all of its energy into the detector this is counted as an entry. For the calculation of total entries within a certain time period the following parameters have to be factored in: the source geometry as depicted in Figure C-1, the activity or number of decay events, the probability of a photon emission per decay event and the photoabsorption probability in 50 µm silicon. All these figures are described and calculated in Appendix C. Figure 7-5 depicts a cluster histogram for two different *GateOff* voltages: -2 V and -3.9 V. A gaussian fit determines the mean value at 21.08 and 32.99 respectively. This yields an internal amplification of

$$g_q = cluster\ mean\ value\ \times DCDB\ LSB\ gain \times \frac{E_{eh}}{E_{photon}} \qquad (7\text{-}8)$$

The DCDB LSB gain was determined at 71.7 nA/ADU from Figure 3-11. The Cd-109 average photon energy $E_{photon} = 22.54\ keV$can be inferred from Table C-1 as the sum weighted product of all XK lines with their respective final absorption energy in silicon and the e/h-pair creation energy E_{eh} is 3.63 eV. Inserting the two cluster mean values from Figure 7-5 at 21.08 ADU and 32.99 ADU, respectively, delivers an internal amplification g_q of $243.3\ pA/e^-$and $380.9\ pA/e^-$. Including a mean noise of 0.54 ADU the signal-to-noise ratio for the first measurement is about 39, for the second measurement around 49 with mean noise at 0.67 ADU. The small hump left to the peak in the bottom diagram comprises 15% of the total hits. It may be attributed to Compton scattering (5.6% according to NIST data, see Figure 7-6), inefficient clustering at the border pixels of the matrix (see Figure 7-7) and to other matrix specific effects.

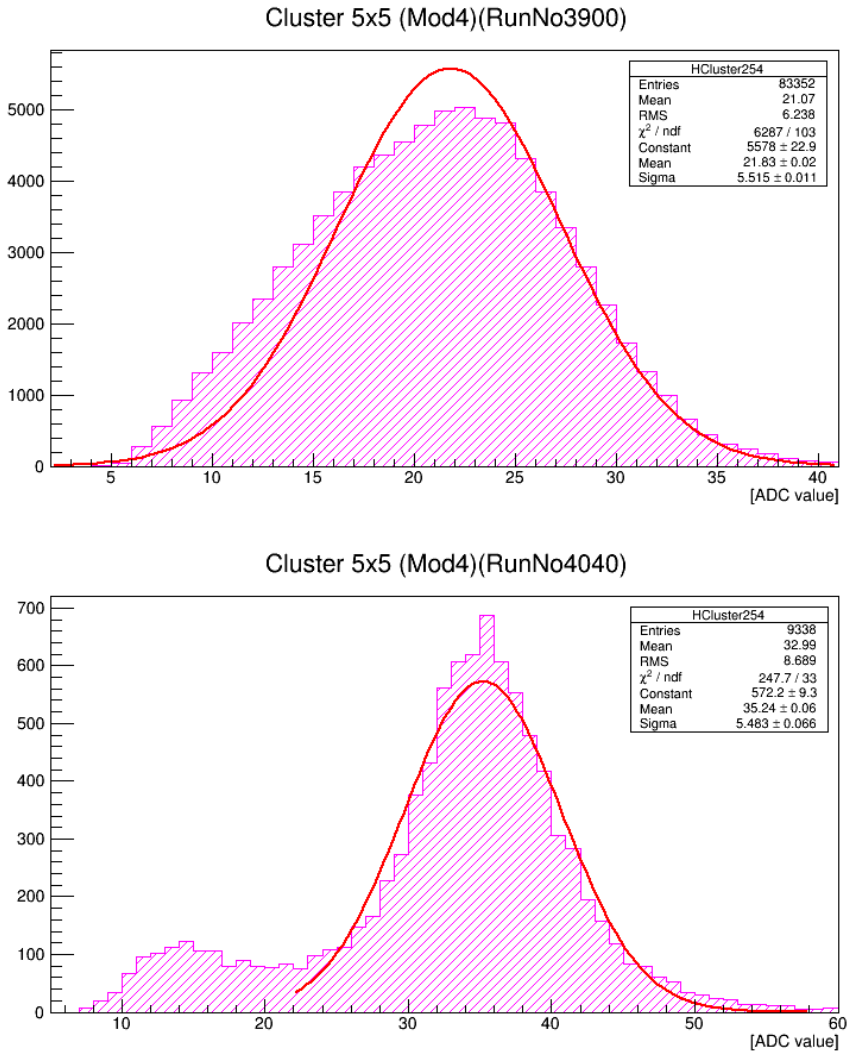


Figure 7-5: Cd-109 source measurements with two different *GateOff* voltages at -2 V (top) and -3.9 V (bottom), respectively. The curves are from fits to the main peaks using a single Gaussian.

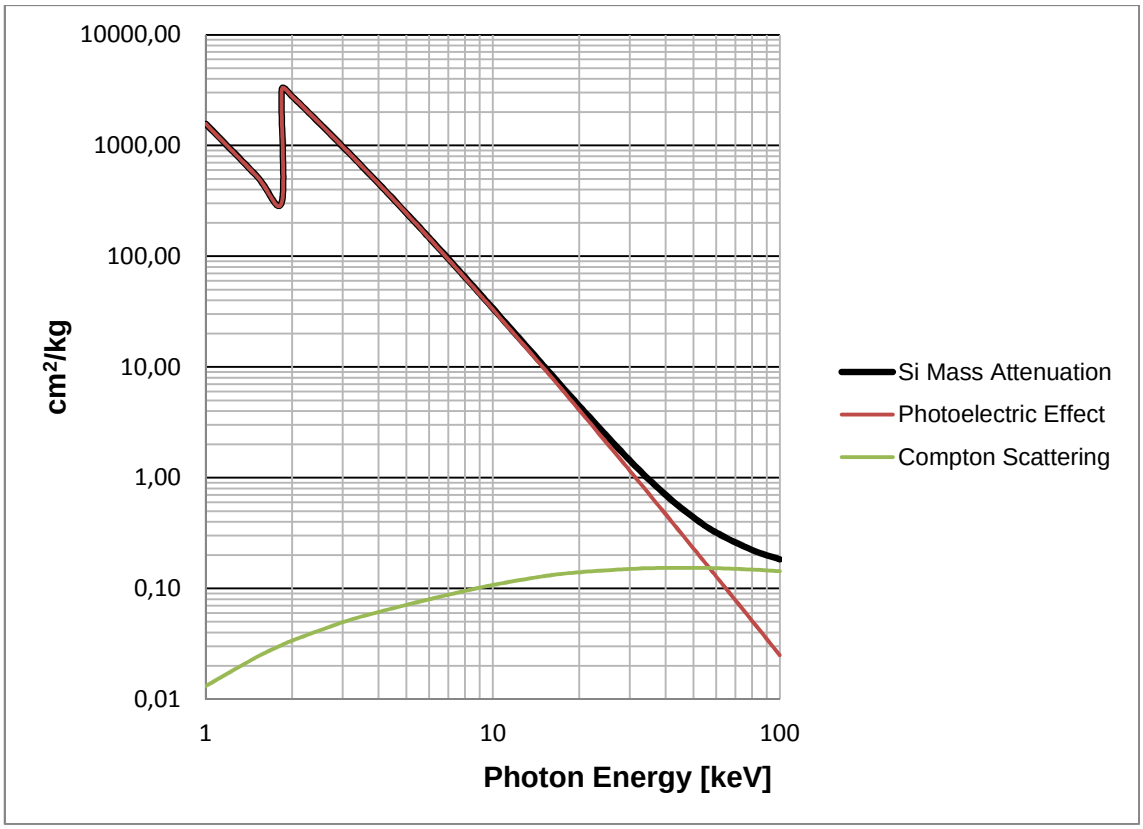


Figure 7-6: Silicon Mass Attenuation 1-100 keV (NIST data)

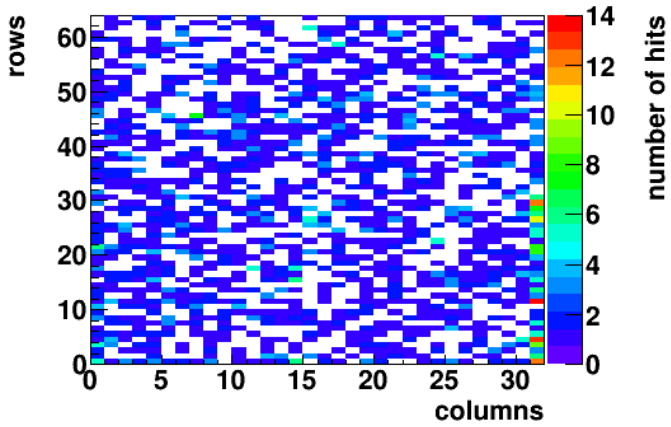


Figure 7-7: Matrix hits smaller than 20 ADUs. Especially on the right edge of the matrix the clustering algorithm seems to not working properly. More specifically, the clustering cannot include pixel hits outside the sensitive area. This effect diminishes with larger matrix areas [96]. Other factors impacting the clustering process may stem from re-combination losses in the p^+ area (as described in Appendix B) or may be due to hits in the active row during readout being not fully collected yet.

7.5 The Gated Mode Sequences

7.5.1 Mapping

In particular, the mapping of the matrix pixels via DCDB channels and the various serialization steps inside the DCDB and the FPGA to the displaying software is by far a non-trivial task.

J. Knopf (Thesis)

The quotation still holds for this analysis. The process of finding the correct mapping was very time consuming, thus it could be convenient to outline the main aspects of a promising approach. Above all it is advisable to read the DCDB reference manual carefully for any updates especially with regard to the clock timings. The first valid byte of conversion data is produced after 191 clock cycles in DCDBv4 (DCDBv2: 171). Ignoring this information shifts the PXD6 matrix by 80 columns and leads to strange observations. As an example, parts of a laser spot placed on the upper edge of the sensor simultaneously appear on the lower edge.

Next, one has to clarify which DCDB channel is connected to which DEPFET column. This can be achieved via channel-wise activation of the digital test injection and writing down, one after another, the matching column observed in the online monitor. The result represents the position number of the relevant column in the output stream. This book-keeping procedure is necessary and can only be done manually. To arrange the matrix pixels in proper order the output stream position must be assigned to the geometrical pixel layout. For this purpose the pad layout of the wire bond adapter has to be compared to the pad arrangement of the DCDB.

7.5.2 Oscilloscope Measurements and Simulation of Strobe Logic

This chapter investigates how fast the system switches in and out of the Gated Mode. The analysis was carried out in a two-step process: First a simulation of the SwitcherB strobe logic evaluates if the program code is correctly implemented [97]. Besides It allows to infer the reaction time under ideal conditions (no rising edges). The output of this simulation can be studied in Appendix E.

Secondly a special test board depicted in Figure 7-8 was bonded on a different hybrid 4 board directly to the SwitcherB outputs introducing the possibility to measure the *Gate* and *Clear* output signals with an oscilloscope as shown for the Gated Mode with readout in Figure 7-9 and the Gated Mode without readout in Figure 7-10.

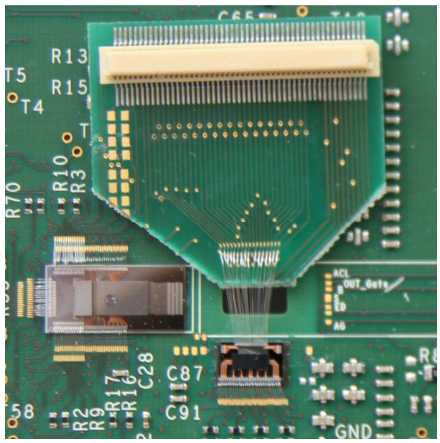


Figure 7-8: Small test board allowing oscilloscope measurements on Switcher outputs.

Gated Mode with readout is activated by a falling edge of *StrG* while *CLK* is on high level. One open *Gate* or active row length (=100 ns) plus about 25 ns later the *Clear* changes to high level on non-active channels for the first SwitcherB channel group (8 channels) at this moment enabling the Gated Mode. The 25 ns delay is contingent on the sequence code and can be shortened to a minimum of 6.25 ns. The measurement conflicts with the description in the SwitcherB19 reference manual, where *Clear* should change to high level immediately on non-active channels. The second channel group is activated/deactivated 100 ns later.

Gated mode without readout is implemented by the fastest sequence code possible. While stopping *CLK* a series of 5 falling *StrG*[103] switches all column groups into the Gated Mode, the first one after 2 falling *StrG* signals. One strobe cycle corresponds to a 1 in the first sub-line of the program code followed by a 0 in the second sub-line equivalent to a total of 6.25 ns. Turning two column groups into the Gated Mode would correspond to 18.75 ns, whereas for all SwitcherB channels it would take 31.25 ns.

[103] here again the measurement and simulation deviates from the reference manual where a minimum length of 8 falling *StrG* is required

Figure 7-9: Oscilloscope measurement of the Gated Mode with readout. The *Clear* shifts down to low level on channels currently enabled.

Getting out of the Gated Mode would take another 31.25 ns as shown in Figure E-2. The lost synchronization can be restored by consecutive fast *CLK* signals. This has to be compared to the Gated Mode with readout sequence where a minimum of 406.25 ns is necessary to switch into the Gated Mode and about 300 ns for returning to normal operation.

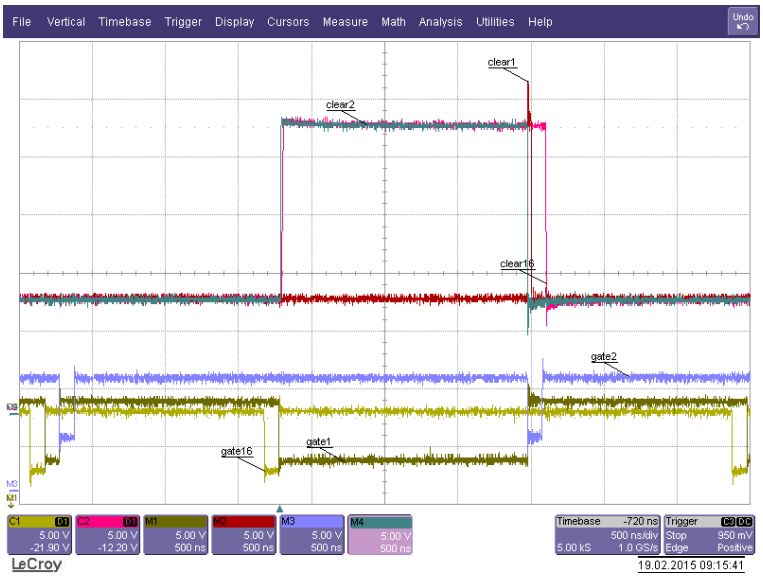


Figure 7-10: Oscilloscope measurement of the Gated Mode without readout. For turning back to normal readout operation the same sequence as for the Gated Mode with readout was applied.

7.5.3 Experiment A: Signal Charge Preservation

In this experiment a laser beam impinges on the DEPFET pixels during sensitive state (*GateOff*, *ClearOff).* Then the Gated Mode is activated and the laser is (almost) switched off. Ideally no charge loss should be observed in the following frames. To optimize the charge loss during gating the laser intensity was reduced in such a way that the charge stored in each of the spot center pixels approximately reproduces one MIP hit.

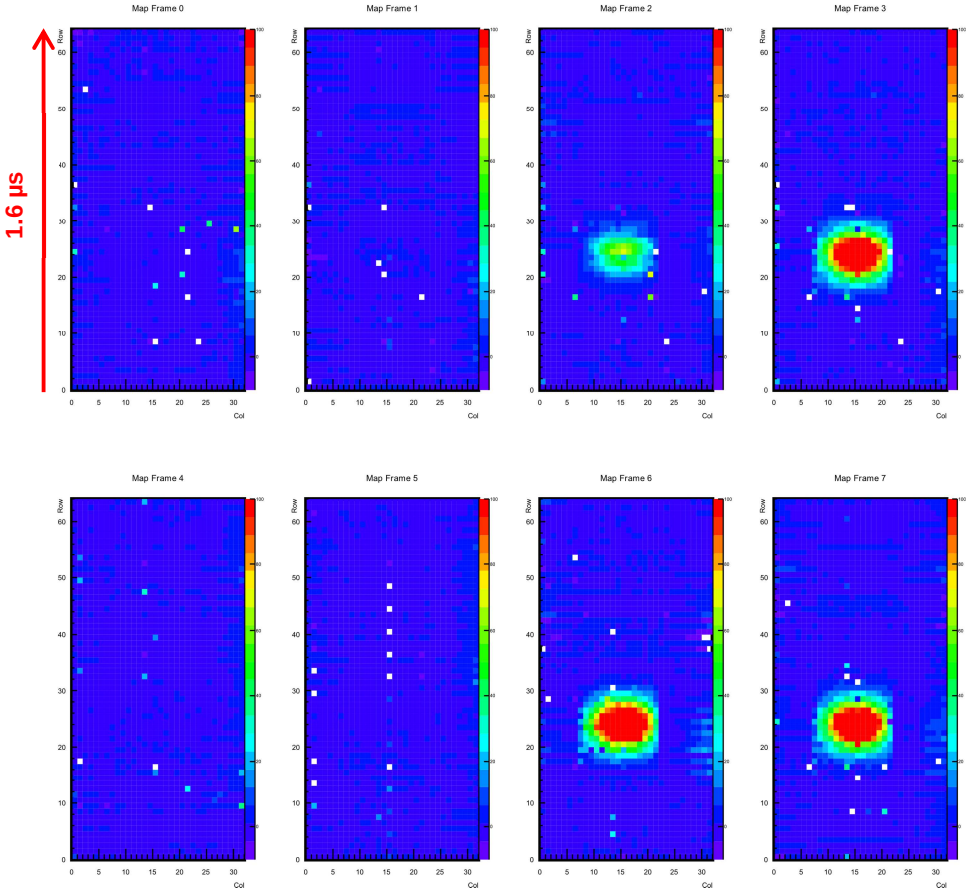


Figure 7-11: SCP sequence R-R-RL-R-G-G-R-C Gated Mode without readout. The frame sequence starts from top left to the right, then from bottom left to the right. For pedestal measurements this loop is repeated a few thousand times. The amplitude and duration of the laser pulse was set, respectively, to 800 mV and 1 µs, corresponding to about 320 MIPs (see Appendix B). For visualization purposes the laser pulse was chosen relatively intense and broad (by increasing the distance between the laser optics and the matrix). The white and light blue pixels outside the laser spot area arise from artefacts or noisy pixels.

The readout in Figure 7-11 starts at the bottom edge of each frame by enabling the first row for 100 ns and moves sequentially to the top row. This rolling shutter mode takes a total of 1.6 µs per small matrix frame. Comparing frame 3 to frame 4 one can observe that the laser pulse was still on while the readout process already passed the spot area, so not all charge could be collected. In order to protect the massive internal charge

from *Clear* the *GateOff* voltage was determined at 8 V and *Clear high* at 18 V. Both voltages stick together in a certain trade-off relation. Lowering the *Clear* voltage too much would not empty the internal gate after applying the short *Clear* pulse of 12.5 ns. In contrast a very high *Clear* voltage would increase the potential difference between *Clear* and internal gate and attract some electrons from the internal gate to the *Clear* contact. A higher *GateOff* voltage in turn protects the stored electron charge though a too high level could lead to unwanted side effects like avalanche breakdown. Pedestals were taken for each frame separately.

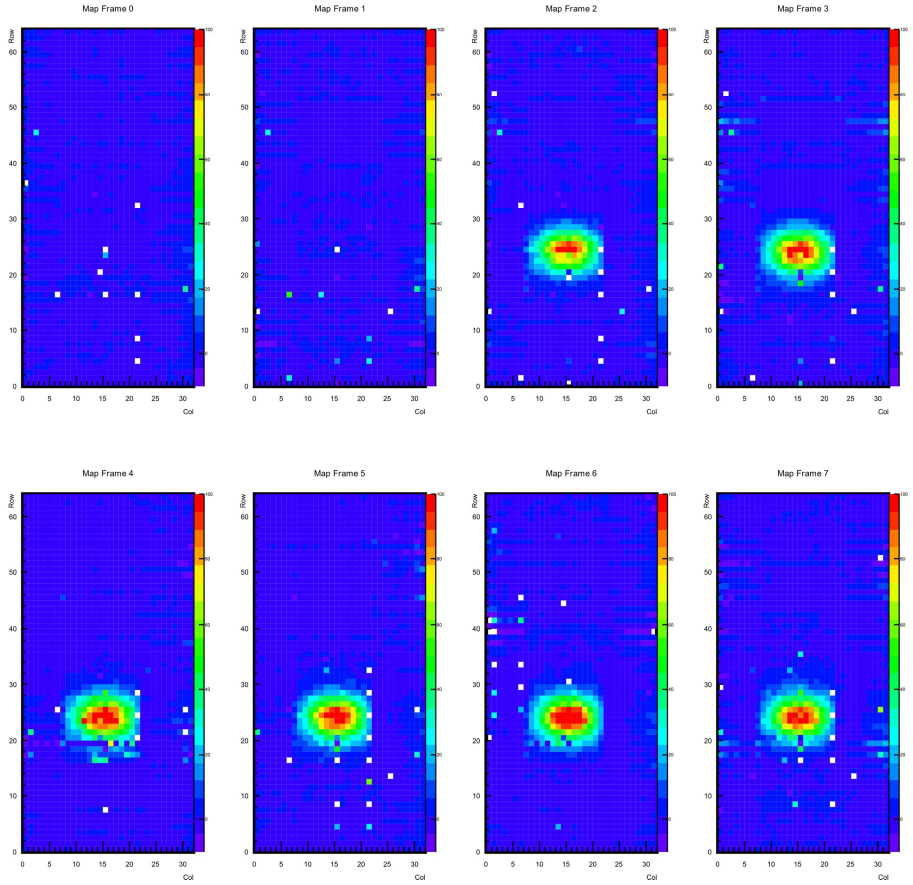


Figure 7-12: SCP sequence R-R-RL-R-G-G-R-C Gated Mode with readout and a laser pulse width of 400 ns and 1 V amplitude corresponding to about 190 MIPs.

The laser pulse in Figure 7-12 was chosen with a higher amplitude of 1 V and a shorter duration of 400 ns. Comparing again frame 3 and frame 4 the charge seems now almost completely collected because the duration of the laser pulse was much shorter and the readout procedure reaches this part of the matrix only after 500 – 600 ns.

For a numerical assessment of the charge losses the laser intensity was significantly reduced to replicate a typical MIP hit involving several pixels. By means of a voltage scan concerning the constellation of *Cleargate, Clear* and *GateOff* the charge loss was minimized. Figure 7-13 visualizes the result in a chromatic diagram for a *Cleargate* volt-

age at -3 V versus source (equivalent to 4 V above ground – *GND*).[104] Comparing the Gated Mode with readout to the Gated Mode without readout the outcome clearly favors the second method. While the Gated Mode without readout can be operated within the full examined voltage range for *GateOff* at 3 – 8 V (equivalent to 10 – 15 V above *GND*) and *Clear* 14 – 18 V (equivalent to 21 – 25 V above *GND*) without losing any charge, the Gated Mode with readout requires a *GateOff* voltage of at least 5 V to preserve all charge. In general the charge storing capacity increases with higher *GateOff* voltages and decreases with higher *ClearOn* voltages. This characteristic was already observed in [98].

An explanation for the restricted voltage range of the Gated Mode with readout may be found in the simultaneous switch between *Gate* and *Clear* voltages which has a certain RC time-lag, in other words the *Clear* pulse might be not hundred percent disabled when the *Gate* is enabled for readout. This potential overlap of the voltage ramps, in turn, could remove parts of the charge from the internal gate to the *Clear* contact.

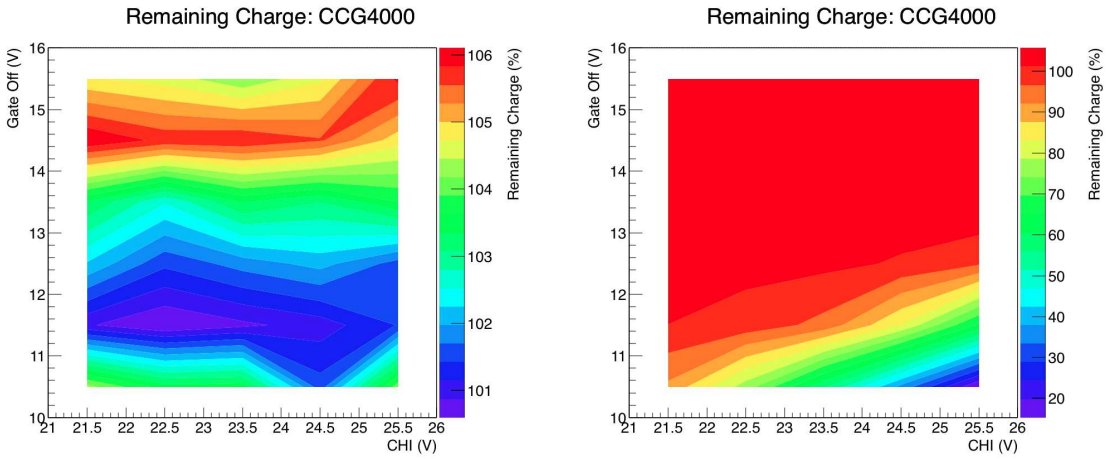


Figure 7-13: Parametric voltage scan minimizing charge losses during the Gated Mode [99]. The *GateOn* voltage was kept at -3.9 V. All voltages in the diagrams are referenced to *GND*. Left: Gated Mode without readout. Right: Gated Mode with readout. Note that the scales differ substantially from the other. Closer inspection shows, that similarly to the Gated Mode without readout, the internal charge would also increase with higher *GateOff* voltages.

The tendency of additional charge at higher *GateOff* voltages, exemplarily shown in Figure 7-14, might be explained by two effects which are both influenced by the strong coupling of the internal gate to the *GateOff* voltage: first, if the internal gate voltage is much larger than the *ClearOff* voltage (constantly held at 3 V during measurements) there might be some electron back emission from the n^+-*Clear* contact. Secondly at higher internal gate voltages the potential gradient to the drain p-n junction increases. This would generate a higher electric field fostering an avalanche mechanism by im-

[104] the best results were achieved at this *Cleargate* voltage

pact ionization. However, it might be also imaginable that there is a superposition of different influences, i.e. although some charge is lost the described effects ensure a balance.

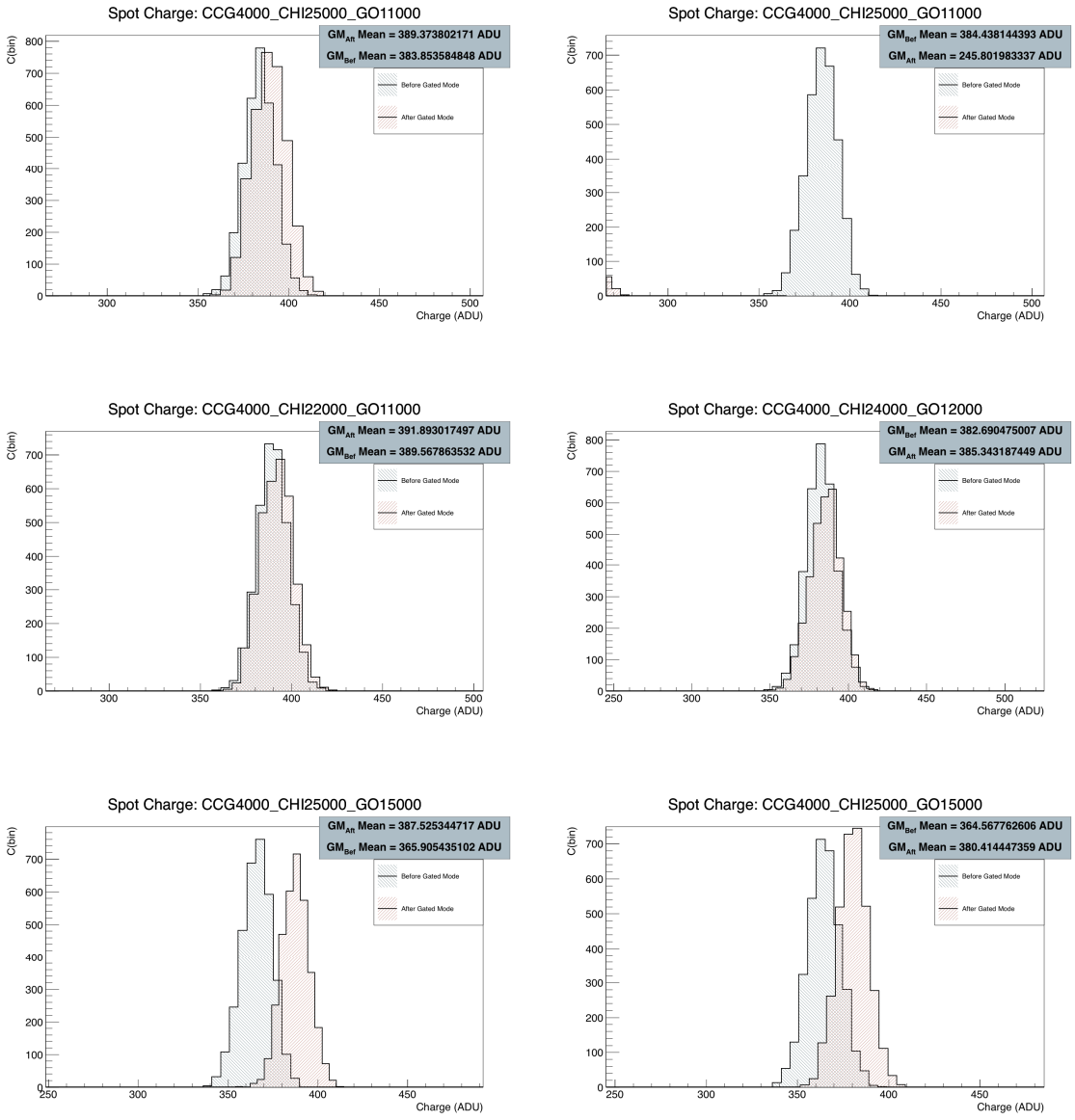


Figure 7-14: All voltages in the diagrams are referenced to *GND*. Left: SCP Gated Mode without readout. In all scanned cases there were no charge losses observed. Raising the *GateOn* voltages too much would increasingly pull the detector out of its operating range and add some extra charge. Right: SCP Gated Mode with readout. Note that GM_{Bef} and GM_{Aft} are now reversed. The charge loss in the top diagram amounts to 36%. The tail of the charge distribution after the Gated Mode is just visible in the left bottom corner of the diagram. If the *GateOn* voltage is reduced further by 1 V to 10 V the charge loss would be curtailed even more to about 85%. Again with higher *GateOn* voltage some charge is added.

7.5.4 Experiment B: Junk Charge Prevention

In contrast to experiment A, the laser now impinges on an empty DEPFET frame during the Gated Mode. Ideally there should be no charge detected in subsequent frames.

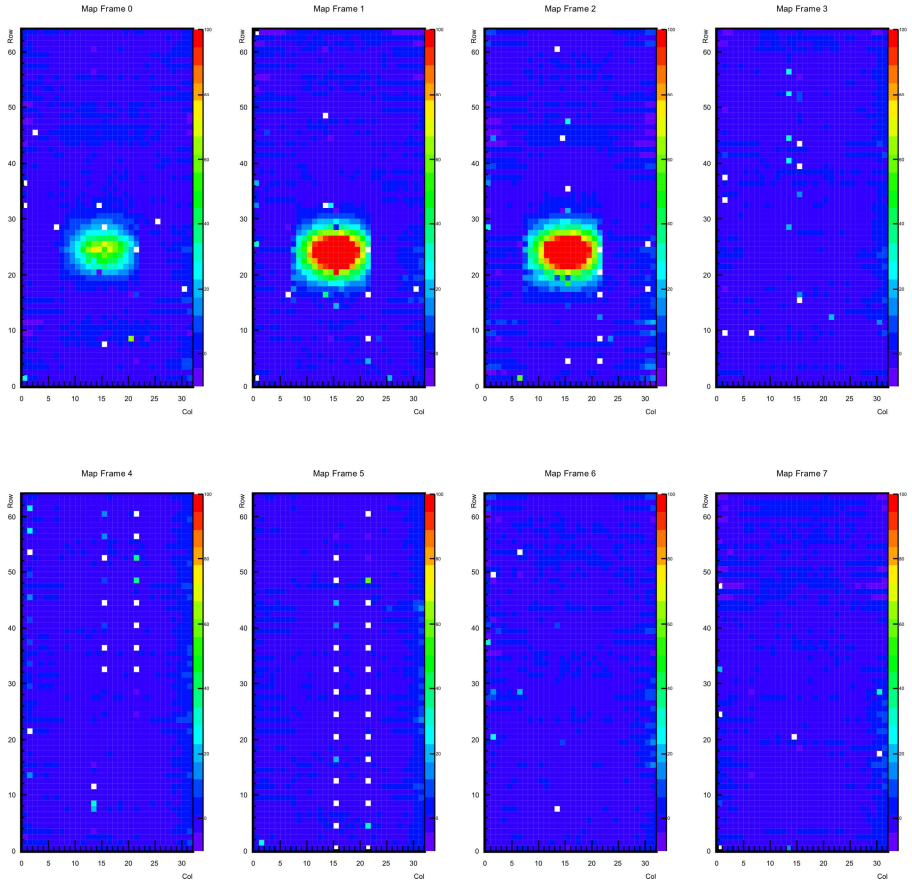


Figure 7-15: JCP sequence RL-R-C-G-GL-G-R-R Gated Mode without readout and a laser pulse width of 1 µs and 800 mV Amplitude.

Figure 7-15 demonstrates that the gated frames can withstand relatively large charge doses. Figure 7-16 on the other hand demonstrates that this is only true for the Gated Mode with readout. Since a *Gate* is still sensitive for 100 ns during readout the laser pulse generates charge which can be faintly seen in frame 6 – 8. To be fair, the Gated Mode without readout keeps one row continuously open and therefore sensitive before returning to normal operation. For the case shown in Figure 7-15 the program code always keeps the bottom row sensitive, so if the laser pulse would have been placed to the lower edge instead, a section of the spot would be visible.

The readout mechanism during the Gated Mode enters a “dead zone”: while the Gated Mode without readout does not allow for data taking at all, the Gated Mode with readout suffers from junk charge and high pedestal shifts producing unusable readout data.

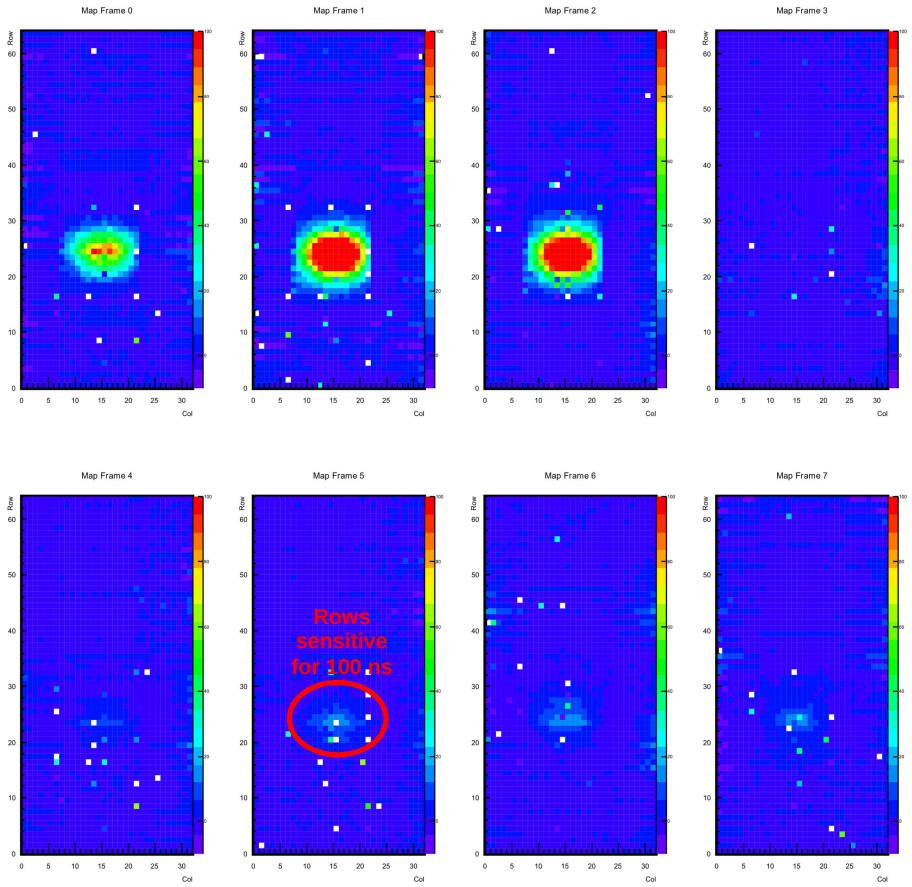


Figure 7-16: JCP sequence RL-R-C-G-GL-G-R-R Gated Mode with readout and a laser pulse width of 1 µs and 800 mV Amplitude.

7.5.5 Pedestal Analysis

The high *Clear* voltage applied to the matrix rows during the Gated Mode capacitively couples to the drain lines. This in turn causes an overshoot or pedestal shift when switching into the Gated Mode or reverting back to normal operation. More specifically a displacement charge induces a current flow which temporarily drives the DCDB out of its operational range. Additionally, the large voltage shift induces current fluctuations within the matrix and the SwitcherB chip, distorting the successive pedestal measurements.

For assessing the benefit of the Gated Mode it is extremely important to know how long the recovery takes after gating. To measure this effect 8 consecutive frame sequences were analyzed: the first frame read & *Clear* serves as a reference base, then two Gated Mode without readout frames follow up, subsequently accompanied by 5 more read & *Clear* frames as shown in Figure 7-17. Since the Gated Mode was not switched off abruptly, frame 4 is considered as a transition frame and hence of restricted use for this analysis.

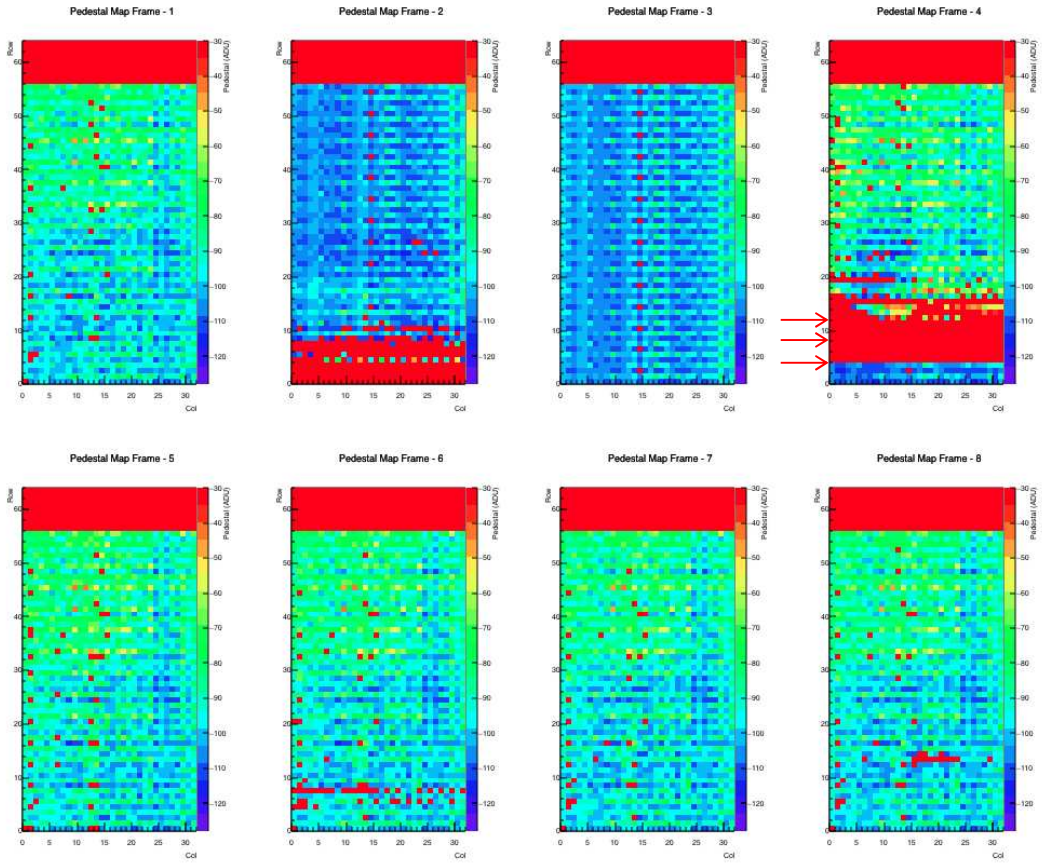


Figure 7-17: Pedestal Frame sequence C-G-G-C-C-C-C-C Gated Mode without readout. The red bar on top of each frame represents a faulty row which was masked for the analysis. The red area at the bottom of frame 4 illustrates that the Gated Mode is not fully disabled after frame 3 but takes additional 300 ns for switching off all channel groups. The red arrows in frame 4 indicate actual readout position when the Gated Mode is switched off for column groups 2,3 and 4, respectively.

The pedestal shift is composed of two influencing variables as shown in Figure 7-18. The first one is a global shift, which can be removed by the common mode correction. The second one is an idiosyncratic increase of each pixel pedestal, which in first order can be approximated to a gaussian distribution with an RMS value of about 2 ADU [99]. However, on closer examination the right diagram in Figure 7-18 exhibits two peaks which can be attributed to the unexpected observation that the matrix appears vertically divided into two parts and the pixels connected to the first 16 DCDB channels of the matrix behave differently compared to the second half.[105] In frames 6 – 8 the RMS value shrinks down to 0.81, 0.33 and 0.13, respectively.

It is difficult to assess whether these fluctuations are low enough to obtain reasonable data. At this point it may be beneficial to recall that the primary reason for the application of pixel detectors is to get a better position resolution.

[105] effectively this diagram represents an overlay of two different distributions

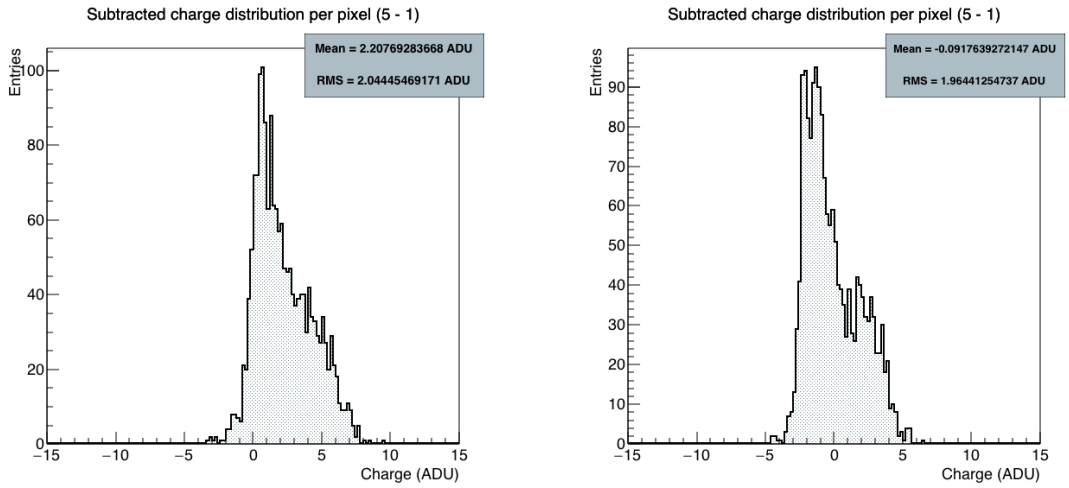


Figure 7-18: Left: total pedestal shift after the Gated Mode. The histogram shows the value difference of each pixel between frame 5 and frame 1. In an ideal world just one single peak at 0 with 2048 entries would appear. Right: pedestal variation after common mode correction basically shifting the mean to the left by 2 ADUs.

In case of a single pixel hit and uniform particle density the average difference between real and measured impact position is given by [100]:

$$\sigma_{position} = \frac{p}{\sqrt{12}} \tag{7-9}$$

with p the pixel pitch. For DEPFET pixels a spatial resolution of $p_x/\sqrt{12} = 14.4\ \mu m$ and $p_y/\sqrt{12} = 21.65\ \mu m$ can be achieved. If the charge is shared by more than one pixel a particular algorithm is needed to cluster the collected data. One of the simplest methods for local position reconstruction is the Center of Gravity (COG) method derived from the well-known Center of Mass formula by replacing the mass term by the charge:

$$\vec{r}_{COG} = \frac{\sum_{ij} q_{ij}\vec{r}_{ij}}{\sum_{ij} q_{ij}} \tag{7-10}$$

with $\vec{r}_{COG}$ the center of gravity coordinates and q_{ij} and $\vec{r}_{ij}$ the charge and mid position of a cluster pixel ij respectively.

Apart from the pixel geometry the detector resolution also depends on the zero suppression cut. Fixing this threshold too high would reduce the detector occupancy, but inevitably part of the information will be lost. On the other hand if this threshold is set too low the position resolution could suffer from noisy pixels adding some fake signals.

To get an idea of the pedestal shift effect, let us construct an extreme example with a possible MIP hit, which is spread on a 3×3 cluster as shown in the left of Figure 7-19. Assuming a perfect detector the COG method would position the hit at (placing the middle of the seed pixel arbitrarily to the origin):

$$\vec{r}_{COG} = \frac{20 \cdot \begin{pmatrix} 0 \\ 0 \end{pmatrix} + 1 \cdot \begin{pmatrix} -50 \\ 0 \end{pmatrix} + 10 \cdot \begin{pmatrix} 50 \\ 0 \end{pmatrix} + 2 \cdot \begin{pmatrix} 0 \\ 75 \end{pmatrix}}{33} = \begin{pmatrix} 13.63\ \mu m \\ 4.54\ \mu m \end{pmatrix}$$

If the zero suppression cut for the neighboring pixels is set to 5 ADUs the center of gravity would change to:

$$\vec{r}_{COG} = \frac{20 \cdot \begin{pmatrix} 0 \\ 0 \end{pmatrix} + 10 \cdot \begin{pmatrix} 50 \\ 0 \end{pmatrix}}{30} = \begin{pmatrix} 16.66\ \mu m \\ 0\ \mu m \end{pmatrix}$$

Now inserting maximum pedestal shift values (±5) just to the upper right region the new position would change to

$$\vec{r}_{COG} = \frac{15 \cdot \begin{pmatrix} 0 \\ 0 \end{pmatrix} + 7 \cdot \begin{pmatrix} 50 \\ 75 \end{pmatrix} + 15 \cdot \begin{pmatrix} 50 \\ 0 \end{pmatrix} + 5 \cdot \begin{pmatrix} 50 \\ 75 \end{pmatrix}}{43} = \begin{pmatrix} 23.25\ \mu m \\ 20.93\ \mu m \end{pmatrix}$$

which deviates from the real position by

$$\begin{pmatrix} 23.25 \\ 20.93 \end{pmatrix} - \begin{pmatrix} 13.63 \\ 4.54 \end{pmatrix} = \begin{pmatrix} 9.62\ \mu m \\ 16.39\ \mu m \end{pmatrix}$$

which is still close to the required spatial resolution of $\begin{pmatrix} 10\ \mu m \\ 15\ \mu m \end{pmatrix}$ for the PXD detector .

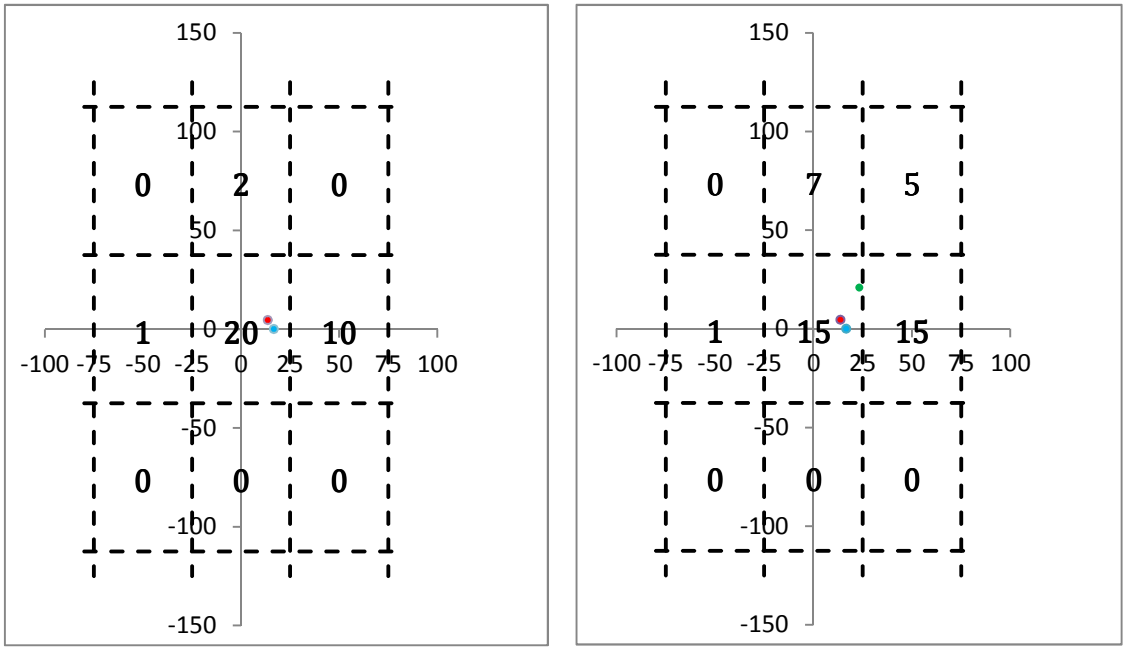


Figure 7-19: Left: 3×3 cluster with ideal (red) and zero suppressed (blue) center of mass position. Right: extreme case where pixel cells are shifted incorporating maximum pedestal shift values. Green spot indicates effective change of position.

The COG method was chosen just for illustrative purposes. For DEPFET pixels much more sophisticated approaches are used. Especially the assumption of a linear relation between the charge fractions and the distance between the centers of two pixels is abandoned. In any case this effect imposes a time penalty on the readout of subse-

quent frames and further investigations, especially Monte Carlo analyses, are necessary to determine the point in time where useful data can be registered.

Another interesting insight into the Gated Mode characteristics is delivered by adding together the pixel values row by row and subtracting them from the corresponding row sum in the reference frame. Figure 7-20 clearly shows the distinct settling down of the amplitudes within the first frame after the Gated Mode (diagram left above) coming almost to rest in the last frame.

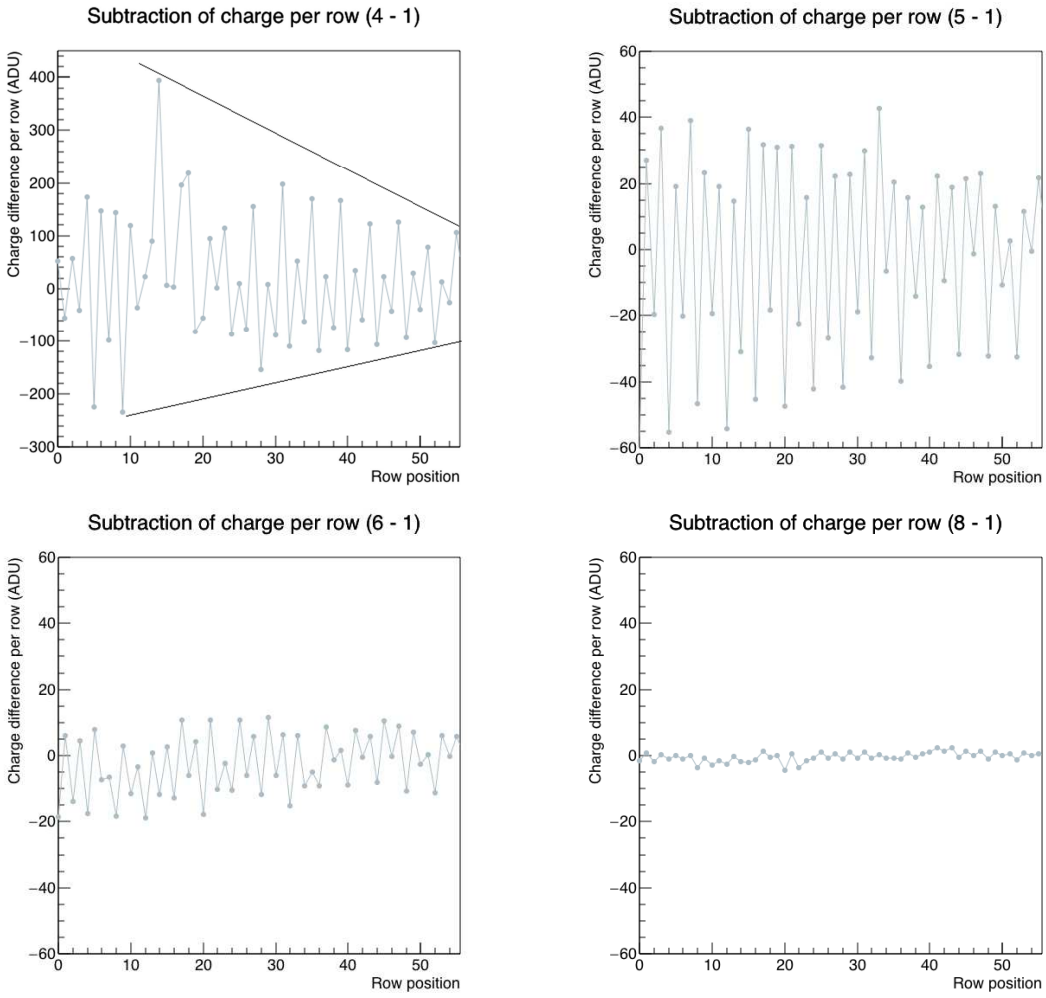


Figure 7-20: Subtraction of summed row values from the corresponding row sum in the reference frame. The big amplitude in row 14 of the first diagram is due to the fact, that the Gated Mode is switched off with a time lag of about 300 ns. To get the average deviation of a pixel the amplitude has to be divided by 32 (pixel number per row).

8 Results

The whole study can be subdivided into two main parts: a characterization of the steering and readout chips related to the Gated Mode and an in-depth analysis of the Gated Mode by means of a detector prototype system.

First of all special attention should be paid to system biasing. This involves both a stable power supply and the determination of the appropriate voltages. The operation of the test setup requires a total of 17 voltages. Even small voltage variations can lead to substantial changes concerning the system characteristics. To provide an example, despite optimized DCDB settings some matrix pixels randomly produced error codes especially apparent in the second and third position after the MSB. As a result many fake hits were detected in the ±32 and ±64 ADU area. Only after changing the digital voltages for DCDB and DCDRO from both 1.8V → 1.9/1.95V respectively this problem could be fixed.

On the matrix side there are a lot of capacitive couplings which have to be scrutinized and adjusted carefully.

The key measurement results are as follows:

- DEPFET detector prototype system was operated at full target speed of 320 MHz.

- DCDB pipeline was optimized to very low noise levels around 0.6 ADUs. The long missing code problem (≥5 ADUs), which affected almost 25% of all ADC channels was still not solved for DCDB pipeline. After extensive measurements under the supervision of the designer the origins of the problem were understood (at least by the designer). A final chip revision will repair this deficiency.

- Various Gated Mode sequences were programmed and tested directly on the SwitcherB output channels in order to find out whether this chip works properly. Apart from some discrepancies to the reference manual with respect to the described reaction time and the actual one measured by an oscilloscope this chip behaved exactly as expected.

- To calculate the number of electrons corresponding to one ADU a calibration is necessary. For this objective a Cd-109 is best suited for DEPFET sensors, since its characteristic photopeak at around 22 keV mimics almost exactly one MIP. At a $GateOff$ voltage of -3.9 V an internal amplification of $380.9\ pA/e^-$ was observed.

- The results of the Gated Mode tests are summarized in Table 8-1:

Criteria	GM w/o RO	GM w RO
Turning full matrix into the Gated Mode	*Minimum 31.25 ns*	*Minimum 406.5 ns (shorter possible at cost of losing synchronization)*
Getting out of the Gated Mode	*Minimum 31.25 ns*	*Minimum 300 ns (lower possible at cost of losing synchronization)*
Charge loss during the Gated Mode	*No charge loss within a wide voltage range*	*No charge loss choosing relatively high $GateOff$ voltage*
Protecting sensor from junk charge	*No junk charge stored*	*Junk charge stored in activated rows*
Sensitiveness of detector during the Gated Mode	*Only actual line is sensitive during the whole gating period*	*Rows switched on subsequently after gating are each sensitive for 100 ns*
Synchronization with downstream electronics	*Out of synchronization since CLK stops toggling (can be restored by applying fast CLK signals)*	*CLK remains synchronized*
Pedestal variation after the Gated Mode	*Very high random pixel shifts immediately after the Gated Mode operation fading out to an RMS of 2 ADUs after 1.2 µs with maximum fluctuations of ±5 ADUs*	
Total time loss for switching in and out of the Gated Mode and turning back to normal readout operation	*300 ns (including fast clocking for synchronization and a full $GateOn$ time of 200 ns during passage of noisy bunches) + 1.2 µs for pedestal fade out (further analysis required for reducing this figure)*	*906.5 ns + 1.2 µs*

Table 8-1: Summary of the Gated Mode results

- As a general result all measurements indicate that the Gated Mode works and could potentially make a major contribution to reduce the PXD dead time during the cooling period of the noisy bunches, though system effects of large matrices were not considered yet.

9 Conclusion and Outlook

The procedure of DCDB settings optimization revealed that some voltages offer just little margin permitting only a very narrow ideal operation range. The long missing code problem can lead to substantial performance deficiencies if not sorted out by the next chip version.

Regarding the Gated Mode operation a strict time limit of 10 µs defines the maximum tolerable gating period. This was inferred from the revolution frequency of the noisy bunches (caused by the continuous injection scheme of SuperKEKB) passing the detector. Taking into account all programming and hardware developing efforts it is essential to keep the total Gated Mode related period well below 5 µs, otherwise all expenditures would not be worth the trouble. In an ideal world the gating mechanism would instantaneously blind the detector during the 100 ns passage of the noisy bunches and afterwards immediately return to normal readout operation. In reality there is a certain time-lag to switch in and out of the Gated Mode followed by serious current fluctuations, that impede readout for a distinct time period. In principle, these two parameters, namely the time to switch into the Gated Mode and the time to switch back into normal operation, are qualified for further optimization and one should bear in mind that every µs saved increases the data gain by 10% throughout the damping time.

Considering the beam injection process the Gated Mode could gain significantly in importance: until now it was assumed that the beam cooling takes about 4 ms. This was simply taken over from former KEK experiences. If the new nano beam scheme causes unforeseen trouble and the damping time elongates the usefulness of the Gated Mode would increase substantially. In the extreme case where the cooling period almost matches the injection interval of 20 ms this feature would be indispensable for a meaningful operation of the PXD at SuperKEKB.

A clear recommendation is given in favor of applying the Gated Mode without readout. On the one hand this reduces the switching time by more than 600 ns. Synchronization issues can be solved by introducing fast clock signals after gating in order to catch up the row delay. This mode also offers much more stability in terms of a wider applicable voltage range concerning signal charge preservation. The high pedestal variations immediately after gating require further in-depth analysis to determine the optimal point in time where the DAQ system is able to accept normal readout data. This could be well below 1.2 µs. In this context it is inevitable to make further measurements on hybrid 4.1 board to determine the absolute minimum for the total gating time.

By all means the situation is different for a full half ladder. Because of larger capacitances one can expect larger RC times and maybe a longer time period for pedestals settling down. Moreover the communication with DHP and DHE introduces additional complexity and must be tested thoroughly. Finally several new, not fully understood

effects, such as for example different pedestal shifts between the first and second horizontal half of the matrix as shown in Figure 9-1, deserve further investigations.

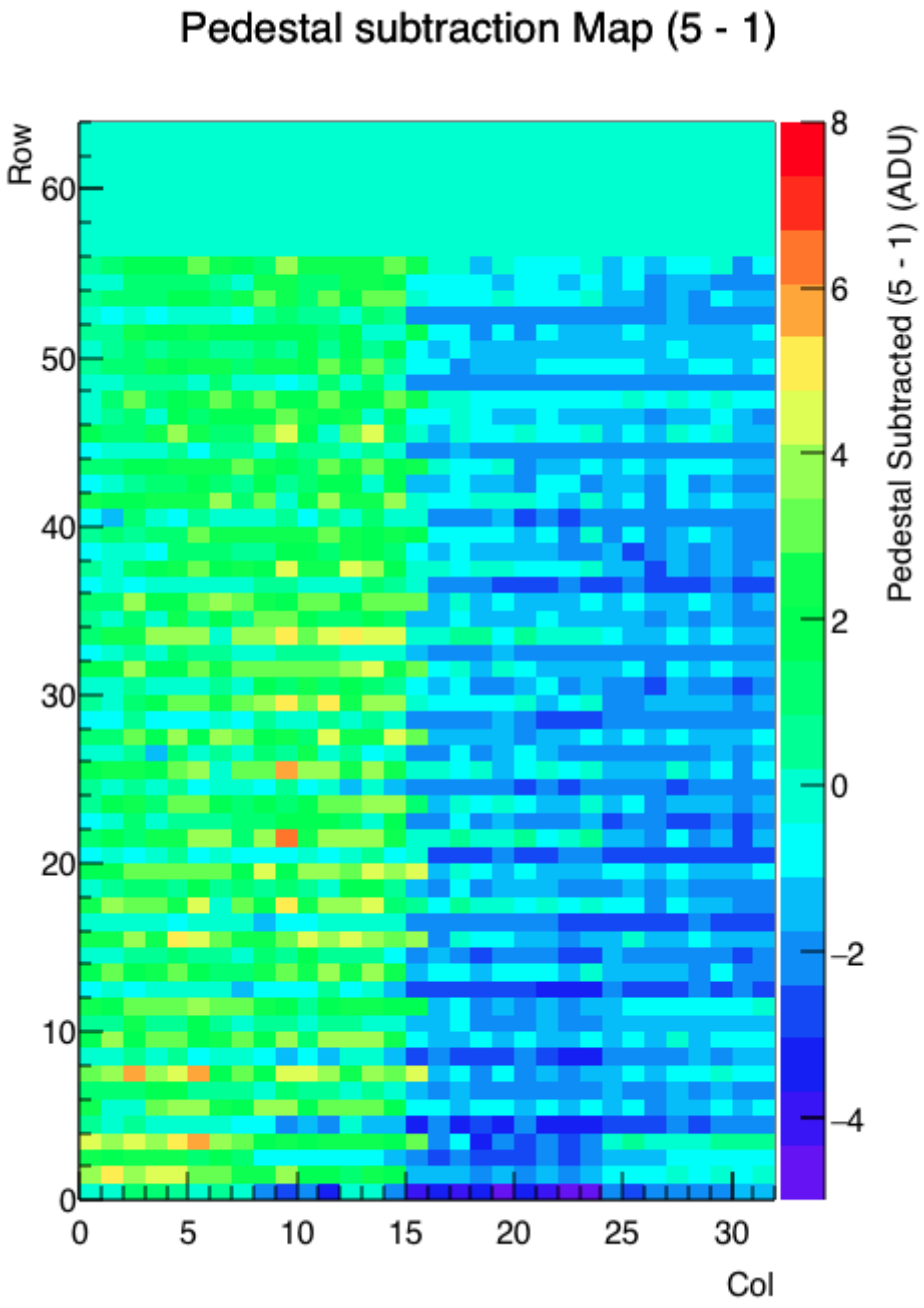


Figure 9-1: Different pedestal shifts in the first and second half of the matrix after applying the Gated Mode

Appendix A: B-Meson Decay

The derivation of the B meson decay distance starts with the center of mass energy E_{CM} for the $\Upsilon(4S)$ resonance using natural units $\hbar = c = 1$:

$$E_{CM} = \sqrt{s} = \sqrt{(p_{HER} + p_{LER})^2} \tag{A-1}$$

with $p_{HER} = (E_{HER}, \vec{p}_{LER})$ & $p_{LER} = (E_{LER}, \vec{p}_{LER})$ as the energy-momentum four-vector of the high energy respectively low energy ring. Assuming a head-on collision $(\cos\theta = -1)$ and applying four-vector properties $(p^2 = E^2 - \vec{p}^2 = m^2)$ the equation for the center of mass energy can be rearranged to:

$$\begin{aligned} s = {} & {p_{HER}}^2 + {p_{LER}}^2 + 2p_{HER}p_{LER} \\ = {} & {m_{HER}}^2 + {m_{LER}}^2 + 2E_{HER}E_{LER} - 2\vec{p}_{HER}\vec{p}_{LER} \\ = {} & {m_{HER}}^2 + {m_{LER}}^2 + 2E_{HER}E_{LER} + 2|\vec{p}_{HER}||\vec{p}_{LER}| \end{aligned} \tag{A-2}$$

$$\approx 4E_{HER}E_{LER} \qquad (E \approx p \gg m)$$

The energy level of the $\Upsilon(4S)$ resonance is known to be 10.58 GeV, accordingly

$$\begin{aligned} E_{CM} = \sqrt{s} = 2\sqrt{E_{HER}E_{LER}} = 10.58\ GeV \\ \Rightarrow E_{HER}E_{LER} = 27.9841 \approx 28 \end{aligned} \tag{A-3}$$

Various energy combinations would fulfill this requirement as for example $5.3 \times 5.3\ GeV$ representing a symmetric energy collider. In the rest frame the center of mass energy of the $\Upsilon(4S)$ resonance corresponds to the mass of a parent particle $M = E_{CM}$ decaying into two B mesons with equal mass $m_B = m_{\bar{B}} = 5.28\ GeV$. They are emitted with an angle of 180° ($\vec{p}_B = -\vec{p}_{\bar{B}}$, $|\vec{p}_B| = |\vec{p}_{\bar{B}}| = |\vec{p}|$) between them.

$$s = M = (p_B + p_{\bar{B}})^2 = (E_B + E_{\bar{B}}, 0)^2 = (E_B + E_{\bar{B}})^2 \tag{A-4}$$

$$M^2 = 2m_B^2 + 2E_BE_{\bar{B}} + 2|\vec{p}|^2 = 2m_B^2 + 2E_B(M - E_B) + 2(E_B^2 - m_B^2) \tag{A-5}$$

$$\Longrightarrow E_B = \frac{M}{2} \tag{A-6}$$

$$|\vec{p}_B| = |\vec{p}_{\bar{B}}| = \frac{\sqrt{M^2 - (2m_B)^2}}{2} = \frac{\sqrt{(10.58^2 - 10.56^2)}}{2} = 0.325\ GeV \qquad \text{(A-7)}$$

Applying an active[106] Lorentz boost transformation in z-direction,

$$\begin{bmatrix} E' \\ p'_x \\ p'_y \\ p'_z \end{bmatrix} = \begin{bmatrix} \gamma & 0 & 0 & \beta\gamma \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ \beta\gamma & 0 & 0 & \gamma \end{bmatrix} \begin{bmatrix} E \\ p_x \\ p_y \\ p_z \end{bmatrix}$$

in the rest frame with $p_z = 0$ would give (A-8)

$$E' = \gamma E_{CM}$$

$$p'_z = \beta\gamma E_{CM}$$

$$\Rightarrow \beta\gamma = \frac{p'_z}{E_{CM}} = \frac{|\vec{p}_B| + |\vec{p}_{\bar{B}}|}{E_{CM}}$$

with $\beta\gamma$ the Lorentz boost parameter. Hence at a symmetric collider the average flight distance $\langle L \rangle$ is

$$\langle L \rangle = \beta\gamma c\tau_B = ((|\vec{p}_B| + |\vec{p}_{\bar{B}}|)/E_{CM})(459\mu m) = (0.65/10.56)(459\mu m) \approx 28\mu m \qquad \text{(A-9)}$$

assuming a mean lifetime of $\tau_B = 1.53 \times 10^{-12}$. One can see that at symmetric colliders the newly created B mesons would remain nearly stationary and hence the decay distance of the B particles would be very small, impossible to be measured by today's vertex trackers.

A method for circumventing this problem is to apply unequal energies, so the entire system experiences a Lorentz boost with respect to the laboratory. For example $8.0 \times 3.5\ GeV$, the asymmetric energy of the former KEK collider is fulfilling condition (A-3). A very large energy asymmetry is provided by the positron-electron-project (PEP-II), a collider hosted by the BaBar (*"B and B-bar"*) experiment at SLAC National Accelerator Laboratory Stanford University with $9.0 \times 3.1\ GeV$.

On the shady side there exists a direct relationship between energy difference and emittance growth. Indeed the higher energy would compress the emittance of the HER but this is bought dearly with a much higher emittance in the LER.[107] Additionally, a higher boost would deteriorate detector acceptance since this would shift the vertices

[106] in active Lorentz transformations the particle gets transformed in contrast to passive transformation where the coordinate system gets transformed

[107] in order to compensate for different emittances, the LER is additionally equipped with a damping ring, while for the HER a low emittance gun is sufficient

more in the direction of the non-sensitive cap region of the PXD detector. The optimal value of the asymmetry must be found by balancing these factors. For SuperKEKB a proportion of $7 \times 4\ GeV$ was chosen primarily in order to reduce emittance growth for the LER thereby supporting the nano beam scheme.

$$p = \begin{pmatrix} E_{HER} \\ 0 \\ 0 \\ E_{HER} \end{pmatrix} + \begin{pmatrix} E_{LER} \\ 0 \\ 0 \\ -E_{LER} \end{pmatrix} \qquad (E \approx p \gg m)$$

$$|\vec{p}| = m\gamma\beta \quad and \quad E = m\gamma \tag{A-10}$$

$$\Rightarrow \beta = \frac{|\vec{p}|}{E} = \frac{E_{HER} - E_{LER}}{E_{HER} + E_{LER}} = \frac{3}{11} = 0.\overline{27} \tag{A-11}$$

$$\gamma = \frac{1}{\sqrt{1-\beta^2}} \Rightarrow \gamma\beta = 0.2835 \tag{A-12}$$

As a result the asymmetric energy mode gives the $B\bar{B}$ system a net laboratory momentum which increases the path length before decay. An overview of Lorentz boosts and decay lengths for different e^+e^- colliders is given in Table A-1.

Collider	HER (GeV)	LER (GeV)	$\beta\gamma$	$\langle L \rangle\ (\mu m)$
PEP II	9	3.1	0.5585	256
KEK	8	3.5	0.4252	195
SuperKEKB	7	4	0.2835	130
CESR[108]	5.3	5.3	0.06	28

Table A-1: Asymmetric colliders facilitate time evolution measurements with far better accuracy: the B meson decay lengths rely heavily on electron-positron energy spread.

In general the following rule holds: the higher the energy difference the higher the decay distance.

[108] Cornell Electron Positron Storage Ring

Appendix B: Pair creation of a 660nm Laser in Silicon

The following formula gives the doping dependence of the energy band gap of silicon [101]:

$$\Delta E_g = -\frac{3q^2}{16\pi\varepsilon_s}\sqrt{\frac{q^2 N}{\varepsilon_s kT}} = -22.5\sqrt{\frac{N}{10^{18}cm^3}}meV\ (Silicon) \qquad \text{(B-1)}$$

where N is the doping density, q the electronic charge, $\varepsilon_s = 11.7$ is the relative permittivity of silicon, k is the Boltzmann's constant and T the temperature in Kelvin.

With help of equation (B-2)

$$E_{photon}[eV] = \frac{hc}{\lambda} = \frac{4.1357 \times 10^{-15} eV \cdot 3 \times 10^8\, m/s}{660 \times 10^{-9} m} \approx 1.88\ eV \qquad \text{(B-2)}$$

where h is the Planck constant, c the speed of light and λ the wavelength, one can easily calculate the energy of a single photon for a laser wavelength of λ= 660 nm:

A laser pulse can be obtained by using a continuous wave (CW) laser in conjunction with an external pulse generator[109] which transmits the light only during selected short time intervals. Ideally the laser pulse resembles a rectangle, in reality the rise and fall time of at least 5 ns [102] could have some impact if a very short laser pulse is applied.

The power is measured in μW with an optical power meter[110]. In order to get the comparable energy of a single pulse it has to be converted in electronvolt and multiplied by the pulse length τ:

$$E_{Laser}[eV] = \frac{Power_{Laser}[\mu W]}{1.602176565 \times 10^{-13}\,\mu J/eV} \cdot \tau \qquad \text{(B-3)}$$

The number of photons produced with one laser pulse is simply the laser energy divided by the photon energy:

$$\#photons = \frac{E_{Laser}}{E_{photon}} \qquad \text{(B-4)}$$

[109] Agilent 33250A

[110] Newport Optical Power Meter Model 1916-R

Another important factor influencing the e/h-pair creation rate stems from the p^+ implant on the backside of the DEPFET sensor. Since all irradiation measurements were executed on the backside of the DEPFT sensor the photons experience a charge carrier loss due to recombination, which is very difficult to evaluate. The doping density distribution after several **annealings** can be approximated by half a Gaussian curve as shown in Figure B-1.

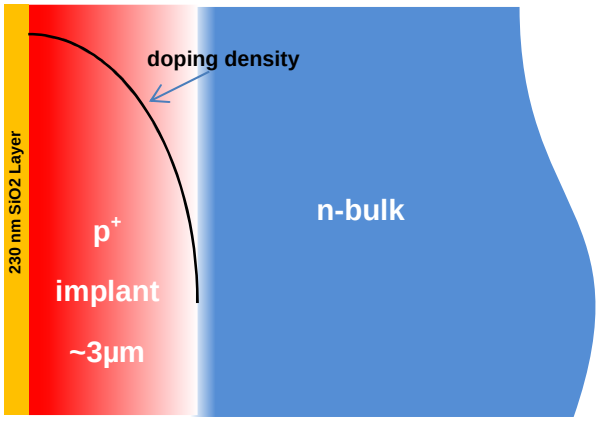


Figure B-1: Cross sectional view on backside of DEPFET PXD6 sensor

Using the well-known mass action law $p \times n = n_i^2$ and inserting a peak doping density of 10^{19} immediately after the SiO_2 layer and an n-bulk doping of 10^{10}, one calculates a very low electron density for this region. The high p^+-n difference causes the recombination procedure to set in very quickly and almost no electron diffuses to the internal gate. As one moves closer to the p-n junction the doping concentration decreases and accordingly the recombination lifetime rises, so more electrons escape to the n-bulk area. A theoretical approach for calculating recombination rates and lifetimes is provided by Shockley-Read-Hall statistics which are described in [40]. However, this assumes that one knows in detail the exact doping density distribution of the p^+ implant. Figure B-2 illustrates the doping profile of the PXD6 sensor on the backside. The data was obtained with help of secondary ionizing mass spectroscopy (SIMS). A primary ion beam removes the p^+ doping area layer by layer and a mass spectrometer determines the elemental composition of the surface. The data left to the first red bar must be ignored as well as the narrow peak which is just an artefact from the transition silicon oxide to the almost 3 µm thick p^+ layer.

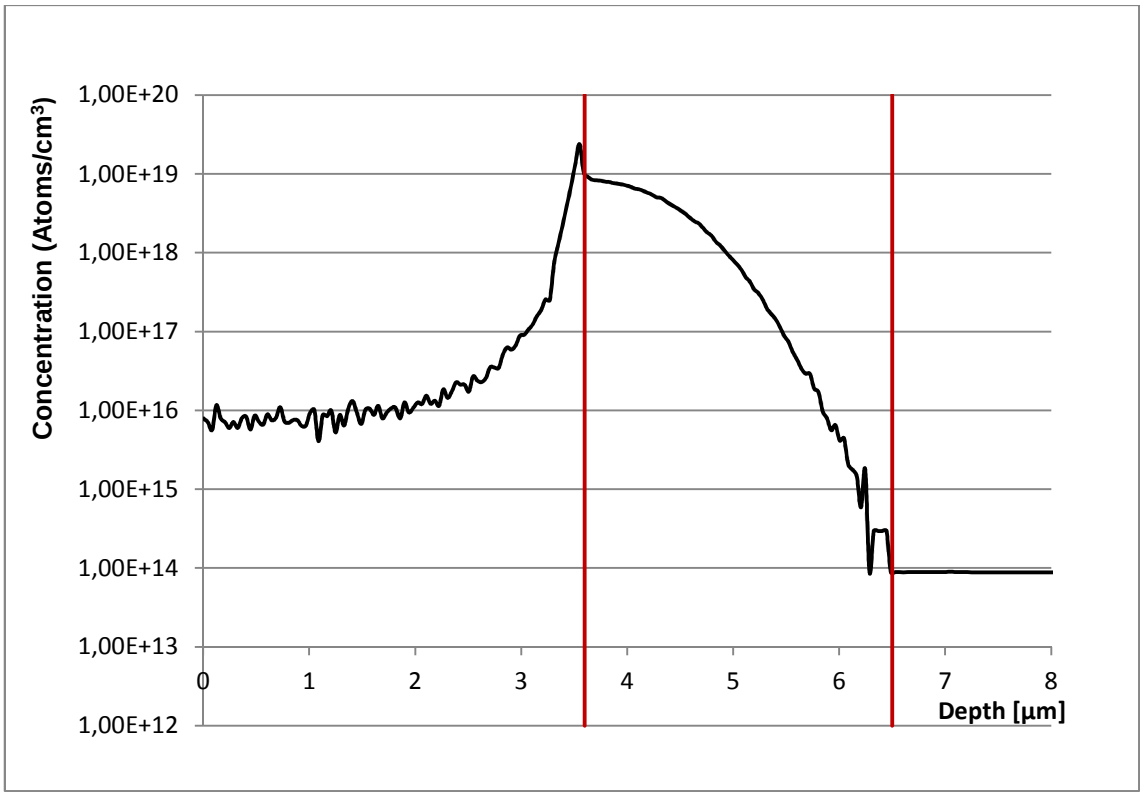


Figure B-2: SIMS depth profiling on PXD6 backside.

An alternative one simply does not care about all these “hard-to-get” parameters like pair creation energy or recombination rates which are anyway afflicted by more or less margins of error. Several companies[111] are specialized to determine the whole detector response function depending on different laser wavelengths. The only requirement is a silicon diode with the corresponding characteristics.

For the calculation of the reflectivity coefficient the 230 nm thick oxide layer has to be factored in. A thorough analysis also includes multiple scattering effects though this is better solved computer-assisted, for example with the open source software *OpenFilters*. As a result the reflectivity for the PXD6 sensor is calculated at 34.88% and the beam intensity decreases in value to $1/e \approx 36.8\%$ after 3.88 µm. Putting everything together:

$$\#electrons = \frac{E_{Laser}[eV] \cdot (1-R)\left(\delta + \exp(-\frac{3}{3.88})\right)}{1.88\ eV\ per\ e^{-}/h\ pair\ in\ Si} \qquad \text{(B-5)}$$

with δ the proportionate share of uncombined electrons diffusing from the p^+ layer to the n-bulk (for the equivalent MIPs calculation in section 7.5.3 and 7.5.4 a $\delta = 10\%$ was assumed). Dividing the measured ADU value by the number of electron delivers the internal amplification g_q.

[111] e.g. Gigahertz-Optik GmbH

Appendix C: Radioactive Source Formulas

A theoretical expression for the straight line distance R an electron covers for reaching its final resting place is given by the Kanaya-Okayama formula [103]:

$$R[m] = \frac{2.76 \times 10^{-11} A E_0^{5/3}}{\varrho Z^{8/9}} \frac{(1 + 0.978 \times 10^{-6} E_0)^{5/3}}{(1 + 1.957 \times 10^{-6} E_0)^{4/3}} \qquad \text{(C-1)}$$

where $A[u]$ is the standard atomic weight, E_0 $[eV]$ the incident energy, ϱ $[g\ cm^{-3}]$ the density, Z the atomic number and the term in brackets is a relativistic correction of energy E_0. The activity or actual number of decay events $A(t)$ of Cd-109 is calculated as:

$$A(t) = A_0 e^{-\lambda/t} \qquad with \qquad \lambda \equiv \frac{\ln(2)}{T_{1/2}} \qquad \text{(C-2)}$$

Cd-109 has half-life $T_{1/2} = 461.9\ d$. The photon emission probabilities, available as number of photons per 100 disintegrations, are taken from [95]. Note that the total emission probability for Cd-109 shown in Table C-1 is higher than one. This is due to the vacancies in the K- and L-shells resulting from EC transitions, inner conversion and from the Auger effect. The interaction or absorption probabilities are calculated with help of equation (7-7) based on interpolated μ/ρ-values taken from [94].

Cd-109 Photon Emissions	Energy [keV]	Photons Source [100 disint.]	Photons escaping Capsule	Photo-absorption [50µm Si (%)]	Final Absorption Silicon
XL	3,191	10,37	0,00527	98,76	0,00005
XK_{a2}	21,9906	29,21	23,5660	1,91	0,00451
XK_{a1}	22,16317	55,1	44,6135	1,88	0,00842
$XK_{b3,1,4}$	25,00	15,25	13,0986	1,46	0,00192
$XK_{b2,4}$	25,48	2,65	2,29488	1,39	0,00032
γ	88,0336	3,66	3,5107	0,10	0,00004
	Σ	**116,235**		without XL+γ	**0,01516**
Total Emission Prob.		**1,16235**			

Table C-1: Photon emission and absorption probabilities

The Cd-109 source is encapsulated in a 1.02 mm Beryllium cover which is backed by 0.127 mm silver. The combined attenuation is shown in column 4 of Table C-1. One can see that the Be-jacket with silver coating significantly impacts the absorption of XL rays, so this peak will not be visible in the detector. On the other side of the spectrum the high intensity γ-rays hardly interact with silicon, so again there will be no signal detected from this energy region. The energy difference of the two XK peaks is merely 3 keV, too low for the detector's intrinsic resolution, hence just one peak will be recorded eventually.

Concerning the source geometry as shown in Figure C-1 one has to consider that the radioactive source is collimated and therefore not all X-rays hit the sensor. Assuming a uniform emission distribution for all solid angles the sensor area can be treated as a sector of a sphere with radius corresponding to the source↔matrix distance of 10.1 mm (1.1 mm capsule thickness, 5.9 mm collimator length, 1 mm distance PCB, 1.6 mm PCB thickness, 0.1 mm glue between PCB and DEPFET sensor, 0.4 mm matrix cavity). The calculated ratio between sphere and matrix area $(1.6 \times 4.8\, mm^2)$ gives 180, thus the whole activity has to be adjusted by this denominator.

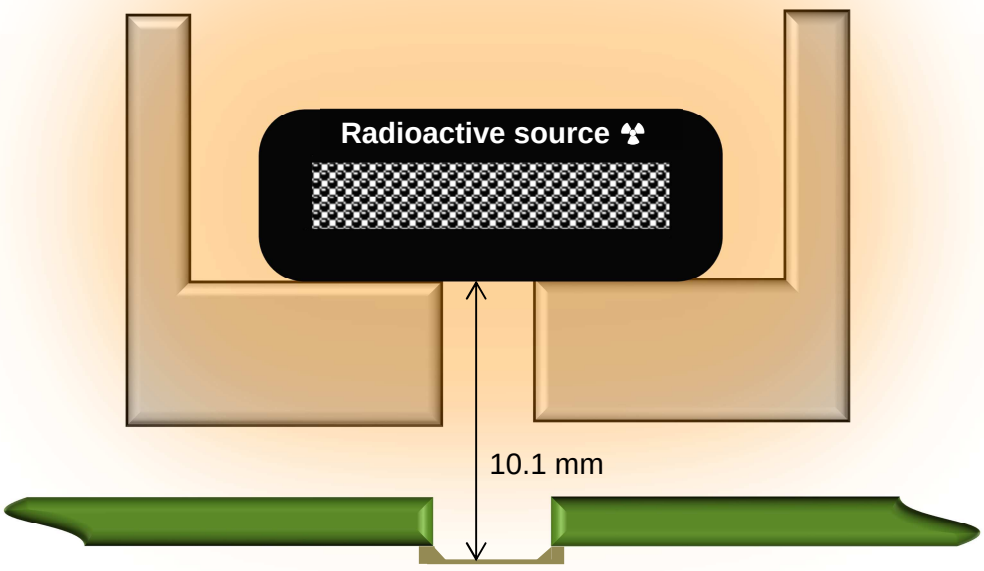
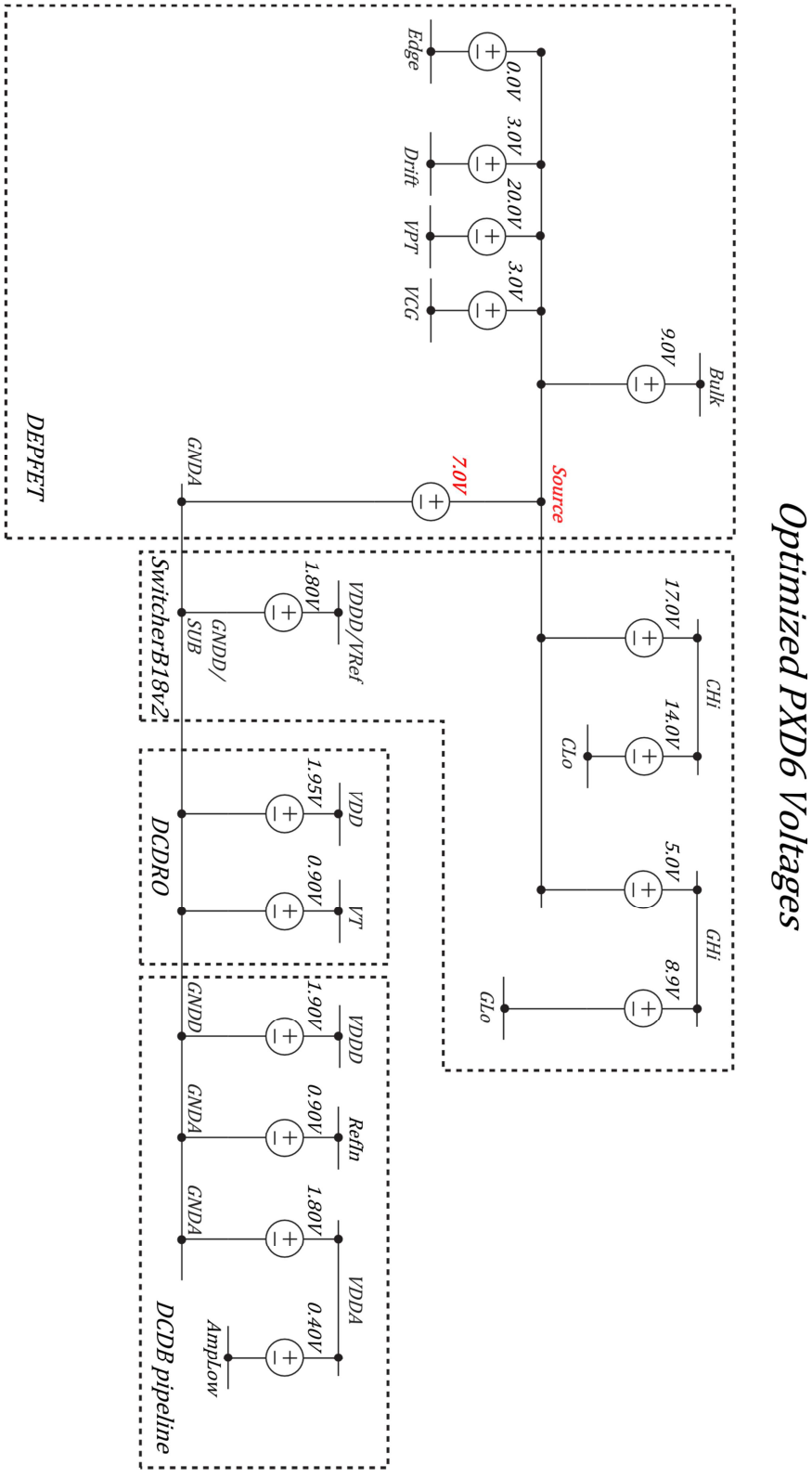


Figure C-1: Radioactive source geometry

Appendix D: Optimized Test Setup Voltages



Appendix E: SwitcherB Sequence Simulation

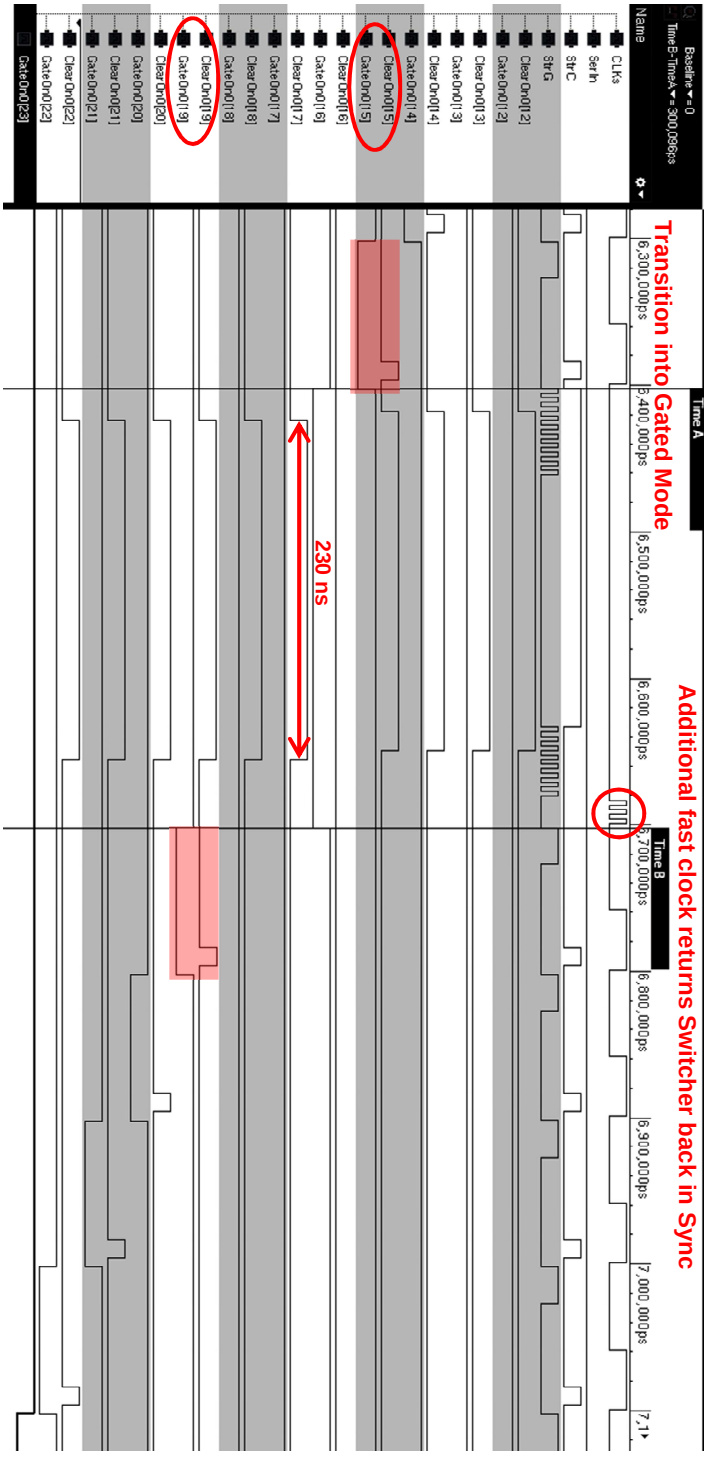


Figure E-1: SwitcherB sequence Gated Mode without readout comprising detail of column group 2 (8-15) and 3 (16-23). After 3 falling edges of *StrG,* the Gated Mode is activated for column group 2, another falling edge later the *Clear* pulses also turn to high for column group 3. Just enabled row 16 remains open for the whole gating period. After a Gated Mode duration of 230 ns the same strobe signals quickly pull out of the Gated Mode. The total time for the Gated Mode amounts to 300 ns. Three fast *CLK* signals ensure that normal read out resumes operation in the correct row 19.

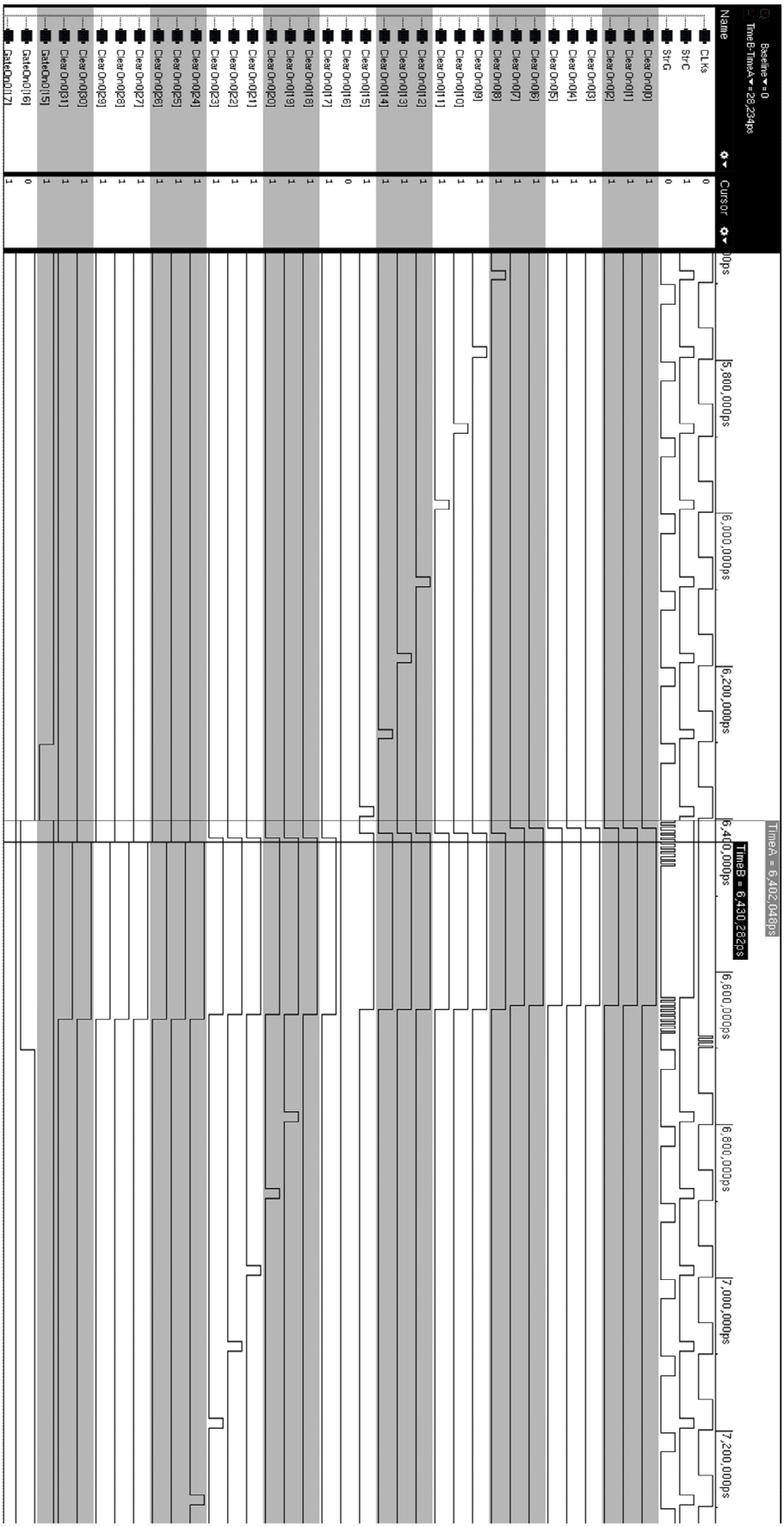


Figure E-2: Gated mode without readout showing all switcher channels while entering and exiting the Gated Mode within 31.25 ns.

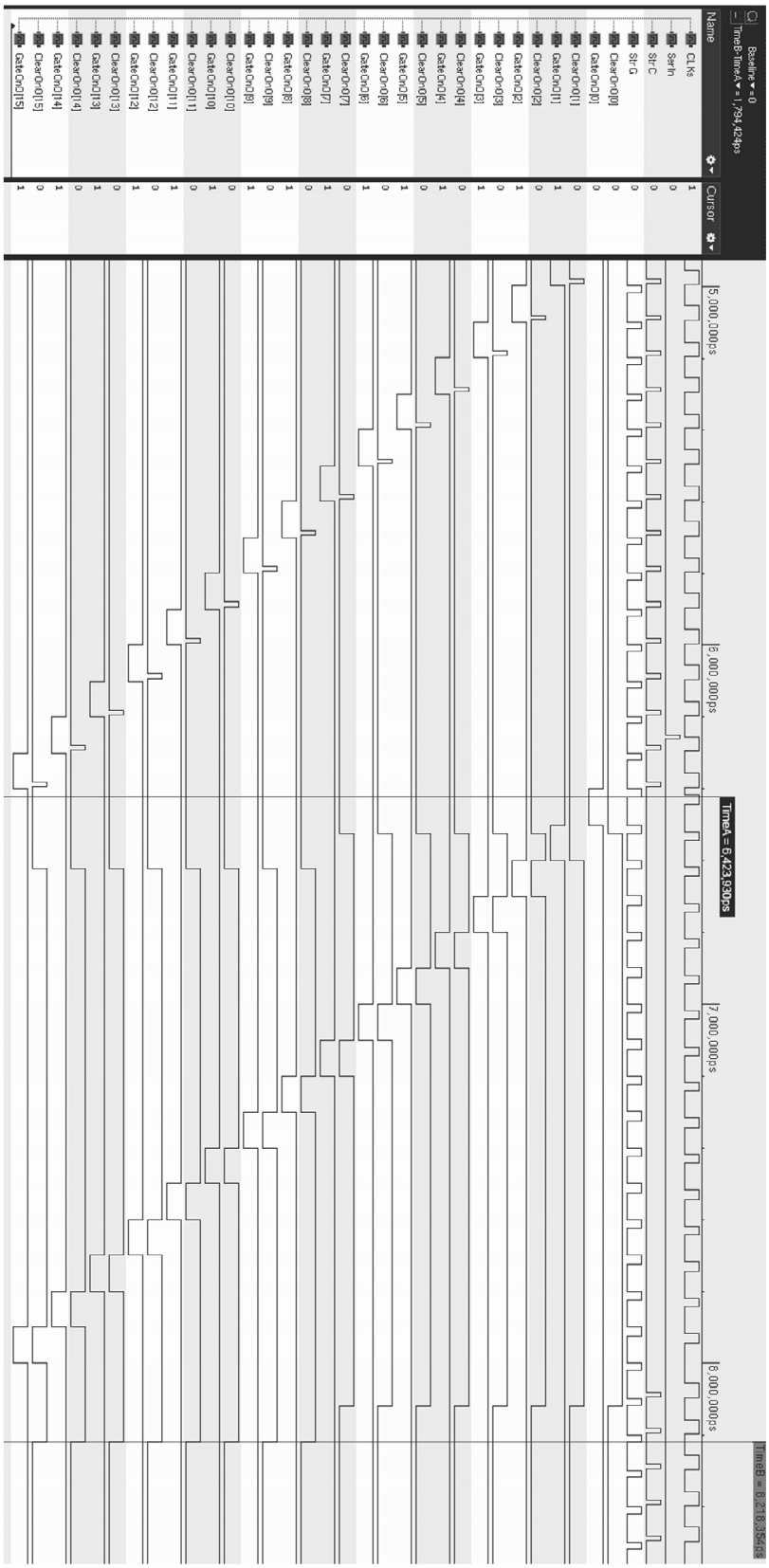


Figure E-3: Switcher sequence Gated Mode with readout. Upper part of the diagram shows a normal read & *Clear* operation. Rows are subsequently enabled for 100 ns and a short *Clear* pulse of 12.5 ns is executed at the end. A falling edge of *StrG* while *CLK* is high initiates the Gated Mode. Rows currently enabled are read out but not cleared. After the falling edge of *StrG* the first column group is activated. The *Clear* changes immediately to low on activated channels.

Glossary

Annealing: wafer annealing is a heating process that activates ion-implanted dopants, reduces structural defects and stress, and reduces interface charge at the silicon-silicon dioxide interface.

Auger Electron: when an electron of an inner shell is removed, leaving a hole, an electron from a higher energy level might jump to fill this hole. Energy must be simultaneously released. Most of the time this energy is released in the form of an emitted photon. Sometimes the energy is transferred to a third electron, the Auger electron, which is ejected from the atom carrying the excess energy in this radiationless process.

Ball Grid Array (BGA): standard chip housing enabling both fast and high density connections for integrated circuits. The bottom surface instead of the perimeter is used for the connections of the device.

Beta(tron) Function β: the β-function is the envelope around all trajectories of the particles circulating in the collider. Within the collider's magnet structure, which has a net focusing effect, the particles perform betatron oscillations with a position-dependent amplitude given by [104]

$$\beta = \frac{\sigma^2 \pi}{\varepsilon}$$

with σ representing the cross-sectional size and ε the emittance of the beam bunch. The range of a particle's transverse motion and the beta function as a measure of the beam cross-section depends on the beam focusing, which varies with position. If beta is low, the beam is narrower.

Bhabha scattering: electron-positron scattering process exchanging a photon without annihilating.

Boundary scan chain: method for testing off-chip interconnections based on IEEE Standard 1149.1

Built-in depletion region: bringing p-type and n-type doped silicon together the mobile charge carriers diffuse away leaving back a depletion region with ionized donor or acceptor impurities. The extension of the depletion region depends on the built-in potential which is caused by the workfunction difference hence on the doping concentration between n-type and p-type semiconductors.

Cherenkov Radiation: When a charged particle travels faster than light does through a given medium, it emits Cherenkov radiation at an angle that depends on its velocity. The particle's velocity can be calculated from this angle. Velocity can then be combined with a measure of the particle's momentum to determine its mass, and therefore its identity.

Chromaticity: the focusing strength of quadrupoles also depends on the beam momentum. Hence a spread in momentum which is natural in storage rings because of

synchrotron oscillations causes a spread in focusing strength. The relationship between the normalized tune spread and the normalized momentum spread is called chromaticity. In order to correct this tune spread it is necessary to increase the quadrupole focusing strength for higher momentum electrons having higher focal lengths, and decrease it for lower momentum electrons. Typically this is controlled with the addition of sextupole magnets.

CMOS: complementary metal-oxide-semiconductor integrating both NMOS and PMOS circuits. Since only one of these transistor types is on at any given time, CMOS chips require significant less power making them very popular for integrated circuits.

Common Mode Noise: the common mode noise represents a row-wise correlated pulse height variation of the DEPFET Matrix originating from low-frequency baseline fluctuations (e.g. RF pickup in the matrix, readout chip or PCB as well as variations of the supply voltages) [45].

Configurable digital logic block (CLB): basic logic unit of FPGAs. The logic functions are implemented in lookup tables (LUTs) that are programmed with the outputs of a truth table. LUTs consist of one bit wide memory cell arrays being either in on or off state. The address lines for the memory cells are inputs of the logic block (or logic blocks) and the one bit output from the memory is the LUT output. The FPGA program defines the inputs to the CLBs selecting the content of one of the stored truth tables as output. Besides it selects the wire segments and switches for interconnection (routing) [105].

Crosstalk: in electronics, crosstalk (XT) is a disturbance caused by the electric or magnetic fields of one circuit or channel creating an undesired effect in an adjacent circuit or channel (electromagnetic interference).

DAC settings: digital-to-analog converters convert digital data to an analog signal. DCDB has 25 current-mode DACs (7-bits each) that generate bias currents (turned into voltages via resistors or diode connected transistors) for the analog channels. The DAC bits are stored in a JTAG accessible global configuration register.

Electron capture: a parent nucleus may capture one of its own electrons, thereby changing a nuclear proton to a neutron and simultaneously emitting an electron neutrino.

Emittance ($\boldsymbol{\varepsilon}$)**:** area in the phase space (ellipse) containing a certain fraction (90%) of beam particles. It remains constant throughout the whole beam transport system. In a collider, keeping the emittance small means, that the particles are confined to a small emission angle and have nearly the same momentum. Accordingly the likelihood of particle interactions will be greater resulting in higher luminosity. It has units of length and is measured in all three spatial dimensions. The dimension parallel to the motion of the particle is called the longitudinal emittance whereas the other two dimensions are referred to as the transverse emittances. Increasing the energy of the beam reduces the emittance.

Enclosed (design) transistors: standard CMOS processes use p-type substrate wafers. Strong irradiation may lead to bulk and surface damages and provoke short circuits in the design. The effect is strongly pronounced under thick oxide regions, where leakage currents appear close to the interface. Especially nMOS transistors with a classical rectangular form would suffer from shallow surface channels if they are separated only by lightly doped p-type silicon. Moreover, the charge accumulated at the ends of polysilicon gates may prevent them to be switched off completely. This is why, the use of enclosed NMOS transistor gates ("enclosed" means a circular design of the polysilicon gate) and p+-type guard-rings of increased doping were introduced especially for high energy physics experiments [106].

Exclusive & Inclusive Decay: exclusive means that a particular decay channel is considered, e.g. $B \to J/\psi K_S$. Inclusive means that all decays are considered, in which, e.g. a J/ψ is produced. An example is $B \to J/\psi X$, where X is any final state kinematically possible.

Flavor Physics: this term was created by Murray Gell-Mann together with his student Harald Fritzsch at an ice-cream store in Pasadena describing the species of elementary particles (leptons and quarks).

GPIB: General Purpose Interface Bus represents an international standard for a parallel bus providing a connection between a PC and measurement instruments or peripheral equipment like printers or plotters.

Hourglass Effect: reduction of luminosity due to the parabolic increase of the beta functions along the bunch during collision [107]. As a rule of thumb holds the lower the beta function the more distinctive the "hourglass bulbs".

Impact parameter: 3-dimensional point of the reconstructed track closest to the real starting point

Infiniband cable: Infiniband is a computer-networking communications standard. It currently provides the fastest transfer rates available for copper cables.

JTAG: the Joint Test Action Group originally developed the standard IEEE 1149.1 for testing finished printed circuit boards after manufacture. Nowadays JTAG protocols allow the programming, debugging and testing of integrated circuits, processors and FPGAs.

LCIO: labels a persistence framework, which is to some extent a middleware. It assists and automates the storage of data into relational databases. Members of the Linear Collider Collaboration were soon realizing that all groups involved in linear collider detector studies developed their own simulation software applications written in a variety of languages and different file formats. LCIO characterizes an effort to establish a common persistency scheme which would allow to share results and compare reconstruction algorithms [108].

LHCb: one of seven particle physics detector experiments at the LHC specialized in b-physics.

LVDS cable: twisted pair copper cables consuming low power and running at high speeds using a specific technical standard that specifies the electrical characteristics of a differential, serial communications protocol.

Minimal Flavor Violation (MFV): MFV hypotheses puts a lower bound on the flavor effects generated by NP given by the flavor-violating couplings present in the SM. This means that all flavor changing transitions are governed by the CKM model with respect to CP violation [109]. In particular there are no FCNC processes at the tree level. Hence a sort of “worst case”-scenario for the flavor-violating couplings exists while larger effects are always possible in many scenarios beyond MFV.

Multiplexer: a multiplexer is a device that has multiple inputs and forwards the selected input line one after another to the single output at different times or speed.

Occupancy: defined as the fraction of channels hit in each triggered event.

Punch-through: punch-through denotes a short-channel effect (occurring whenever the channel length is of the same order of magnitude as the depletion layer widths) in a MOSFET where the depletion layers around the drain and source regions merge into a single depletion region. The field underneath the gate can no longer be effectively controlled by the gate but becomes strongly dependent on the drain-source voltage. Hence punch-through causes a rapidly increasing parasitic current with increasing drain-source voltage. This effect is undesirable as it increases the output conductance and limits the maximum operating voltage of the device.

Quantum excitation (radiation damping): the energy radiated per turn is quantized. The discreteness of photon emission causes the charged particles to undergo a random walk or diffusion process hence increasing the oscillation amplitudes.

Photopeak: arises when the gamma ray deposits all of its energy in the detector. The most likely interaction is the photoelectric effect, where an incident gamma essentially gives all its energy to eject an inner shell electron from one of the silicon atoms. The ejected electron exhibits a significant kinetic energy which is lost via exciting and ionizing additional silicon atoms.

Printed circuit board (PCB): thin board made of layers of conductive and non-conductive laminate material. Conductive tracks, pads and other features etched or “printed” onto the PCB board, connecting different components such as transistors, resistors and integrated circuits.

Radiation length: mean distance over which a high-energy electrons loses all but $1/e$ of its energy by electromagnetic interaction (bremsstrahlung) or where a high-energy photon loses $7/9$ of the mean free path for pair production. It is measured in $g \cdot cm^{-2}$.

Resistive Plate Chamber: gaseous parallel-plate detectors that combine good spatial resolution with a time resolution comparable to that of scintillators.

Ring buffer: the ring or circular buffer refers to an area in memory which is used to store incoming data in a circular software queue. When the buffer is filled, new data is written starting at the beginning of the buffer and overwriting the old (FIFO - first in first out principle).

ROOT: ROOT is an object-oriented program and library for data processing developed by CERN. It provides among many other things automatic generation of histograms and graphs to view and analyze distributions and functions, regression analysis and other statistics tool, mathematical functions, access to databases and multivariate data analysis.

Sakharov conditions: in 1967 Russian physicist Andrei Sakharov, Nobel price awardee and developer of the Tsar Bomb the most powerful nuclear weapon ever detonated, formulated three conditions that a baryon-generating interaction must satisfy to produce matter and antimatter at different rates:

- Baryon number violation
- CP violation
- Interactions out of thermal equilibriums

Single event upset (SEU): ionizing radiation can cause a change of state in a flip-flop or a node in a micro-electronic device leading to an error output.

Slow control: Slow Control Systems are used for setup and monitoring of hardware that is not time-critical, and can be run at a low priority. Slow Control systems in a typical experiment are often used to setup and/or monitor components such as high voltage modules, temperature sensors, pressure gauges, leak detectors, RF generators, PID controllers etc. often from a large number of hardware vendors.

SMA: Sub Miniature version A fiber-optic cable coaxial connector that uses a threaded plug and socket. It has a screw type coupling mechanism and was the first connector for optical fibers to be standardized.

SMU: source measurement unit is a power sourcing instrument that provides voltage and current sourcing and measurement at high precision.

Synthesized Design: logic synthesis is one aspect of electronic design automation supported by a computer program, the so-called synthesis tool. It describes a process where a desired circuit behavior will be implemented into a specific design in terms of logic gates and sequential logic.

Touschek effect: the concentration of many electrons into small bunches increases the probability for large angle Coulomb collisions that lead to momentum transfers into the longitudinal phase space. If the RF-bucket acceptance is exceeded particles get lost.

Transfer Curve (Transfer Function): relates the input signal to the generated digital output code. The transfer function looks like a staircase in which each tread represents a particular digital output code and each riser represents a transition between adjacent codes. These transitions are not sharply defined but resemble a probability function in

which the ADC converts more and more frequently to the next higher output code as the input current slowly increases.

Via: a via is a small opening in an integrated circuit or PCB that allows a conductive connection between different insulated layers.

***.xml* file:** XML stands for eXtensible Mark-up Language representing a textual data format which is both human readable and machine readable. It is mainly used for a platform independent exchange of data between different computer systems especially via internet. XML is complementary to HTML in that sense that HTML is about displaying information, whereas XML is about describing information.

Wiggler Magnet: a wiggler magnet is made of a series of dipole magnets with alternating polarity so that the total bending angle is zero. The lateral deflection of charged particles create a change in acceleration which in turn produces synchrotron radiation. At SuperKEKB they are used to adjust emittance and damping time.

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Acronyms

ADC	Analog to Digital Converter
ADU	Analog Digital Unit ≡ LSB
ARICH	Aerogel Ring-Imaging Cherenkov Detector
ASIC	Application Specific Integrated Circuit
ATCA	Advanced Telecommunications Computing Architecture
BELLE	is not an acronym meaning beauty in French – studying b quarks
CCD	Charge Couple Device
CDC	Central Drift Chamber
CG	Cleargate
CKM	Cabbibo Kobayashi Maskawa matrix
CLB	Configurable digital Logic Block
CMC	Current Memory Cell
CN	Compute Node
CMP	Comparator
COG	Center of Gravity
DAC	Digital to Analog Converter
DAQ	Data Acquisition system
DC	Direct Current
DCD-B	Drain Current Digitizer for Belle II
DCDRO	Drain Current Digitizer Read Out
DEPFET	Depleted P-Channel Field Effect Transistor
DHC	Data Handling Controller
DHE	Data Handling Engine
DHP	Data Handling Processor
DNL	Differential Nonlinearity
DSSD	Double Sided Silicon Strip Detector
DUT	Device Under Test
ECL	Electromagnetic Calorimeter
FCNC	Flavor Changing Neutral Current

FPGA	Field Programmable Gate Array
GPIB	General Purpose Interface Bus
GUT	Grand Unified Theory
HER	High-Energy Ring
IEEE	Institute of Electrical and Electronics Engineers
ILC	International Linear Collider
INL	Integral Nonlinearity
IP	Interaction Point
JCP	Junk Charge Prevention
JTAG	IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture
KLM	K_L and Muon Detector
LCIO	Linear Collider I/O
LER	Low-Energy Ring
LHC	Large Hadron Collider
LHCb	Large Hadron Collider beauty
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signaling
MAPS	Monolithic Active Pixel Sensors
MC	Monte Carlo Simulation
MSB	Most Significant Bit
NP	New Physics
PCB	Printed Circuit Board
PID	Particle Identification Device
PMOS	p-channel MOSFET
PMNS	Pontecorvo Maki Nakagawa Sakata matrix
PP	Patch Panel
PT	Punch-Through
PXD	Pixel Detector
RAM	Random Access Memory
RC	Resistor Capacitor
RICH	Ring Imaging Cherenkov Detector

RF	Radio Frequency
RPC	Resistive Plate Chamber
RSD	Redundant Signed Digit
SC	Signal Charge Preservation
S/H	Sample-and-Hold Buffer
SFF	Super Flavor Factory
SIMS	Secondary Ionizing Mass Spectroscopy
SM	Standard Model
SMA	Sub Miniature version A
SMU	Source Measurement Unit
SNR	Signal to Noise Ratio
SVD	Silicon Vertex Detector
TIA	Transimpedance Amplifier
TOP	Time of Propagation
TRG	Triggering scheme
VXD	VerteX Detector (SVD+PXD)

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Declaration of originality

I hereby declare that I wrote this thesis independently, without the unauthorized help of third parties and without using any resources other than those specified.

Place, date

Signature

Erklärung

Hiermit erkläre ich, die vorliegende Arbeit selbständig verfasst zu haben und keine anderen als die in der Arbeit angegebenen Quellen und Hilfsmittel benutzt zu haben.

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