Readout Optimization for the Belle II Pixel Detector

– Characterization by ADC Transfer Curves

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Optimierung des Auslesechips für den Belle II Pixeldetektor

– Charakterisierung mittels AD-Transferkurven

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– Characterization by ADC Transfer Curves

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Abstract

The Super-KEKB accelerator at the KEK high energy research center in Tsukuba, Japan will provide a 40 times higher luminosity. To cope with this high luminosity the Belle detector is improved to Belle II, which includes the integration of a two layer DEPFET Pixel Detector (PXD) resulting in a higher vertex resolution. The task of the read-out electronics is to process the high data rate of the PXD. To fulfill these requirements, three different types of ASICs were designed. The foremost of them called Drain Current Digitizer (DCD) converts the drain currents of the DEPFET pixel sensors into digital code. Since the PXD will be equipped with 160 DCDs, automatic testing of the chips is needed. Analog to digital transfer curves are an appropriate tool for error recognition and optimization of the digitization process within the DCD. A detailed description of different defect types and their origins will be presented. Particular attention is paid to the missing code error, which arises from a transistor mismatch in the DCD, as it is still a prototype version. On this basis an optimization routine is developed, which compensates defects by an adjustment of settings. In an exemplary optimization, the number of channels containing missing codes is reduced to 6.25 %, at a combined defect number of 8.2 %. Finally, a fast routine speeding up the characterization time by a factor of $\sim$90 is proposed.

Kurzfassung

Der Ausbau des Teilchenbeschleunigers SuperKEKB am japanischen Institut für Hochenergiephysik KEK soll die Erforschung neuer Physik ermöglichen. Dazu wird seine Luminosität um den Faktor 40 erhöht. Gleichzeitig wird auch der neue Belle II Detektor mit einem hochauflösenden, zentralen DEPFET-Pixeldetektor ausgerüstet um eine genauere Track- und Vertexauflösung zu erreichen. Der Detektor wird eine enorme Datenmenge produzieren, die nur von eigens dafür entwickelten Auslesechips verarbeitet werden kann. Als Erster digitalisiert der sogenannte DCD die Signalströme der Pixelsensoren. Da es sich noch um einen Prototypen handelt, treten Umwandlungsfehler auf. Um den besten Arbeitspunkt aller verbauten 160 DCDs zu finden, wird ein automatisiertes Testverfahren erstellt. Die verschiedene Parameter, Spannungen und Ströme, die die Funktionsweise des DCDs steuern, werden mit Hilfe von Transferkurven überprüft. Dadurch können die unterschiedlichen Fehlertypen nach Klassen geordnet und auf ihre Ursprünge zurückgeführt werden. Anschließend wird anhand eines Beispiels gezeigt, wie die Anzahl der fehlerhaften Analog-Digital-Wandler innerhalb eines DCDs auf ein Minimum reduziert werden kann. Das Optimierungsverfahren bedient sich dabei verschiedener Teststromquellen, wodurch der Gesamtanteil an Umwandlungsfehlern auf 8.2 % gesenkt wird. Ein besonderes Augenmerk liegt dabei auf den sogenannten Missing Codes, die als Lücken in den Transferkurven auftreten und deren Anteil auf 6.25 % reduziert wird. Schlussendlich wird ein verbessertes Verfahren präsentiert, bei dem die benötigte Messdauer auf 1/90 verringert werden kann. Die gezeigten Methoden haben sich als zuverlässig erwiesen und stellen ein geeignetes Mittel zur Optimierung der AD-Wandler des DCDs dar.

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1 Introduction

The mathematical sciences particularly exhibit order, symmetry, and limitation. These are the greatest forms of beauty. – This statement from Aristotle from around 350 BC survived a very long time as a fundamental hypothesis of natural science. All the more astonishing was the detection of the violation of combined Charge Parity (CP) symmetry by Cronin and Fitch in a kaon decay system in 1964 [1]. It took several years until Kobayashi and Maskawa proposed a new scheme of weak interaction explaining the discovery in 1972. Their theory predicted a third family of quarks at a time where neither the bottom nor the top quark were experimentally discovered [2]. CP violation and the flavor mixing due to charge-current interaction were finally integrated into the Standard Model (SM) by the Cabibbo–Kobayashi–Maskawa (CKM) formalism. CKM predicted the highest significance of CP Violation for a B-meson system, which was confirmed with remarkable consistency by the two independent experiments *BaBar* at SLAC in California and *Belle* at KEK in Japan, awarding Kobayashi and Maskawa the Nobel price in 2008 [3]. Despite the great success of the Standard Model in describing matter and its behavior, still some fundamental questions remain unanswered.

In 1967 Sakharov identified CP violation as the source of the domination of matter over antimatter in the universe [4]. Nevertheless, the Kobayashi–Maskawa model, which is the only source of CP violation in the Standard Model, cannot explain the magnitude of the observed Baryon asymmetry [5]. Unknown sources must exist somewhere.

To reveal further secrets of nature, several enormous particle accelerators have been built over the past decades. Some, like the Large Hardron Collider at CERN operating at a center-of-mass energy of up to 14 TeV, are searching for new physics at high energies. Others are attacking the Standard Model with high statistics at the precision

frontier. A significant upgrade of the Belle experiment at the super flavor factory Super-KEKB in Tsukuba, Japan is expected to further enlighten unknown sources of CP violation beyond the Standard Model [6].

1.1 The Belle II Experiment at Super-KEKB

Like its predecessor, Super-KEKB at the Japanese Research Institute for high energy physics KEK is an asymmetrical electron-positron collider with a circumference of 3 km. Fig. 1.1 shows a photograph of the entire facility in the Tsukuba plane. Its general goal is the production of boosted B-mesons, which is why it is also known as a *B-factory*. The probability for the generation of B-meson pairs is highly increased at the Υ(4s) resonance with a center-of-mass energy of 10.58 GeV. Since the electrons and positrons are accelerated in two separated rings at different energies of 7 GeV and 4 GeV respectively, the particles get Lorentz-boosted.

In order to prove deviations from the Standard Model, a significant reduction of the measurement inaccuracies compared to former experiments must be achieved. This should be obtained by an increase of the accelerator luminosity as well as an improvement of the detector sensitivity.

The luminosity of a storage ring is defined as:

$$\mathcal{L} = \frac{f N_{e^-} N_{e^+}}{A} \tag{1.1}$$

where f is the bunch collision frequency, N_{e^-,e^+} the number of electrons and positrons in a bunch and A the bunches' cross section. By increasing N_{e^-,e^+} and particularly, by reducing the beam size with an innovative nano beam scheme, it is planned to reach a peak luminosity of $\mathcal{L} = 8 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$, which is 40 times higher than the world record so far held by KEKB. [8]

The luminosity improvement is estimated to not only increase the rate of events by a factor of 50, but as a drawback also the rate of second-order events representing the

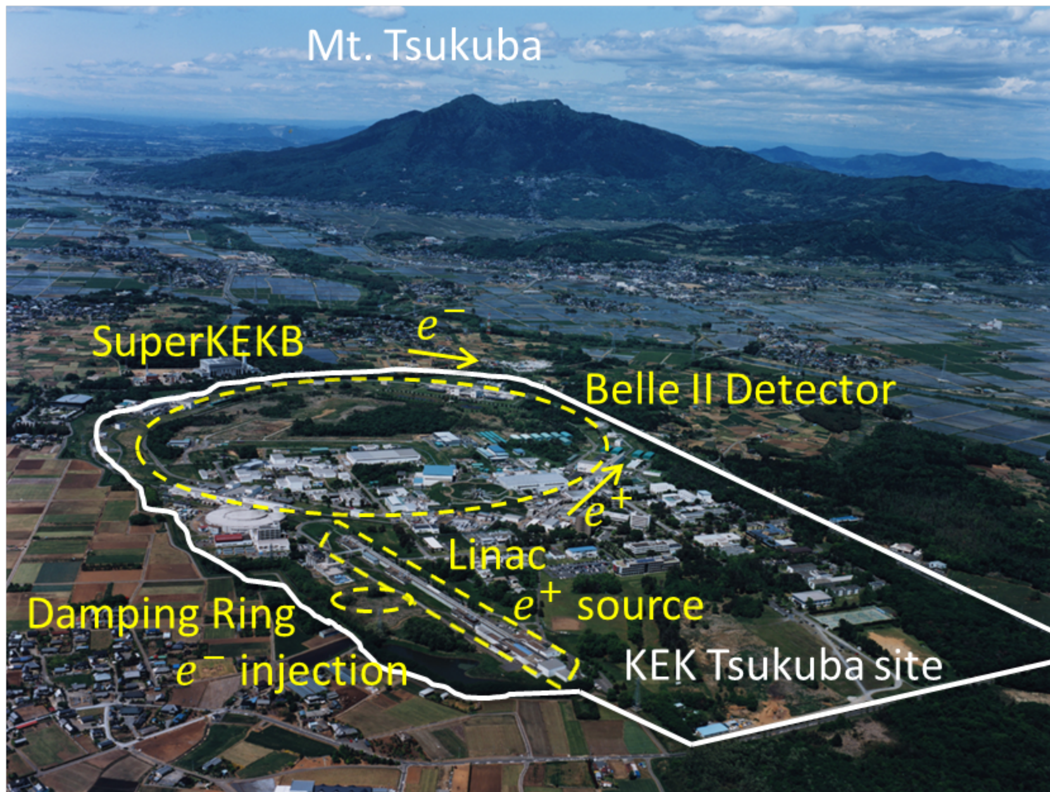


Figure 1.1: The Super-KEKB accelerator at KEK in Tsukuba, Japan. Electrons and positrons are injected into two separated storage rings from a low emittance electron/positron gun at a rate of 10 Hz. The Belle II Detector is placed at the interaction point, where bunches collide every 4 ns. [7]

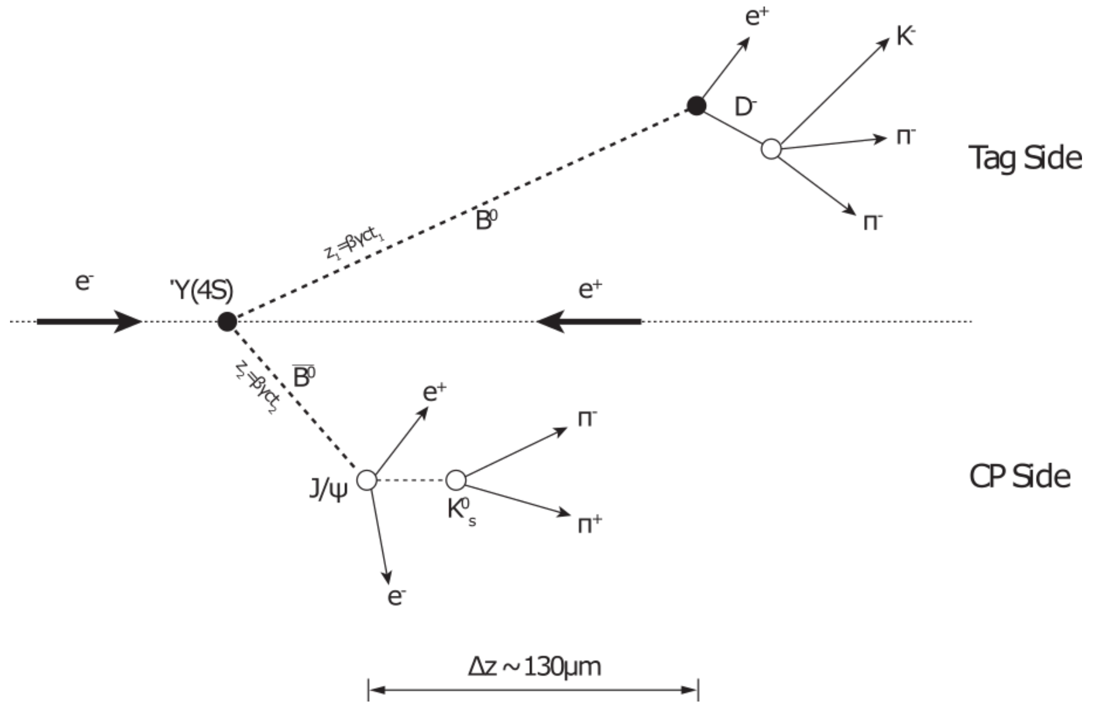


Figure 1.2: An exemplaric decay of two neutral B-mesons. The reconstruction of the decay vertexes is the primary goal of the detector. [9]

background, by a factor of 20 compared to KEKB [8]. This is only one of the challenges the detector has to deal with.

As already mentioned, B-meson decays are used for determining CP violations. A prominent example of such a decay is illustrated in Fig. 1.2. At the interaction point, the collision of an electron and a positron excites the Υ(4s) resonance. This state almost immediately decays into a pair of neutral B-Mesons. One meson decays into a J/Ψ on the CP side, while the other decays into a D and a charged lepton. The only chance to determine which path one of the B-mesons took is to measure the charge of the lepton on the Tag side [10]. The difference in the decay time $\Delta\tau$ indicates the CP violation parameters. Due to the Lorentz boost the time difference $\Delta\tau$ is transferred into a spatial resolution Δz. In this way the precise measurement of the decay vertexes is a key to determine CP violation.

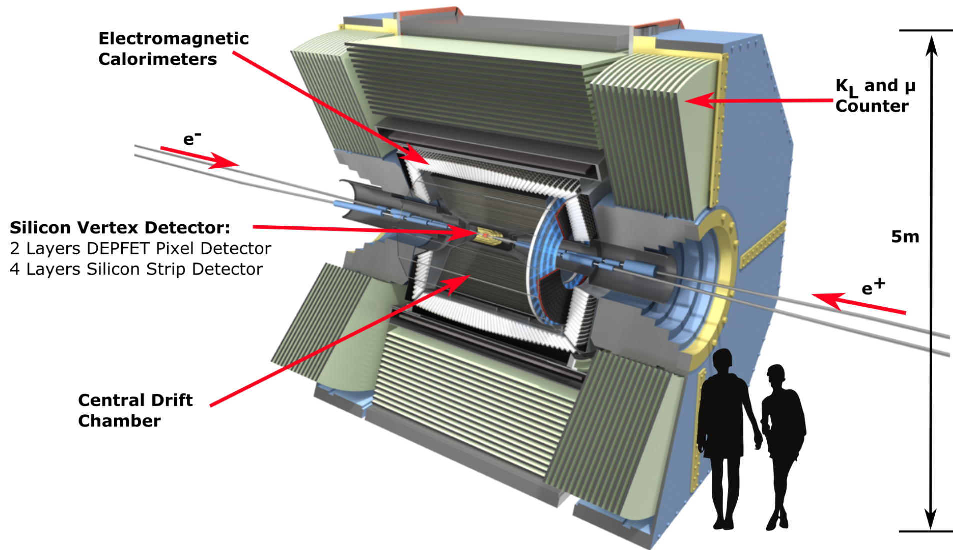


Figure 1.3: The Belle II Detector. [12]

1.2 The Belle II Detector

The Belle II Detector is located around the beam pipe at the interaction point. Its main task is the reconstruction of particle trajectories emerging from particle collisions. Like most modern detectors in high energy physics, it is arranged in the typical onion shape formed by different subdetector systems [11]. Fig. 1.3 illustrates the detector structure.

As closest to the beam pipe, the silicon Vertex Detector (VXD) is placed. Consisting of two layers of pixel sensors (PXD) followed by four layers of silicone strip sensors (SVD), it guarantees highest accuracy in particle vertex reconstruction. A combined spatial resolution of $\sim$20 µm ensures precise identification of trajectory origins, which is not only powerful in measuring CP violation observables but also in discriminating interesting events from the background [8].

The VXD is enclosed by a Central Drift Chamber (CDC), which precisely measures momenta and trajectories of charged particles. Furthermore, it is utilized as a trigger source.

The CDC is surrounded by a Particle Identification System (PID) with the main purposes of separating kaons from pions. Electromagnetic calorimeters consisting of

CsI scintillator crystals ensure precise energy measurements. The outermost part of the detector is formed by a system that identifies K_L and muons. Moreover, the Belle II detector features further important components, e.g. trigger generator, data acquisition and grid computing. A detailed description can be found in [13].

1.3 Overview of the Presented Work

The main focus of this thesis is the optimization and characterization of the front end readout electronics of the Pixel Detector within the detector environment.

Therefore, Chapter 2 provides a brief overview of the Pixel Detector and the DEPFET sensors it is composed of. Furthermore, its readout and steering chips, so-called ASICs, are introduced. Special attention is paid to the front-end readout chip, called Drain Current Digitizer (DCD) in Chapter 3. This chip converts the signal currents of the DEPFET sensors into digital code. A profound understanding of its conversion principle is needed, as the reduction of conversion errors is the overall aim of this work. A short overview of the used test setup and test modules is given in Chapter 4. In Chapter 5, the different defect types that can arise during the digitization process are defined. Chapter 6 then describes the development of a characterization strategy for the DCD using different test current sources. The full optimization routine is presented for an exemplary DCD. Thereby, different setting parameters are probed on their impact on conversion errors. Finally, a fast routine speeding up the characterization time by a factor of $\sim$90 is introduced.

2 The Pixel Detector of Belle II

The Belle II Pixel Detector uses DEPFET sensors for high accuracy measurements of the local resolution needed for the reconstruction of decay vertexes. The following section briefly summarizes their working principle.

2.1 The DEPFET Sensor

In 1987 Kemmer and Lutz from the Technical University and the Max-Planck Institute for Physics and Astrophysics in Munich proposed a new type of sensor, combining signal detection and amplification within a single transistor [14]. During the following years the technology was developed and further improved by the Semiconductor Laboratory of the Max-Planck Society. The sensor is based on a conventional p-channel MOSFET placed on a depleted silicon substrate, which is why it is called Depleted p-channel Field-Effect Transistor (DEPFET). Fig. 2.1 provides a schematic drawing of the sensor.

The n-doped silicon substrate, marked in white, represents the sensitive volume of the sensor. A full depletion of the substrate is reached by means of sideward depletion. A negative voltage is applied to both the source as well as the back contact. As a consequence, a layer of potential minimum for electrons is created at the transition of the two depletion volumes. This layer is shifted very close to the top side by applying a much more negative back voltage than source voltage. In addition, a n-doped region is implanted directly underneath the gate contact, which results in a general potential well for electrons called internal gate.

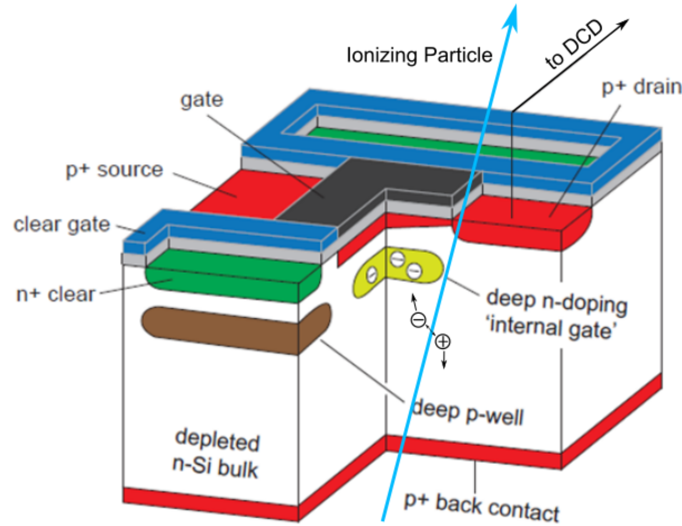


Figure 2.1: The DEPFET Sensor. Ionizing particles create electron- hole pairs when they traverse the silicon. Due to the applied voltages they drift apart. The electrons accumulate in the internal gate, where they modulate the source drain current. Clear gate and clear voltage are used to empty the internal gate after each readout cycle.

If the sensor is traversed by a particle of sufficient energy, electron hole pairs are created in the silicon. Due to the sidewards depletion the electrons drift from all over the substrate into the internal gate, whereas the holes are absorbed by the back contact. In a conventional field effect transistor the source-drain current I_{SD} is a function of the gate voltage V_G. In the case of the DEPFET, the electrons in the internal gate also create an electrical field effecting a broadening of the conducting channel.Consequently, I_{SD} is the sum of the current evoked by the "external" gate called pedestal current I_{ped} and the current of the internal gate I_{signal}.

$$I_{DS} = I_{ped} + I_{signal} \tag{2.1}$$

In this way, it becomes possible to detect traversing particles by means of the electrons in the internal gate. Furthermore, the signal is immediately amplified due to the transistor effect. The internal amplification of the DEPFET is defined as:

$$g_q = \left.\frac{\partial I_{SD}}{\partial Q_{sig}}\right|_{V_G, V_{DS}} \tag{2.2}$$

For the expected ranges, g_q can be assumed as constant. It amounts to $g_q \approx 400\,\mathrm{pA/e^-}$ at an external gate voltage of -1 V.

Since the measurement is performed in an indirect way, which is not affecting the number of electrons inside the internal gate, it becomes necessary to remove the charge after each readout cycle. To this end, the DEPFET sensor features additionally positive clear contacts, which are able to empty the internal gate by applying a high positive voltage. In order to prevent a loss of signal electrons during the accumulation phase, the clear contact is shielded by an additional clear gate and a p-doped region inside the substrate. A detailed description of the DEPFET principle can be found in [15] and [16].

The readout of the DEPFET takes place in three iterative steps:

- Sensitive phase: Ionizing particles traversing the DEPFET create electric charge, which accumulates in the internal gate. At the same time, the external gate voltage is set to a positive value leading to a complete pinch-off of the conducting channel.
- Readout phase: The MOSFET is switched on by applying a negative voltage to the external gate. Thus, a conducting channel between drain and source is established. Subsequently, the drain current composed of I_{ped} and I_{signal} is sampled. For this readout scheme the pedestal current must be known in order to calculate the signal current according to Eq. 2.1. In a dedicated measurement the pedestal current is therefore pre-stored before the readout cycle begins.
- Clear phase: Accumulated electrons are removed from the internal gate by means of a voltage pulse on the clear contact.

In this way the whole readout cycle is controlled via the gate and clear voltage. A sampling of the drain current is only required during the readout phase.

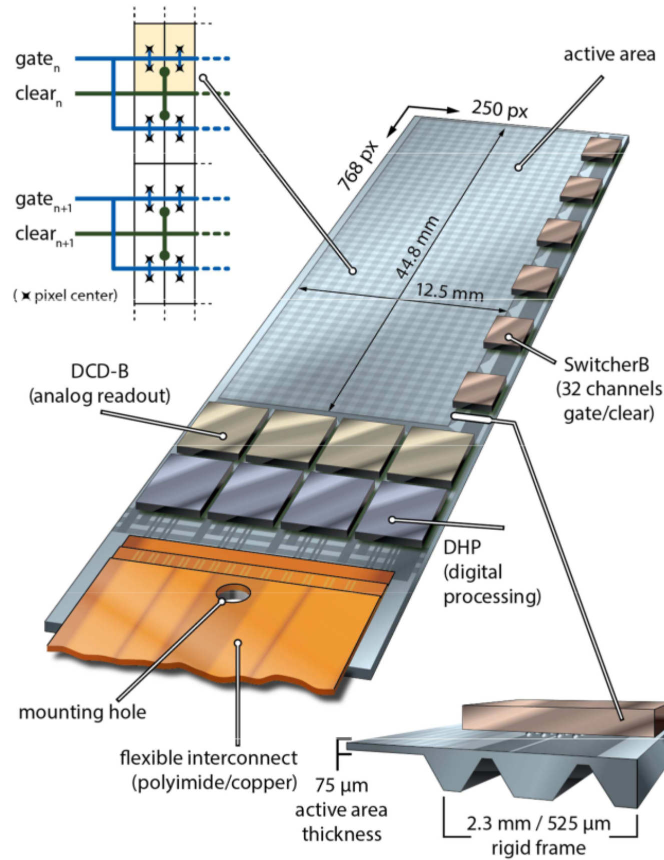


Figure 2.2: A half-ladder for the pixel detector. The active area consists of 768 · 250 DEPFET pixel. Only the active area is thinned to 75 µm, leaving a self supporting structure at the sides. The readout is performed in rolling shutter mode controlled via 14 ASICs. [17]

2.2 A Half-Ladder Module

For the purpose of building a pixel detector, the DEPFET sensors are arranged in arrays of 768 · 250 pixels, called half-ladders (Fig. 2.2). The excellent signal-to-noise ratio of the DEPFETs allows a thinning of the sensitive area to 75 µm. Since only the sensitive area is thinned, a self supporting frame remains at the sides. The steering and readout of all 192 000 pixel is an enormous challenge. To deal with this, three different types of Application-Specific Integrated Circuits (ASICs) have been designed.

2.3 ASICs

The Switcher, which is placed on the long side of the ladder generates the clear and gate voltages for the DEPFETs. The matrix is operated in fourfold rolling shutter mode. This means that the clear and gate contacts of four pixel rows are connected together. Such a block is called an electrical row and contains 1000 pixel. The 192 electrical rows are readout subsequently, i.e. only one electrical row is active at a time. Simultaneously, the other 191 rows are in the sensitive phase. This allows for a parallel connection of the drain contacts of each column. Due to the fourfold readout, the number of drain lines has to be quadrupled too. In this way the $768 \cdot 250$ physical pixel can be understood as $192 \cdot 1000$ electrical pixel.

A readout of the full matrix is called a frame and was determined to 20 µs. This leaves ~104 ns per electrical row for the readout and clear phase. Another ASIC called Drain Current Digitizer (DCD) was designed for sampling and digitizing the drain current during this time period. Since each DCD contains 256 Analog-to-Digital Converter (ADC), four of them are sufficient to process all 1000 drain lines in parallel. A resolution of eight bit is sufficient to meet the signal-to-noise requirements of the detector. Furthermore, this chip guarantees a constant potential of the drain line capacitance. The presented thesis is focused on the optimization of the digitization process within the DCD. Thus, a detailed explanation of this chip will be given in the next chapter.

The output data of the DCD is transmitted to the Data Handling Processor (DHP). Its main task is data reduction, since the huge amount of data produced by the DCD would overload the connections to the outside. Therefore, the DHP applies so-called zero-suppression to the data. In a first step the common mode calculated for each electrical row is subtracted. Subsequently the pre-stored pedestal values are subtracted for each pixel individually. Only signals being still above a threshold are further transmitted via high speed links.

2.4 The Pixel Detector

The Pixel Detector consists of 20 full ladders which approximately form a barrel shape through polyangular arrangement in two layers (see Fig. 2.3). A full ladder is formed by gluing together two half-ladders at their short side. The two layers have a distance to the interaction point of 14 mm and 22 mm and are composed of eight and twelve ladders respectively. The outer ladders have a size of roughly 15.4 mm $\times$ 170 mm and are thus longer than the inner ones with 15.4 mm $\times$ 136 mm.

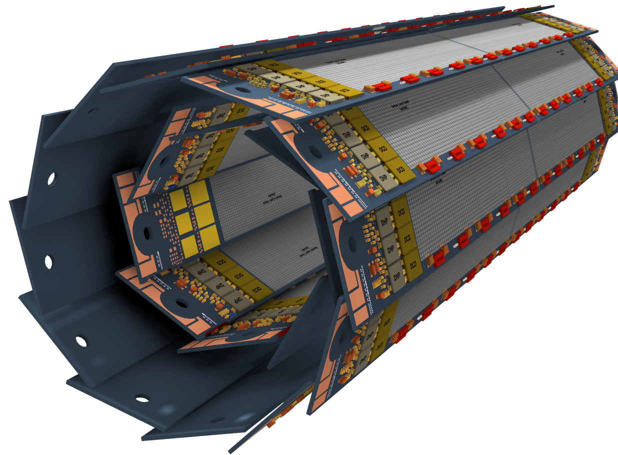


Figure 2.3: The Pixel Detector is formed by two layers of sensors in polyangular arrangement. [18]

The main goal of the PXD is to enhance the reconstruction of decay vertexes. Thereby, the reconstruction resolution is depending on a geometrical and a multiple scattering term. With this arrangement, the combined impact parameter resolution σ of the SVD is expected to be $\approx 20\,\mu\text{m}$.

The PXD features a lot more interesting aspects, whose description would go beyond the scope of this work. The interested reader is referred to [16].

3 The Drain Current Digitizer

With the development of the DEPFET sensors by J.Kemmer and G.Lutz in 1987 [14], the need for suitable readout electronics converting the signal currents of the pixel matrix into digital data arose. In order to cope with the complexity of this non-standard application, the design of a dedicated chip, so called Application-Specific Integrated Circuits (ASICs), became necessary. In the case of the DEPFET sensors used for the Belle II Pixel Detector (PXD) this chip had to fulfill the following requirements.

- The main task of the chip is the digitization of the signal currents. A digitization precision of eight bit is sufficient to meet the signal-to-noise requirements.
- Since the PXD is the innermost part of the Belle II detector it is located very close to the interaction point. Therefore the readout chips, which are mounted on the edge of the sensors, will be exposed to high radiation doses. Thus the chip must tolerate an expected radiation dose of at least 70 kGy [19].
- In consideration of the expected high signal background the PXD subdetector requires a sampling rate of 50 MHz [16] in order to enhance the physical performance of the Belle II detector. Since the matrix is arranged in 192 electrical rows, a sampling period of $\sim$100 ns per ADC must be maintained.
- Furthermore, parallel readout of the 1000 electrical columns of a half ladder is needed. Therefore several chips with a channel number in the order of hundreds are required.
- The drain lines of the matrix have a capacitance of $\sim$50 pF [19]. The current receiver of the chip must provide a stable potential to ensure fast and precise readout.

- All the mentioned requirements have to be realized on limited space on the edge of the silicon ladder.

It was in the early 2000s when the group of Prof. Peter Fischer from the Institute of Computer Engineering at the University of Heidelberg started working on a readout chip for the DEPFET Sensors. Leading designer Ivan Perić's main idea was to use current memory cells to memorize and process the signal currents. In this way the whole conversion process is done in current mode. Thus, simplicity is retained, allowing an easier implementation of radiation-tolerant layout techniques, as well as making the use of any pre-converting or pre-amplification unnecessary [19]. The first version of their chip was inspired by the readout chip *CURO* designed by M. Trimpel at the University of Bonn [20]. By improving the current memory cell with a differential transconductor and by implementing this cells as cyclic ADCs, they created the working principle of the cells now used in the PXD. Since then, various enhanced prototypes have been developed [21], but they all share the same conversion procedure. This iterative algorithm is called *redundant signed digit* conversion and consists of three basic steps.

1) The input current is sampled and memorized.

2) The sampled current is compared to two thresholds, one low (LO) and one high (HI). If the signal is lower than the low threshold, the reference current, which is 1/4 of the input range, is added and the output number is set to -1. If the signal is higher than the high threshold, the reference current is subtracted and the output number is set to +1. If the signal is in between the thresholds no current is added or subtracted and the output number is set to 0.

3) The current resulting from 2) is multiplied by two and feed as input to 1).

Subsequently the algorithm starts again from 1). Fig 3.1 shows the transfer characteristic of the algorithm, with the input current on the x-axis and the resulting output current of step 2) on the y-axis. The multiplication of step 3) is not shown.

The redundant signed digit conversion is an iterative algorithm, where every cycle produces one output number a_i. The results can be translated to a binary number D:

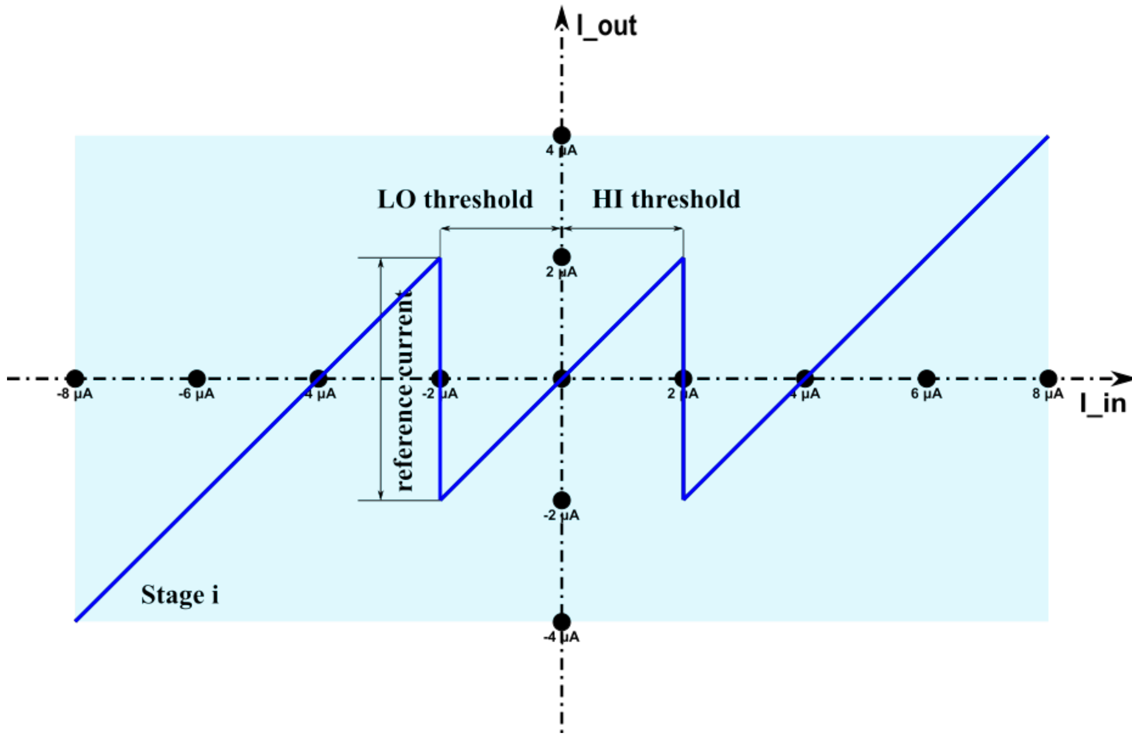


Figure 3.1: The transfer characteristic of the redundant signed digit conversion

$$D = \sum_{i=0}^{n} 2^{n-i} a_i \tag{3.1}$$

In this way, n cycles of the conversion algorithm result in the $n+1$ bit long signed digit D. The right choice of the threshold and reference current is essential for the algorithm to work properly. But before addressing this problem, it is advisable to understand how the conversion procedure is implemented in hardware.

3.1 The Pipeline ADC

The latest Version of the readout chip is called DCDBv4, which is short for Drain Current Digitizer for Belle version 4. Two different subversions with 256 channels have been manufactured: one with a pipeline ADC and another one with two cyclic ADCs

per channel. In this work only the pipeline version was used and therefore will be referred to as DCD in the following.

3.1.1 Conversion Principle

Fig. 3.2 shows the pipeline ADC of one DCD channel. It consists of eight double cell blocks, each containing two comparators and two Current Memory Cells (CMCs). Inside the double cell blocks both comparators are connected to the first CMC. The left side of the figure shows a detailed view of three of the blocks, where the operation cycle is emphasized for stages 2 to 4. The analog-to-digital conversion is performed in four states, which is very similar to the algorithm described above [19].

State 1:
The current from the previous cells (in the case of the first double cell block this is the input signal) is copied to memory cell *CM0*. The comparators connected to this cell are in reset state, no output is produced.
(Active steering signals: *Wr0*=1, *Rd23*=1, *Res*=1)

State 2:
The current from the previous cells is copied to memory cell *CM1*. Simultaneously, the two comparators connected to *CM0*, namely *Cmp.Lo* and *Cmp.Hi*, are switched to active state and compare the current of *CM0* to their thresholds.
(*Wr1*=1, *Rd23*=1)

State 3:
Comparators are now latched and reproduce the conversion results from state 2. Those are used for two purposes. Firstly to control the switchable current sources of *CM0* and *CM1* and secondly to produce the digital output. If the current is higher than the high threshold, the reference current is subtracted and the low and high output bits are set to l=0, h=1. If the current is lower than the low threshold, the reference current is added and the output bits are set to $l = 1, h = 0$. If the current is in between the thresholds no current is added or subtracted, h and l are 0. If the reference current and the thresholds are properly

chosen, the sum of the residual currents flowing out of *CM0* and *CM1* fits into *CM2*. Since all memory cells are of the same type this is equal to multiplication by two.
(*Wr2*=1, *Rd01*=1, *Lt*=1)

State 4:
The currents of *CM0* and *CM1* are copied to *CM3*. At the same time the comparators of *CM2* are in compare state.
(*Wr3*=1, *Rd01*=1)

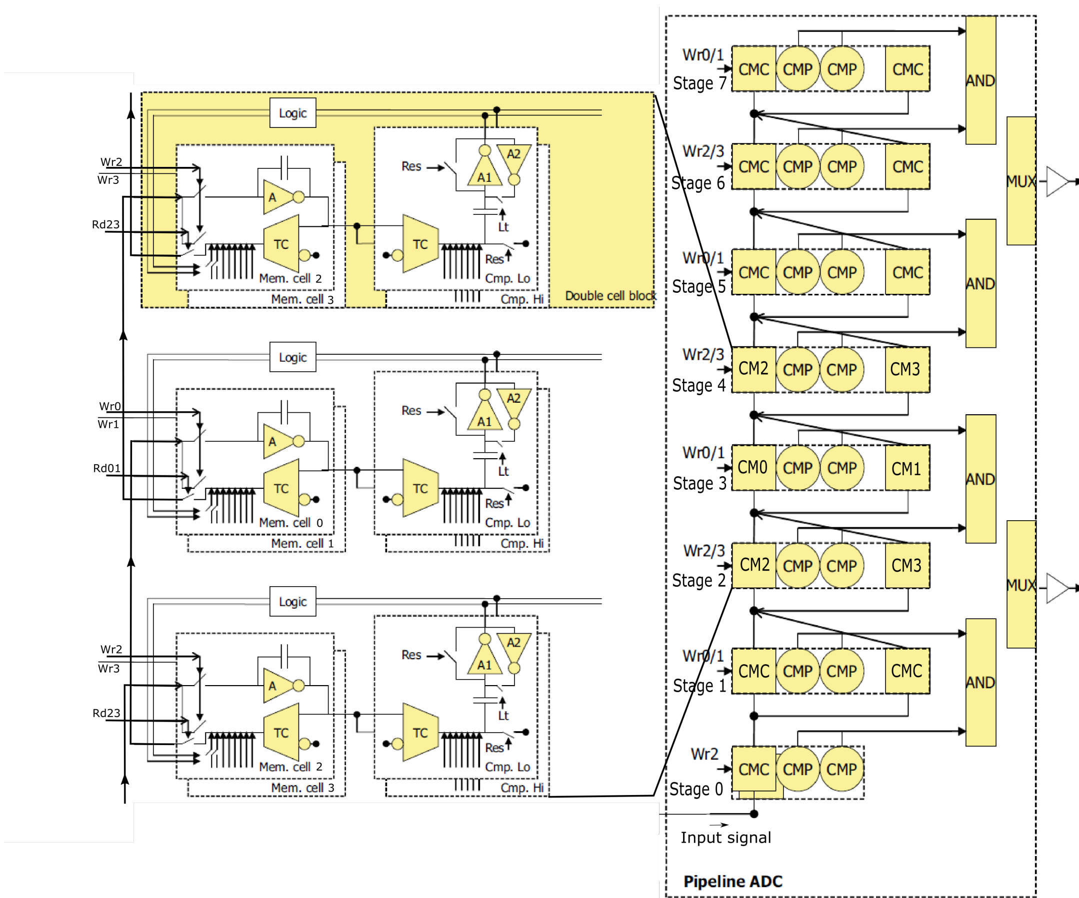


Figure 3.2: The pipeline ADC is composed of eight double cell blocks, which contain two current memory cells (*CMP*) and two comparators (*CMP*) each. The output bits of two blocks are merged via *AND* operators and multiplexed to two output lines. On the left side, three of the double cell blocks are shown in detail, including the control signals *Wr* and *Rd*. Adapted from [22].

From now on states 1 - 4 repeat. With a global clock of 76.23 MHz[1] every state takes 26.6 ns. Therefore the total conversion time in eight blocks amounts to 420 ns. Nevertheless, a new signal can be sampled every 105 ns while the previous signals are still in the pipeline. There is a small difference in the first double cell block. Here, both CMCs sample the input signal simultaneously during state 3, in contrast nothing happens during state 4. Thereby the input range of the ADC is doubled (the current splits up to two cells) and the sampling time is reduced to 26.6 ns.

While the comparators of *CM0* in stage 3 produce valid output, the ones of *CM2* in the next block are in reset state. Therefore it is possible to merge the data of each two blocks via and-operation (*AND*). The number of lines transmitting the conversion results to the digital part can be reduced to four ($2 \cdot 2$ bit) by additional time multiplexing (*MUX*).

In this way the conversion produces eight digital output pairs $(l_0, h_0), ..., (l_7, h_7)$ per current sample. According to the conversion algorithm as it was described above, h and l correspond to $a_i = h_i - l_i$. Using Eq. 3.1 the signal current can be expressed as discrete signed number $I_{Signal} = D\frac{R}{128}$, with R being the reference current.

3.1.2 Digital Control Sequence

Each DCD channel has a decoder which generates the digital sequence controlling the ADC. It receives the two bit synchronization signal (*Sy0* and *Sy1*) as well as the clock signal (*bitCk*) from the chip's digital part. Thereof it generates *Rd01*, *Rd23* and *Wr0* to *Wr3*, which steer the respective states of the CMCs. The latch and reset signals of the comparators, *Lt* and *Res*, are coupled to the *Wr* signals. Fig. 3.3 shows the temporal sequence of the control signals.

1 This is the nominal clock frequency of the detector, leading to a sampling rate of 50 MHz. The clock frequency can be reduced to 62.5 MHz in order to guarantee stable testing conditions.

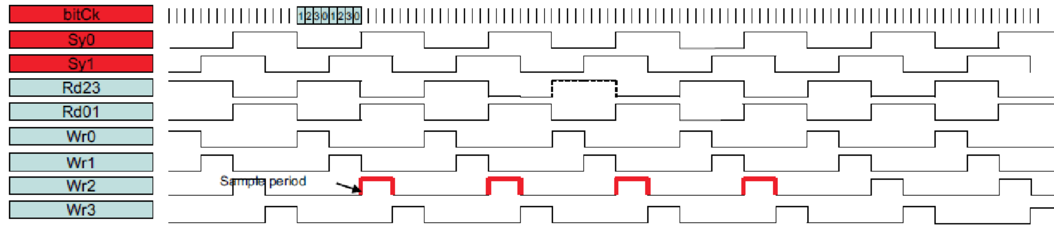


Figure 3.3: The digital control sequence of the pipeline ADC. The sampling periods are marked in red. [22]

3.1.3 The Current Memory Cell

The current memory cell is the fundamental building block of the pipeline ADC. It is an analog-memory element, memorizing and reproducing currents.

The Basic Cell

The working principle of a current memory cell is best explained by the simplest version, shown in Fig. 3.4a. It is implemented with a single Metal-Oxide Semiconductor (MOS) transistor, three switches and a hold capacitor.

In the read state switches $S1$ and $S2$ are closed. The input current I_{IN} flows through $S2$ into transistor $M1$. At the same time one part of I_{IN} flows through $S1$, where it loads the hold capacitance C_h and generates a negative feedback at the transistors gate. Once the system is in balance and the total current is dumped to ground via $M1$, the storing process is finished. By opening $S1$, the gate voltage of $M1$ is locked in C_h. In the write state only switch $S3$ is closed and the copied current I_{OUT} flows out of the cell. Notice that the output current has the same sign as the input current. Moreover the current memory cell has the ability to sample and reproduce currents of both signs, which is necessary when writing from one cell to the next.

This basic cell has two drawbacks. Firstly, signal dependent charge injection compromises the stored voltage of C_h. The charge injection arises during the opening of switch S_1. It depends on the signal level, if the source and drain potential of S_1 varies with the signal level, as it is the case within the basic cell. In order to achieve high

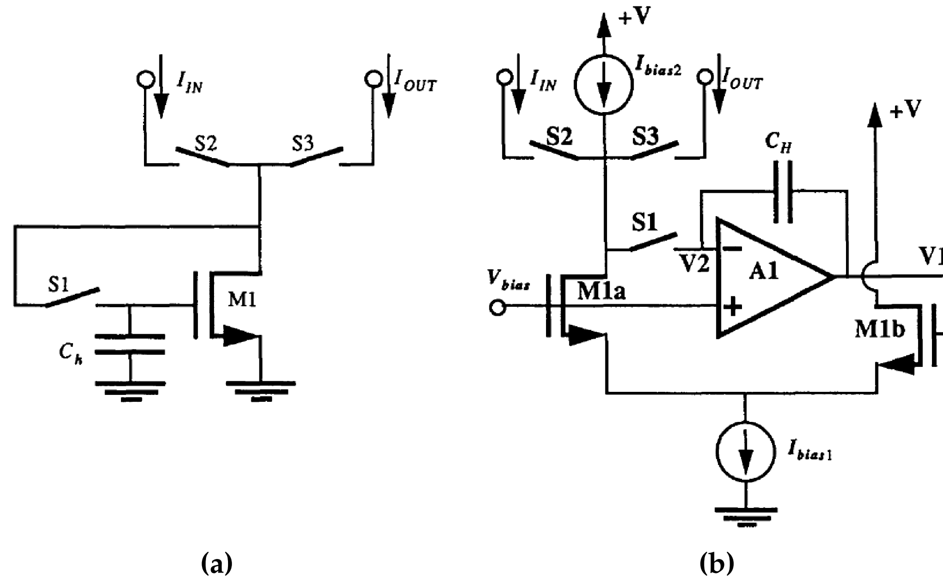


Figure 3.4: a) The basic current memory cell. b) The zero voltage switching cell, including amplifier *A1* and the differential pair *M1a* & *M1b*. [23]

precision of the stored voltage, which represents the current sample, both ends of $S1$ must be kept at a constant level. Secondly, the memory cells output resistance differs between read and write state. This finite output resistance of $M1$ limits the sampler's accuracy when current is transferred from one cell (in read state) to the next (in write state).

The Zero Voltage Switching Cell

The zero voltage switching cell (Fig. 3.4b) introduced by D. Nairn overcomes those drawbacks [23]. Here, amplifier *A1* and hold capacitance C_h are used to sample the signal. The more complex differential pair transconductor, implemented in the zero voltage switching cell, works in a similar way as *M1* in the basic cell. Again C_h is used as memory element. Out of the stored voltage the amplifier *A1* generates a voltage *V1* proportional to the input current I_{IN}. *V1* acts on one input of the transconductor (gate of *M1b*). The other input is fixed (V_{bias}) as well as the sinks ($+V$) and the source (I_{bias1}) of the transconductor. In this way $V1$ controls which fraction of current from I_{bias1} flows in the right arm of the transconductor. The rest of I_{bias} has to flow through *M1b* in the left arm, where it causes negative feedback

to I_{IN}. Once the system is in balance, *S1* is used to freeze the voltage across C_h. Afterwards the sampled current is reproduced and transferred to the output via *S3*.

Notice, that the source I_{bias2} adds a small amount of current in order to ensure minimum speed in the case of small input currents. Therefore it holds $I_{OUT} = I_{IN} + I_{bias2}$. Contrary to the basic cell, the potential at *M1a's* ends remains constant in this circuit, due to the negative feedback of *A1*. Thereby the circuit shown in Fig. 3.4b provides a solution to both problems of the basic cell. For one thing, the charge injection of *S1* becomes mostly signal independent. For another thing, the effective input impedance is reduced significantly by holding the sampler's input node at constant level. An additional advantage of the constant potential is the admission of the use of P-channel Metal-Oxide Semiconductor (PMOS) transistors only, which tolerate higher radiation doses than N-channel Metal-Oxide Semiconductor (NMOS) transistors.

The Pipeline ADC Current Memory Cell

Fig. 3.5 provides a detailed view of the latest version CMC used in the pipeline ADC. The cell basically resembles the zero voltage switching cell, nevertheless some components were adjusted for the use in the pipeline ADC. The main difference is the current adding or subtracting part (*Add* and *Sub*) necessary for the analog-to-digital conversion algorithm. The switchable current sources *Add* and *Sub* are controlled by the comparators *CMP1* and *CMP2*, described in the next section. Beside this, some smaller changes of implementation details are made. Amplifier *A1* is realized as gain stage with the current source *IAmpPBias*. Its ground is defined by the *AmpLow* voltage. The transconductor *TC* takes the output voltage of the amplifier as input on its right side, in the same way as in the zero voltage switching cell. Its source *IFBPBias* and its sinks *IPSource2* have a nominal current of 24 µA. The *TC's* left input is controlled by fixed but configurable voltage *RefFB*. The cascodes *IFBNCasc* are attached to both outputs in order to increase stability of the system. While the right output is kept at the fixed potential *RefIn*, the left side is connected to the cells input and output via node 4. *IPsourceCasc* adds constantly a current of

8 µA, while *Sub* and *Add* add or subtract a current of 4 µA according to the comparison result. The input range of the cell is ±8 µA while the output range is limited to ±4 µA.

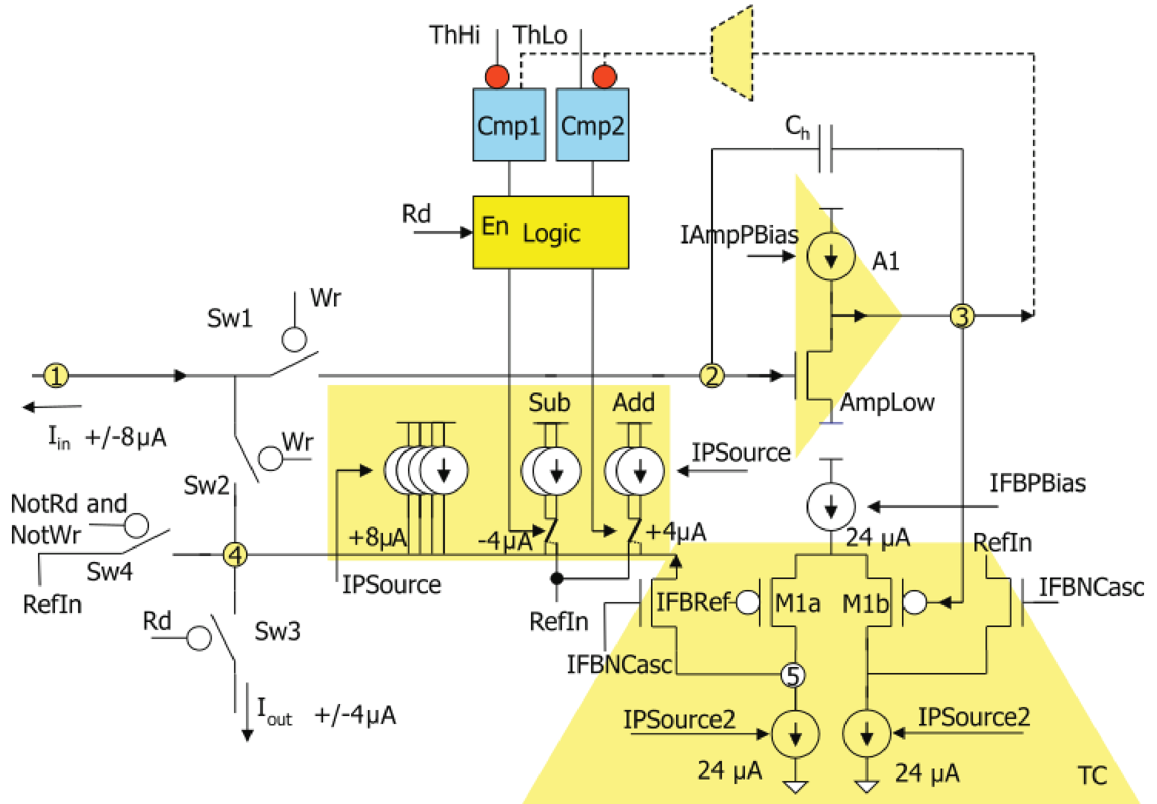


Figure 3.5: A detailed schematic of the current memory cell. The dotted line marks the connection to the comparators Cmp1 & Cmp2 with the logic block controlling the switchable current sources *Add* & *Sub*. [22]

The ongoing processes in the CMC might be best understandable by giving an example. Let's assume an input current I_{in} of 5 µA. The system is in the write state (state 1 according to section 3.1.1). *Sw1* and *Sw2* are closed, the logic block is disabled and currents of *Sub* and *Add* are dumped to *RefIn*. On its way over node 4, I_{in} picks up additional 8 µA by *IPSource* so that a current of 13 µA arrives at node 5. According to Kirchhoff's circuit laws the sum of currents flowing into the node must be zero. Therefore the current of *M1a* has to take a value of 11 µA. This leads to 13 µA for *M1b*. As long as *M1b* does not fulfill this condition, a part of I_{in} loads the hold capacitance C_h where it generates negative feedback on the gate of *M1b*.

Once the system is in balance and the total of I_{in} flows in node 5, the sampling process is finished. When the system changes to state 2, switches 2 and 3 are opened and the voltage is saved in C_h. In this state the output voltage of the amplifier is feed to the comparators via node 3. In the meanwhile the output current is dumped to *Refin* via *Sw4*.

In the read state (state 3 and state 4) the *Rd* signal activates $Sw3$ as well as the logic block. In the example of 5 µA the comparison would result in $h = 1$, $l = 0$, leading to a subtraction of 4 µA. Therefore a current I_{out} of 1 µA would flow out of the cell. Remember that the outputs of both CMCs of a double cell block are summed and feed as input to the next cell block. Thus, the input of the next cell would be 2 µA.

Control parameters

As can be seen in the block diagram, the CMC possesses over a variety of configurable current sources that generate the bias voltages for the CMC. Those are the tuning parameters for optimizing the ADC, which is the aim of this thesis. All this current sources are realized as 7-bit Digital-to-Analog Converter Units (DACs), meaning in a range of 0 to 127, with a full scale of 10 µA. The DACs are globally set for all channels of one DCD and can be accessed via Joint Test Action Group Standard (JTAG). Table 3.1 provides a complete list of the CMC's configurable current sources with a short description.

In order to provide high sampling precision, exact timing of the switching processes is required (e.g. open *S1* prior to *S2*). Therefore some of the write and read signals have to be delayed by a few ns. This is done by delay elements controlled by *IPDel* and *INDel*.

The reference ground signals *AmpLow* and *RefIn* are generated by the power supply and feed to the DCD as analog signals.

IAmpPBias	The load current source of the amplifier.
IFBNCasc	The control voltage of the stability cascodes at the outputs of the transconductor.
IFBPBias	Controls the source of the differential pair transconductor
IFBRef	The control voltage of the fixed input of the transconductor acting as reference to the second input.
IPSource	The control voltage of the switchable current sources *Add* & *Sub*.
IPSource2	Controls the current sinks of the differential pair transconductor.
IpSourceCasc	A cascode voltage, improving the stability of the *IPSource* current source (not shown in the figure).
IPDel	Sets delays for *Wr* and *Rd* signals (not shown in the figure).
INDel	See IPDel.

Table 3.1: Configurable current sources of the CMC, where *I* denotes the current source nature of the DACs, *FB* stands for feedback transconductor and *P* & *N* refer to the transistor (PMOS or NMOS) used for converting the current into the control voltage.

3.1.4 The Comparator

Fig. 3.6 shows a schematic drawing of the comparator. The value of the threshold *Th*, which is 6 µA for a low comparator and 10 µA for a high comparator, is the only difference between them. As already mentioned, both comparators are connected to node 3 of the first CMC of each double cell block. In this way they see the output voltage of the CMC's amplifier. Since the comparators and CMCs use equal transconductors this voltage is converted into equal current. Consequently the output current of the comparator's transconductor is in the range 0 µA to 16 µA. This current is compared to the threshold. In the case of a low comparator, current below 6 µA results in a negative comparison result I_{result}. The same holds for the high comparator and currents below 10 µA. In this way the thresholds decide about the sign of I_{result}.

The output stage of the comparator is a latch-like structure, implemented with two cross coupled amplifiers *A1* and *A2*. Both use the same supply and ground voltages as the CMC's amplifier. According to the conversion algorithm, the stage has three exclusive states indicated by the control signals *Res* and *Lt*. In reset state I_{result} is dumped to *RefIn* via *Sw1* and the amplifiers don't produce valid output. In compare state (neither *Res* nor *Lt* signal) I_{result} dynamically pushes *A1* to either of two directions depending on its sign. This is followed by the latch state, in which the amplifiers are latched. Thereby amplifier *A2*, which is driven by the positive feedback of *A1*, produces the output signal. This is used by the small logic block (compare Fig. 3.5) to control the switchable current sources. The digital output of the ADC is also produced in this step.

Most of the controlling DACs are the same as for the CMC. In addition, the comparators use the DACs *INMOS* and *IPMOS* to limit the current I_{result} flowing into the amplifiers, where only the sign is relevant. Remember that the CMC has an input range from −8 µA to 8 µA, where a current of 8 µA is added constantly. This current has to be taken into account (and therefore subtracted), which is why the thresholds in terms of the input range are −2 µA and 2 µA (compare to Fig. 3.1).

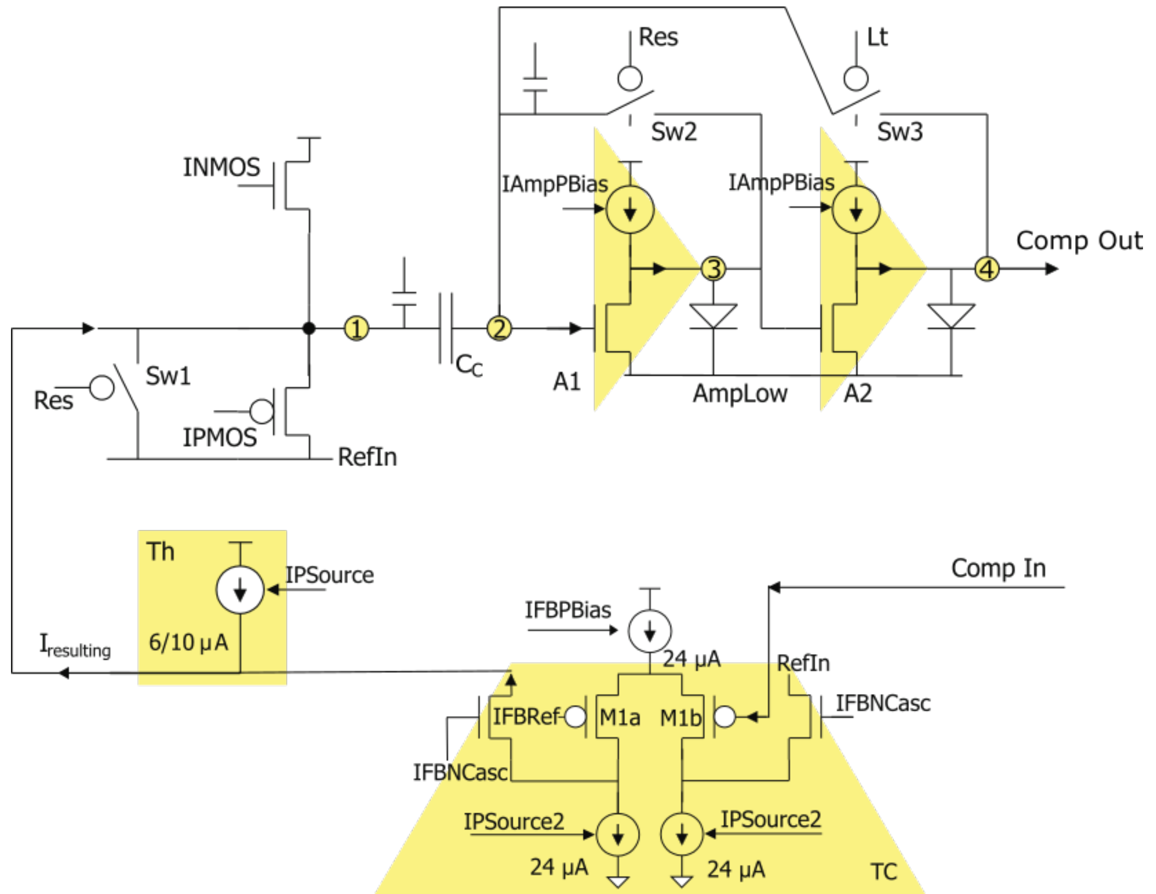


Figure 3.6: A detailed schematic of the comparator of the ADC. Low and high comparators are distinguished by their threshold of 6 µA and 10 µA respectively. [22]

3.2 The Analog Channel of the DCD

Besides the pipeline ADC the analog channel of the DCD consists of further components shown in Fig. 3.7. One DCD features 256 of such analog channels.

3.2.1 Offset Compensation

A wide spread of the drain currents can be expected among DEPFET pixels. In order to reduce this and fit the drain currents into the dynamic range of the ADC, the DCD provides a two bit wide offset compensation for each channel. The *DAC* holds three current sources proportional to the global configurable source *IPDAC*. It is foreseen

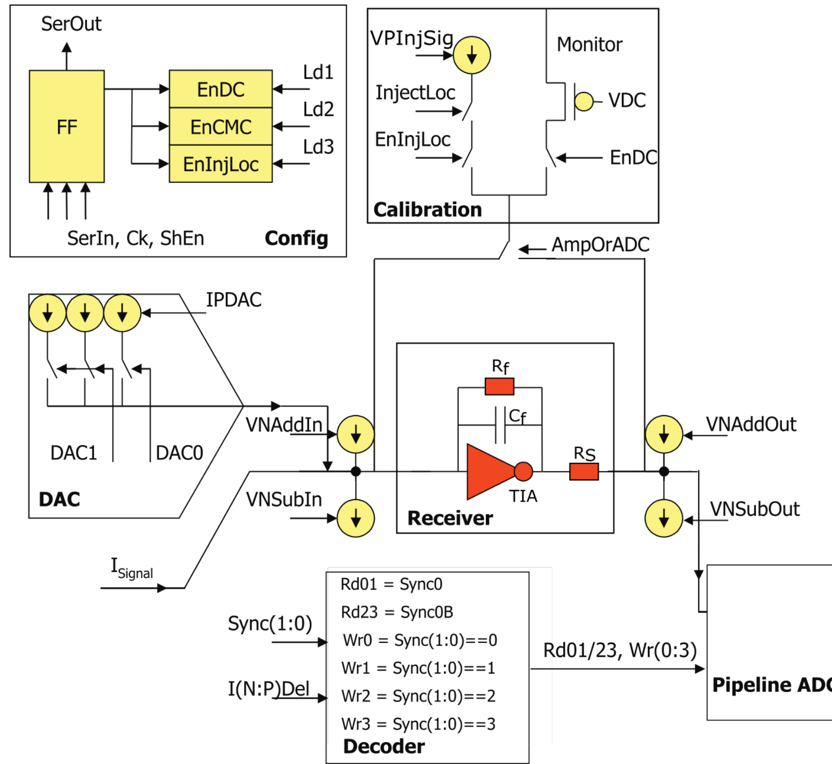


Figure 3.7: Overview of the analog channel of the DCD. [22]

to measure the pedestal currents for each pixel at a time when no events occur and to store the value in the DHP memory. During data taking, those values are used to control whether three, two, one or none of the sources are added to the signal current of an individual channel. Therefore the pre-stored two bit values *DAC*(0:1) for each individual channel are loaded into the DCD by every new sampling period.

The left side of Fig.3.8 shows how the pedestal spread is reduced in this way. Once signals are on the same level, the global source *VNSubIn* subtracts a current in order to shift the entire distribution into the dynamic input range of the ADCs. In case of currents that are too low *VNAddIn* is employed. While those sources cover a wide range in coarse steps, *VNAddOut* and *VNSubOut* are used for fine tuning directly before the input of the ADC.

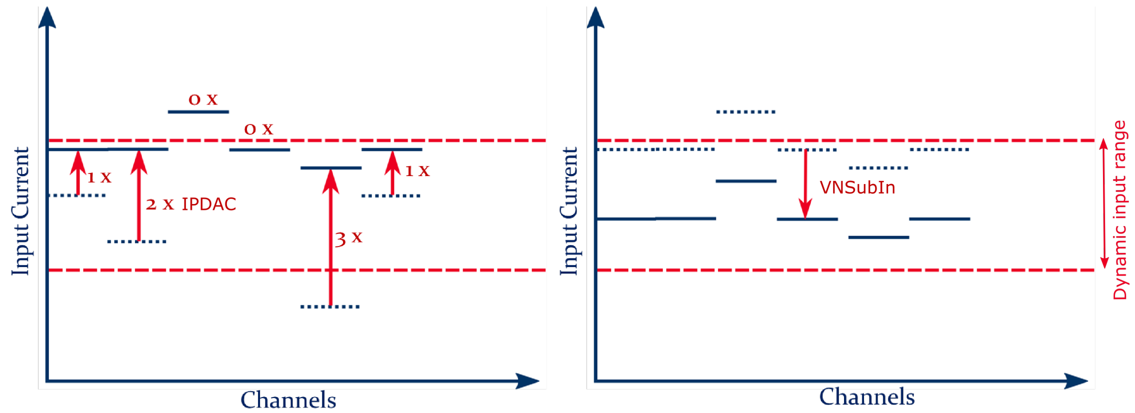


Figure 3.8: The offset compensation principle. At first the spread among channels is reduced by an individual addition of *IPDAC*, then channels are collectively pulled into the dynamic range by *VNSubIn*.

3.2.2 The Current Receiver

As mentioned before, it is essential for the current memory cells to keep their input nodes at a constant potential independent of the current flowing into it. Usually this is ensured by the output of the previous cell. For the first two cells the resistive current receiver takes on this task.

Its main building block is a transimpedance amplifier (TIA) that converts the input current into voltage. The TIA's feedback splits up into two paths, one holding resistance R_f and the other holding capacitance C_f. At its output, the resistance R_s converts the voltage back into current. C_f, R_f and R_s are programmable parts and offer the possibility to adjust the receiver. R_f can be switched to either 30 kΩ or 60 kΩ, thereby limiting the input dynamic range of the receiver to 16 µA or 8 µA accordingly. In contrast, R_s defines the output dynamic range, which is 16 µA for $R_s = 15\,\mathrm{k\Omega}$ and 32 µA for $R_s = 30\,\mathrm{k\Omega}$. Changes of the in and output ranges naturally affect the gain. Therefore the gain is defined as

$$G = \frac{R_s}{R_f} \tag{3.2}$$

The low pass filter C_f can be set to different values in the range from 60 fF to 460 fF, which can help to reduce noise. This also affects the settling time τ of the TIA, for which

holds

$$\tau =\propto C_f R_f \tag{3.3}$$

Moreover the receiver offers an analog common mode compensation. Since this is not used in this work, the interested reader is referred to [22]. A detailed description of all configuration parameters of the current receiver can also be found there.

3.2.3 Calibration and Configuration

The calibration circuits are used for testing purposes (see Fig. 3.7). They can either be connected to the input of the ADC or to the input of the receiver through the global switch *AmpOrADC*. Besides the global configuration bits, the DCD's shift register (*Config*) offers three individual bits for every channel.

EnDC controls the channels connection to the monitor pin. This pin can be used for voltage and current measurements as well as for the injection of test signals. There are two possibilities to inject a test current via the monitor pin. Firstly, by connecting an external current source, secondly by using the internal slow current injection of the DCD.

The internal fast current injection, controlled by DAC *VPInjSig* is activated by global bit *InjectLoc* and local bit *EnInjLoc*. Unfortunately this current source could not be used for this thesis, due to synchronization problems between DCD and DHP.

The third local bit *EnCMC* activates the common mode compensation. The pixel shift register can be accessed via JTAG with *Ld*, *Ck* and *ShEn* signals. For the description of the decoder see section 3.1.2.

3.3 The Digital Block of the DCD

Besides the 256 analog channels, the DCD possesses a large digital block. Among its tasks, the high speed data transmission and the conversion of raw digitization values into standard binary representation are especially interesting in the context of this work.

3.3.1 Data Conversion

For every current sample the pipeline ADC produces eight pairs of output bits (h, l). This representation contains redundant information, which is why a conversion into standard binary code reduces the amount of data. Due to the fact that transmission lines between DCD and DHP are limited in space, it is preferred to do the conversion inside the DCD. Therefore it has a large digital part, which contains a finite state machine as proposed in [24]. Since it uses the Least Significant Bit (LSB) first, the order of the ADC code has to be flipped in a bi-directional shift register before entering the state machine.

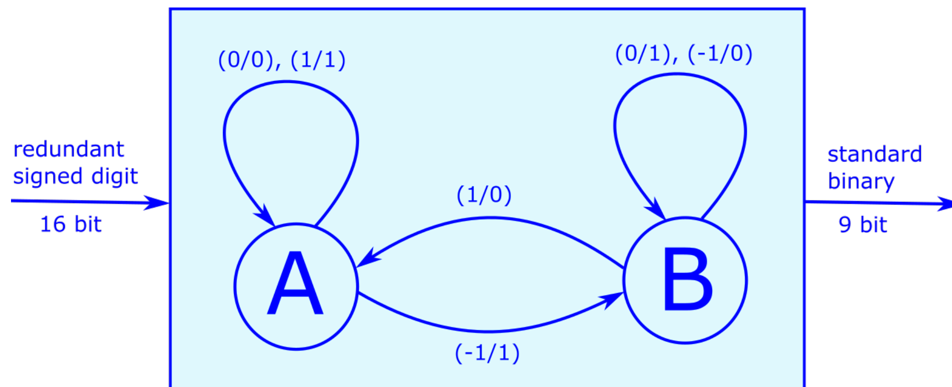


Figure 3.9: The state machine converts redundant signed digit code from the ADC into standard binary representation.

The state machine works in synchronization with the ADC. With every clock cycle it takes a new bit pair $(h,\ l)$ as input, which can be represented as signed number $a = h - l \in \{-1, 0, 1\}$. This is translated to a single output bit $\in \{0, 1\}$. The state machine's logic is depicted in Fig. 3.9. Depending on the state of the system (A or

B), every in, in this case the stages outputs a_i, produces a corresponding out (in/out). Starting from state A, this results in eight bits of output code. An additional ninth bit, which can be interpreted as the sign of the code, is determined by the final state of the system. If the machine ends in state A this will be 0, which stands for positive, if it ends in state B this will be 1, which stands for negative. In this way a nine bit standard binary code, in the range -255 to 255, is obtained out of the 16 bit code, coming from the ADC.

3.3.2 Data Transmission

Since the DCD is specified for a conversion resolution of eight bit, a transmission of nine bit would be a waste of transmission bandwidth. Therefore it was decided to neglect the LSB, in order to reduce the output code to a range of -127 to 127. The same result could be obtained by reducing the number of the ADC's conversion stages from eight to seven. Nevertheless, for an easier digital design and serialization strategy, a reduction of bits was preferred over a reduction of cell blocks [25].

The digitization values are transmitted to the DHP on an eight bit wide output bus, where every bit of the word is transmitted on a different transmission line. Since the number of transmission lines is limited, a further signal serialization is needed. In order to do so, the 256 channels of the DCD are divided in eight groups of 32 channels each. Every group is multiplexed to one eight bit bus, on which the data of its channels is transmitted in series. Consequently, the transmission frequency has to reach 32 times the sampling rate, which adds up to 305 MHz.

4 The Test Setup

In order to test the interaction of the individual PXD components, a test setup was assembled. It features a half ladder prototype plus power supply and first level data processing. The test module is linked to a patch panel via a flexible Kapton cable. From here the data is transferred to the DHE via a 15 m Infiniband cable. The analog and digital supply voltages are generated by the power supply (PS). The setup is controlled by a *Scientific Linux 6* computer using *EPICS* and *CS-Studio*. The measurement and analysis scripts were written in *Phython 2.7*.

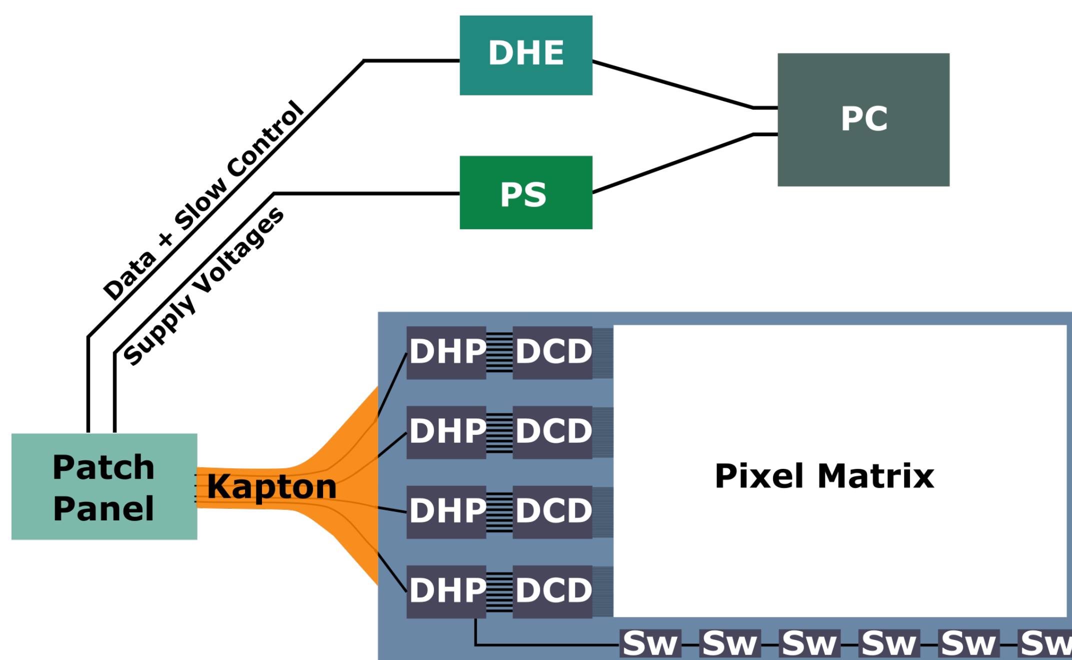


Figure 4.1: The test setup. The half ladder module is connected via a Kapton cable to a patch panel. From there power and data lines split up to the power supply and the DHE respectively. A computer controls the whole setup.

4.1 Test Modules

The test module is the heart of the test setup. This is a prototype of one of the half ladders, of which the final detector will contain 40. The two different test modules, which have been used in this work, are described in the following.

4.1.1 The EMCM Board

The Electronic Multi Chip Module (EMCM) was build for tests of the electric components. Therefore it is equipped with the full set of ASICs, mounted on a dummy of the true half ladder size. This module does not contain a pixel matrix.

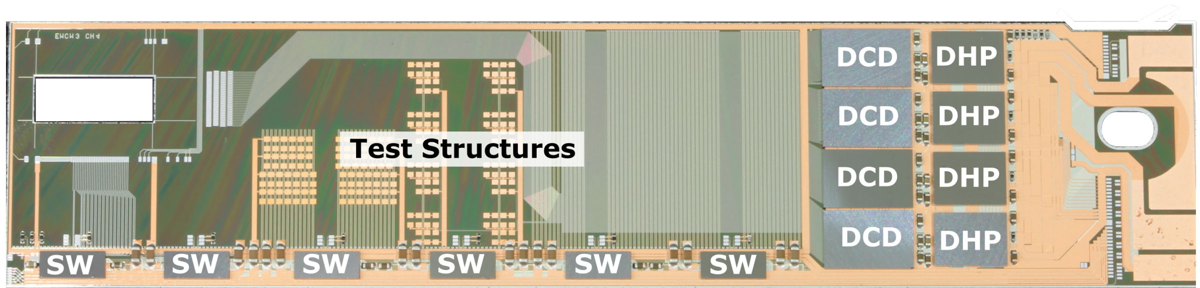


Figure 4.2: A photograph of the EMCM. [26]

4.1.2 The PXD9 Pilot Module

The PXD9 Pilot module is an improved prototype with a fully functional pixel matrix of full size. All kinds of functionality and irradiation tests are possible on this module. This includes a characterization of the DCD within the detector environment for the first time.

Figure 4.3: Photograph of the PXD9 Pilot module with the full pixel matrix. [26]

4.2 Data Transmission

A stable data connection between the module and the computer has to be guaranteed before performing measurements. Therefore the DHP offers a set of adjustment options.

4.2.1 DCD – DHP Communication

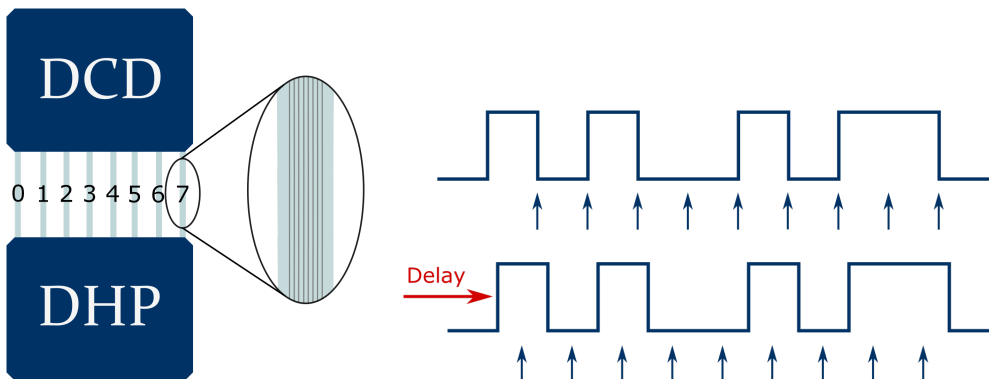


Figure 4.4: Each of the 64 transfer lines can be delayed individually in order to shift the sampling point (blue arrows) to the middle of the signal plateau.

The data of the DCD is transferred to the DHP via eight 8-bit buses on a nominal frequency of 305 MHz (see chapter 3.3.2). In order to ensure highest signal integrity, each of the 64 physical transfer lines can be delayed individually by up to 15 programmable delay elements. Furthermore the global sampling point can be adjusted via a shift of the controlling clock. Fig. 4.4 illustrates how the delay can be used to shift the sampling point towards the middle of the signal plateau. The DCD

offers the possibility to generate a test pattern, which can be used for delay adjustment.

4.2.2 DHP – DHE Communication

On the output side the DHP transmits the data via a flexible Kapton cable, the patch panel and a 15m Infiniband cable to the DHE. Over this distance a pre-amplification of the signal is needed to compensate the attenuation of the high frequency component lost during data transmission (see Fig. 4.5). The DHP's output driver features a programmable preemphasis via three parameters *Bias*, *Bias D* and *Bias Delay*. A detailed description of the DHP's output driver can be found in [27].

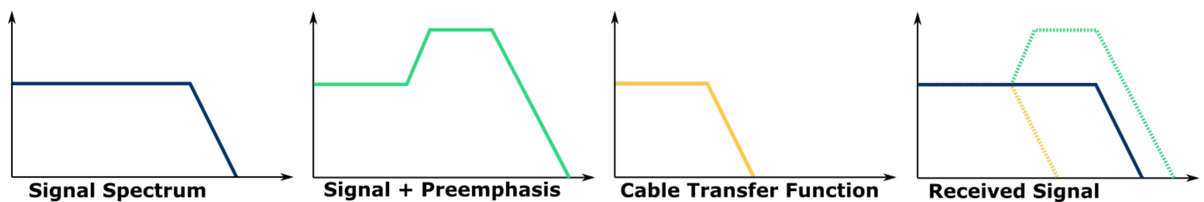


Figure 4.5: A signal preemphasis is needed to compensate the loss caused by the cable transfer function.

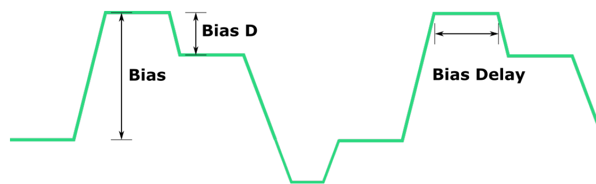


Figure 4.6: Amplitude, overshot and length of the preemphasis are controlled by *Bias*, *Bias D* and *Bias Delay*.

4.3 Test Sources

In chapter 3.2.3, the calibration circuit of the ADC channel was described. This includes a monitor pin, allowing the connection of a current source for testing purposes (see Fig. 3.7). Due to the chip design, the monitor pin can just be activated for one channel at once, which is controlled by the local variable *EnDC* in the pixel shift register. At

the same time other channels have to be masked out in the DHP's memory to allow zero suppressed readout. This is achieved by setting the pedestal threshold of the corresponding pixels to 255.

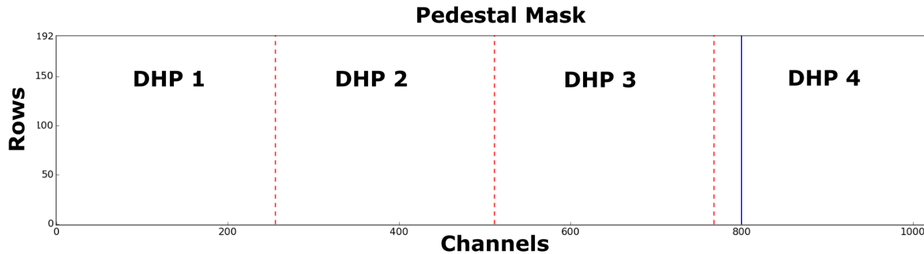


Figure 4.7: The pedestal mask for the internal and external current source plotted in electrical mapping. In this case channel 32 of the fourth DCD is activated. With this mask channel 32 is sampled 192 times within one frame.

4.3.1 The Internal Current Source of the DCD

The DCD features a current source exclusive for testing purposes, which can be connected to the monitor pin. Actually it is composed of three DACs, with 127 settings each. For Fig. 4.8 the current source was recorded with a Source Meter/Measuring Unit (SMU). It ranges over 32 µA in 381 steps. The gain was fitted as $(83.236\,511 \pm 0.026\,381)$ nA/DAC.

Besides a relatively restricted range, the internal current source has one large disadvantage. The fact that it is controlled via JTAG, necessitates a waiting time after setting a DAC value. It was found out that this has to be 100 ms to work correctly. Hence, the waiting time for the full range sums up to 38.1 s, making a characterization of the DCD with the internal current source very time consuming.

4.3.2 The External Current Source of the DHE

An external source can be connected to the monitor pin also. For this purpose the DHE includes its own current source. With a scope of 248 µA in 65000 steps, it exceeds both the precision as well as the range of the internal current source by

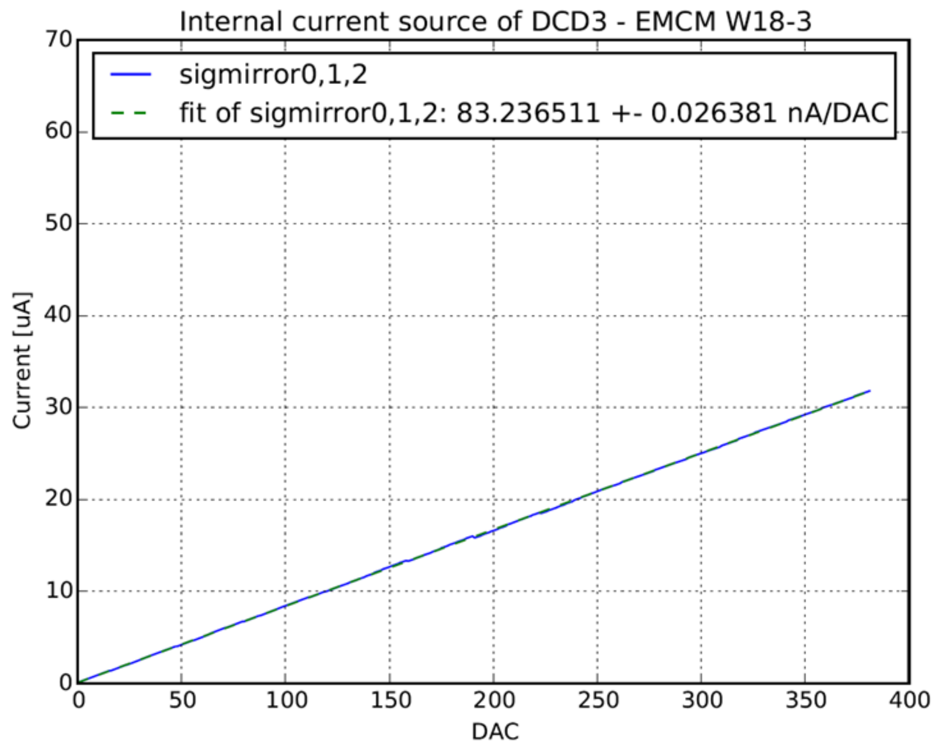


Figure 4.8: The internal current source of the DCD.

far. Moreover this source can be switched much faster, resulting in a measurement time of $\sim$2 s per transfer curve. A fit of the gain yielded a resolution of $(3.815\,478 \pm 0.000\,002)$ nA/DAC.

Also the external current source has a big drawback. While the current source itself shows very low noise, a lot of it is picked up on the path to the module. On the one hand the 15 m Infiniband cable is not designed for current supply. On the other hand the connection on the patch panel is bridged by unshielded wiring. Consequently the transfer curves recorded with the external current source show a much higher noise than those of the internal source.

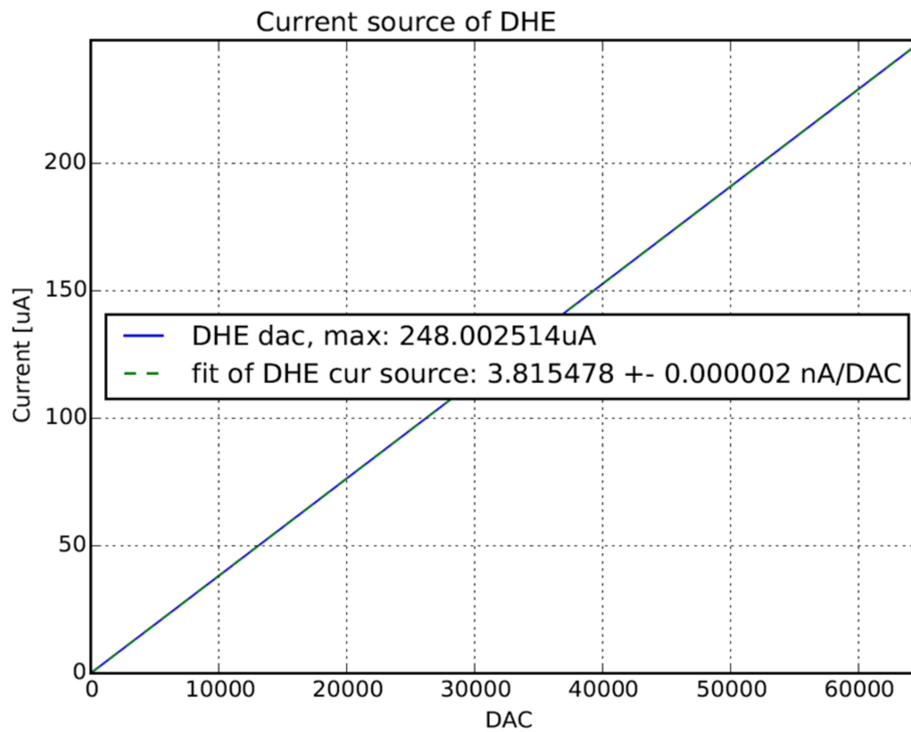


Figure 4.9: The external current source of the DCD.

4.3.3 DEPFETs as Current Source

So far there has been the choice between a very slow switching and a noisy current source. This is why the idea arose to utilize the DEPFETs as current source.

As every Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) the DEPFETs show an increase of the drain current with increasing negative gate voltage. Fig. 4.10 shows the transistor characteristics of the DEPFET. Since the linear range of the ADC is limited, the plot is put together of multiple measurements where different values of the current source *VNSubIn* were added. The area from $-1500\,\mathrm{mV}$ to $-200\,\mathrm{mV}$ is more than sufficient to cover the whole input range of the ADCs. In this way the DEPFETs form an additional test current source, which is controlled via the gate voltage.

When using this source, it has to be ensured that only one matrix row is activated in the DHP memory to guarantee zero suppressed readout. While on the one hand a large

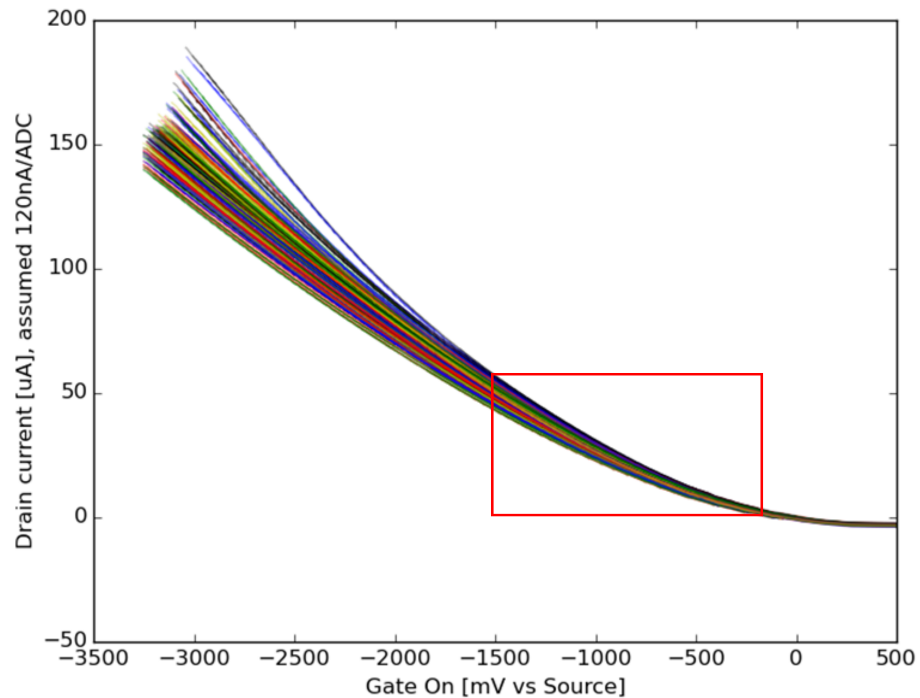


Figure 4.10: Transistor characteristic of the DEPFETs. The red square marks the area used as a test current source. [28]

deviation from linearity must be accepted, the DEPFET current source overcomes the problem of the monitor pin restriction on the other hand. This source can be applied to all channels of all four DCDs of one half ladder at once, resulting in a huge speedup of the ADC characterization.

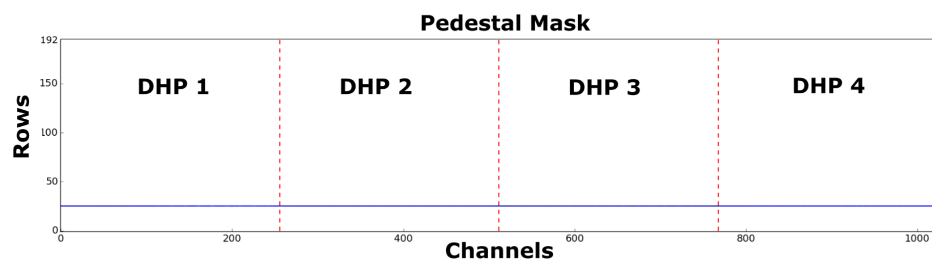


Figure 4.11: The pedestal mask for the DEPFET source plotted in electrical mapping. In this case only row 25 is activated for all four DHPs. This results in one reading of each channel per frame.

5 Transfer Curves for ADC Characterization

The test setup described in the previous chapter can be used for a characterization of the DCD. The development of sophisticated test methods is motivated by several reasons:

Debugging of prototype:
This non-standard chip was specifically designed for the readout of the Belle II pixel detector. DCDBv4 pipeline is the latest release in a long development process, but not yet the serial version for the final detector. Hence it still may contain minor design errors, e.g. mismatching components, leading to defective operation. Thoroughly testing of the chips functionality becomes exceedingly necessary. Especially the testing of the chip within the detector system can provide important feedback, needed for the development of the final DCD version.

Optimization of serial production:
The PXD will contain 160 DCDs, including 40 960 ADC channels with 1.3×10^6 CMCs and comparators. With regards to this huge number, statistical deviations among cells that lead to defects must be expected. In order to prevent malfunction and to minimize the percentage of non functional channels, individual adjustment of every single DCD's setting is an essential task.

Readjustment due to radiation errors:
Moreover, the chip will be operated in a radiant environment. Though there is no experience in long term radiation exposure for the DCD, it is save to assume that the chips' performance will change over time. This effect must

be compensated in order to prevent the PXD from deterioration. This can be achieved by readjustment of the DCD's settings, but therefore characterization of the chips during the running experiment becomes indispensable.

In consideration of the mentioned challenges, the development of suitable testing and optimization routines for the DCD is a very important task for guaranteeing the full functionality of the PXD. Appropriate tools to characterize the ADCs are so called analog-to-digital transfer curves. Instead of the DEPFET's signal currents a test current source is applied to the ADCs here. While the current is gradually increased, the digital output codes of the ADCs are recorded. In this way the Digital-to-Analog Converter Units (DACs) of the test source, which correspond to a known current, can be related to the digital output code of the DCD.

Conversion errors can be detected from the comparison of the test current to the digital output. Therefore, the test source should provide a high degree of linearity, as well as a fast switching ability and low noise. Additionally, a higher resolution than the ADC over the full dynamic input range is needed, in order to cover all digitization values (ADU). For the following measurements the current sources described in Chapter 4 were used. Fig 5.1a shows an idealized test current source with the corresponding transferred ADC curve (Fig. 5.1b).

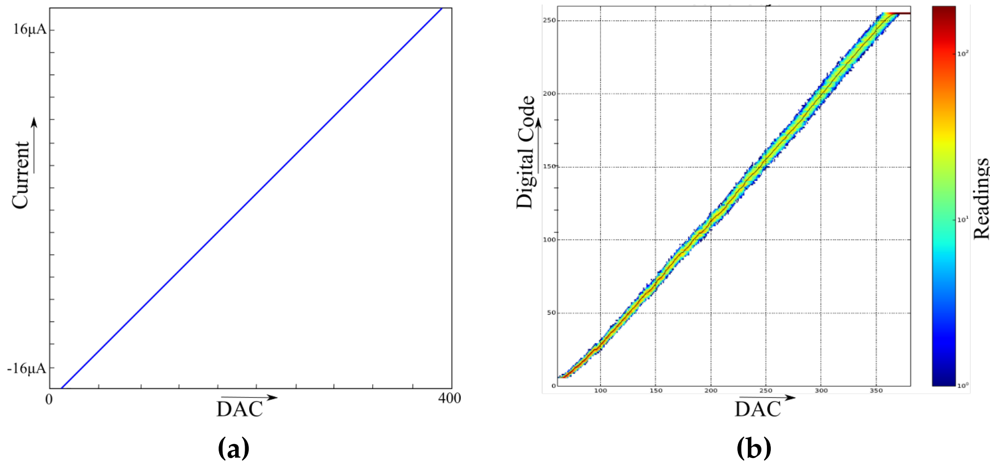


Figure 5.1: Transfer of a test current into digital code. Every DAC value has been sampled 512 times. The color code in b) marks the number of readings.

5.1 Properties of the ADC Transfer Curves

The properties which are used to evaluate the quality of a transfer curve are described in this section. First of all, it has to be considered, that an ADC converts a continuous analog signal into discrete digital numbers. Consequently, a loss of information depending on the ADCs resolution occurs. This so called quantization error is naturally to all analog-to-digital conversions. The mean quantization error σ_{Qnoise} is defined by

$$\sigma_{Qnoise} = \frac{\Delta I}{\sqrt{12}} \tag{5.1}$$

where ΔI is the current difference of two consecutive steps. This results in $\sigma_{Qnoise} = 0.3$ ADU, which represents the lower limit of noise. In the case of the eight bit pipeline ADC, the conversion results in a staircase with 256 steps (see Fig. 5.2a). Ideally, the step size would be the same for all stairs over the full range. Since this is not always correct, two methods are used to determine deviations.

Integral Nonlinearity

The first method is called Integral Non-Linearity (INL). It describes the divergence between the ideal line transfer function f_{ideal} and the actual output M. Here, M is the

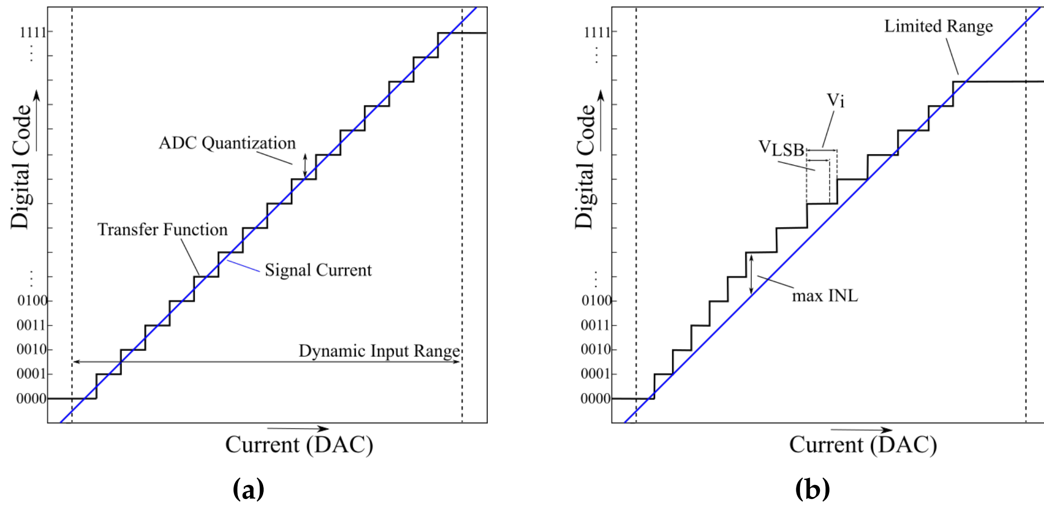


Figure 5.2: a) The ideal transfer function of an ADC (4 bit), where the blue line marks the input current. b) A defective transfer function containing deviations in DNL, INL and range.

mean of all readings per DAC.

$$INL(x) = M(x) - f_{ideal}(x) \tag{5.2}$$

The ideal line is calculated with the method of least trimmed squares [29], [30]. Compared to the standard least squares, this is more robust because outliers are excluded. For further robustness, only data points at least 10 ADU higher than the minimum and 10 ADU lower than the maximum are considered for the ideal line calculation. Due to the staircase nature of the actual transfer function, the INL typically shows a saw tooth behavior. Absolute INL values higher than 0.5 indicate nonlinearity. Often only the maximum of the INL function is stated, as it is mostly sufficient to rate the linearity of a transfer curve.

Differential Nonlinearity

The second approach, called Differential Non-Linearity (DNL), measures deviations of single step sizes. In ideal case, the step size is exactly the 256th part of the full input

range, which is called the Least Significant Bit (LSB). The DNL is defined as the ratio between the real step size and the ideal value.

$$DNL(i) = \frac{V_{i+1} - V_i}{V_{LSB}} - 1 \quad \text{for } 1 \leq i \leq 254 \tag{5.3}$$

The ideal step size V_{LSB} is calculated by the method of least trimmed squares as for the INL. V_i is the average DAC value per ADU. DNL values different than 0 indicate deviations in step size. Absolute DNL values higher than 1 lead to non monotonic transfer functions, also known as missing codes.

Range

Apart from linearity, the quality of a transfer curves also depends on its range. This may seem trivial, but it turned out that the digital output codes often do not reach the full range of 255 ADUs. Then, the transfer curve is limited at certain ADU values. This can happen at the upper as well as at the lower end. Therefore, the minimum and maximum ADU values are included into the quality control. Notice that the minimal ADU value is 1, while the maximum value is 255. You may wonder why only 255 values exist, instead of the 256 usual for 8 bit precision. This originates from the fact, that the DCD produces signed output code in the range ± 127, involving ± 0. The twofold meaning of 0 gets lost in later conversion, where simply 128 is added, leading to final digitization results in range 1 to 255.

Noise

The last evaluation property of a ADC curve is its noise. In order to determine the noise, a statistic of at least 512 samples for every DAC value was measured, where the noise is defined as the standard deviation of the samples. The median noise over the full dynamic range is an appropriate indicator for defect classification.

5.2 Analog Defects

The properties defined above can be used for defect detection. An overview of the different defects types, with an explanation of their cause, is given in the following. It is distinguished between analog and digital defects. Analog defects originate in the analog domain of the ADC, where they are caused either by mismatching components or wrong settings.

5.2.1 Limited Range & Gain Deviations

Among the parameters of the DCD, *IPSource*, *IPSource2* and *IFBPBias* have by far the largest impact on the ADC performance. They have in common, that they do not only influence one type of defect, but multiple. Fig. 5.3 shows how the parameter *IPSource* affects the range and the gain of a transfer curve. The gain reaches from 0.02 µA/LSB for *IPSource*=20 to 0.11 µA/LSB for *IPSource*=120. Actually it was intended to set the gain in the current receiver only, but in fact it turned out that it also scales with *IPSource*. This is not a defect in the classical sense, but it has to be considered when tuning *IPSource* in order to fix other defects.

The curve reaches a maximum range of 255 ADU for *IPSource* values from 60 to 80. Above this, the range rapidly shrinks up to poorly 139 ADU for *IPSource*=120. Below *IPSource*=50 more and more errors occur, untill the transfer curve totally collapses at *IPSource*=10.

This behavior can be explained in terms of the transfer model (Fig. 5.4). In order to work properly, the size of the cell must cover at least $\pm 4 I_{ref}$. With increasing *IPSource*, both I_{ref} and the thresholds increase. In this way the condition is no longer fulfilled and high currents don't fit in the cell anymore, which results in a limited range. According to the conversion algorithm, the change of the gain can be explained by the shift of the thresholds.

IPSorce2 and *IFBPBias* control the size of the cell, marked by red in the model (Fig. 5.4). Fig. 5.5 shows the effect of *IPSource2* on the transfer curves. Again, a strong influence

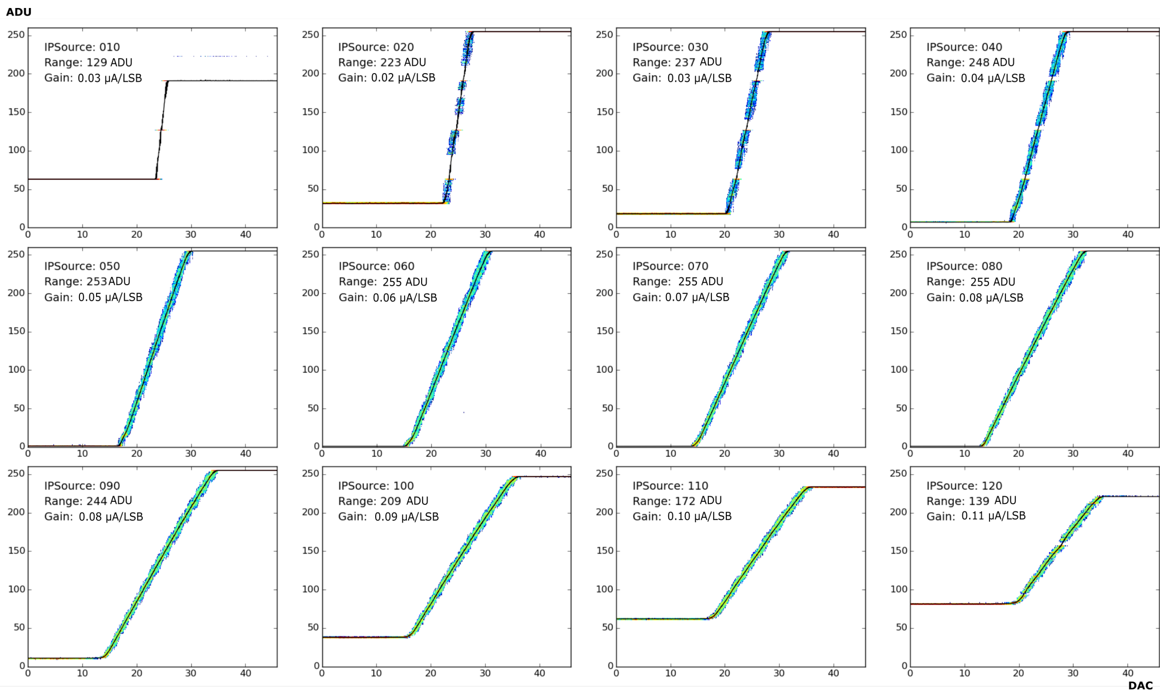


Figure 5.3: Impact of *IPSource* on an ADC channel. *IPSource* is sweeped from 10 to 120 in steps of 10 with otherwise fixed settings .

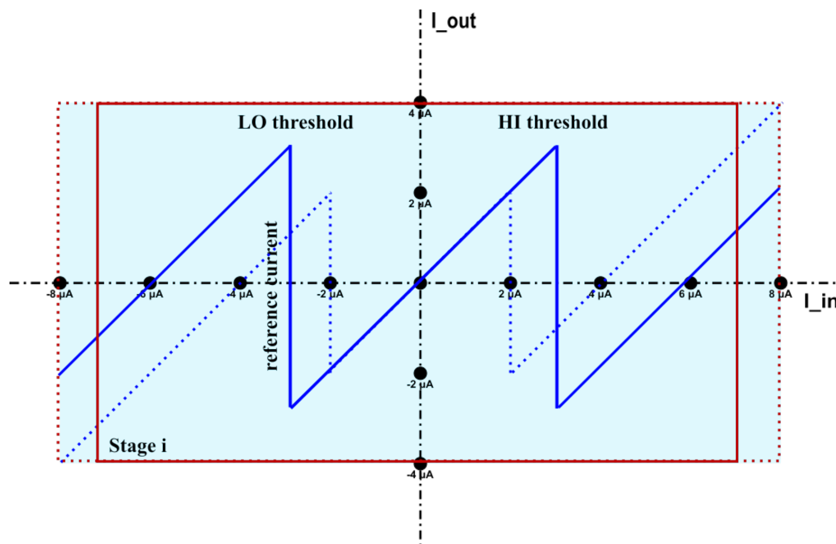


Figure 5.4: Effect of *IPSource*, *IPSource2* and *IFBPBias* on the transfer model. The dotted blue line markes the nominal transfer function, while the solid blue line refers to an increased *IPSource*. The range of the cell (red square) is controlled by the parameters *IPSource2* and *IFBPBias*.

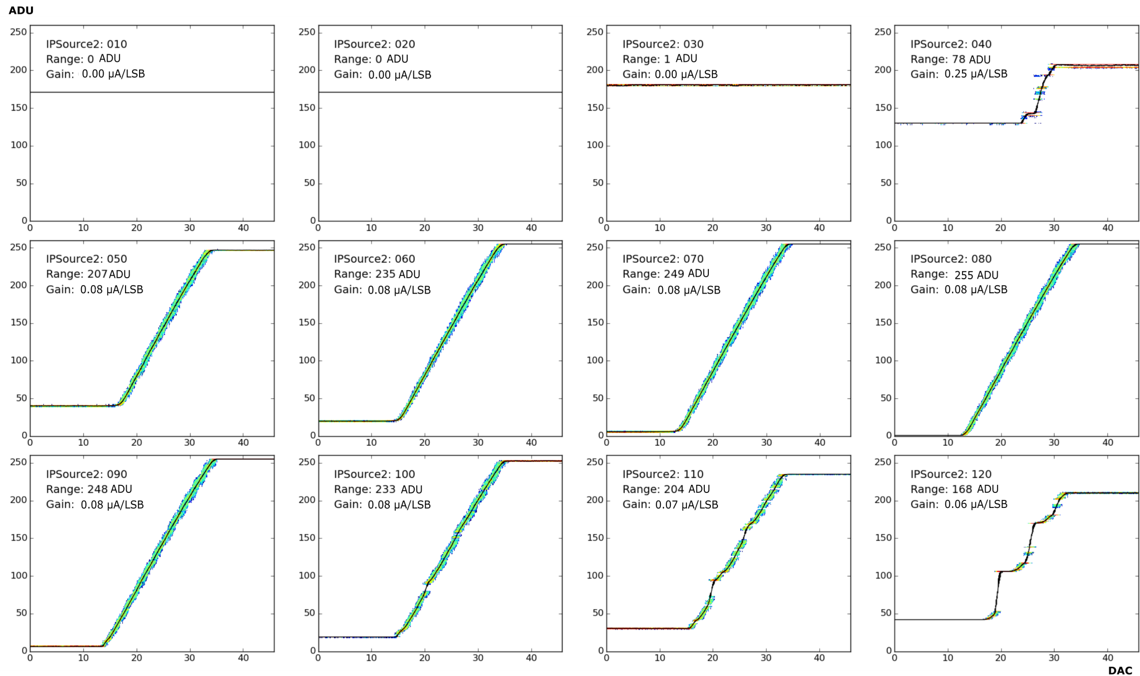


Figure 5.5: Impact of *IPSource2* on an ADC Channel. *IPSource2* is sweeped from 10 to 120 in steps of 10 at otherwise fixed settings.

on the range can be recognized. The sector from 60 to 90 is well fitting here, whereas the outer regions show lethal defects.

Parameter *IFBPBias* has a slightly different effect on the transfer curves (Fig. 5.6). The range increases linearly with this parameter. From *IFBPBias*=80 on, the full range is reached. Hardly recognizable are the missing codes, occurring for *IFBPBias* > 100.

In this work a channel is defined as defective, if its minimum range is higher than 20 ADU or if its maximum range is less than 250 ADU. This definition, evolves from the so far experience about the general behavior of the transfer curves. We assumed this range is sufficient to guarantee a successful contribution of the DCD. Nevertheless, the definition can be adapted to the physical needs at all time.

Of particularly importance for the cell size are not so much the absolute values of the parameters, but the right balance of them. Moreover, it has to be considered, that the parameters apply to all channels of a DCD simultaneously. Optimizing one channel is simple, the challenge is to find the best working point for all 256 of them.

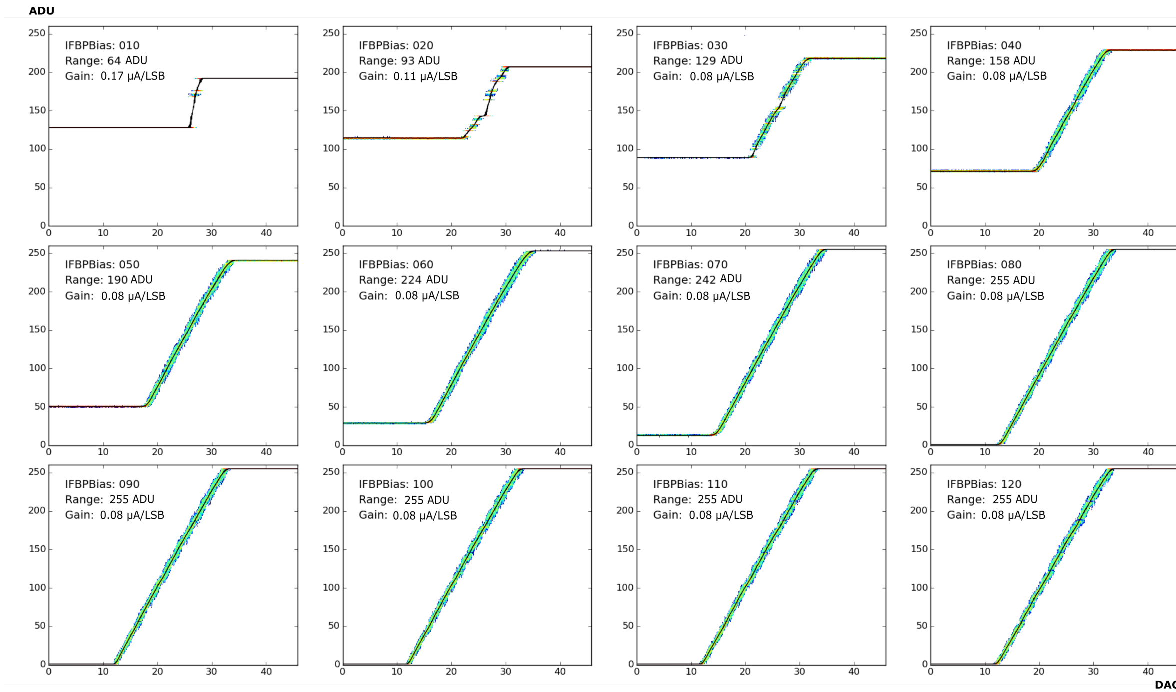


Figure 5.6: Impact of *IFBPBias* on an ADC Channel. *IFBPBias* is sweeped from 10 to 120 in steps of 10 with otherwise fixed settings.

5.2.2 High Noise

Beside the range limitations more specific defects occur . These are also affected by the settings. For example some of the ADC channels show higher noise than others, which are classified as defects, too. Thereby, it has to be considered that the measured noise is composed of different parts. The total noise divides into extrinsic noise on the one hand, which originates from the test current source, the wiring and the electrical connections and intrinsic noise of the ADC on the other. Only the intrinsic part, for which a dependence on the ADC's settings was found, is of interest for the ADC optimization. That is why the noise threshold for rating a channel as defective has to be chosen carefully. External influences depending on the experimental setup have to be filtered out.

Fig. 5.7 shows a noisy and a less noisy channel of the same DCD. The median noise of channel 48 is 4.51 LSB, while for channel 232 it is 6.19 LSB [1]. Increasing *IPSource* from 80 to 110 reduces the noise by roughly 30 %. Notice that the range of the ADC curves also changes with *IPSource* due to its influence on the gain.

5.2.3 Nonlinearity

Similar to the noise, the linearity of the transfer curves is also depending on intrinsic and extrinsic effects. Most probably the extrinsic part originates from the capacitance of the drain lines, which is assumed to be $\sim$50 pF [31]. Unfortunately, there is no possibility to disconnect the drain lines from the ADCs during transfer curve measurements (compare Fig. 3.7). Hence a charging and discharging of the drain lines can't be avoided, leading to deviations in linearity. Nevertheless, the unused channels[2] can be taken as reference.

Fig. 5.8 provides a comparison between a connected and a not connected channel, namely 8 and 11. They show a large difference in the INL function, where the maximum of the absolute value is 31 LSB and 0.9 LSB for channel 8 and 11 respectively. Decreasing parameter *AmpLow* from 380 mV to 280 mV, with otherwise identical settings, achieves a reduction of the INL by a factor of 2. The DEPFETs were switched off during the measurements by setting the gate voltage to +3 V.

Given the influence of the drain line capacity, which also fluctuates among channels, defining a hard limit for the INL is pointless. It must be the aim of the optimization process to end at the best possible INL for the respective DCD, instead.

1 An optimal ADC should ensure a median noise less than 1 LSB. The exemplary channels need to be further optimized, even though the largest part of the noise there is caused by the test current source.

2 Since four DCDs hold 1024 ADC channels for 1000 drain lines, 24 of them are not connected. These are the channel numbers 10 to 15 of each DCD.

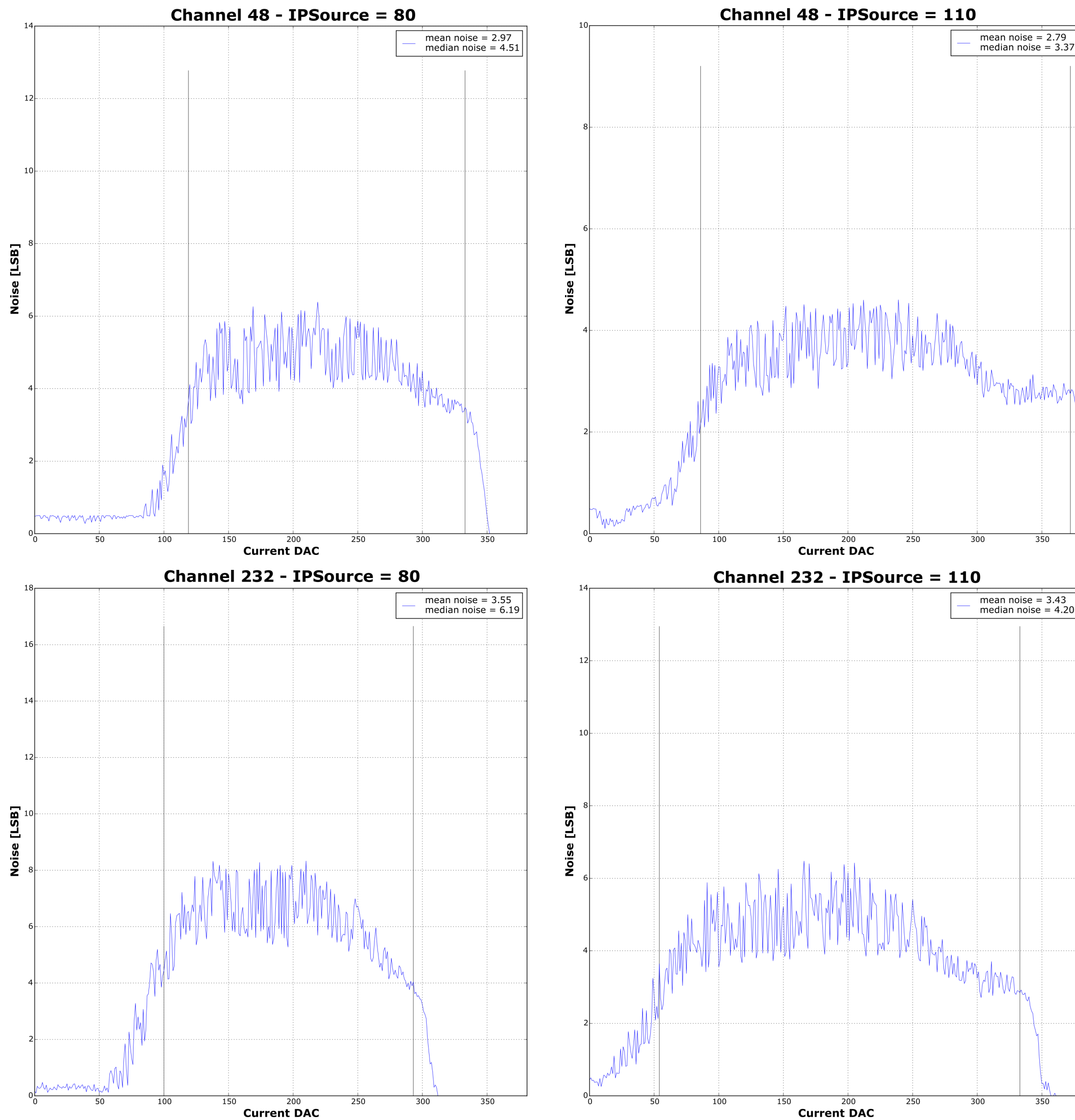


Figure 5.7: The noise of two different channels of the same DCD. An increase of *IPSource* is accompanied by a reduction of the median noise. The black lines mark the range used for noise calculation.

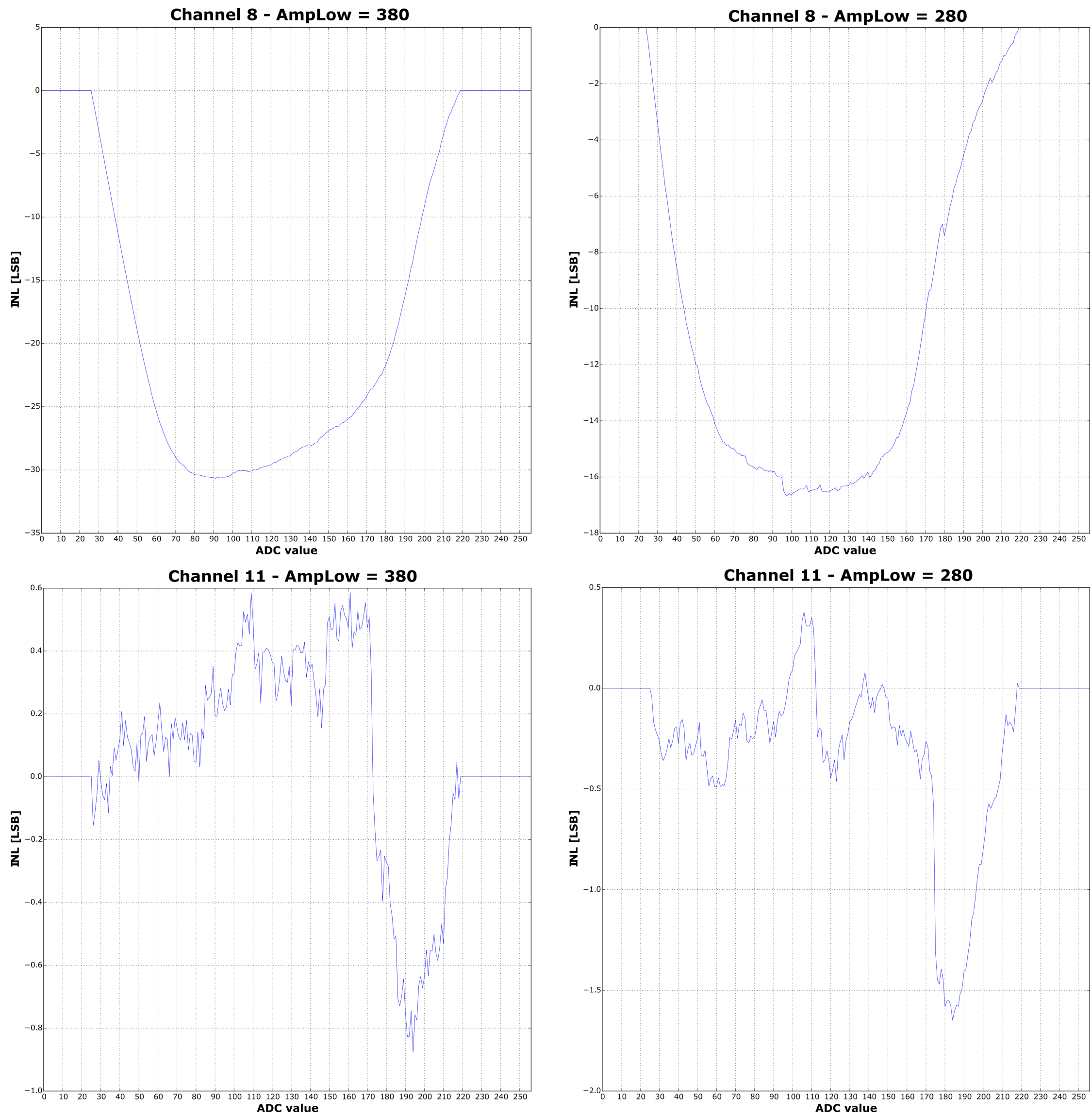


Figure 5.8: Channel 8 is connected to a drain line, while channel 11 is not. Optimization parameter *AmpLow* has a big impact on the INL.

5.2.4 Missing Codes

The most interesting as well as challenging defect is the so called missing code phenomenon. That means that a part of the transfer curve is partially or completely missing (examples can be found in Fig. 5.11). This defect was already observed on previous DCD versions, which used two cyclic ADCs. These were clocked two times faster, which was assumed to cause the missing codes. For this reason, the pipeline ADC which needs twice as much space, but can be operated on half of the clock speed, was introduced [21]. Nonetheless, it still shows missing codes. Therefore, understanding where the code gets lost and how to prevent this is a main goal of the ADC optimization. In this chapter an improved model explaining the origin of the missing codes is presented.

Origin of Missing Codes

All transistors show small deviations from their nominal values. This was taken into account by the DCD designers, which is why they implemented the redundant signed digit conversion. This algorithm features a strong robustness against perturbations. Thus, deviations from the nominal threshold value do not affect the conversion result as long as they are smaller than $\frac{1}{8}$ of the input range, which is 2 µA in this case. Missing codes occur if the offset, however, exceeds this limit. Four different types of offsets are possible. They can be represented in the transfer model (Fig. 5.9). Remember that this model represents only one of the eight stages of the pipeline ADC. An offset error can arise in each of them.

The offsets in the model can directly be related to a mismatch of transistors between the current memory cell and the comparator. Fig. 5.10 shows the transconductors of both of them (compare to Fig. 3.5 and Fig. 3.6). In this case transistor *M2a* of the copy transconductor has a bias current of 26 µA instead of nominal 24 µA. This causes an offset to the output current of 2 µA, which then becomes 10 µA. A HI comparator with a threshold of also 10 µA is drawn. In such a case the current can overcome the threshold, leading to a wrong comparison result. Thereby, a mismatch of only $\frac{2}{24} = 8,3\%$ of one transistor can cause a missing code. For the depicted stage,

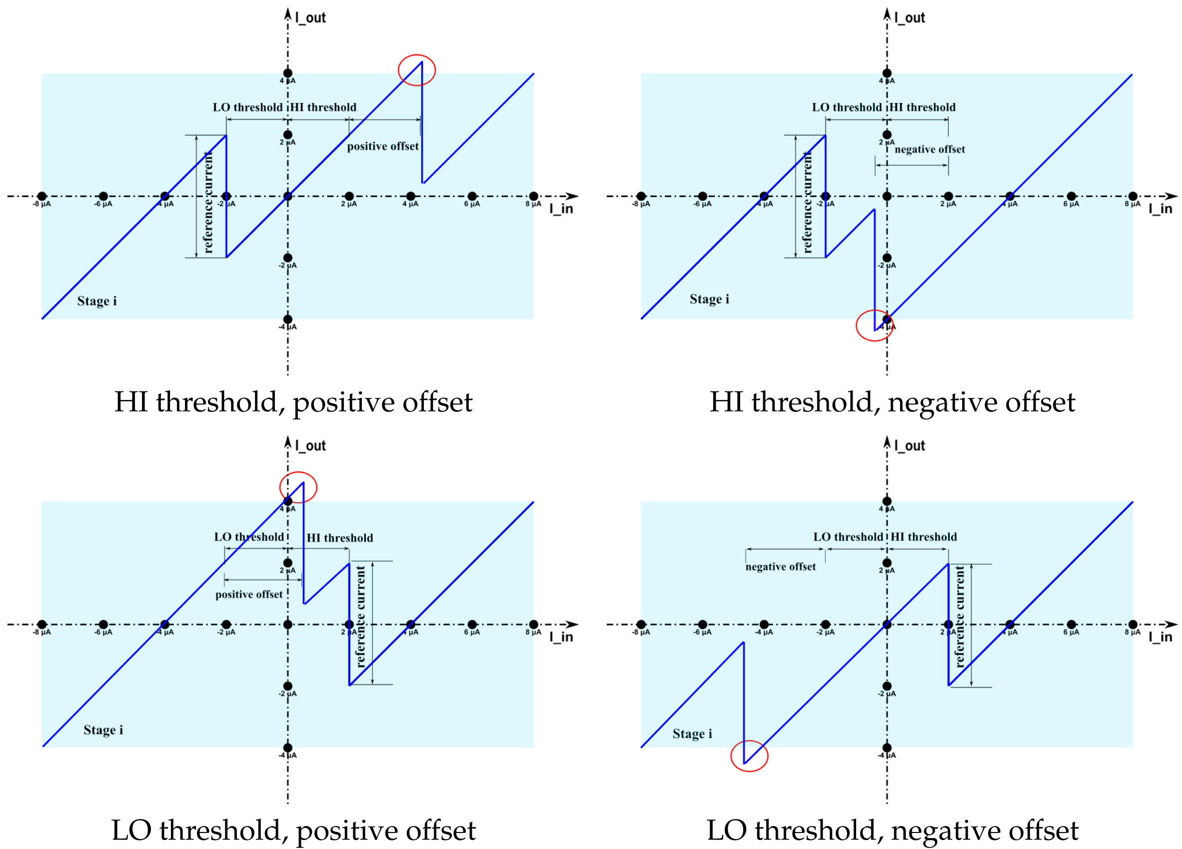


Figure 5.9: Different types of offsets in the transfermodel. If the offset to the thresholds exceeds 2 µA, the transfer function ends up outside of the cell size. This causes a malfunction of the ADC, which manifests as a missing code in the transfer curve.

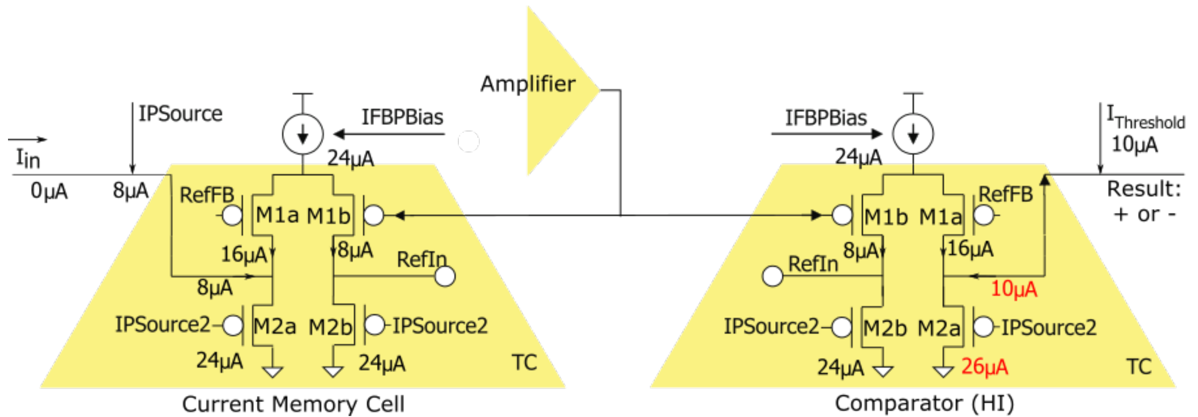


Figure 5.10: The transistor M2a in the copy transconductor of the comparator has an offset of 2 µA. As a consequence the copied current differs also by 2 µA, causing a wrong comparison result. Adapted from [22],[21]

the output code would falsely be $+1$ instead of 0. The depicted error in the transistor schematic corresponds to a HI threshold with negative offset in the transfer model.

Furthermore, Fig. 5.10 illustrates that the total offset is composed of contributions from *M1a*, *M1b*, *M2a* and *M2b*, making a high offset more probable. It also becomes clear, that the offsets again are strongly influenced by *IPSource*, *IPSource2* and *IFBPbias*.

Missing Code Detection

Some examples of missing codes, that occur in different stages, are plotted in Fig. 5.11. In a) the high comparator has a positive offset of $\sim$5 µA in stage 0. Within the input range from $+2$ µA to $+4.5$ µA, the stages conversion result is 0 instead of $+1$ (see Fig. 5.9). Until the current reaches $+4$ µA, the error of stage 0 is compensated by the lower stages. For $+4$ µA the conversion results of the stages is: a_0=0, a_1=+1, a_2=+1, a_3=+1, a_4=+1, a_5=+1, a_6=+1. Using the conversion equation $D = \sum_{i=0}^{n} 2^{n-i} a_i + 128$ (see Eq. 3.1), this translates to 191 ADU. All lower stages are at their maximum at this time and can't compensate stage 0 anymore. From now on the output code clamps at 191 ADU, until the current rises to 4.5 µA, where it finally overcomes the threshold of stage 0. The ADC then finally jumps back into normal operation, leaving a gap in the ADU code. The width of the gap depends on the offset level.

If the lower threshold is affected, the only difference is the value of the clamping conversion result. In b) this is a_0=-1. Consequently, the output code clamps at 127 ADU (-1, +1, +1, +1, +1, +1, +1). If the offset affects stage 1 (as in c)) the number of missing codes increases. The output pattern is shifted to the right by one stage ({-1, 0, +1}, -1, +1, +1, +1, +1, +1), leaving three options for a_0. The code then clamps at three positions: 63 ADU, 127 ADU and 191 ADU. The plot in d) can be deduced to a positive offset on stage 2 ({-1, 0, +1}, {-1, 0, +1}, -1, +1, +1, +1, +1). You may wonder why there are exactly seven missing codes in the curve. This is related to the redundancy of the conversion algorithm. Each of a_0 and a_1 can either be -1, 0 or $+1$, which allows nine combinations. Since a_0 is weighted by 64 and a_1 by 32,

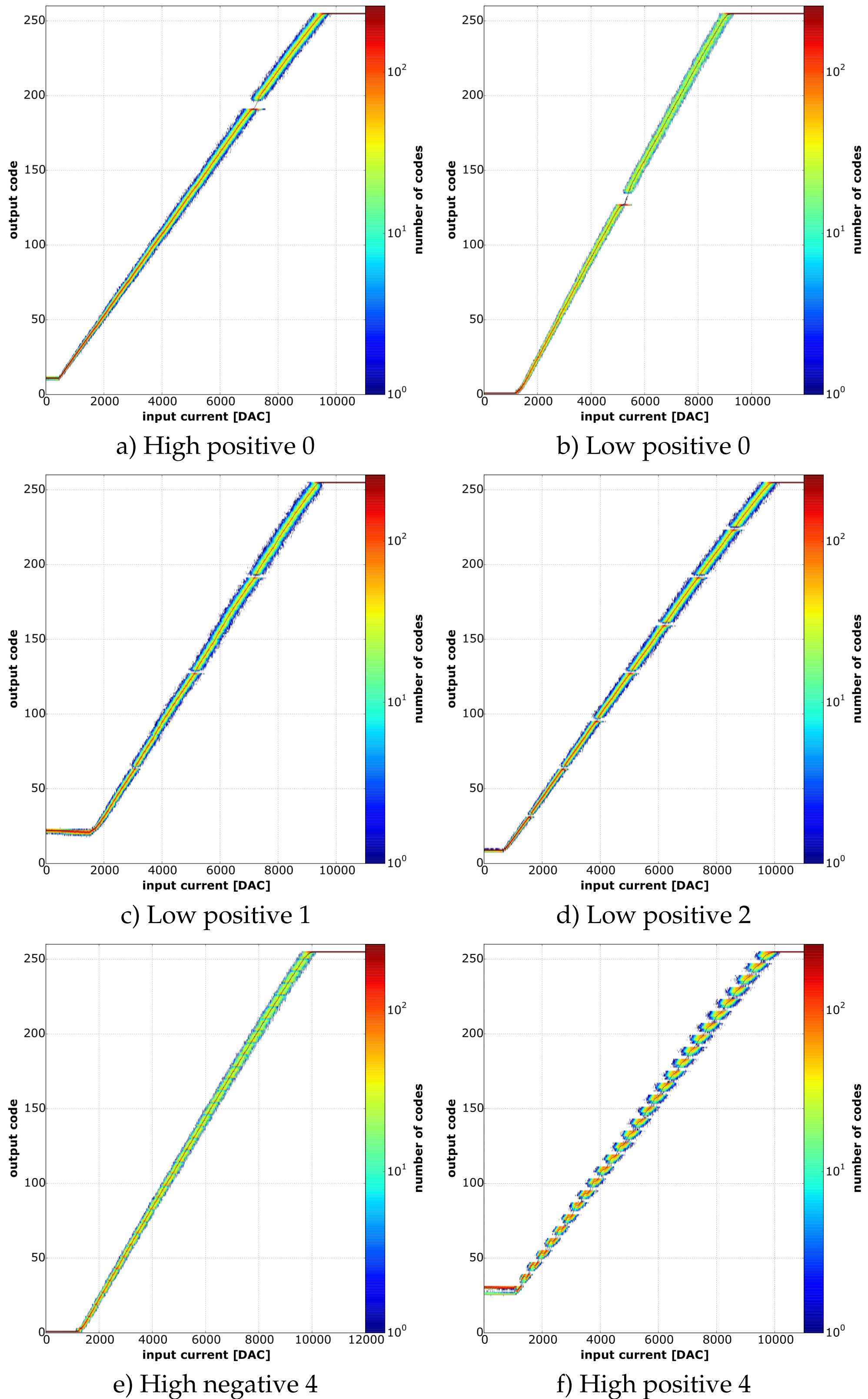


Figure 5.11: Examples of missing codes. They are caused by offset in the low or high comparators. The offsets can be positive or negative and can arise in all conversion stages.

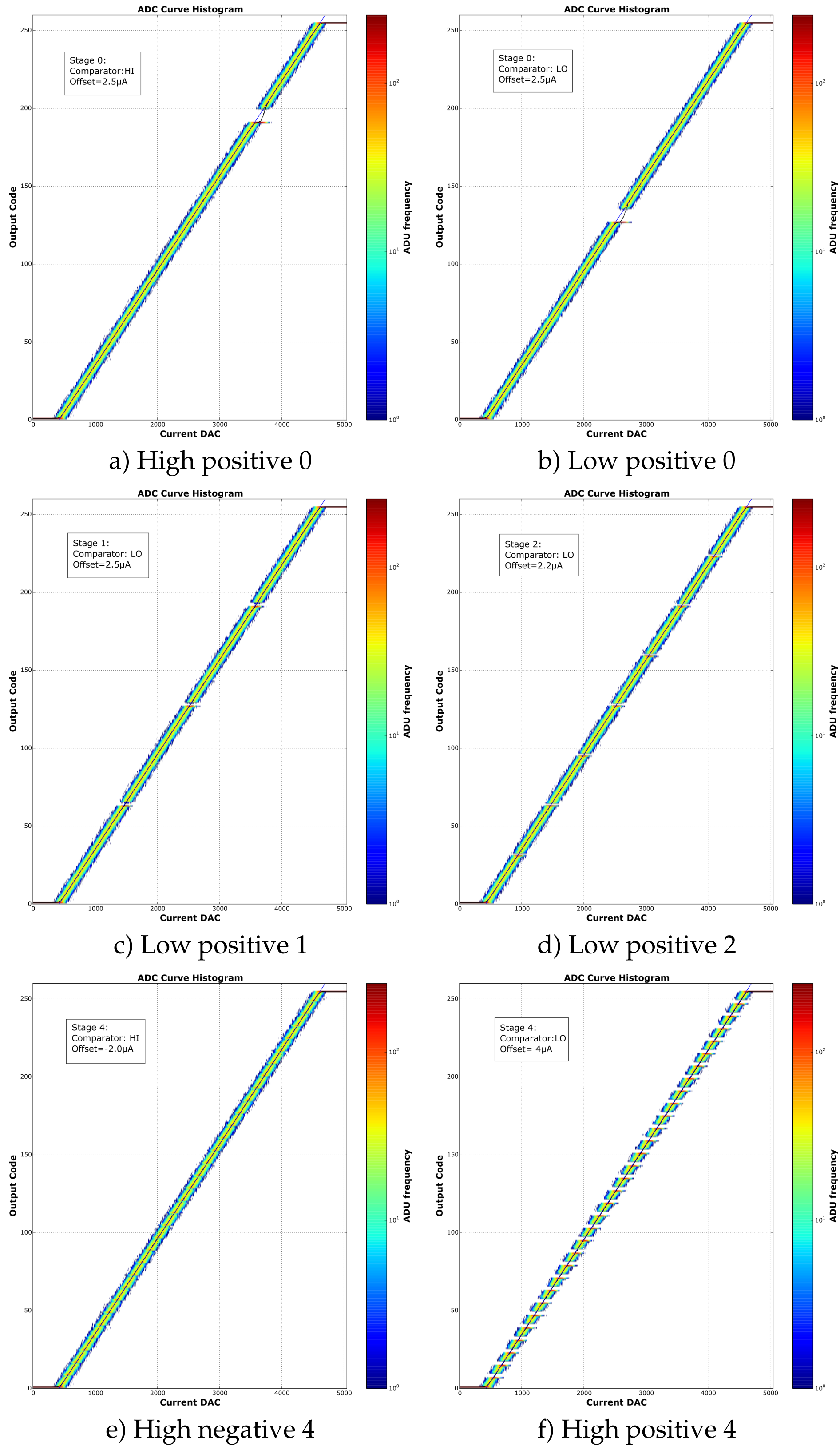


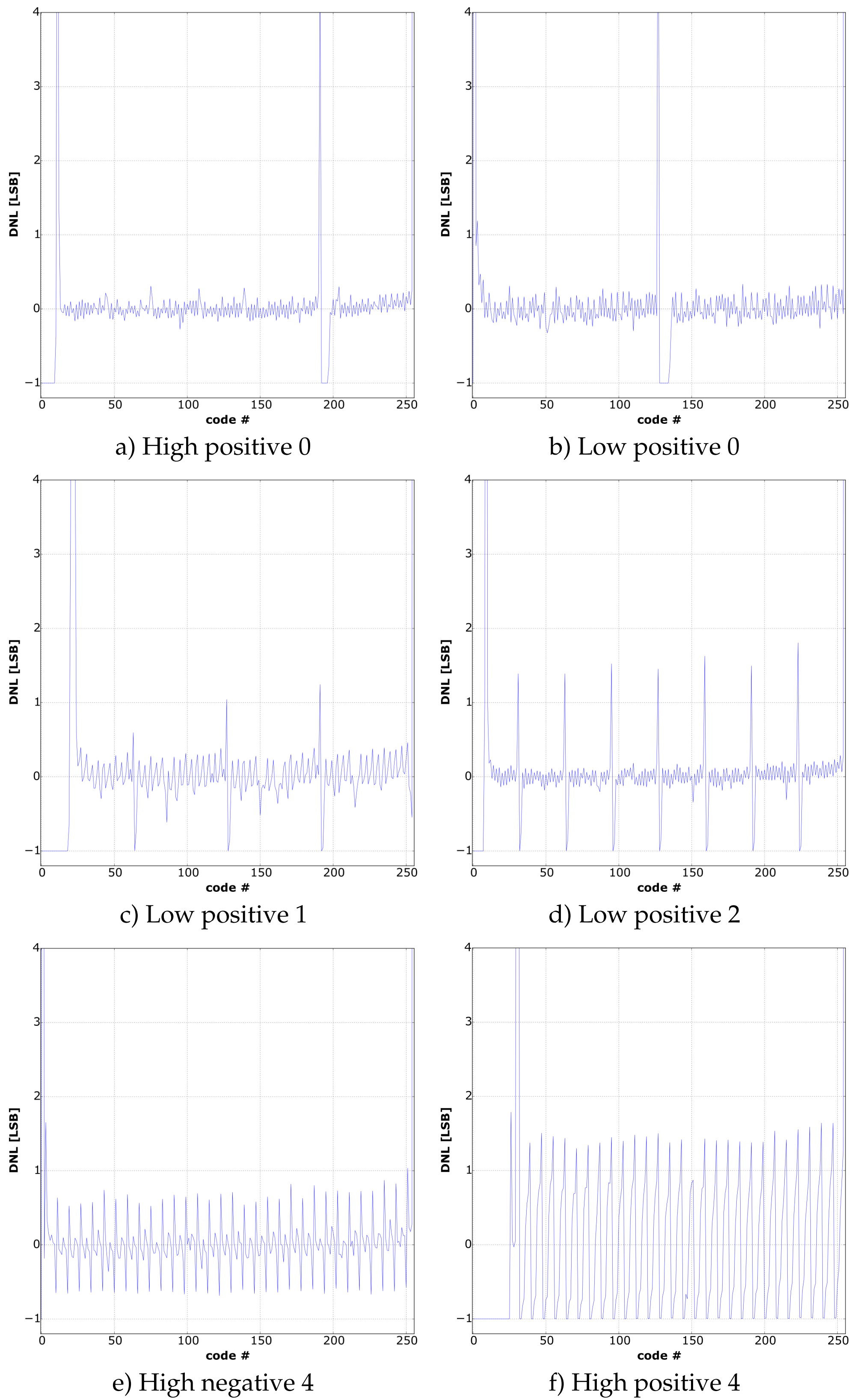
Figure 5.12: Simulation of the errors of Fig. 5.11

the combinations (-1, 1) and (0, -1) both result in -32. The same holds for (1, -1) and (0, 1) with 32. Therefore seven clamping positions exist. d) shows an example with a negative offset. In this case the clamping position is above the missing part and the lower stages turn to -1({-1, 0, +1}, {-1, 0, +1}, {-1, 0, +1}, {-1, 0, +1} +1, -1, -1, -1).

In order to proof this theory, the conversion principle was modeled. This model is not based on transistor simulations, but it is basically the algorithm described in Chapter 3, where offsets can be added to each of the stages. For Fig. 5.12 the simulation was used to reproduce the errors of Fig. 5.11. A more detailed Monte Carlo simulation on the origin of the mismatch can be found in [32].

According to Eq. 5.3 a clamping code generates a peak in the DNL, whereas two consecutive missing values result in a DNL of -1. This makes the DNL function very useful for missing code detection. Fig. 5.13 shows the DNL functions belonging to the transfer curves from Fig. 5.11. In this work a missing code is defined as a single peak with a DNL higher than 1 LSB, while its direct neighbors are smaller 0.8 LSB of which at least one is smaller than -0.8 LSB. With this definition, all curves except e) are recognized as defects.

The ADC parameters apply simultaneously to all stages of all channels. This means, if one reduces *IPSource2* in order to reduce the positive offset of one channel, this might push another channel beyond the negative limit. It is therefore unavoidable to sweep over different settings and count the number of missing codes for finding the best working point.



a) High positive 0
b) Low positive 0
c) Low positive 1
d) Low positive 2
e) High negative 4
f) High positive 4

Figure 5.13: DNL functions of the transfer curves corresponding to Fig. 5.11

5.3 Digital Defects

Digital defects are not influenced by the ADC's settings and therefore can not be optimized with them. Nevertheless they have to be distinguished from analog defects, in order to exclude them from the ADC optimization process.

5.3.1 Communication Errors

The output code of the DCD is transferred to the DHP via eight output buses, each of them eight bit wide. Each 32 channels are grouped to one of the output buses. Thereby the eight bit output code of every channel is send in parallel, so that every bit of a word is send on a different transfer line. On the DHP side, the send code must be sampled at the right time. To this end every transfer line has adjustable delay elements with 16 delay options. In order to adjust them, the DCD offers the possibility to send a test pattern. Nevertheless, a correct data transmission could not always be guaranteed. Sometimes the DHP shows a certain probability to interpret a 0 as 1. This is depending on cross-talk between neighboring channels as well as on the previously send signal [33]. Consequently communication errors arise, which become visible in the transfer curves. In the following the convention of the DHP is used, where bit number 0 denotes the LSB and bit number 7 the Most Significant Bit (MSB).

Fig. 5.14 shows some examples of communication errors. In a) bit 7 stuck to 1. Notice that bit 7 is interpreted reverse than the lower bits. This is due to the data format of the DCD and causes a down shift of 128 ADU on the right half of the transfer curve, where bit 7 is wrongly interpreted. On contrary, in plot b) parts of the curve are shifted upwards. Since bit 4 is always read as 1, every part of the curve where this is wrong, is shifted by 16 ADU. In general it holds, that the transfer curve is shifted by $S = 2^n$ ADU with a frequency of $N = 2^{7-n}$, where n is the bit number. In this way, 32 parts of the transfer curve in c) are shifted upwards by 4 ADU. The signal of bit 4 in plot d) was not always interpreted as 1, but with a probability

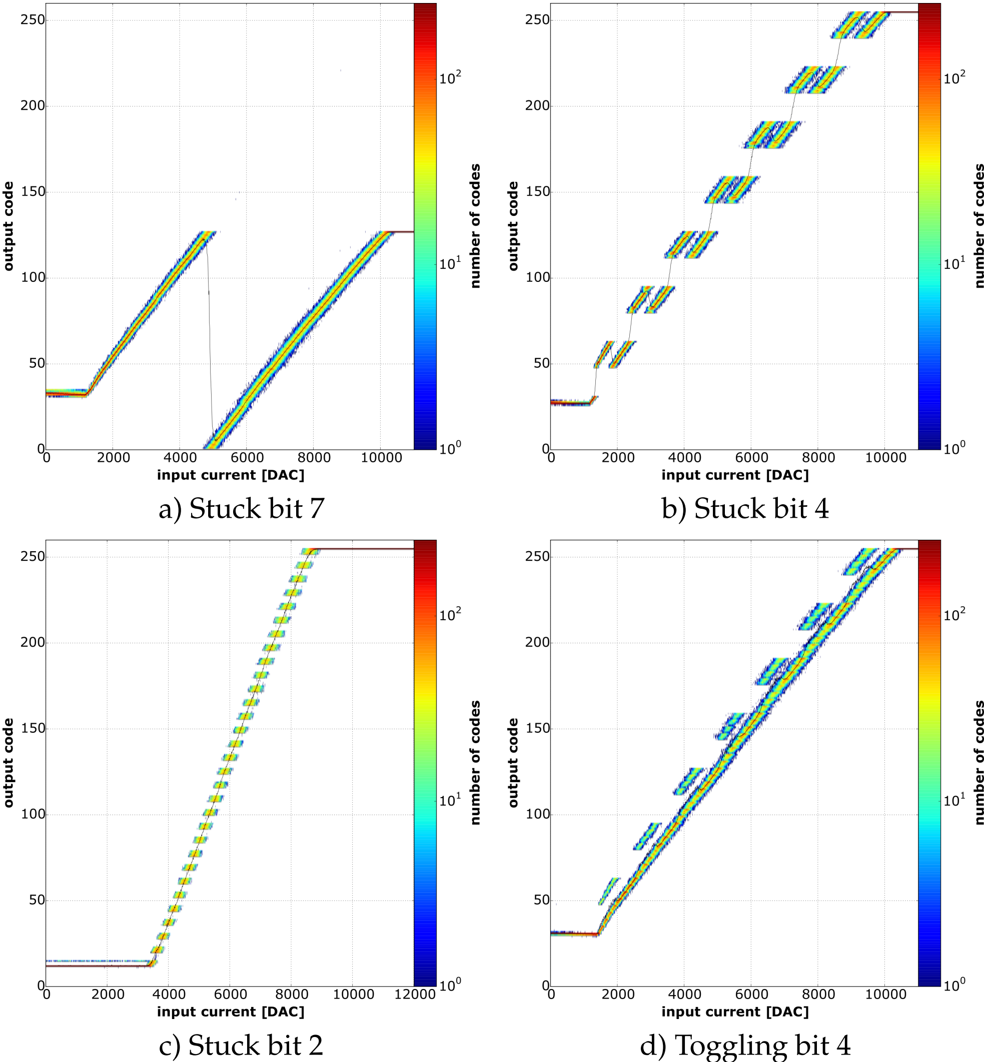


Figure 5.14: Different communication errors measured.

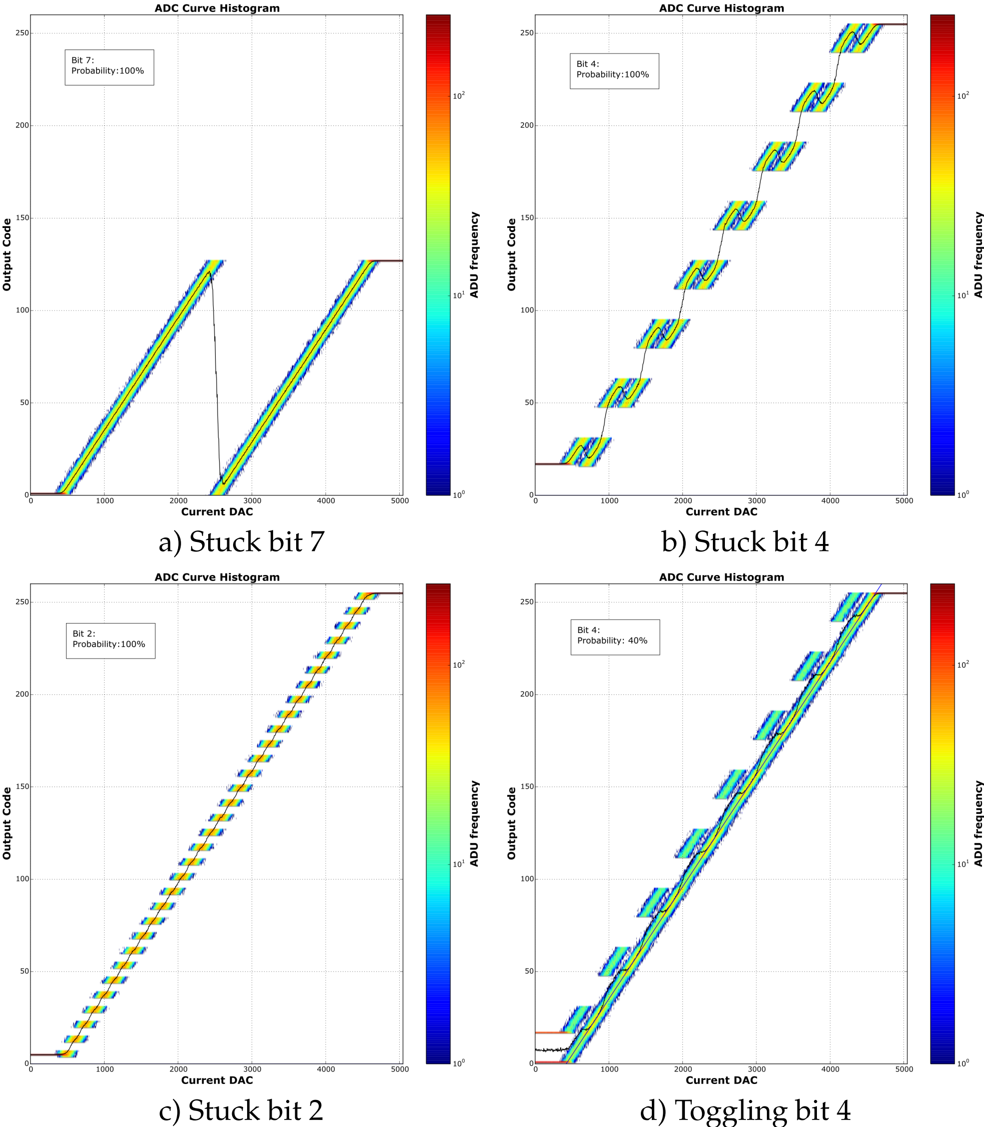
of $\sim$40 %. In principle all probabilities between 0 % and 100 % are possible. Multiple occurrences of different bit errors within the same transfer curve were found also.

It is possible to generate the communication errors in simulation, similar as for the missing codes. For doing so the simulated data was partially overwritten by 1. In Fig. 5.15 the transfer curves of Fig. 5.14 are reproduced.

Again, the DNL function can be used to detect these errors. Fig 5.16 shows the belonging plots. This allows to easily detect the shown bit errors. However, the differentiation between missing codes of high stages and communication errors of low bits is rather difficult. Bit errors with a probability below 20 % are also hardly detectable in the DNL.

5.3.2 Single Outliers

Some of the transfer curves show single outliers, as in Fig. 5.17. They are not to be confused with communication errors of very low probability. Since their appearance was found only in combination with the use of the external test current source, it is most likely that they are wrongly generated in the test source during fast switching. For that reason they simply are ignored in the optimization process.



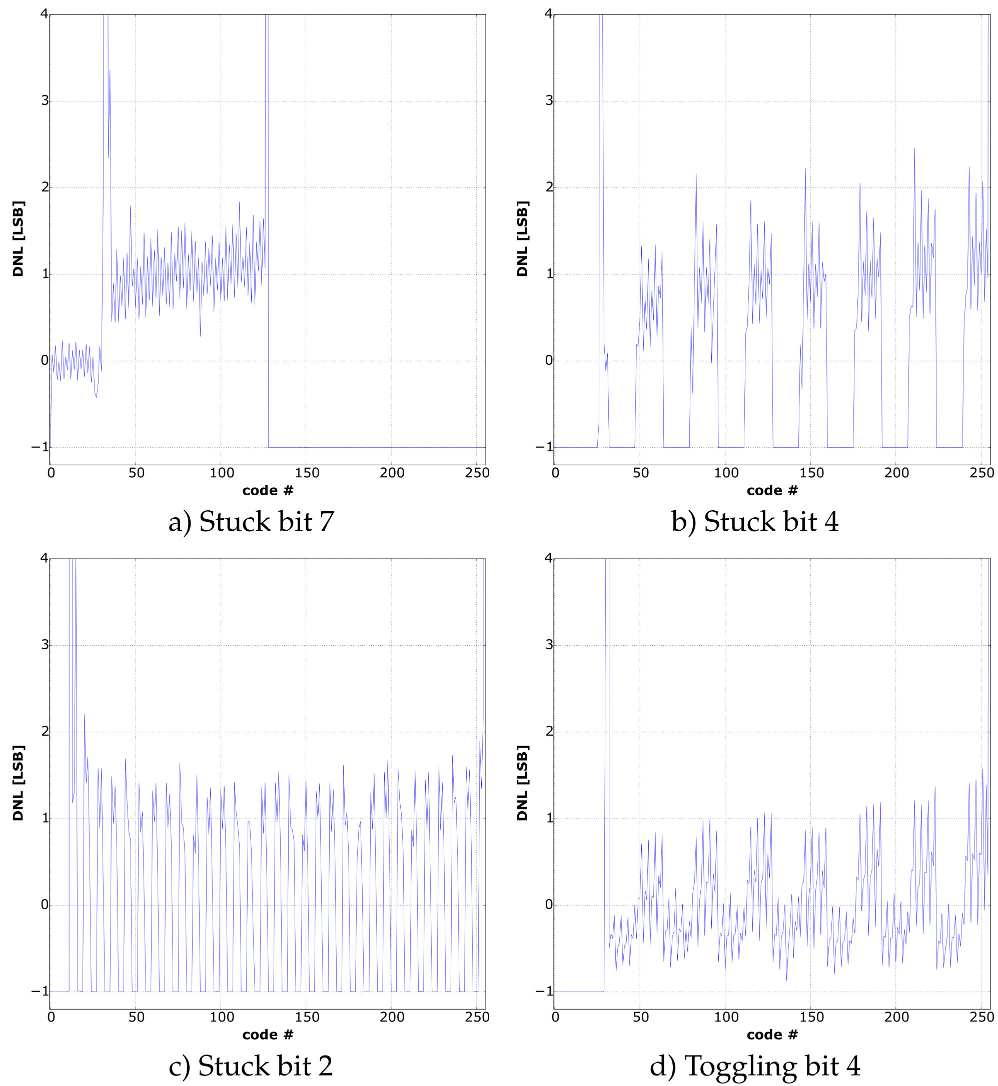
a) Stuck bit 7

b) Stuck bit 4

c) Stuck bit 2

d) Toggling bit 4

Figure 5.15: Simulation of the communication errors corresponding to Fig. 5.14



a) Stuck bit 7 b) Stuck bit 4

c) Stuck bit 2 d) Toggling bit 4

Figure 5.16: The DNL functions of the transfer curves of Fig. 5.14

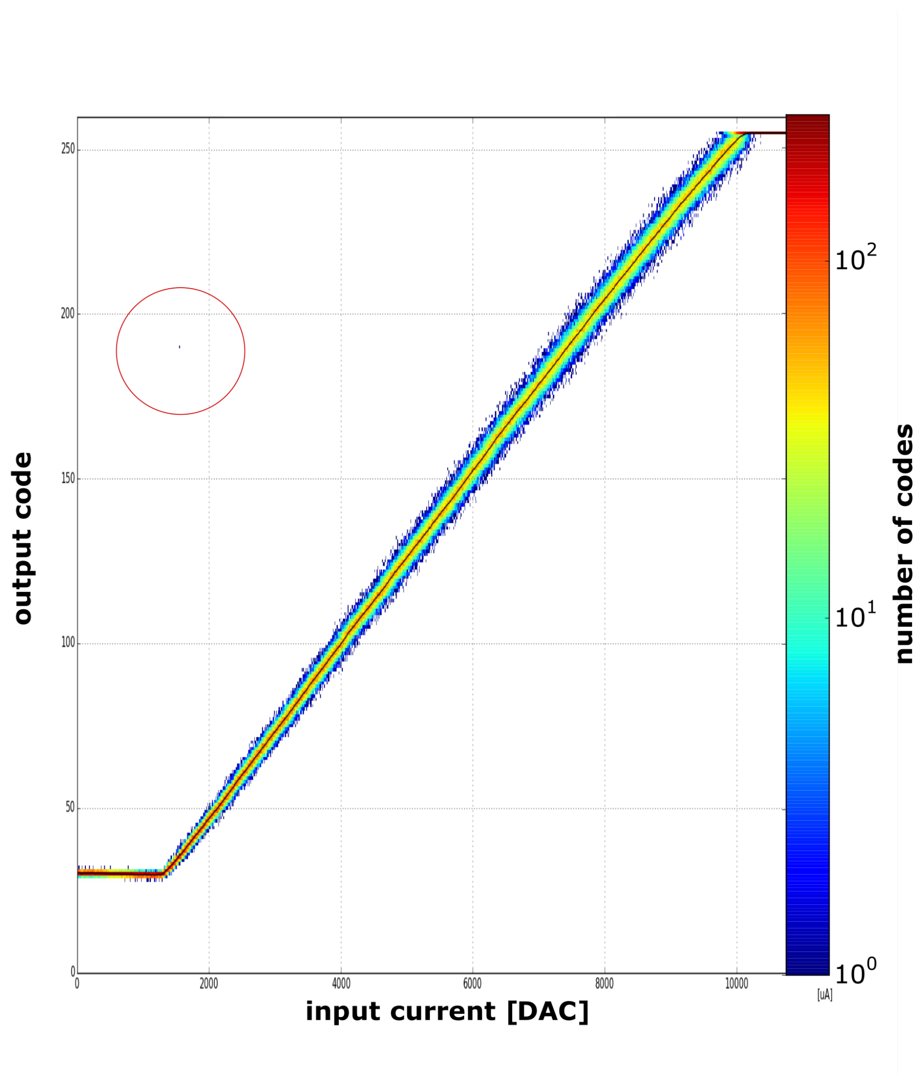


Figure 5.17: A single outlier.

6 ADC Optimization

The aim of this chapter is to find the best working point of the ADC. This is achieved through iterative sweeps of the DCD's parameters, where the classification of defects defined in the previous chapter is applied for error detection. In the following the full optimization procedure will be demonstrated as example on the PXD9 Pilot module W30 OB2 using the internal current source.

6.1 Establishing a Data Connection

First of all a stable data connection has to be established. This is adjusted in the DHP for both the DCD – DHP and the DHP – DHE connection.

6.1.1 DHP Delays

Fig. 6.1 shows the signal integrity of all 64 data transfer lines between the DHP and DCD of module W30 OB2 asicpair 4. As described in Chapter 3.3.2, the 256 channels are organized in eight blocks of 32 channels each. Here, each block belongs to one row of the figure. Furthermore, each block holds eight separate transfer lines for the eight bit data words. These are aligned as columns in the figure. The x-axis represents the global delay settings and the y-axis the local delay settings, which both can be adjusted in the DHP (see chapter 4.2.1). The color code displays the number of wrong readings during synchronization with the test pattern. The dark blue region defines the delay space where data is always transmitted correctly. A detailed description of the delay adjustment can be found in [34].

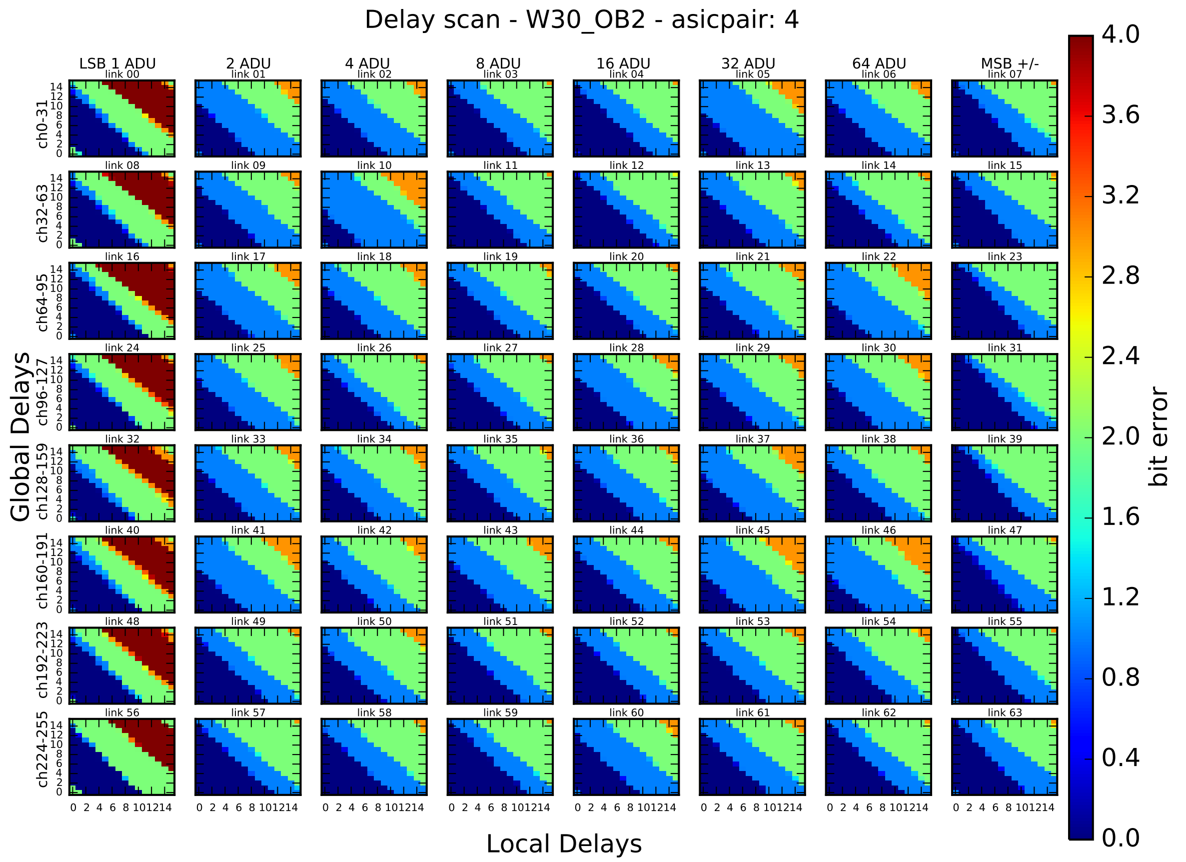


Figure 6.1: Link integrity for a global clock of 76.23 MHz on PXD9 Pilot module W30_OB2 asicpair 4.

Some transfer lines have a small delay space, which may result in the failing of the link. This instability has two reasons: for one thing the output driver of the DCD is too weak. For another thing the DHP's[1] input pads are disturbed by parasitic capacities of their electrostatic discharge protection [35]. Since a link instability seriously impedes the ADC optimization, it was decided to circumvent this problem by reducing the global clock speed. Fig. 6.2 shows the same transfer lines for a global clock of 62.5 MHz, there the delay space is much larger. In this way it is possible to avoid communication errors completely. Although, the clock also effects the speed of the ADCs, this is assumed to not influence range, linearity and missing code errors of the transfer curves. Moreover, the DCD and the DHP are operated at slightly increased supply voltages for further enhancement of the data connection.

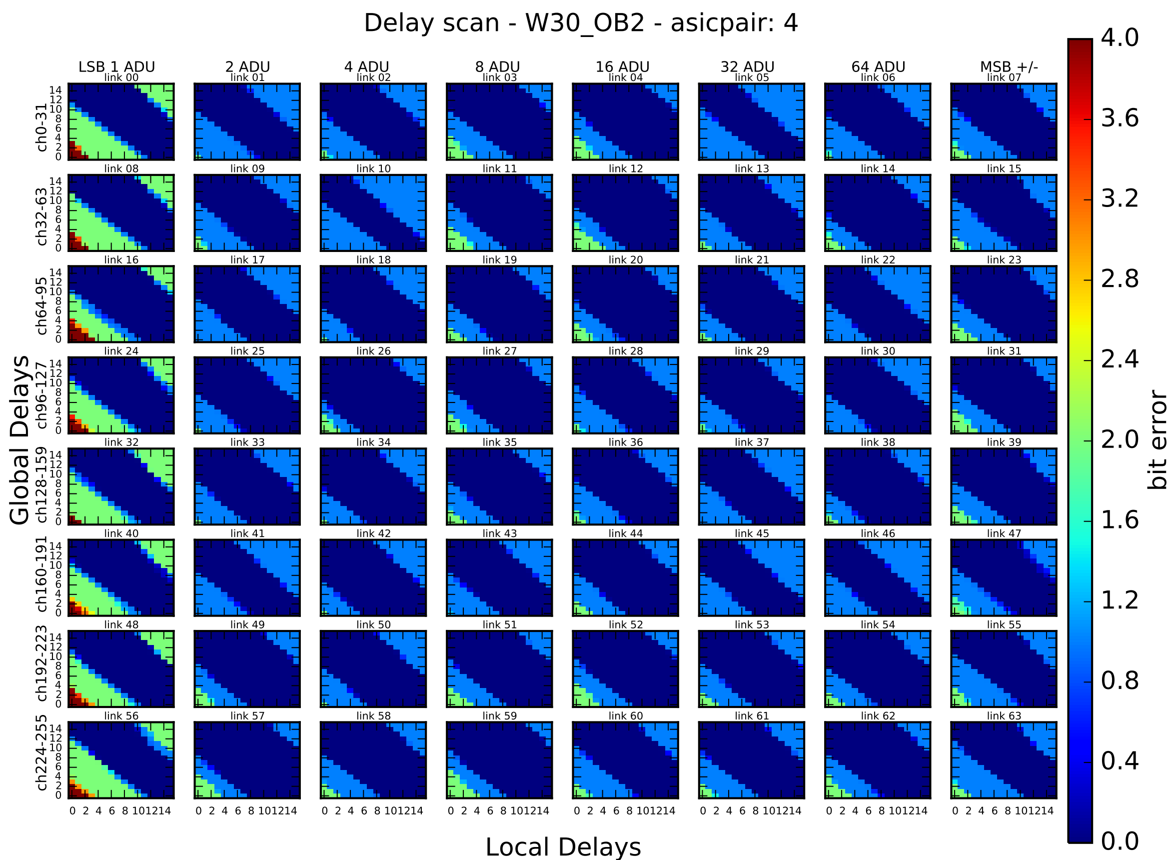


Figure 6.2: Link integrity for a global clock of 62.5 MHz.

1 version DHPT 1.0

6.1.2 High Speed Link

The high speed link's preemphasis is controlled via *Bias*, *Bias D* and *Bias Delay* (see Chapter 4.2.2). Fig. 6.3 shows a sweep of *Bias* versus *Bias D* for fixed *Bias Delay* = 0 at a clock frequency of 62.5 MHz. The color code refers to the data eye opening. The red regions correspond to high signal integrity, whereas the blue and white regions correspond to a disruption of the connection. DHP 4 shows the best behavior, which is why it was chosen for the following optimization.

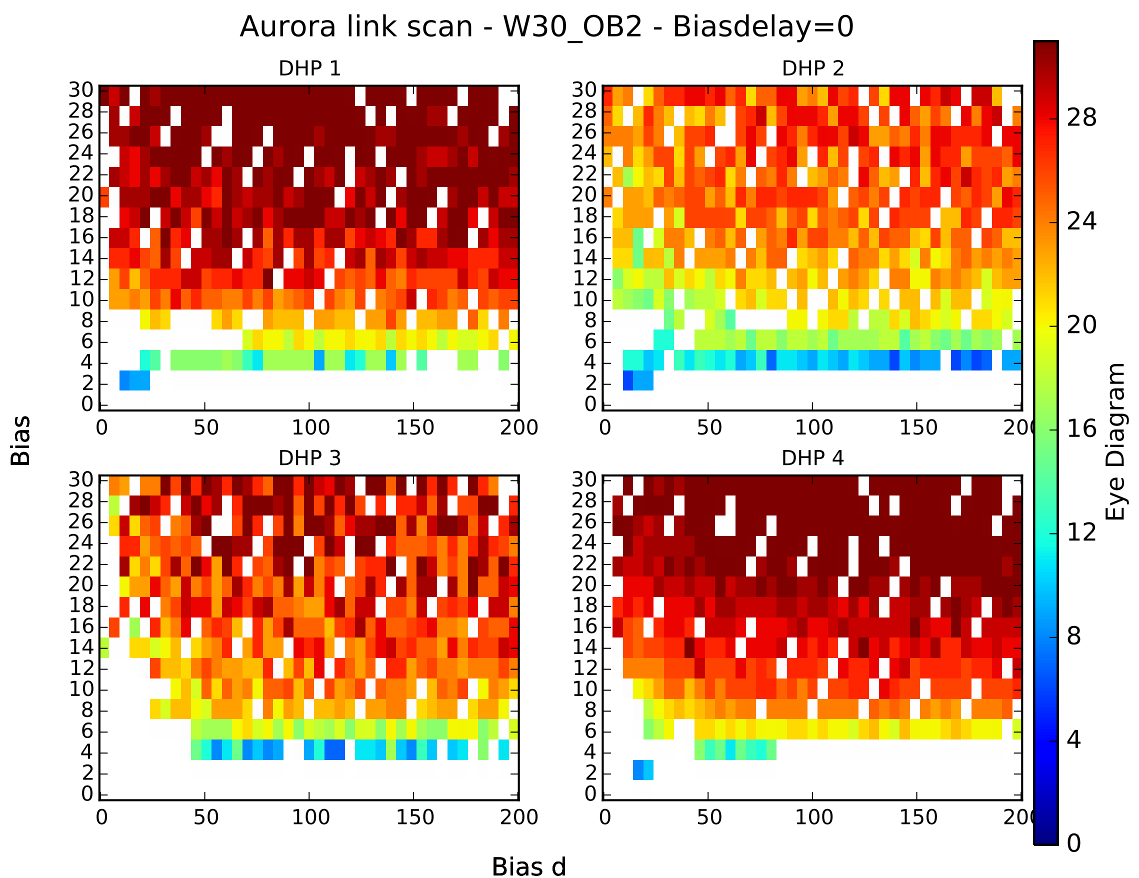


Figure 6.3: Adjustment of the high speed link

6.2 Full Optimization of a Module

Chapters 3 & 5 pointed out that the ADC's performance mainly depends on the three settings *IPSource*, *IPSource2* and *IFBPBias*. Sweeping over them and counting the number of defects is the procedure used for optimization.

First of all the question arises, from which values to start and over which range to sweep. From previous measurements it is known that the optimal working point must be around a value of 90 for all three settings, which is why this is chosen as a starting point. The range of the sweep is more than anything limited by the measurement time. Sweeping from 70 to 110 in steps of 5 seems to be a good compromise between time constraints and measurement accuracy.

There is no alternative to the internal current source, when categorical searching for the optimal working point. For the price of a long measurement time, it ensures most precise defect identification. It has to be considered that the internal current source reaches over 32 µA only, which is equivalent to the ADC's dynamic input range. But in this case some transfer curves are shifted beyond the input range due to the channels' different offsets. Hence, the gain of the current receiver is set to 2, which doubles the scope of the internal current source.

	internal	external	DEPFET
median noise	0.95	7.00	0.84
maximum INL	6.12	11.44	18.77

Table 6.1: Noise and linearity of an exemplary channel for different test current sources.

6.2.1 One-Dimensional Sweeps

At first a one-dimensional sweep over each of the three settings is performed. Every eighth of the 256 ADC channels is scanned, which are 32 channels in total. This seems to be an adequate statistic for evaluating the entirety of the channels. With this subset of channels the measurement time amounts to 3.6 h per parameter. The analog defects defined in Chapter 5 act as quality criteria.

	channel defective if
lower limit	minimum ADU > 20
upper limit	maximum ADU < 250
missing code	DNL peak > 1 LSB neighbours < 0.8 LSB one neighbour < -0.8 LSB
linearity	maximum INL > 10 LSB
noise	median noise > 1.5 LSB

Table 6.2: Defect criteria.

IPSource

Fig. 6.4 shows a scan of different *IPSource* settings. Each of the six subplots present a histogram of one defect type, where the color as well as the height of the bars correspond to the number of channels fulfilling the respective defect criterion. The range criterion is applied to the two upper subplots. On the upper left the number of channels with a minimum ADU below 20 ADU is drawn. The same is done for channels with a maximum ADU higher 250 ADU on the upper right. Particularly interesting is the subplot to the mid left. It shows the percentage of channels containing missing codes. The plot to the mid right provides information about linearity, which is measured by the maximum INL. The noise criterion is applied to the lower left. As a final result, the product of all criteria is build on the lower right, showing the number of channels fulfilling all criteria.

The plot clearly shows how the lower range breaks down at *IPSource*=95. A reduction of the upper range starts from *IPSource*=95. Clearly evident is the function of missing codes that reaches a maximum at *IPSource*=105. This is in good agreement with the linearity criterion. With the noise being always under the threshold, it comes to an trade-off between missing codes plus linearity on the one hand and range on the other hand. The result is a best setting of *IPSource*=90.

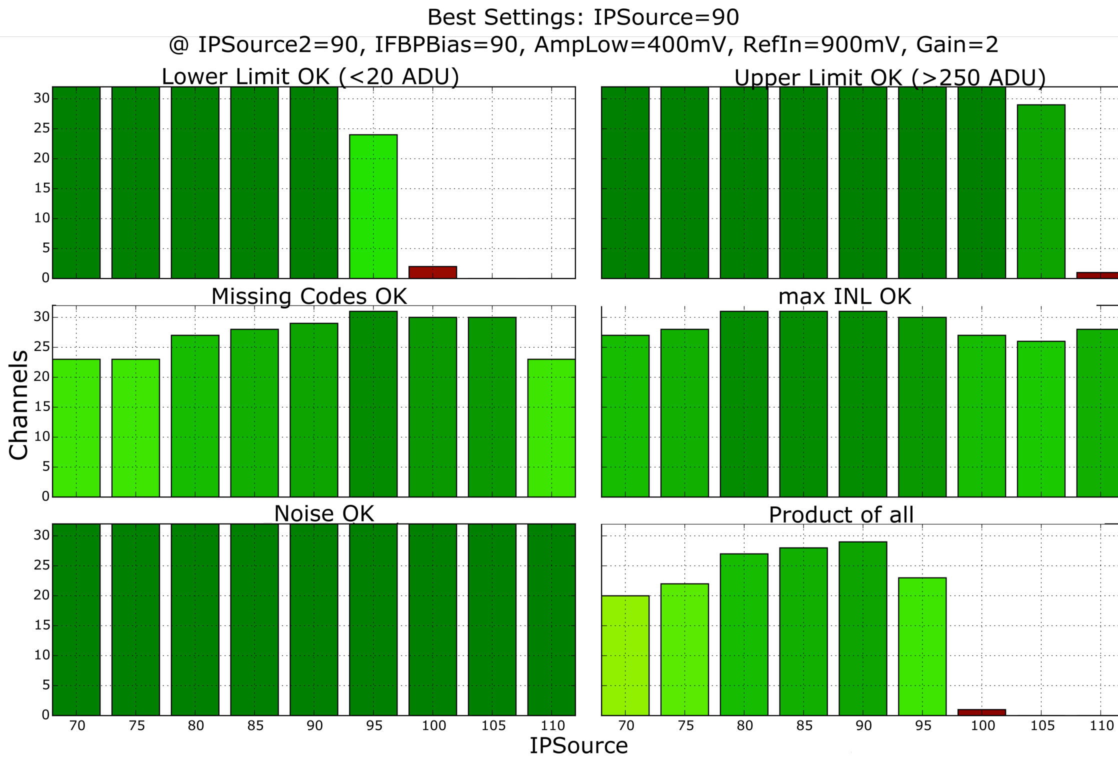


Figure 6.4: Sweep of *IPSource*

IPSource2

Fig. 6.5 provides the same plot for a sweep through *IPSource2*. For a value of 100 none of the 32 channels shows a missing code. This agrees very well with the optima of the other criteria. For that reason *IPSource2* = 100 is defined as new best setting and hence inserted in the following sweep.

IFBPBias

IFBPBias mainly influences the range of the transfer curves, as can be seen in Fig. 6.6. From *IFBPBias* = 85 all channels fulfill the range criterion. Opposed to this, the other criteria are hardly affected. At *IFBPBias*=70 and *IFBPBias*=75, 12.5 % of channels show missing codes, while this error does not occur for higher values. Unfortunately, the first appearance of all channels perfectly working was chosen as best setting due to an error in the automatic testing software. *IFBPBias* = 95, which is centered in

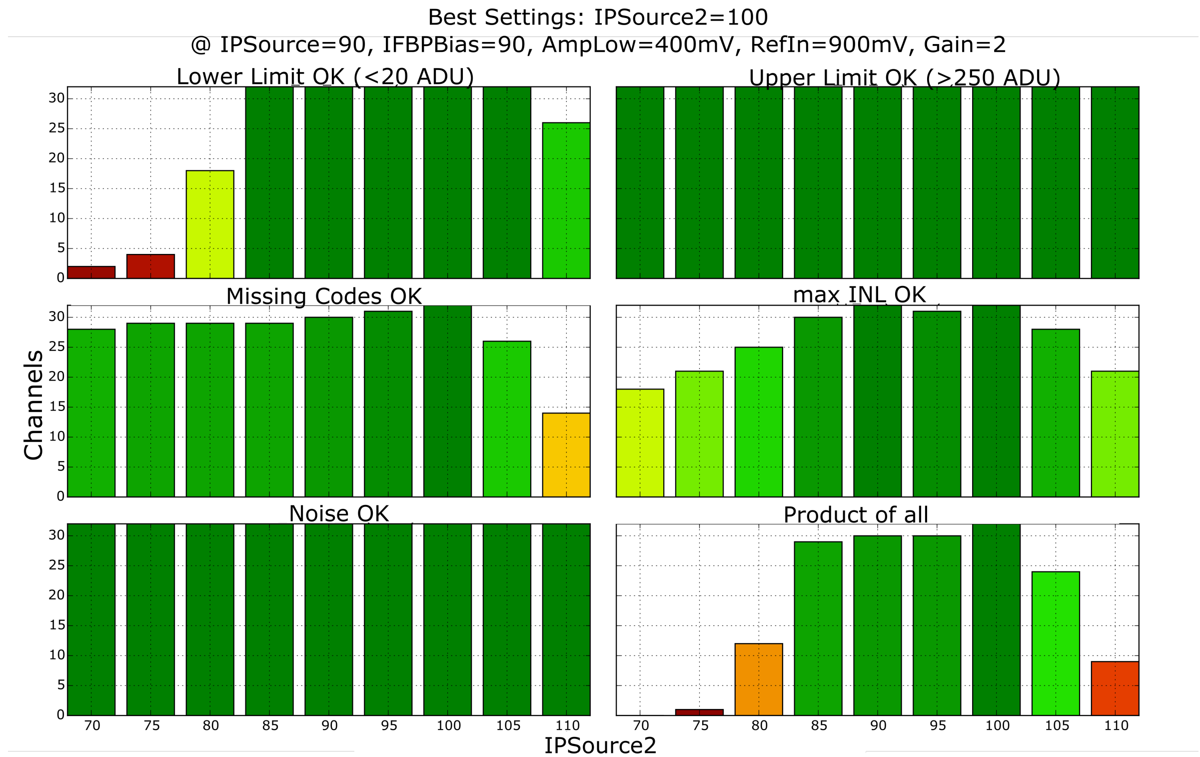


Figure 6.5: Sweep of *IPSource2*

the good region, would have been the better choice. But due to time limitations the sweep could not be repeated. For that reason *IFBPBias*=85 is passed to the next sweep.

6.2.2 Two-Dimensional Sweeps

As already mention, it is the right balance of *IPSource*, *IPSource2* and *IFBPBias* that guarantees faultless function of the ADC. For that reason, the mutual interaction of the parameters will be examined in the following. To this end two of the parameters are sweeped against each other, while the third stays fixed. This is for the simple reason that measurement time would increase exponentially for a three dimensional sweep. Starting from the values found in the one-dimensional sweeps, the parameters are run over a range from -15 to $+15$ in steps of 5. The measurement time of one run amounts to 19.6 h.

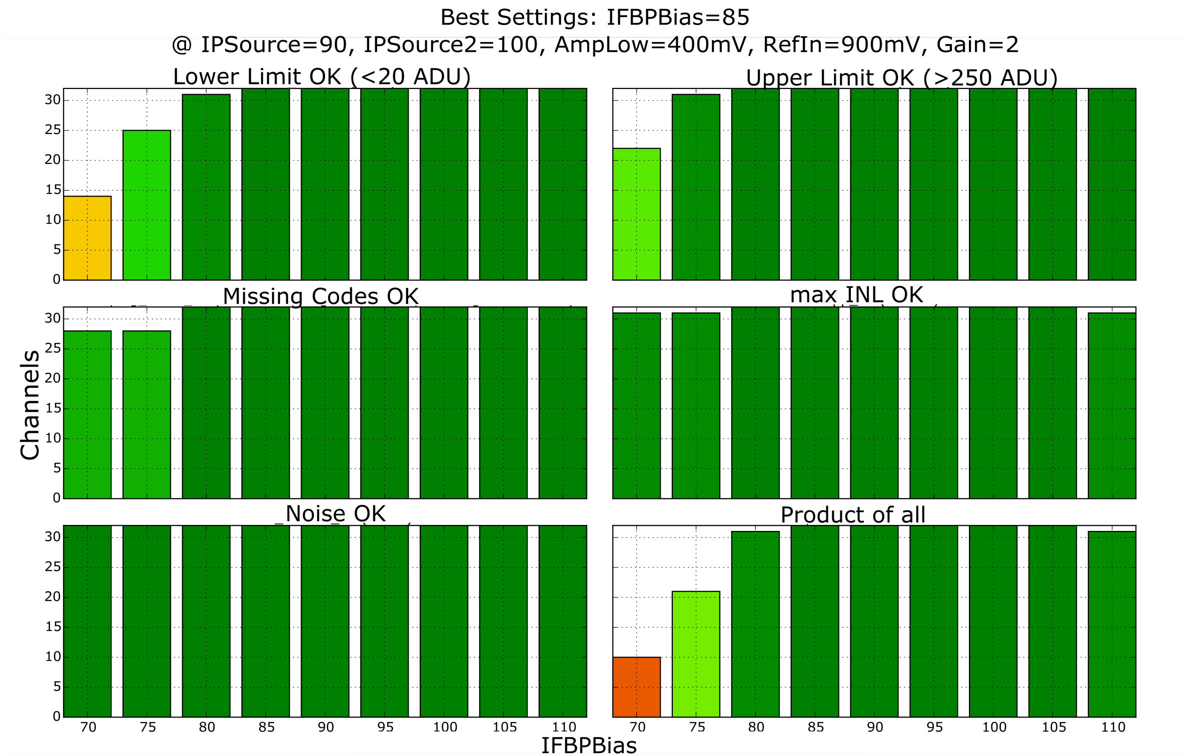


Figure 6.6: Sweep of *IFBPBias*

IPSource – IPSource2

IPSource2 and *IFBPBias* determine the size of the current memory cell, which is the fundamental building block of the ADC. Fig. 6.7 provides an overview plot of the two dimensional sweep, where the x-axis refers to *IFBPBias*, the y-axis to *IPSource2* and the color code to the number of channels without defects.

As expected, the range scales with both parameters. This effect is less pronounced for the missing codes, which occur frequently for *IPSource2* > 100. As in the one dimensional sweep the linearity is depending very weakly on *IFBPBias*, but stronger on *IPSource2*. So far there is no explanation for the appearance of high noise at *IFBPBias*=100 and *IPSource2* ≤ 90. The best region for all criteria is around *IPSource2*=100 and *IFBPBias*=85.

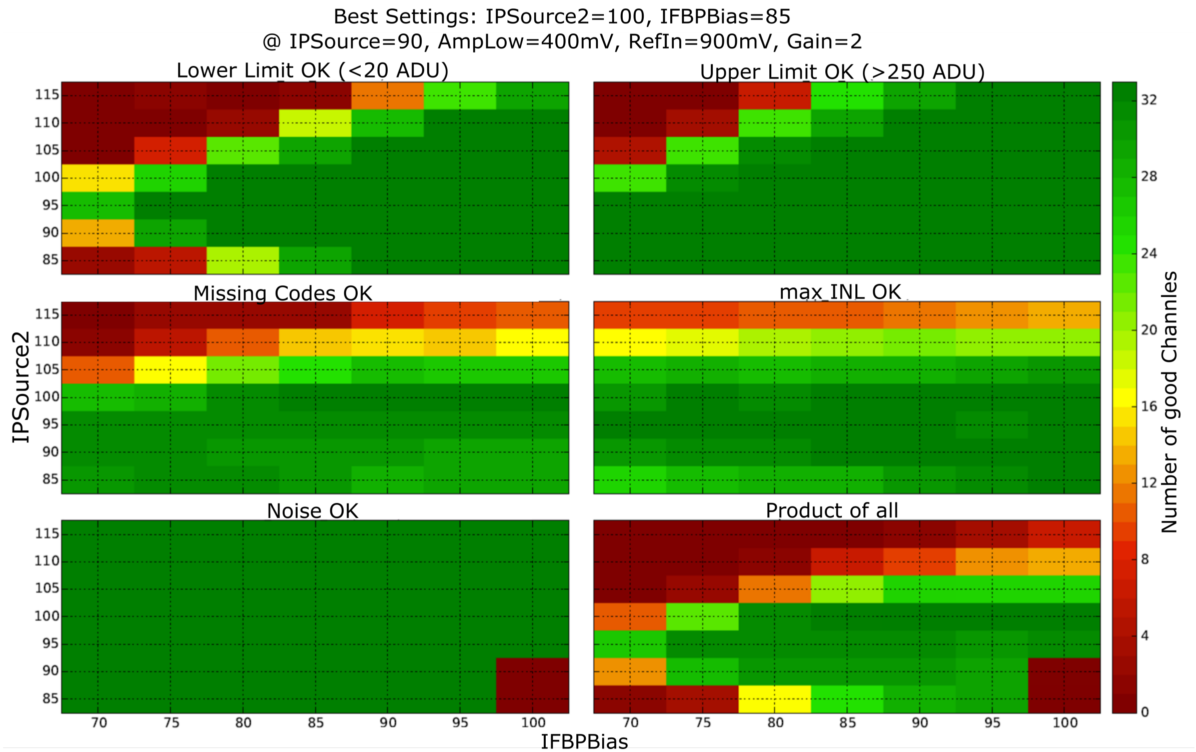


Figure 6.7: Sweep of *IPSource2* against *IFBPBias*. The color code refers to the number of good channels.

IPSource2 – IFBPBias

Fig. 6.8 shows the equivalent sweep for *IPSource* against *IPSource2*. A band of good settings traverses the lower range plot everywhere where the two parameters take similar values. The same characteristic is found in a broader version at the upper range. This dependency is continuing also for missing codes and linearity. Over all *IPSource* and *IPSource2* show a strong influence on each other. The ADCs work best for a slightly higher *IPSource2* than *IPSource*, with their best working point at *IPSource*=95 and *IPSource2*=100.

IPSource – IFBPBias

Fig. 6.9 shows the interference of *IPSource* and *IFBPBias*. Again, the parameters affect the lower range more than the upper range. A large region of settings is

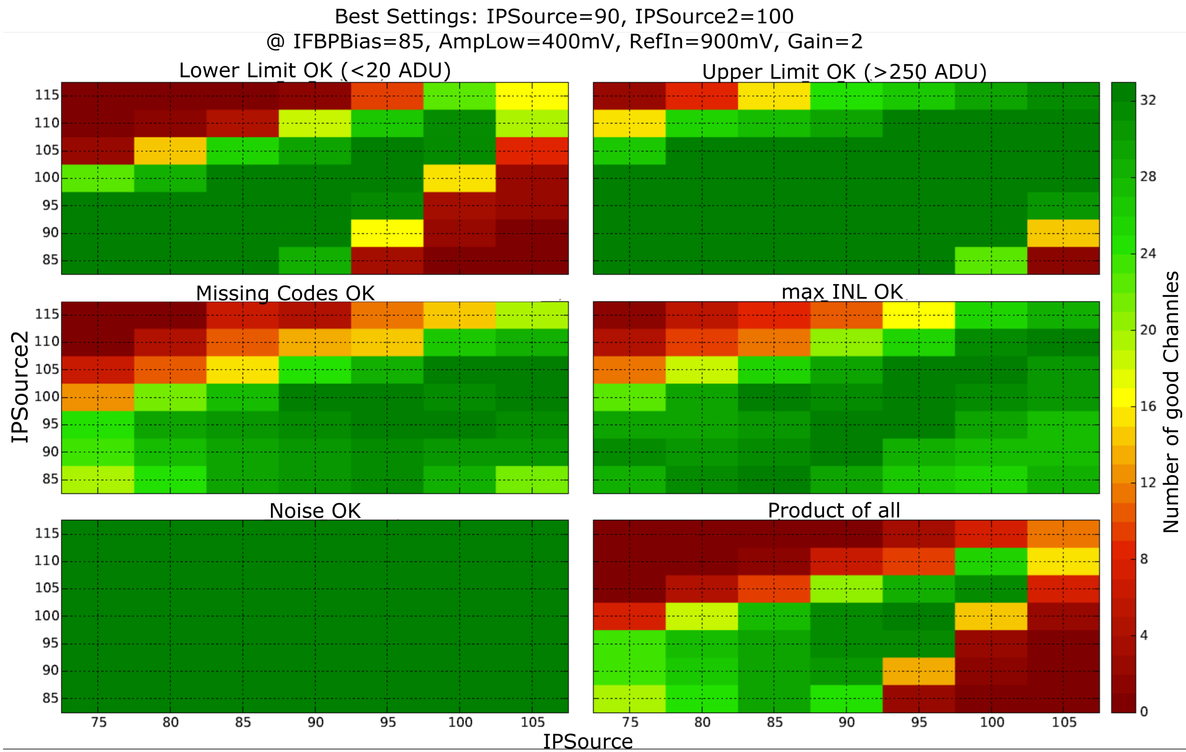


Figure 6.8: Sweep of *IPSource* against *IPSource2*.

free of missing code errors. With this sweep, the optimization of the three parameters is finished. Several combinations reach the full number of working channels. Among them *IPSource*=95, *IPSource2*=100 and *IFBPBias*=95 are chosen as best working point.

6.2.3 Supply Voltages

Besides the parameters optimized above, the supply voltages of the ADC also have a strong influence on the transfer curves. In contrast to the DACs, they are not generated inside the DCD, but feed to the chip from the power supply directly.

AmpLow

AmpLow is the ground voltage of the amplifiers used by the CMCs and comparators (see Chapter 3.1.3). Fig. 6.10 provides an overview of the defects depending on *Am-*

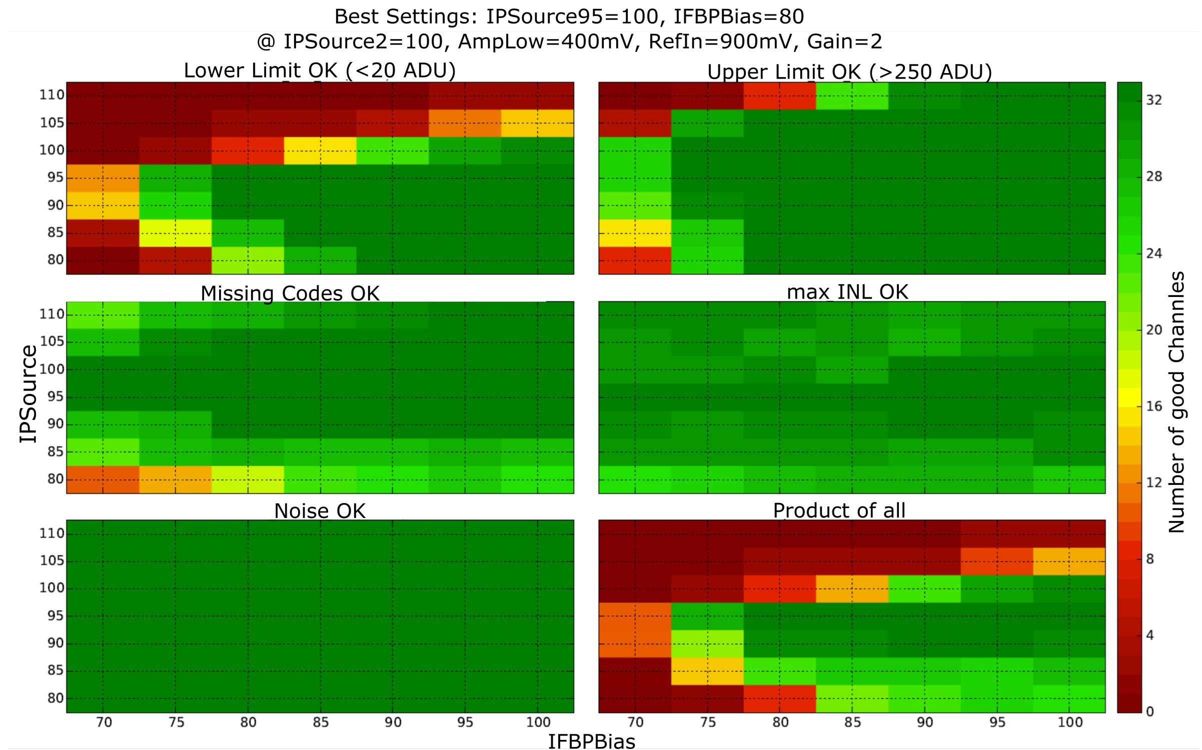


Figure 6.9: Sweep of *IPSource* against *IFBPBias*.

pLow for a range from 200 mV to 600 mV. As expected, the range of the curves is not affected by this parameter. Low *AmpLow* values cause a breakdown of the missing code criterion, while the noise increases strongly at high values. Consequently, the acceptable scope of settings is limited from 300 mV to 450 mV, with an optimum at 400 mV. Thus it is exactly the value used during the preceding sweeps. It is not sure to what extend the optimum of *AmpLow* is depending on the current values of *IPSource*, *IPSource2* and *IFBPBias*. However, former optimizations with different settings produced similar *AmpLow* optima.

RefIn

The same is true for *RefIn*, which is the reference voltage of the ADC. In Fig. 6.11 it is sweeped over 700 mV to 1100 mV. The impact on missing codes is conspicuous here, which reach a sharp maximum at 900 mV. For *RefIn* $<$ 850 mV nonlinearity also increases strongly. The general optimum at 900 mV is consistent with the value used for

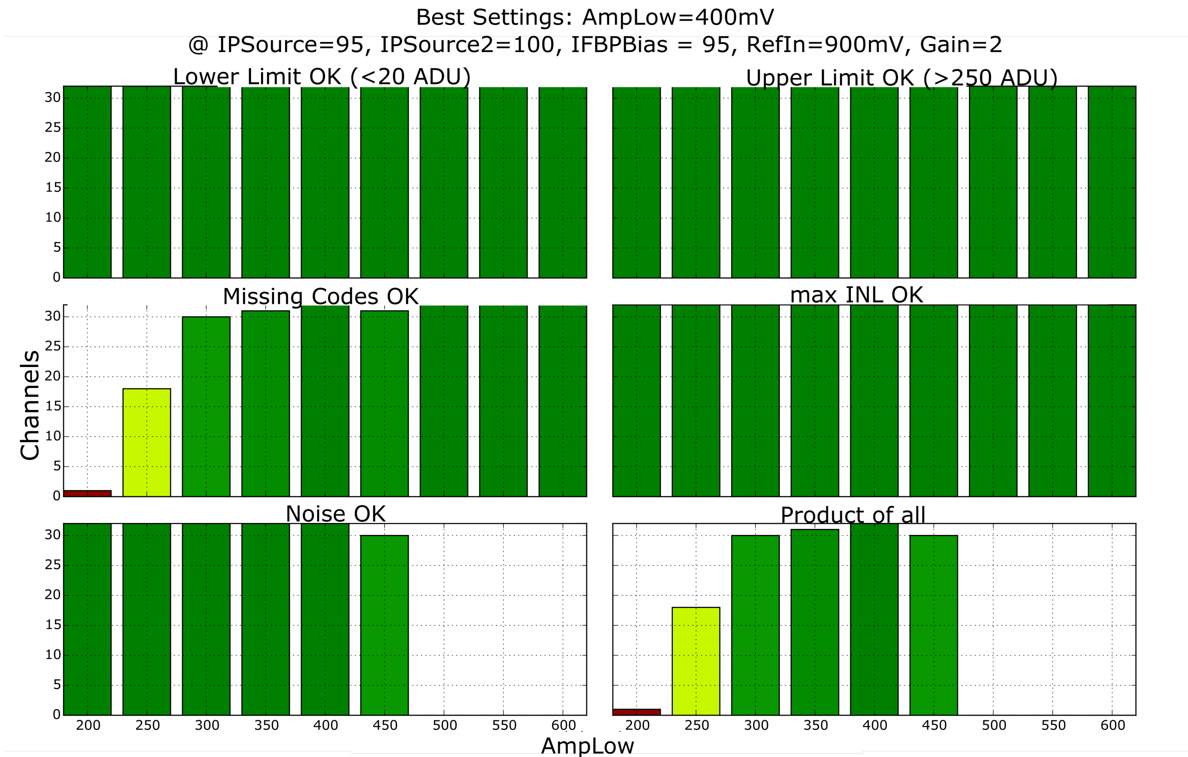


Figure 6.10: Sweep of *AmpLow*

the previous optimization.

6.2.4 Complete Set of Channels

Table 6.3 summarizes the optimization result of the 32 channels, which do not contain any defect. The values of other important DACs are also listed in the table. The gain of the current receiver was set to 2 via parameters *EnHigh*, *En30* and *En60*.

With these settings a scan of all 256 DCD channels was performed. Table 6.4 lists the percentage of the different defects. A range error was found at four channels. When looking at the detailed transfer curves of the affected channels, it turned out that they are shifted out of the dynamic range so they can not reach the full range. Since these are the adjacent channel numbers 58 to 61, a deviation at this position must be causing the offset. The offset can either originate inside the DCD or in the pixel matrix. It should be

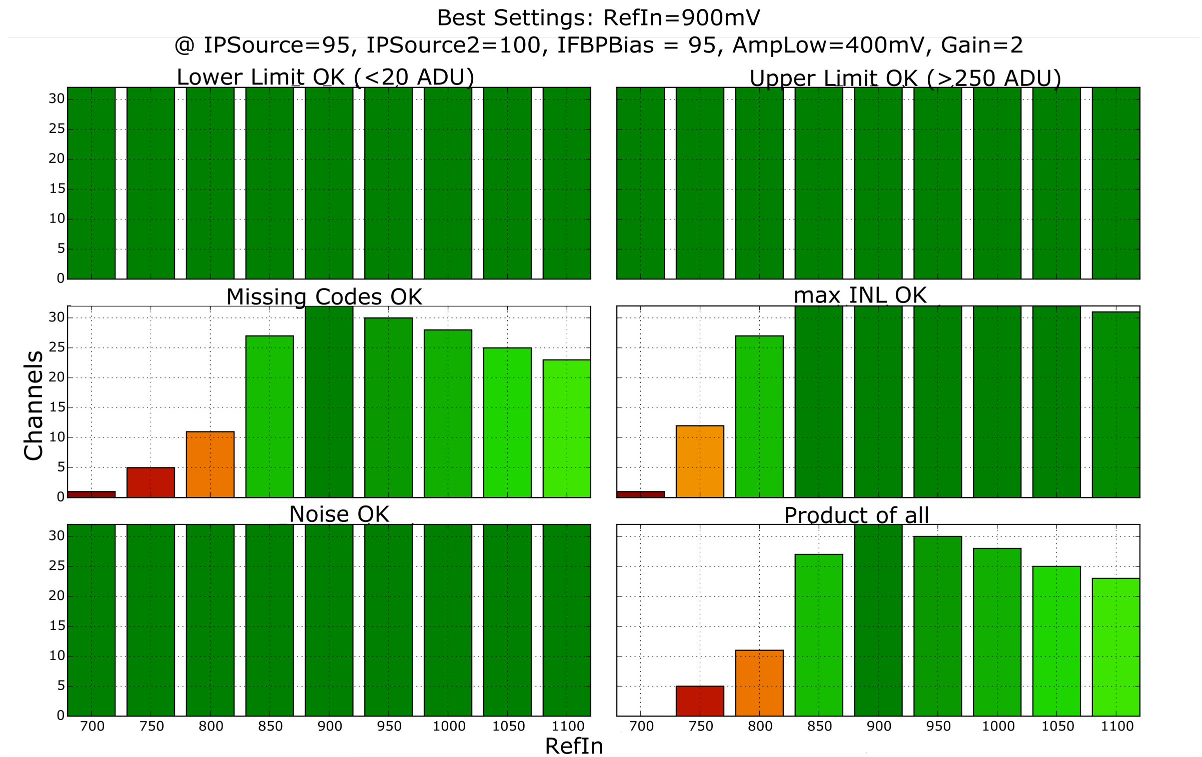


Figure 6.11: Sweep of *RefIn*

easy to fix this defects with the 2 bit offset correction, which was not ready for use during this scan.

16 channels are affected by missing codes, of which four are caused by positive offsets and twelve by negative offsets. The high comparator is involved at two channels, the low comparator at 14 channels. The majority of the missing codes is related to conversion-stage 0. Stage 1 is affected two times, stage 2 and stage 3 one time each. Lower stages did not cause missing codes.

The appearance of positive as well as negative offsets is a strong indicator of intrinsic transistor offsets, whereas wrong settings would cause only one kind of offset. As expected, the offsets have the most effect on the input stage 0, while they are better compensated at lower stages. So far there is no explanation for the increased incidence of affected low comparators. A correlation of the appearance of missing codes and the channel position on the chip was not found.

None of the channels showed a high noise nor a decreased linearity defect. Channel

optimization parameter	optimal value
IPSource	95
IPSource2	100
IFBPBias	95
AmpLow	400 mV
RefIn	900 mV
other ADC settings	**value**
IAmpBias	45
IFBNCasc	0
IFBRef	64
INMOS	120
IPDel	127
IPMOS	120
IPSourceCasc	64
RefNWELL	64
VNDel	127
VNSubIn	6
VNSubOut	0
IPMOS	30
IPDel	30
INDel	30
VNSubIn	13
VNSubOut	0
gain settings	**value**
EnHigh	1
En30	1
En60	0

Table 6.3: Optimization results for the internal current source plus used values of important ADC and gain settings.

number 188 was broken, not giving any signal. In total 21 of the 256 ADC channels of DCD4 of module W30 OB2 had a defect.

defect type	affected channels
limited range	1.6 %
missing codes	6.25 %
nonlinearity	0 %
high noise	0 %
dead channel	0.4 %
product of all	8.2 %
missing codes	thereof
positive offset	25 %
negative offset	75 %
HI comparator	12.5 %
LO comparator	87.5 %
Stage 0	75 %
Stage 1	12.5 %
Stage 2	6.25 %
Stage 3	6.25 %

Table 6.4: Percentage of defective channels of all 256 ADC channels of module W30 OB2 DCD4. The subtypes of missing codes are specified in detail.

6.3 Relation to Physics

In conclusion, the question remains in which way the conversion errors affect the physical performance of the detector.

6.3.1 Calibration

At first, a calibration of the system is required. In order to generate a test beam onto the detector matrix, a Cd-109 source is used, creating an average photone energy of $E_{photon} = 22.54\,\mathrm{keV}$. Such a photon generates approximately 6000 electron-hole pairs in silicone, which is in good agreement to the number of electrons generated by a Minimum Ionizing Particle (MIP) in a 75 µm thick silicone sensor. A detailed description of the calibration procedure is provided by [36]. According to this, the internal amplification g_q of the DEPFET sensors is defined by:

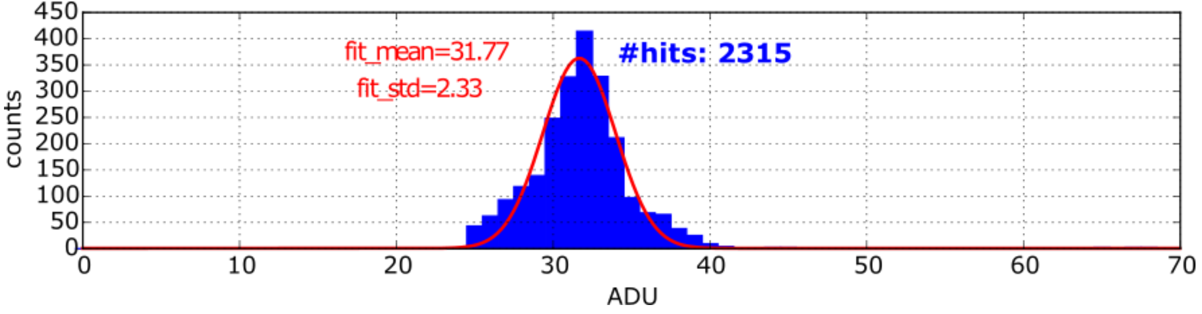


Figure 6.12: Histogram of photon hits from a Cd-109 source on a PXD9 Pilot matrix at a gate voltage of −1000 mV. The Gaussian fit on a total number of 2315 hits returns a mean of 31.77 ADU with a standard deviation of 2.33 ADU.

$$g_q = ADU_{mean} \cdot ADC_{gain} \cdot \frac{E_{e,h}}{E_{photon}} \tag{6.1}$$

The average energy required for the creation of an electron-hole pair in silicone is $E_{e,h} = 3.60\,\text{eV}$ at 300 Kelvin [37]. The mean ADU value caused by a photon of the Cd-109 source $ADU_{mean} = 31.77\,\text{ADU}$ was calculated by a Gaussian fit of 2315 single events measured on a PXD9 Pilot module (see Fig. 6.12). At the same settings, the median gain was measured as $ADC_{gain} = 83.99\,\text{nA/ADU}$. This was done using the internal current source of the DCD on 32 channels. The external gate voltage, which is crucial for the DEPFET gain, was set to −1000 mV (compare to Fig. 4.10). This results in an internal gain of the DEPFET sensor of $g_q = 429.7\,\text{pA/e}^-$.

6.3.2 Results

Table 6.5 summarizes the median values of the 256 channels of the optimization with the internal current source. The median ADC gain, which is not to be confused with the gain setting of the current receiver, was measured as 86.61 nA. The difference compared to the value used in the calibration is due to a different *IPSource* setting. Thus, a LSB corresponds to ∼202 electrons in the internal gate. The median range of the channels is 249.1 ADU, which gives 20.7 µA. The median noise of 0.70 ADU complies to ∼141 electrons. The median of the maximum INL is 8.28 ADU and corresponds to 1672 electrons.

First of all, a signal-to-noise ratio of ∼30 can be calculated from the values. This, however, is not including other defects than noise. The main impact is caused by linearity deviations, which may strongly reduce the signal-to-noise ratio. The corresponding part of the DEPFET and of the ADC is not understood so far. The missing code defect typically only affects 1 to 3 ADU at a single position. In addition, the number of defective channels is in the low one-digit percent range. Consequently, the missing code errors can be assumed to not strongly influence the performance of the detector.

median gain	median range	median noise	median max INL
86.61 nA/ADU	249.1 ADU	0.70 ADU	8.28 ADU

Table 6.5: Median values of the 256 optimized channels.

6.4 Fast Optimization with the DEPFET Current Source

The optimization by the internal current source clearly defines an optimal sector of the parameters. Nonetheless, this method is not feasible for the adjustment of all 160 chips of the PXD due to time constraints. The measurement period of the full optimization with the internal current source lasted ∼80 h. When using the DEPFET current source, the time period for characterizing all 1000 ADC channels of the four DCDs of a half ladder can be reduced from 12.5 h to ∼8 min (see Chapter 4.3.3). Yet, a strong deterioration in linearity must be accepted. However, for settings close to the optimal working point, where linearity has been proved, the DEPFET current source is well fitting for individual adjustment. All of the three other criteria – noise, range and missing codes – can be examined precisely with this current source.

A three-dimensional sweep of the parameters *IPSource*, *IPSource2* and *IFBPBias* was performed in range from ±5 around the optimal working point. Table 6.6 summarizes the best working points with the number of defects for three ASIC pairs of module W30 OB2. Unfortunately, DHP3 lost the highspeed data connection during the measurement.

The number of limited range errors lies between 3.1 % and 7.8 %. The missing codes for the DCD4 were further reduced to only 0.8 %. All channels fulfilled the noise criterion. The gain setting of the current receiver did not significantly affect the defect numbers. The optimal working points differ among the DCDs.

	optimal working point			percentage of defects		
	ipsource	ipsource2	ifbpbias	limited range	missing codes	high noise
Gain 1						
DCD1	100	95	100	5.5 %	7.8 %	0 %
DCD2	100	95	90	7.4 %	5.9 %	0 %
DCD3	–	–	–	–	–	–
DCD4	95	95	90	3.1 %	0.8 %	0 %
Gain 2						
DCD1	100	95	100	5.5 %	8.2 %	0 %
DCD2	100	95	90	7.8 %	5.9 %	0 %
DCD3	–	–	–	–	–	–
DCD4	95	95	90	3.1 %	0.8 %	0 %

Table 6.6: Optimization result and percentage of defective channels of the DCDs of module W30 OB2 recorded with the DEPFET current source. This was done for two different gain settings of the current receiver.

7 Conclusion

The Drain Current Digitizer of the Belle II pixel detector works faultlessly for the most part. Nevertheless, version B4 pipeline contains a small number of ADC channels showing conversion errors. These errors can be deduced to different origins, distinguishable in between analog and digital defects. Digital errors result from transmission losses between the DCD and the DHP, while analog errors arise inside the ADC channels.

Within the analog defects, the so-called missing code error is of particular interest. This error originates from a statistical variation of transistors causing a discrepancy between the transconductor of the current memory cell and that of the comparator. This effects an offset current distorting the conversion result. In addition, the missing code error can be described in a theoretical model of the conversion algorithm, where offsets are added to certain conversion stages. In this way, 32 different cases of missing codes were identified differing in the sign of the offset, the affected comparator and the stage of appearance. The correctness of the theory was confirmed by simulation, which was able to reproduce all measured missing codes in full agreement.

A classification of defects was defined. Besides missing code errors, this includes limited range, nonlinearity and high noise defects. Digital errors are listed separately. The classification was used for a characterization of the ADC channels. An appropriate tool for this task are the so-called transfer curves. Thereby, a test current is applied to the channels, while the transferred curve is recorded. Defects appear clearly in the INL and DNL function of the transferred curve.

The number of channels containing defects can be reduced by an adjustment of settings. For this purpose the DCD offers a number of parameters, of which *IPSorce*, *IPSorce2* and

IFBPBias are the ones with the largest influence. Since defects are distributed statistically, every of the 160 DCDs of the PXD has to be adjusted individually. The adjustment is performed as an iterative optimization of settings. Due to the high degree of interdependence among the parameters, multidimensional sweeps over them are necessary.

In an exemplary optimization of DCD4 on PXD9 Pilot module W30 OB2, the number of channels containing missing codes was reduced to 6.25 %. The over all number of channels working faultlessly amounted to 91.8 %.

The former optimization was performed using the internal current source of the DCD, which is very time consuming. In order to accelerate the adjustment process, a new method utilizing the DEPFET sensors as test current source was developed. In a fast optimization which lasted $\sim$1 h, all four DCDs of a half ladder were optimized. This resulted in an total number of 90 % working channels, where the number of channels with missing code defects was 8 %.

In this work it was shown how a full optimization of all DCDs of a half ladder can be performed within limited time. Moreover, the full functionality of the automatic optimization routine has been demonstrated. The results of this adjustment influenced the development of the next DCD version. Nevertheless, there still remain several challenges.

So far the ASICs were operated on a reduced clock speed of 62.5 MHz during the optimization in order to circumvent transmission problems. For that reason, new versions of the DHP and the DCD are in development. They will overcome this restriction and guarantee stable inter-chip communication. Thus, an optimization at the full clock frequency of 76.23 MHz will become possible.

Moreover the new DCD version will contain further improvements regarding the missing code problem. Several subversions will be manufactured, all containing antenna diodes and dummy structures to minimize the comparator offsets. In addition, another subversion will include larger ADC transistors as well as a uniform orientation for better transistor matching [38]. The optimization routine can then be applied in order to deduce if the improvements reduce the number of missing codes.

During the Belle II experiment the ASICs will be exposed to high radiation doses. As a consequence, readjustment of settings is needed to compensate radiation damages. A test beam is planned, where the optimization routine can demonstrate if it is prepared for this task.

Finally, the ADC optimization routine developed in this work will be employed for the characterization and the adjustment of the 160 DCD chips, which will be installed in the Pixel Detector of the Belle II experiment.

List of Abbreviations

ADC Analog-to-Digital Converter 11
ASIC Application-Specific Integrated Circuit 10
CMC Current Memory Cell 16
DAC Digital-to-Analog Converter Unit 23
DCD Drain Current Digitizer 11
DEPFET Depleted p-channel Field-Effect Transistor 7
DHP Data Handling Processor 11
DNL Differential Non-Linearity 44
INL Integral Non-Linearity 43
JTAG Joint Test Action Group Standard 23
LSB Least Significant Bit 30
MIP Minimum Ionizing Particle 82
MOS Metal-Oxide Semiconductor 19
MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor 39
MSB Most Significant Bit 60
NMOS N-channel Metal-Oxide Semiconductor 21
PMOS P-channel Metal-Oxide Semiconductor 21
PXD Pixel Detector 13
SMU Source Meter/Measuring Unit 37

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Erklärung

Hiermit versichere ich, dass ich die vorliegende Arbeit selbstständig verfasst und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe, dass alle Stellen der Arbeit, die wörtlich oder sinngemäß aus anderen Quellen übernommen wurden, als solche kenntlich gemacht und dass die Arbeit in gleicher oder ähnlicher Form noch keiner Prüfungsbehörde vorgelegt wurde.

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