Universität Bonn

Physikalisches Institut

Data Handling Processor and Signal Transmission in the Belle II DEPFET Pixel Detector

Leonard Germic

The high precision measurements at the B factories have generated a new insight of the Standard Model with respect to CP violation and delivered higher constraints on the Standard Model parameters, i.e. CKM matrix. The upgrade of the asymmetric electron-positron collider KEKB in Japan to SuperKEKB introduces new challenges as the luminosity increases by a factor 40. The high luminosity forces the inclusion of a highly segmented detector, i.e. pixel detector, close to the interaction point, in order to improve the vertex resolution. The result is a complete new detector, Belle II. Due to the integrated pixel sub-detector the total data rate of Belle II increases 50 fold. The newly introduced pixel sub-detector generates roughly 95% of the total data. Thus online data reduction is inevitable to cope with the amount of data sent to the back-end of the detector system. This thesis investigates the capability of the on-module ASIC to cope with the high data rates, i.e. 1.6 Gbps, and proves that the transmission line system of the pixel detector is sufficiently designed to guarantee high signal integrity over approx. 3 m of transmission. The Data Handling Processor on the pixel modules is designed to handle, reduce the pixel data generated in the pixel array of the module and to transmit them to the back-end system.

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Data Handling Processor and Signal Transmission in the Belle II DEPFET Pixel Detector

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CHAPTER 1

Introduction and Motivation

To give a meaningful perspective of humans on earth, humans interpret the nature as a logic-based system of interactions of objects. Thus nature obeys rules and laws such that humans, as intelligent beings, are capable of understanding the reason why we are here and our determination. This is a very anthropological way of interpreting our motivation of conducting physics experiments. Since Archimedes and his famous sentence 'Heureka!' when he understood the behaviour of objects floating in water, phenomena give rise to curiosity. Ever since, through the fall experiments by Galileo Galilei at the Pisa Tower[1], the dipole experiment by Heinrich Hertz to validate James Clerk Maxwells theoretical proposed field equations up to the discovery of radioactivity by Pierre and Marie Curie in the early 20^{th} century, many experiments have been conducted and lastly four fundamental interactions were discovered. These four fundamental interactions are the gravitational, electromagnetic, weak and strong force. The order of the four forces indicates also the time line of discoveries. The state-of-the-art model of the fundamental interactions, excluding gravity, is the Standard Model (SM) of particle physics. It incorporates the electromagnetic, weak and strong force. The electromagnetic and weak force are unified to the electro-weak force. The attempt to unify all fundamental forces is the greatest challenge in modern physics.

1.1 Standard Model of Particle Physics

The SM particles are subdivided into leptons, quarks and gauge bosons, that mediate the fundamental forces between the leptons and quarks, completed by the Higgs boson responsible for mass generation. The matter particles, i.e. fermions consisting of leptons and quarks, are grouped in three families (or generations) with increasing mass with respect to increasing family, namely (up, down), (charm, strange) and (bottom, top). Leptons are grouped as (electron, electron-neutrino), (muon, muon-neutrino) and (tau, tau-neutrino). All SM particles have counterparts called anti-particles. They are copies of the 'ordinary' particles with equal mass but opposite additive quantum numbers, e.g. electric or colour charge and lepton number, etc. These particles are called Dirac particels. Particles with additive quantum number equal to zero are their own anti-particle and called Majorana particles. The gauge bosons mediating the electromagnetic, weak and strong forces are spin 1 particles, therefore also called vector bosons. The vector bosons are the photon γ, $W^{\pm}/Z$ and gluon for the electromagnetic, weak and strong force, respectively. The photon is charge- and massless. Being without electric charge it does not interact with other photons. The gluon has colour charge, like the quarks, and thus interacts with other glouns.

[1] Most likely just a popular myth

The Higgs boson has spin 0 (scalar boson) and is the excitation of the Higgs field [1]. The weak force mediates the transition through quark generations, whose probability amplitudes are represented by the entries of the Cabibbo-Kobayashi-Maskawa (CKM) matrix for quark mixing [2].[2][3] The quark-mixing is the fundamental principal causing radioactive decays. In the weak sector the SM introduces charge-parity (CP) violation by an irreducible complex phase in the CKM matrix. CP-violation corresponds to an asymmetry of the decays rates of particles and their anti-particle within the same decay channel. This means, if a particle is decaying by a transition $|p_1\rangle \rightarrow |p_2\rangle$ the exchange of the particle by its anti-particle should have the same probability to do so $|\bar{p_1}\rangle \rightarrow |\bar{p_2}\rangle$. Direct CP-violation has been observed at the BaBar (SLAC [6]) and Belle (KEK [7]) experiment in the B sector.

Limitations of the SM As the SM describes the interaction of fundamental particles, it is known to be incomplete. There are several unexplained phenomena like

- Gravitation is not included in the SM.
- Dark matter and dark energy is not described in the SM. Roughly 95% of the observed universe is made up by dark matter and dark energy [8].
- Only left-handed neutrinos are observed. If neutrinos have mass m_ν (Dirac-like particles), right-handed neutrinos have to be observed too. Question is, if neutrinos are Dirac-like particles (massive) or Majorana-like particles (massless).
- Due to the Higgs mechanism masses of the fermions m_f are proportional to the expectation value of the shift of the vacuum f, $m_f = g_Y \cdot f$. There is no explanation of the origin of the Yukawa coupling constants g_y.
- The asymmetry of matter and anti-matter cannot be explained by the CP violation. Since no structures made out of anti-matter is observed, the question arise; why only matter and no anti-matter is present in our present universe?

1.2 B factories

In order to probe the model parameters of the SM model, e.g. CP-violation, besides of searching for new, exotic, massive particles at high energies, experiments with high statistics are needed to reduce the statistical error of the measurements. These two complementary approaches are called 'High-Energy-Frontier' and 'High-Luminosity-Frontier', respectivelly. The ATLAS experiment at the LHC (CERN, Switzerland) is chasing for the high-energy-frontier with center of mass energies of up to 14 TeV (14×10^{12} eV) in order to generate new massive, exotic, short lived particles. This approach led to the discovery of the Higgs boson in the year 2012[9][10]. With the Higgs boson the last known, theoretically predicted, piece of the SM has been found.[4] On the other hand the KEKB accelerator (KEK, Japan) has

[2] Cabibbo described first in 1963 the quark mixing within two generations (only up, down and strange quark has been discovered by that time) [3]. Later in 1973, Kobayashi and Maskawa generalised the quark mixing to three generations. The work of Kobayashi and Maskawa has been awarded with the half of the Nobel Prize in 2008. However, Cabibbo has been forgotten for unknown reason.

[3] In analogy to the CKM matrix for quark mixing, the Pontecorvo-Maki-Nakagawa-Sakata matrix represents the leptonic mixing [4][5].

[4] Peter W. Higgs and François Englert (with his deceased colleague Robert Brout) formulated in 1964 independently a theory of how particles acquire mass. Nowadays referred to as 'Higgs mechanism'. Higgs and Englert have been awarded with the Nobel Prize in 2013.

been used as a B-factory to pursue the high-luminosity-frontier with the Belle detector. B-factories are specially designed high luminosity colliders to generate and probe B mesons at the $\Upsilon(4S)$ resonance. B mesons consist of one heavy Bottom quark (third family) plus another flavoured quark.

CP-violation measurements The 'golden decay channel' for precise measurements and determination of CP-violation is

$$\mathrm{B}^0 \to \mathrm{J}/\psi \mathrm{K}^0_s \quad \text{and} \quad \bar{\mathrm{B}}^0 \to \mathrm{J}/\psi \mathrm{K}^0_s$$

where $\bar{\mathrm{B}}$ is the anti-particle of B.[5] Due to the B-meson mixing, B-$\bar{\mathrm{B}}$ mix with a characteristic frequency propotrional to the mass difference Δm of the heavy and light mass eigenstates [11]. Pairs of B-$\bar{\mathrm{B}}$ mesons are entangled in a coherent quantum state. Figure 1.1 shows the decays of B and $\bar{\mathrm{B}}$ with B-$\bar{\mathrm{B}}$ mixing for direct CP-violation measurements. The mixing amplitudes V can be determined by the decay rate. The branching ratio of $\mathrm{J}/\psi\mathrm{K}^0_\mathrm{S}$ in the final state with quarks $\mathrm{J}/\psi \to q\bar{q}$ and leptons $\mathrm{J}/\psi \to l\bar{l}$ is 0.04% and 12% respectively [12]. Figure 1.1 shows the direct decay of a $\bar{B}$ meson (a) and the decay via B-$\bar{\mathrm{B}}$ mixing (b).

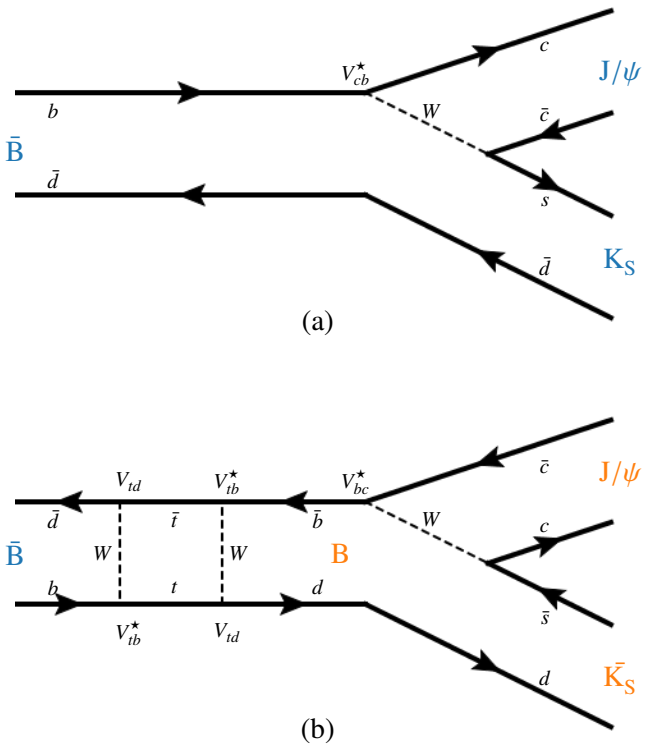


Figure 1.1: Feynman diagrams of B meson decay (a) and additional B-$\bar{\mathrm{B}}$ mixing (b). The box diagram in (b), i.e. here mixing via top quark t and W boson, can be rotated by 90 degree to obtain an additional valid diagram. Vertices of quark propagators represent mixing amplitudes V_{xy} with x and y being quark flavours. Time line from left to right.

[5] Henceforth B^0 will be denoted as B.

1.3 SuperKEKB and Belle II

For the next generation high-luminosity collider, the ring accelerator KEKB in the TRISTAN storage accelerator tunnel is upgraded to SuperKEKB. The goal is to achieve 40 times higher peak-luminosity as its predecessor, i.e. $8 \times 10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ that corresponds to 50 times more data collected compared to the collection within the runtime of the Belle experiment. SuperKEKB is a asymmetric ring collider with two acceleration rings for electron e^- and positron e^+, respectively. The center of mass energy is at the $\Upsilon(4S)$ ($E_{cm} = 10.58\,\mathrm{GeV}$) resonance to purely generate B mesons. In order to increase the desired luminosity the design of the focusing system has been changed. SuperKEKB uses the nano-beam approach to decrease the cross section and therefore increase the luminosity. The cross section of the focused electron-positron beam measures only $48\,\mathrm{nm} \times 63\,\mathrm{nm}$ at the interaction point (IP) [13]. Due to the stronger focusing the beam current increases by a factor of 2 [14]. The SuperKEKB facility with the Belle II detector is shown in figure 1.2 (left). The change of the beam geometry is shown in figure 1.2 (right).

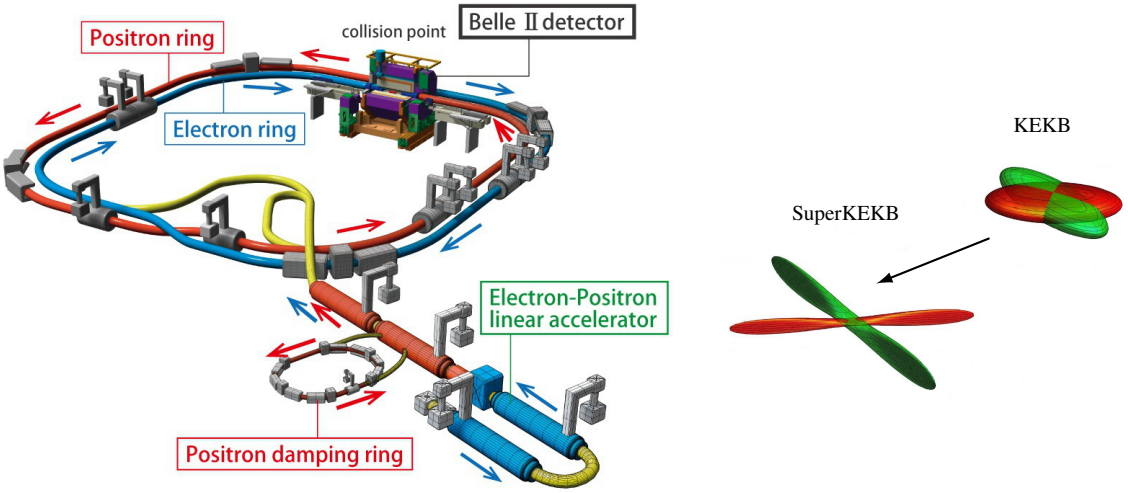


Figure 1.2: SuperKEKB facility with its linear accelerator and the two storage rings (left). The Belle II detector is placed at the interaction point where the electron-positron beams are focused and intersect. The beam geometry has changed and the beam current increased by a factor of two to achieve the higher luminosity (right). Beam geometry to scale.

Since the nanobeam approach increases the scattering of particles in the IP the beam current asymmetry has been decreased for SuperKEKB to avoid higher peak energies of the beams. Touschek background, i.e. Coulomb scattering of electrons and positrons inside the colliding bunches, increases with the fourth power of the particle energy and is the dominant effect of the beam life time [15]. The higher luminosity implies higher event rate, higher background and thus requires an new detector. Higher event rate introduces:

- higher trigger rates
- tighter event window → fast read-out

Additionally higher background implies:

- higher radiation damage

- more hits and thus higher detector occupancy
- fake hits and pile-up (multiple hits not able to time resolve)

The Belle II detector consists of several sub detectors shown in figure 1.3. The sub detectors are arranged in a barrel-like structure around the Beam pipe with the IP in the centre. The smallest entity directly wrapping the beam pipe is the vertex detector (VXD) which consists of two layers of pixelated DEPFET sensors Pixel Detector (PXD) and four layers of double sided P-N-silicon strip sensors (SVD). Tracks reconstructed by data acquired by the SVD are extrapolated towards the PXD to define Regions Of Interest (ROI). This reduces the effective data to be read out from the PXD, see section 2. The VXD is surrounded by the Central Drift Chamber (CDC). The CDC is composed of more than $55,000$ wires in 56 cylindrical arranged layers around the VXD. The gas filled is a mixture of low Z helium and ethane to exploit the unique $^{dE}/_{dx}$ characteristic of elementary particle. This particle identification is complemented with charged particle momentum reconstruction. Additional particle identification is done in the Time Of Propagation (TOP) detector and in the Aerogel Ring Imaging Cherenkov detector (ARICH). TOP consists of segmented quartz crystals with one coated side (high reflectivity) and an array of micro photo-multiplier on the other side. The Cherenkov light-cone emitted by particles, which move faster than the speed of light in the crystal, is reflected within the crystal and sampled by the photo-multiplier. The angle of the light-cone can be related to the propagation time within the crystal. ARICH consists of segmented parts with aerogel blocks of two different refraction indices. The Cherenkov light-cone of both blocks overlap at the position of the read-out plane. Spatial sensitive avalanche photo diodes detect the Cherenkov rings. The Electromagnetic Calorimeter (ECAL) is built out of scintillators (CsI(Tl)) with photo-multiplier read-out. Electro-magnetically interacting particles deposit energy in the scintillators resulting in $e^- - e^+$-showers. The 1.5 T–super-conductive solenoid magnet outside of the ECAL bend of the charged particles within the volume. The K_L- Muon detector (KLM) is the outer shell of the Belle II detector.

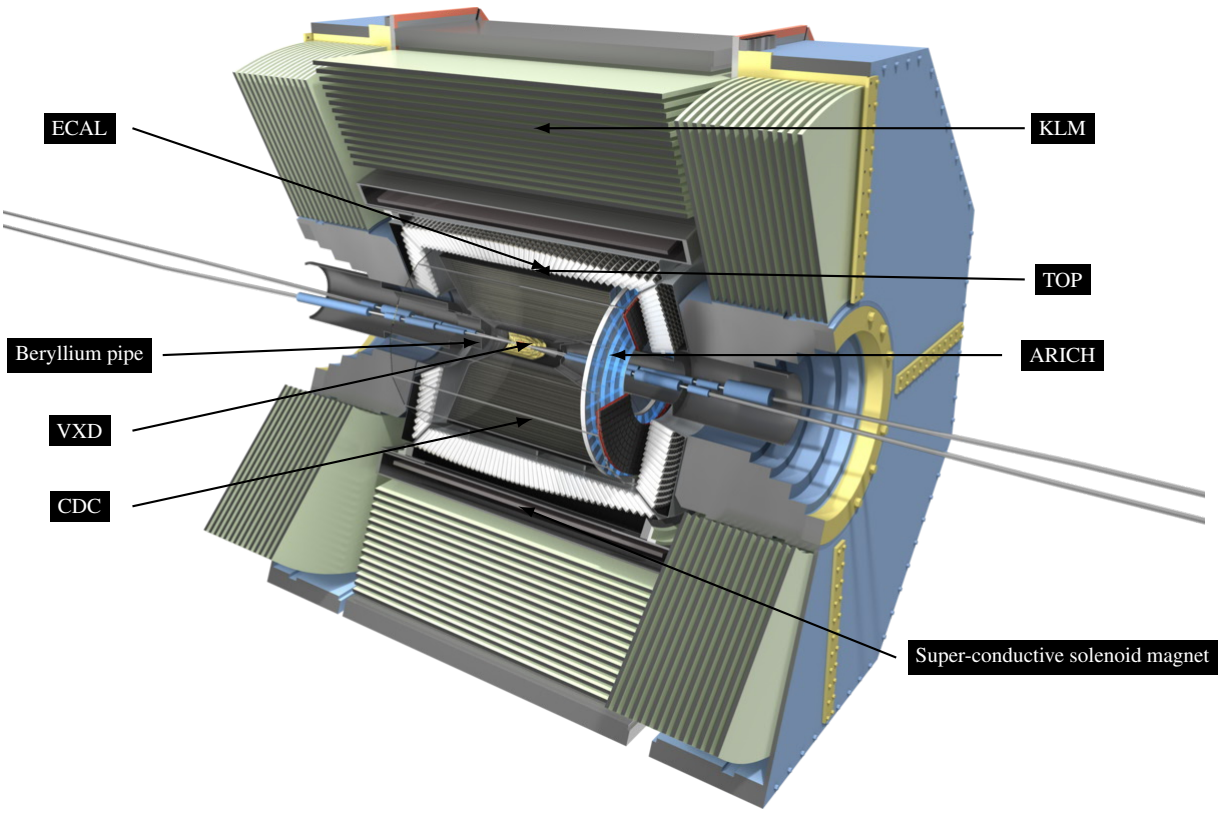


Figure 1.3: Cross section of the barrel-like structure of the Belle II detector with its sub-detectors. The beam pipe (centre) is surrounded by the vertex detector (VXD) and the central drift chamber (CDC). The electro-magnetic calorimeter (ECAL) and the time-of-propagation detector are arranged cylindrically around the vertex detector. The Cherenkov detector (ARICH) covers the end cap region. Covering all the sub detectors, the super-conductive solenoid generates a homogeneous magnetic field. The kaon/muon (KLM) detector is the largest sub detector.

CHAPTER 2

The Pixel Detector of the Belle II Experiment

The VXD consists of six layers of sensors arranged in a barrel like structure around the IP. The services, e.g. powering and data cables, are attached at the two end sides of the detector. The PXD consists of 40 modules, see figure 2.1. Two modules are glued face-to-face making up a ladder. Eight ladders are installed at a distance of 14 mm around the berillium beam-pipe to a cylindrical entity, called the first layer. The second layer consists of 12 ladders and is placed at a distance of 22 mm to the IP. The total sensitive area of the pixel sensors is approx. 0.027 m^2. To avoid multiple scattering low material budget

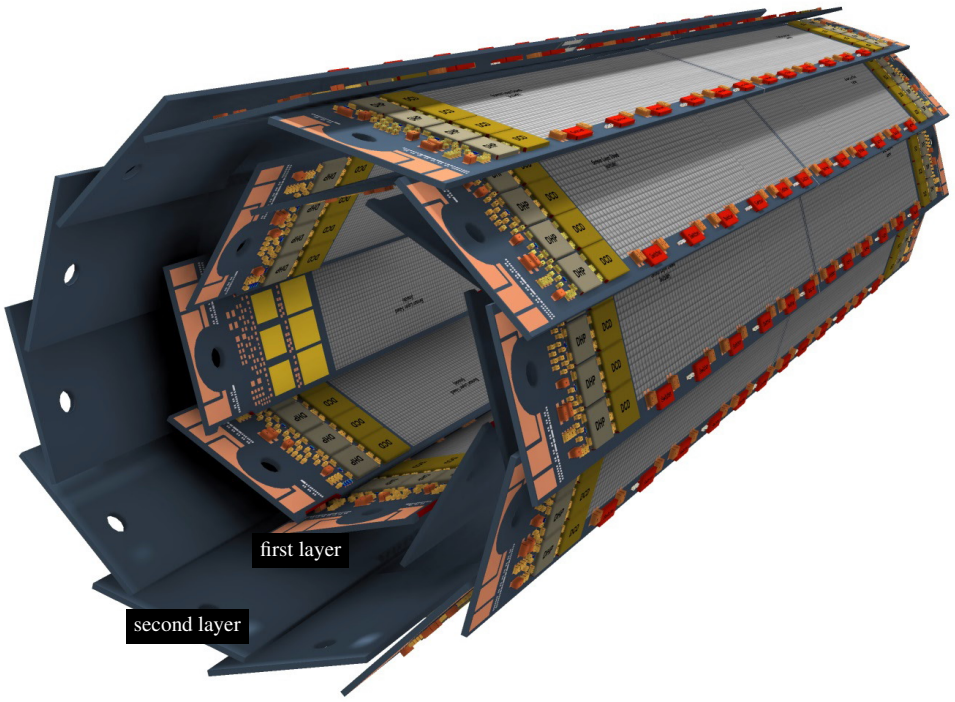


Figure 2.1: Two layers of DEPFET pixel sensors. The pixel detector consists of 40 sensor modules arranged in a barrel like structure with overlapping edges.

inside the sensitive volume is needed. The average material budget per layer is 0.21% X_0, with X_0 being the mean free path of the material. This can be achieved by thinning down the silicon at the sensitive area of the pixel matrix to 75 µm. The pixel size is $50 \times 75\,\mu m^2$ and the acceptance of the sensitive area reaches from 17° to 155°. The integration time is 20 µs for the full PXD. Due to the increased luminosity

the occupancy of the detector rises to max. 3% and the detector will suffer a total ionising dose (TID) of 20 kGy per year. This implies for all electrical parts within the sensitive volume:

- Radiation hardness up to 10 years of operation, TID up to 200 kGy
- High neutron flux → High single event upset rate (bit flips of SRAM cells)
- Coping with up to 3% data occupancy

2.1 The PXD module

The Sensitive area is the monolithicly processed Depleted P-channel Field Effect Transistor (DEPFET) pixel matrix. The pixels are arranged in a (250×768)-sized matrix making up a total pixel number of $192,000$ per module. The DEPFET is a modified p-channel FET with an additional for e^- attractive n^+

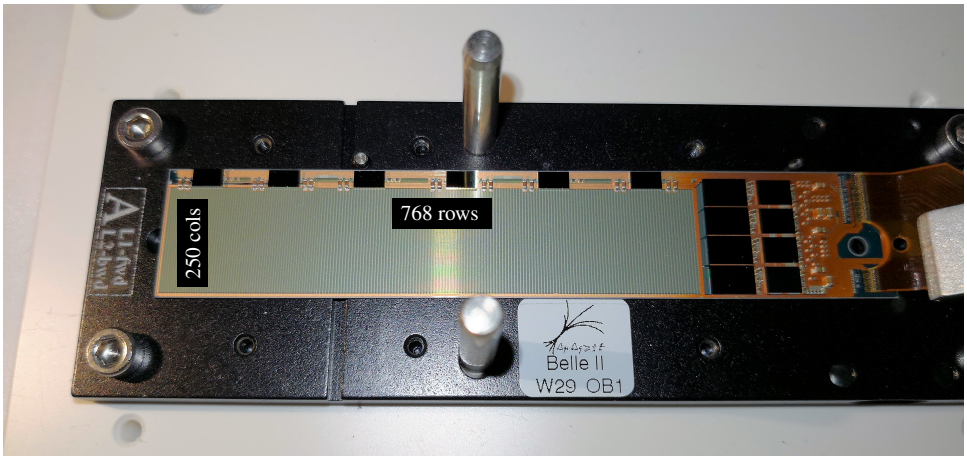


Figure 2.2: Single PXD module with pixel matrix and ASICS attached on a carrier jig for testing and transportation purpose.

doping region below the gate channel. A reverse biasing is applied to the DEPFET and the bulk region is fully depleted, i.e. no free charge carriers present. Ionising particles penetrating the bulk of the DEPFET create electron-hole pairs. The electrons drift in the electric field and are collected within the internal gate. The charges persist in the internal gate until a clear potential is applied depleting the internal gate and therefore remove all charge. Due to capacitive coupling of the internal gate with the p-channel, the charge in the internal gate introduces a modulation of the drain current if the external gate, source and drain potentials are fixed. The DEPFET acts like a voltage-controlled current source such that the change of the drain current is proportional to the amount of charge Q_{inter} collected in the internal gate,

$$g_q = \frac{\partial I_d}{\partial Q_{inter}} \propto \frac{g_m}{WL \cdot C_{ox}} \tag{2.1}$$

with the standard FET gain $g_m = {}^{\partial I_d}/_{\partial V_{gs}}$, the channel width W and length L and the specific oxide capacitance C_{ox}. The g_q parameter defines the gain of the first amplification stage in the signal processing. Due to the persistent charge within the internal gate, multiple sampling of the drain current can be performed without clearing the internal gate. Four rows of DEPFET pixels are combined to one 'gate' entity. These 192 'gates' are connected to six **Switcher** with 32 'gates' each. The Switcher selects the

'gates' via the rolling shutter mode. The 'gates' are successively selected, beginning from the side closest to the IP. All 192 'gate' (one frame) are read in 20 μs. The Switcher enables the potentials needed to operate the DEPFET and connects the drain current to the drain lines. The drain lines are routed all over the long side of the matrix to the near-end called end-of-stave (EOS) region. Four **Drain Current Digitizers** (DCD) [16] convert in parallel the drain currents via a trans-impedance amplifier and 256 (8 bit) pipeline ADCs in each DCD. The four DCD transmit the data to four **Data Handling Processors** (DHP). The data rate per DCD–DHP pair is approx. 19.51 Gbps with a clock frequency of 304.92 GHz. The first data reduction step is performed in the DHP by zero-suppression read-out, see chapter 4. The high speed data stream output of one DHP has an effective data rate of 1.22 Gbps via a 1.52 Gbps serial link[1]. Figure 2.3 shows the on-module ASICs and the back-end solution of the PXD module. The digitised DEPFET pixel data are driven by the serial link of the DHP and sent via $\sim$ 50 cm flat-band Kapton to the patch panel. The low material flat-band Kapton is used to transmit the data within the tight environment inside the Belle II detector. The patch panel is placed at the outside of the VXD and connects the Ethernet, Infiniband and power cables to the flat-band Kapton. The Dock Box is placed at the outside of the Belle II at the end-caps. It embeds a optical transmitter and the interface connecting the slow control signals, which are used to steers the DHP (see chapter 4), via the Ethernet cable. The high speed serial link of the DHP is connected via the Infiniband cable. The power cable is used to provide the DEPFET potentials. The high speed data are fed into the optical transmitter and sent via optical fibres to the back-end system. The slow control data are sent from the Slow control host via the Data Handling Hybrid over $\sim$ 15 m Camera Link cable to the Camera Link Break-out Board (CLCBB) which hosts the optical transmitter. The high data rates, originated from the high luminosity (and/or by noise) of the accelerator, have to be properly transmitted for further processing and analysis. This thesis comprises the basics of signal transmission and transmission lines in the following chapter 3. The front-end processing chip, namely the Data Handling Processor, is described and the optimisation and validation shown in chapter 4. Using the optimised front-end chip measurement methods related to signal integrity are discussed in chapter 5 and the results of the full scale transmission line system presented in chapter 6.

[1] Effective data rate accounts for 8b10b encoding and overhead due to framing.

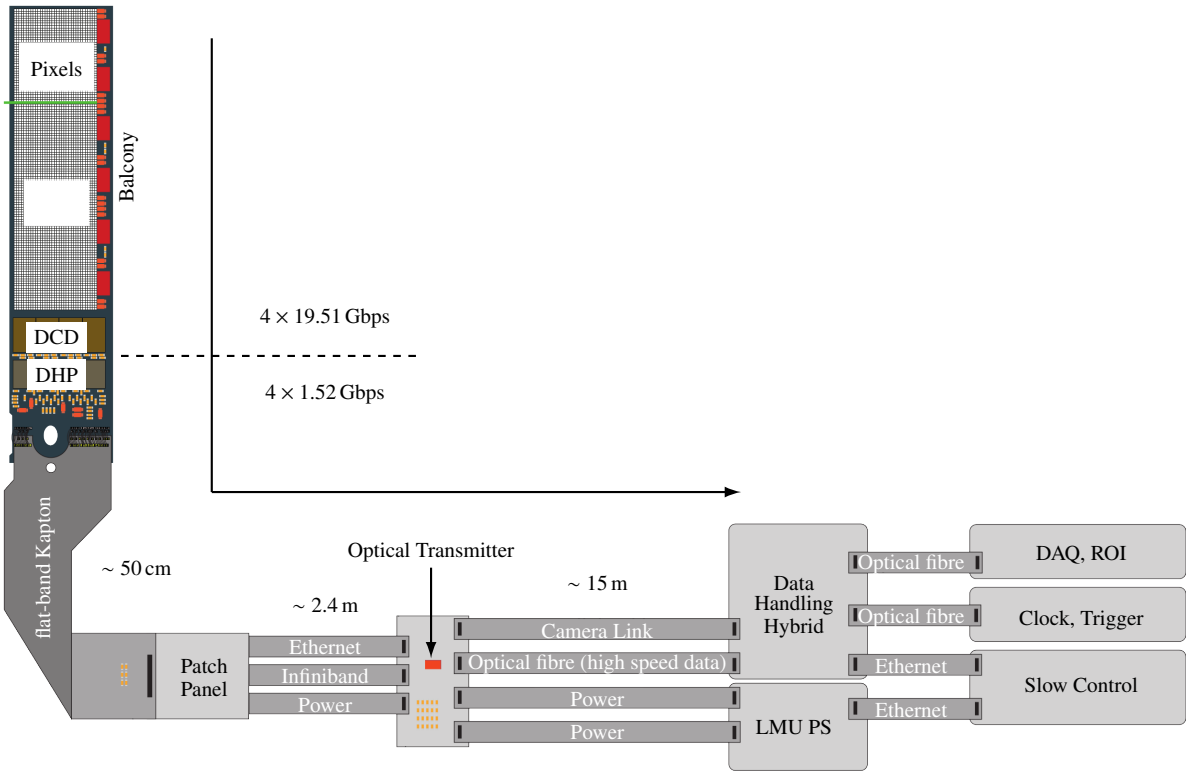


Figure 2.3: PXD module with DEPFET pixel matrix, balcony, on-module ASICs and back-end system. Data have to be sent over 20 m cables. PCB for connecting different connector types are foreseen, i.e. Patch Panel (PP), Dock Box (DB). The optical transmitter on the DB converts the high speed serial data to optical signals. The reference clock, configuration data and trigger are transmitted via copper.

CHAPTER 3

Principles of signal integrity

Any external source, like electromagnetic waves, can trigger transitions of states of a particular physical system. The response of the system to the external source is of major interest in electronics. It has to be understood in order to design a circuit which behaviour is predictable. In the following, the fundamental mathematics and principles of signal theory are presented.

3.1 Signal properties and system respond

The induced transition of states can be measured. This signal can be mathematically represented by means of the Fourier series[1]. For each plane wave within the series a tuple (A_n, ϕ_n, n) can be assigned which represents the amplitude A_n, phase ϕ_n and mode n of the plane wave, respectively. The total decomposition is,

$$\mathcal{S}(t) = \frac{A_0}{2} + \sum_{n=1}^{\infty} A_n \cdot \cos\left(\frac{2\pi \cdot n}{T} t - \phi_n\right) \tag{3.1}$$

The time scale and mode-dependent phase of the time-varying signal is denoted by the period T and ϕ_n, respectively. The set of pairs (A_n, n) is called the spectrum of the signal with phase relation (ϕ_n, n). The Fourier coefficients are

$$\begin{aligned} A_n &= \sqrt{a_n^2 + b_n^2} \\ a_n &= \frac{1}{\pi} \int_{-\pi}^{+\pi} \mathcal{S}(t) \cdot \cos\left(\frac{2\pi n}{T} t\right) \mathrm{d}t, \quad \forall n \in \mathbb{N}_0 \\ b_n &= \frac{1}{\pi} \int_{-\pi}^{+\pi} \mathcal{S}(t) \cdot \sin\left(\frac{2\pi n}{T} t\right) \mathrm{d}t, \quad \forall n \in \mathbb{N} \end{aligned}$$

From Parseval's theorem[2], one can deduce that the energy contained in the waveform of signal $\mathcal{S}$ is equivalent to the energy of its spectrum, see equation 3.2. This equivalence can be used to relate any

[1] Signals which are not well defined, i.e. not continuously differentiable, can not be represented as such Fourier series. Within the scope of our assumptions we declare signals to be well defined and periodic.

[2] Marc-Antoine Parseval stated in 1799, without prove, that the inner product of two Riemann-integrable complex functions A and B equals the sum of the product of their Fourier coefficients a_n and b_n. This theorem has been proven meanwhile in many disciplines of science [17].

variation of the spectrum to the time domain representation.

$$\int_{-\infty}^{+\infty} |\mathcal{S}(t)|^2 \, \mathrm{d}t = \frac{1}{2\pi} \sum_{n=0}^{\infty} |A_n|^2 \tag{3.2}$$

The frequency response $\mathcal{S}_{out}$ of a system M to an initial signal $\mathcal{S}_{init}$ is called the transfer function $\mathcal{T}_{\mathrm{M}}$ of system M. It relates the initial signal to the output of system M in the frequency domain. In order to compute the transfer function the Fourier transformation can be applied. If analytic solutions are of interest the Fourier transformation is not suitable in all cases. The signal has to be absolutely integrable, i.e. $\int_{-\infty}^{+\infty} |\mathcal{S}(t)| \mathrm{d}t < \infty$. For digital waveforms like clock signals the convergence is not given. One can introduce a windowing function that scales the integrand by $\mathrm{e}^{-\alpha t}$, $\forall \alpha \geq 0$. This leads directly to the Laplace transformation $\mathcal{L}\{\}$, that can be performed independent of the intrinsic convergence of the signal itself.

$$\text{Fourier } \mathcal{F}\{\mathcal{S}(\mathrm{t})\}: \quad \int_{-\infty}^{+\infty} \mathcal{S}(t) \, \mathrm{e}^{-\mathrm{i}\omega t} \, \mathrm{d}t \quad \longrightarrow \quad \text{Laplace } \mathcal{L}\{\mathcal{S}(\mathrm{t})\}: \quad \int_{0}^{+\infty} \mathcal{S}(t) \, \mathrm{e}^{-(\alpha+\mathrm{i}\omega)t} \, \mathrm{d}t$$

The real argument ω is now replaced by the complex frequency $s = \alpha + \mathrm{i}\omega$. The special case $\alpha = 0$ relates the Laplace to the Fourier transformation. In order to find the analytical expression for the transfer function for a given system M, M is modelled and described by partial differential equations (PDE). For transient terms in the PDE, the Laplace transformation is useful to transform a differential equation into an algebraic one. Time derivatives $\frac{\partial}{\partial t}\mathcal{S}(t)$ are transformed to products $s \cdot \mathcal{L}\{\mathcal{S}(t)\}(s)$.

For passive systems, due to energy conservation, $\mathcal{L}\{S_{out}(t)\}(s) \leq \mathcal{L}\{S_{init}(t)\}(s)$ holds and thus the transfer function $\mathcal{T}_M(s) \leq 1$.

$$\mathcal{L}(t)\{S_{out}\}(s) = \mathcal{T}_M(s) \cdot \mathcal{L}(t)\{S_{init}\}(s) \tag{3.3}$$

From equation 3.3, one can write for multiple systems M_N interacting serially with the initial signal,

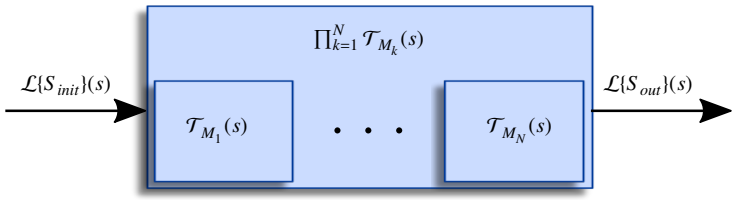


Figure 3.1: Response of serially connected multiple systems M_N to an incident signal S.

$$\mathcal{L}\{S_{out}(t)\}(s) = \mathcal{T}_{M_{tot}}(s) \cdot \mathcal{L}\{S_{init}(t)\}(s) = \prod_{k=1}^{N} \mathcal{T}_{M_k}(s) \cdot \mathcal{L}\{S_{init}(t)\}(s) \tag{3.4}$$

The transfer function $\mathcal{T}(s)$ can be decomposed in its amplitude and phase component by the Euler representation,

$$\mathcal{T}(s) = |\mathcal{T}(s)| \cdot \mathrm{e}^{\mathrm{i} \cdot \arctan\left(\frac{\mathrm{Im}\,\mathcal{T}(s)}{\mathrm{Re}\,\mathcal{T}(s)}\right)} = \mathcal{A}(\omega, \alpha) \cdot \mathrm{e}^{\mathrm{i}\Phi(\omega,\alpha)} \tag{3.5}$$

with the real-valued amplitude $\mathcal{A}(\omega, \alpha)$ and real-valued phase relation $\Phi(\omega, \alpha)$. $\mathcal{A}(\omega, \alpha)$ reflects the frequency dependent attenuation of the the output signal. The Bode plot[3] is obtained by computing

[3] Named after Hendrik Wade Bode, a Dutch engineer who aimed for an easy graphical representation of the frequency

$\sqrt{\mathcal{T}(s)\overline{\mathcal{T}}(s)} = \mathcal{A}(\omega, \alpha)$ and executing the limit $\alpha \to 0$ to obtain the real-valued attenuation $\mathcal{A}(\omega)$. [4]

Summary: The equivalence stated by Parseval, equation 3.2, allows to use the frequency representation rather than the time domain as it is more convenient for calculation purposes. The crucial point of signal integrity is to understand the system response by calculating the transfer function or measuring the frequency dependent attenuation. In detectors for high-energy physics, wired transmission lines have to be used to mitigate additional electro-magnetic interferences in wire-less transmission. Such wired transmission lines are discussed in the following section.

3.2 Transmission lines

A common transmission line (TML) architecture for connecting different devices at different locations is a single shielded wire. A dielectric separates the inner conductor from the outer conductive shield. The topology and the equivalent electrical circuitry is shown in figure 3.2. It represents an element of a infinite series of lumped LRCG elements with quantities $\mathrm{L}' = {}^{\mathrm{dL}}/_{\mathrm{d}x}$, $\mathrm{R}' = {}^{\mathrm{dR}}/_{\mathrm{d}x}$, $\mathrm{C}' = {}^{\mathrm{dC}}/_{\mathrm{d}x}$ and $\mathrm{G}' = {}^{\mathrm{dG}}/_{\mathrm{d}x}$, representing the inductance, resistance, capacitance and conductance per unit length respectively. From this model the corresponding differential equations, called Telegrapher's equation, 3.6 and 3.7 can be deduced and the solutions for the voltages V and currents I derived, see 3.8.

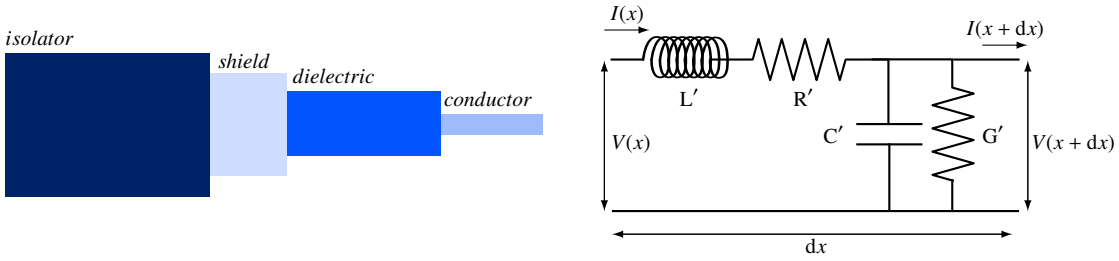


Figure 3.2: Sketch of a simple cable geometry. Conductive core wrapped by a dielectric and an outer shield (left). Equivalent circuit element with infinitesimal length dx modelled by a lumped LRCG circuit (right).

$$0 = \frac{\mathrm{d}V(x,s)}{\mathrm{d}x} + (s \cdot \mathrm{L}' + \mathrm{R}') \cdot I(x,s) = \frac{\mathrm{d}V(x,s)}{\mathrm{d}x} + \mathbf{Z} \cdot I(x,s) \tag{3.6}$$

$$0 = \frac{\mathrm{d}I(x,s)}{\mathrm{d}x} + (s \cdot \mathrm{C}' + \mathrm{G}') \cdot V(x,s) = \frac{\mathrm{d}I(x,s)}{\mathrm{d}x} + \mathbf{Y} \cdot V(x,s) \tag{3.7}$$

$$V(x,s) = c_1 e^{\gamma(s)\cdot x} + c_2 e^{-\gamma(s)\cdot x}, \quad I(x,s) = -\frac{c_1}{Z_0} e^{\gamma(s)\cdot x} + \frac{c_2}{Z_0} e^{-\gamma(s)\cdot x} \tag{3.8}$$

The model parameters per unit length can be summarised;

L′: Inductance describing the magnetic behaviour of the conductive wire by present current (Law of Biot-Savart).

R′: Resistance describing the voltage drop along the conductive wire due to present current (Ohm's law).

C′: Capacitance deduced by Poisson's equation. Relation of electric potential and electric charge.

dependent gain and phase-shift of an electrical system.

[4] Henceforth, for calculation the complex frequency s is used and for physical relevant expressions $\omega = 2\pi f$. Since for physical interpretations only amplitudes (of complex functions) are of interest the limit $\alpha \to 0$ is valid.

G′: Conductance describing current loss by finite resistivity of the dielectric. Static current present through the transconductance.

The longitudinal complex resistance $\mathbf{Z} = s \cdot \mathrm{L}' + \mathrm{R}'$ and the transversal complex resistance $\mathbf{Y} = s \cdot \mathrm{C}' + \mathrm{G}'$ are the impedance and admittance of the cable model, respectively. The general solution of equation 3.6 and 3.7 are plane waves with damping constant α and phase constant β combined to the wave constant $\gamma = \sqrt{\mathbf{Z} \cdot \mathbf{Y}} = \alpha + \mathrm{i}\beta$. The characteristic impedance $Z_0 = \sqrt{\mathrm{Z}/\mathrm{Y}}$ can be approximated by $Z_0 = \sqrt{\mathrm{L}/\mathrm{C}}$ for high frequencies. Since L and C are geometrical dependent quantities, the characteristic impedance of transmission lines can be properly controlled by geometrical considerations. Any discrepancy along the TML directly translates into impedance mismatches and causes reflections. The reflection coefficient[5] $\mathcal{R}$ can be related directly to Z_0;

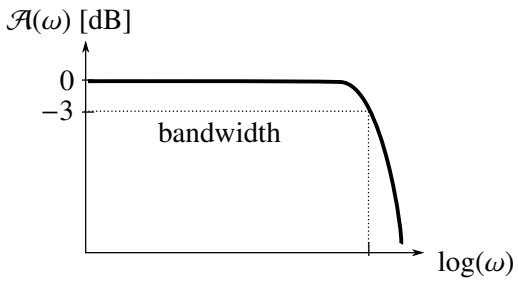
$$\mathcal{R} = \frac{Z(x) - Z_0}{Z(x) + Z_0}, \quad -1 \leq \mathcal{R} \leq +1 \tag{3.9}$$

with x being the point along the cable. Table 3.1 summarises the effects of impedance mismatches. Lossy

Impedance mismatch	Reflection coefficient	
$Z(x) < Z_0$	$\mathcal{R} \in (-1, 0)$	Reflection with opposite polarity
$Z(x) = Z_0$	$\mathcal{R} = 0$	No reflection
$Z(x) > Z_0$	$\mathcal{R} \in (0, +1)$	Reflection with same polarity

Table 3.1: Cases of impedance mismatches.

transmission lines attenuate the incident signal according to the damping constant α. The frequency dependent attenuation of the transmission line can be represented in the Bode plot. A typical example of a Bode plot is shown in figure 3.3.



$$\mathcal{A}(\omega) = \frac{V(x = l, s)}{V(x = 0, s)} = \frac{V_{out}(\omega)}{V_{in}(\omega)} \tag{3.10}$$

Figure 3.3: Sketch of a typical Bode plot of a transmission line with length l. The bandwidth of the transmission line is defined as the frequency the attenuation drops below −3 dB.

The physical reasons for frequency independent damping of transmitted signals are ohmic and dielectric losses due to finite R′ and G′, respectively. Voltage drops across the TML, due to R′, and charge loss through the dielectric, lowers the potential. On the other hand frequency dependent losses are introduced by the finite capacitance C′ and the Skin effect. For high frequencies $\omega \to \infty$ the impedance of the capacitance C′ vanishes and acts like a short between the conductive core and the grounded shield.

[5] A deeper discussion on implications of impedance mismatches and reflections are conducted in section about measurement methods 5.1.

From Maxwell's equations of electrodynamics, one can derive the diffusion equation 3.11. Let z be the spatial coordinate along the symmetry axis and y the coordinate originated from the surface and pointing perpendicular to the symmetry axis of a cylindrical conductor. The solution of the current density distribution J_z inside the conductor has its maximum shifted toward the surface for frequency $\omega \to \infty$. The Skin depth δ_{skin} describes the penetration depth of the current density which drops to $^1/_e$ of its surface amplitude, see equation 3.12, 3.13 and figure 3.4.

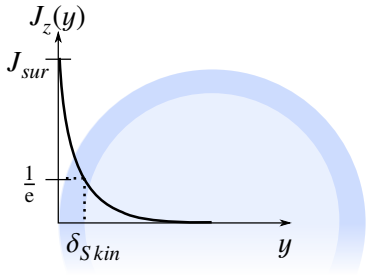


Figure 3.4: Skin depth within the context of a cylindrical conductor. z denotes the axis along the symmetry axis of the conductor. y denotes the radial dimension of the conductor on which the z component of the current density falls off exponentially towards the center.

$$\frac{\partial^2}{\partial y^2} J_z(t,y) = \mu\sigma \frac{\partial}{\partial t} J_z(t,y) \tag{3.11}$$

$$\mathcal{L}\{J_z(y)\}(s) = J_{sur} \cdot e^{-\frac{y}{\delta_{skin}(s)}} \tag{3.12}$$

$$|\delta_{Skin}(s)|_{\alpha\to 0} = \sqrt{\frac{1}{\mu\sigma \cdot \omega}} \tag{3.13}$$

In addition to the Skin depth, the temperature distribution has to be taken into account for cables conducting high currents [18]. For cables with data transmission purposes, the temperature distribution can be assumed to be uniform across the conductor. From figure 3.4 one can deduce that the effective cross-section, i.e. the ring defined by δ_{Skin}, is linearly dependent on the radius of the conductor, i.e. $A_{eff} = 2r\pi \cdot \delta_{Skin} - \pi\delta_{Skin}^2$. Thus the effective resistance becomes lower for thicker conductors. The Skin depth itself is a function only dependent on material properties shown in equation 3.13, i.e. absolute permeability μ and conductivity σ, and independent on the current strength.

Summary: Signals over TML suffer from frequency dependent (finite capacitance and Skin effect) and independent effects (finite longitudinal resistance and conductance). The characteristic impedance Z_0 is a system property used to characterise the frequency behaviour of a TML. Impedance mismatches will cause reflections superimposing the initial signal. For common conductors like copper, the Skin depth at frequencies of 1 MHz measures about 65 μm. Higher frequencies demand thicker conductors to compensate the Skin effect. In order to cope with this effect, gold or silver plating is common for sup-GHz transmission lines to increase surface conductivity and thus reduce resistivity.

3.3 Signal types

Due to constraints given by the specific application, different standards for signal transmission are used. Typical figure of merits for choosing standards are frequency range, spacing requirements of cables and connectors, transmitters (TX) and receivers (RX) power and area constraints.

Single-ended Signalling

For low frequency applications, single-ended signalling can be used. Signals are transmitted via a single wire connecting transmitter and receiver. The wires are commonly shielded from external electromagnetic fields by a conductive mesh or foil, e.g. BNC cables. Single-ended signalling is preferred in applications where cables are in use of small radii and the implementation of transmitters and receivers are less complex. If higher frequencies and less severe space constraints are in question, when cable size nor TX/RX space limitations are given, differential signalling is preferred.

Differential Signalling

A common standard in high frequency signal transmission is low-voltage-differential signalling (LVDS). While shielding is crucial for single-ended cables, unshielded differential cables are common. Those cables have multiple pairs of leads. The leads within a pair are routed closely to sense common noise coupling that is induces by external electromagnetic fields. Both leads are exposed to the same vicinity and therefore noise coupling is similar. If differential cables are driven in odd mode, i.e. one leader transmits the signal $\mathcal{S}(t)_+$, the other the inverted $-\mathcal{S}(t)_+ = \mathcal{S}(t)_-$. Noise δ can be cancelled out by using a differential receive $\mathcal{S}(t)_{out} = (\mathcal{S}(t)_+ + \delta(t)) - (\mathcal{S}(t)_- + \delta(t)) = 2 \cdot \mathcal{S}_+$. Low voltage signalling also implies low power and is therefore attractive for such purposes. Since differential cables have pairs of leads transmitting the information, impedance mismatches in one leader will cause data corruption. Therefore, in case of odd mode transmission, the differential impedance is defined as

$$Z_{\text{diff}} = 2 \cdot Z_0 = 2\sqrt{\frac{\mathrm{L}_{\text{self}} - \mathrm{L}_{\text{mut}}}{\mathrm{C}_{\text{self}} + \mathrm{C}_{\text{mut}}}} \tag{3.14}$$

The self inductance and capacitance is determined by the geometry of the pair itself, whereas the mutual inductance and capacitance are determined by the geometry of neighbouring pairs. To reduce mutual capacitances and inductances cable geometry with many pairs have to be well shielded. With smaller distance between leads within a pair the self capacitances increases and the inductance decreases, see figure 3.5. The self inductance and capacitance for a single pair of cylindrical wires can be calculated

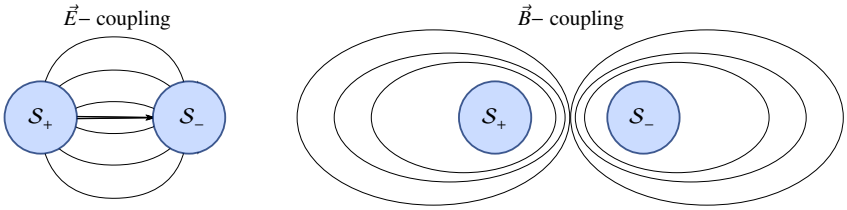


Figure 3.5: Electric (left) and magnetic (right) coupling of two conductors driven in odd mode.

with Gauss law and are given by,

$$\mathrm{C}_{\text{self}} = \frac{\pi\epsilon_0\epsilon_r \cdot l}{\operatorname{arccosh}\left(\frac{2a}{r}\right)} \qquad \mathrm{L}_{\text{self}} = \frac{\mu_0 \cdot l}{\pi} \operatorname{arccosh}\left(\frac{2a}{r}\right) \tag{3.15}$$

with absolute ϵ_0 and relative permittivity ϵ_r of the vacuum and the wire material, respectively, l the length of the wires and permeability μ_0 of the vacuum, by assuming $\mu_r = 1$. The geometry information is embedded in a, the distance of the symmetry axis of the two wires and in the radius r. If $a >> r$, the

inverse hyperbolic cosine can be replaced by the natural logarithm, since $\operatorname{arccosh}(x) = \ln(x + \sqrt{x^2 - 1})$. For real cable geometries $\frac{2a}{r} \approx 10$.

3.4 Methods and techniques

In order to cope with the above mentioned effects of signal distortion, different standard techniques have been developed. Signal integrity can be investigated on different system layers. The lowest layer hereby is the physical layer, where analogue measurements can spot problems of the design. Once layout of cables and PCBs of the system is fixed, signal-integrity issues on the physical layer, caused by impedance mismatches and overall attenuation of the signal, cannot be cured and solutions at higher abstraction layers are needed. Data generation can be reviewed and changed in order to compensate effects induced by transmission lines.

Sources of data corruption

A simulated signal is shown in figure 3.6. The common mode, i.e. time-average of the signal, varies. This effect is called **inter-symbol interference**. The characteristic time needed for charging and discharging the conductor limits its bandwidth. If the driver loads the cable with multiple ones, the wire charges up to an extent that a single bit flip cannot compensate and therefore the minima cannot be reached. Those signal are called un-balanced. Signals with stable common mode are called **DC balanced**. Due to the

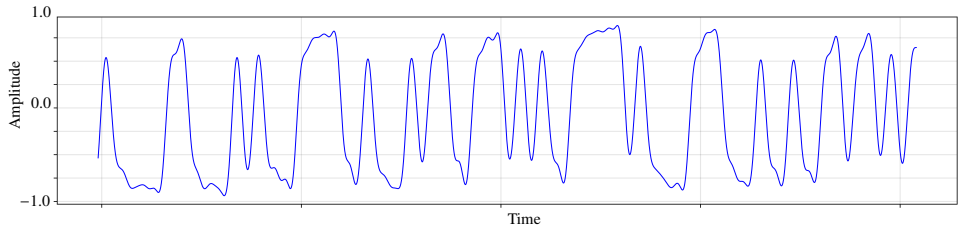


Figure 3.6: Waveform of a non DC balanced signal. The average at intermediate time scales is oscillating around zero.

effect of inter-symbol interference the signal might not cross the threshold of the receiver and bit errors arise. To avoid long sequences of ones or zeros different approaches have been approved that will be discussed in the following.

Manchester coding The IEEE 802.3 standard defines each bit as a pair of bits. Bit «high» is represented as «low-high» and «low» as «high-low». This decreases the bit rate by a factor of two but introduces naturally DC balancing.

8b10b encoding To mitigate long sequences of same-valued bits, 8b10b encoding has been introduced. This encoding permits only bit sequences with a maximum number of 5 same-valued bits. For each 8 bit word two 10 bit words are assigned. Each 10 bit word has a quantity called disparity (RD). It represents the difference of numbers of ones and zeros within the word, such that each 8 bit word has a 10 bit RD^+ and RD^- pendent, where + and − denotes more ones and more zeros, respectively. The 8b10b-encoder module keeps track of the running disparity and chooses the right 10 bit word for each next 8 bit word in the sequence to compensate an excess of imbalanced numbers of ones and zeros. This ensures a DC balanced signal over an intermediate time scale. To store the 10 bit words a look-up table (LUT) is used. Such a LUT can be implemented inside the encoder/decoder, thus occupies memory space.

Signal shaping In addition to the above mentioned techniques, shaping of the waveform can improve the limitations introduced by low bandwidth TML. In order to compensate the high frequency dependent losses and minimizing the effect of inter-symbol interference the initial signal can be reshaped by enhancing the high frequency content of its spectrum and lowering the low frequency part. There are two major types; pre shaping, called pre-emphasis, and post-shaping, called equalisation. The first refers to modulation of the signals spectrum at the near-end (Transmitter), i.e. before passing the TML. A realisation of this is shown in section 4.2.2. The second method is used at the far-end (Receiver). The equalisation is boosting the high frequency part of the incoming signal by a analogue amplifier. This amplifier has to match the transfer function of the TML and therefore the boost settings are adjustable through standard industrial receivers with embedded equalisation [19].

3.5 Analytic Solution of Signals with pre-emphasis

In order to amplify the high frequency component of a digital signal, the transition region is modulated. As an example we assume a periodic box shaped signal $v(t)$ with unit amplitude, centred around the x axis, e.g. clock signal. The linear combination of two rectangular signals with amplitude a and b shifted against each other by τ yields a signal with transition modulation, as shown in figure 3.7.

$$v_{res}(t) = a \cdot v(t) - b \cdot v(t-\tau), \quad 0 < b < a, \quad v_{res}(t) = 0, \ \forall t \leq 0 \tag{3.16}$$

To obtain the spectrum of such modulated signal the properties of the Heaviside function can be exploited.

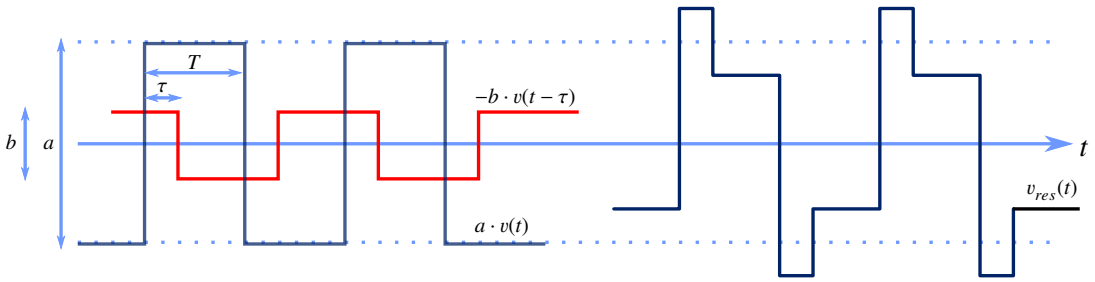


Figure 3.7: Example of pre-emphasis. Time domain waveform of a periodic rectangular shaped signal with additional enhancement at the transition region.

The Heaviside function and its Laplace transform is defined by equation 3.17 and 3.18, respectively.

$$\Theta(t-t_0) = \begin{cases} 0 & t \in [0, t_0) \\ 1 & t \in [t_0, \infty) \end{cases} \tag{3.17}$$

$$\mathcal{L}\{\pm\Theta(t-t_0)\}(s) = \pm\frac{e^{-t_0 s}}{s} \tag{3.18}$$

A box function $u_T(t)$ can be represented by two Heaviside functions shifted against each other by T. A box function $\tilde{u}_T(t)$, which is centred around the x axis, is given by

$$\tilde{u}_T(t-t_0) = \Theta(t-t_0) - \Theta(t-t_0-T) - \frac{1}{2} = u_T(t-t_0) - \frac{1}{2} \tag{3.19}$$

where t_0 is an arbitrary shift of the boxed-shaped waveform. Adding box functions $\tilde{u}_T(t)$ periodically with displacement of period $2T$ generates a clock-like waveform, which is represented by

$$v(t) = \sum_{k=0}^{\infty} \left(\Theta(t - (t_0 + 2kT)) - \Theta(t - (t_0 + (2k+1)T))\right) - \frac{1}{2} \tag{3.20}$$

Applying the Laplace transformation of the Heaviside function, equation 3.18, and using the closed form of the geometric series yields[6],

$$\mathcal{L}\{v(t)\}(s) = \left(\sum_{k=0}^{\infty} \left(\mathrm{e}^{-2Ts}\right)^k\right) \cdot \mathcal{L}\{u_T(t - t_0)\}(s) - \frac{1}{2s} = \left(\frac{1}{1 - \mathrm{e}^{-2Ts}}\right) \cdot \mathcal{L}\{u_T(t - t_0)\}(s) - \frac{1}{2s} \tag{3.21}$$

Finally write the Laplace transform of the resultant waveform $v_{res}(t)$ from equation 3.16,

$$\mathcal{L}\{v_{res}(t)\}(s) = a \cdot \mathcal{L}\{v(t)\}(s) - b \cdot \mathrm{e}^{-\tau s} \cdot \mathcal{L}\{v(t)\}(s) = \left(a - b \cdot \mathrm{e}^{-\tau s}\right) \cdot \mathcal{L}\{v(t)\}(s) \tag{3.22}$$

Using the Euler representation of a complex function

$$\mathcal{L}\{\mathcal{S}(t)\}(s) = \mathcal{A}(\omega, \alpha) \cdot \mathrm{e}^{\mathrm{i}\Phi(\omega,\alpha)}$$

one can write the amplitude $\mathcal{A}$ for the case $t_0 = 0$[7] and the limit $\alpha \to 0$,

$$\mathcal{A}(\omega \mid a, b, \tau, T) = \underbrace{\frac{1}{\omega}}_{\text{envelope}} \left(\underbrace{\left(a^2 + b^2 - 2ab \cdot \cos(\omega\tau)\right)}_{\text{pre-emphasis part}} \underbrace{\frac{1 - \cos\left(\frac{\omega T}{2}\right)}{1 + \cos\left(\frac{\omega T}{2}\right)}}_{\text{spectral part}} + \underbrace{\frac{b-a}{2}\left(a - b\frac{P(\omega \mid \tau, T)}{P(\omega \mid 0, T)} + \frac{b-a}{2}\right)}_{\text{offset term}} \right)^{\frac{1}{2}} \tag{3.23}$$

with

$$P(\omega \mid t, T) = \cos(\omega t) - \cos(\omega(2T - t)) - \cos(\omega(T + t)) + \cos(\omega(T - t)) \tag{3.24}$$

The amplitude $\mathcal{A}$ is composed of several contributions, i.e. the scaling envelope, pre-emphasis part, containing the parameters corresponding to the signal shape, the spectral part that expresses the resonances at odd modes of the base frequency $\omega_0/2\pi = 1/2T$ and the offset term that is introduced by the offset in equation 3.19. The relevant portion of equation 3.23 is the pre-emphasis and offset term that contains information of amplitude a, pre-emphasis strength b and width τ. Function $P(t)$ introduces resonances at shifted frequencies $\omega = (n + 0.5) \cdot \omega_0$ corresponding to mode n. The oscillation of the pre-emphasis part is defined by the parameter τ. There are three interesting cases for the pre-emphasis part in which,

$$\text{(i)} \quad \tau = 0$$

$$\text{(ii)} \quad \tau = T$$

$$\text{(iii)} \quad 0 < \tau < T$$

for given constant a and b. Case (i) reflects constant attenuation of the signal, i.e. $a - b$. In case (ii) the maxima of the cosine is at the odd modes and thus the maximum is $a + b$. The last case represents the

[6] To use the geometric series we have to force $|\mathrm{e}^{-2Ts}| = \sqrt{\mathrm{e}^{-2Ts}\overline{\mathrm{e}^{-2Ts}}} = \mathrm{e}^{-2T\alpha} < 1 \to \alpha > 0$.

[7] This is an arbitrary chose to simplify the equation.

intermediate scenario that is shown with case (i) and (ii) in figure 3.8. If the spectrum in figure 3.8 is compared for no pre-emphasis (blue) and case (iii) (red), the spectrum is reshaped in benefit for higher modes. Modes $n = 1$, $n = 9$ and $n = 11$ are attenuated whereas modes 3, 5, 7 are enhanced.

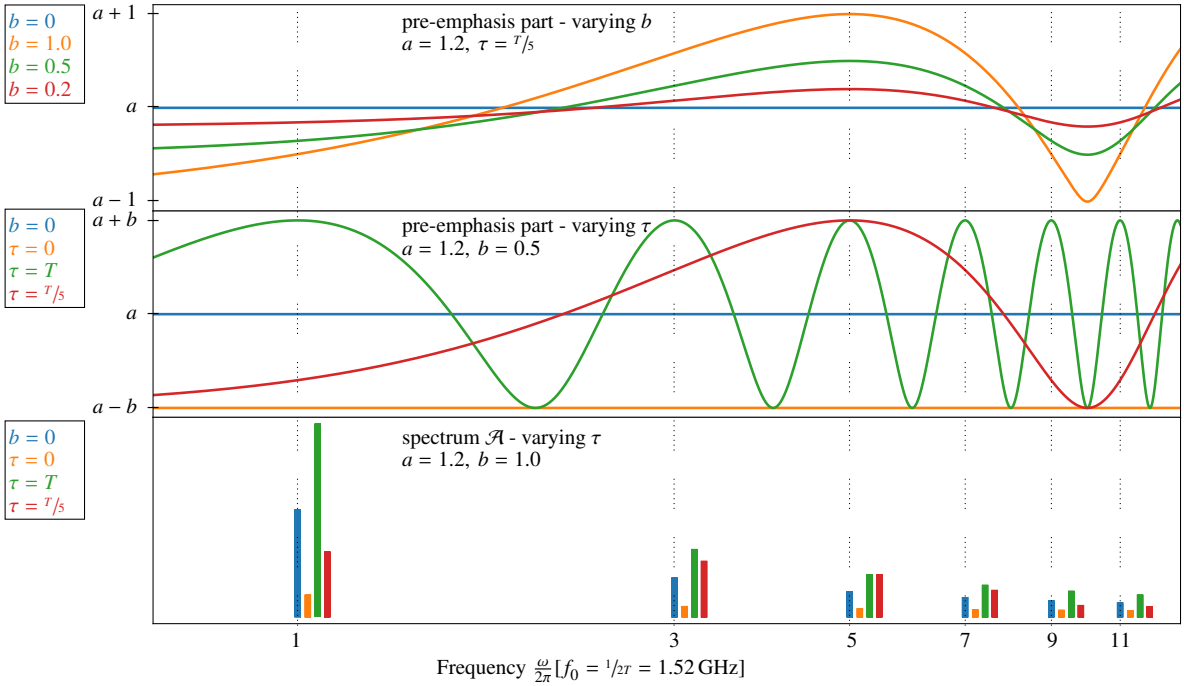


Figure 3.8: Visualisation of the analytic solution of the Laplace Transform of a rectangular periodic signal in arbitrary units. The square-root of the pre-emphasis part shown in equation 3.23 is plotted for different pre-emphasis strengths b (top) and different pre-emphasis widths τ (centre). The total spectrum $\mathcal{A}$ (bottom) is plotted for the cases (i) $\tau = 0$, (ii) $\tau = T$ and (iii) $\tau = T/5$. Blue curves represent signal without pre-emphasis ($b = \tau = 0$). The spectra in the bottom plot are shifted for display purposes.

Summary: Although this model assumes a periodic boxed-shaped waveform the findings can be transferred to any kind of waveform. If data streams are sent, inter-symbol interference can be minimised by applying pre-emphasis to the data stream beforehand. With the right choice of the parameters, i.e. amplitude a, pre-emphasis strength b and width τ, amplitudes of long sequences of same-valued bits (low effective frequency) can be attenuated while simultaneously enhancing fast toggling bit sequences (high effective frequency). In this case $\tau = T$, thus all odd modes of the base frequency, i.e. $(2n+1)\frac{\omega_0}{2\pi}, n \geq 0$, are enhanced and the effective lower frequencies are attenuated. To implement pre-emphasis in the driver hardware, constraints have to be met in order to either set the parameter appropriately or setting up a finite programmable parameter space for a, b and τ. This requires knowledge about the TML in use. To understand the effects of material properties and TML design an analytic model of a differential cable is presented next.

3.6 Analytic Solution of special Differential TML Model

A cross-section of a differential cable model, and its admittance is depicted in figure 3.9. The model accounts for parasitic resistances at the interface of components, e.g. conductor to dielectric. This model can be expanded by the longitudinal equivalent circuit resulting into the complete model shown in figure

3.10.

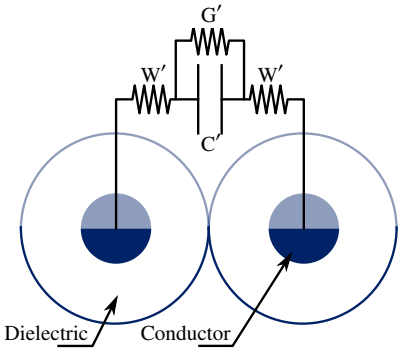


Figure 3.9: Transverse sketch of a simple differential cable model. Two conductors are isolated via dielectric material.

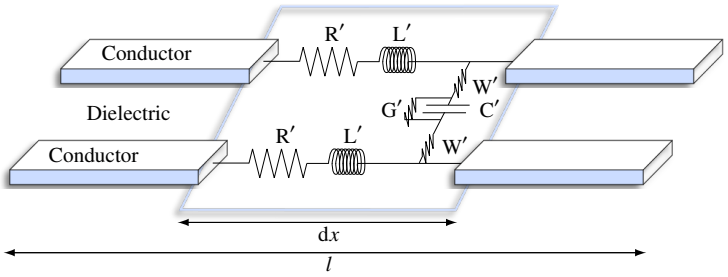


Figure 3.10: Complete differential TML model.

		Description
R′	$[\Omega m^{-1}]$	(DC) Series resistance of the conductor
L′	$[Hm^{-1}]$	Series Inductance of the conductor
W′	$[(\Omega m)^{-1}]$	(bleeder) leakage resistance
G′	$[(\Omega m)^{-1}]$	(bleeder) leakage resistance
C′	$[Fm^{-1}]$	Capacitive coupling of the conductors

Table 3.2: Description of the electric quantities of the TML Model shown in figure 3.10.

Table 3.2 summarises the electrical quantities of the model. All quantities are scaled to unit length. In case of odd-mode driven differential TML the symmetry of the model can be exploited to obtain the simplified equivalent circuit shown in figure 3.11.

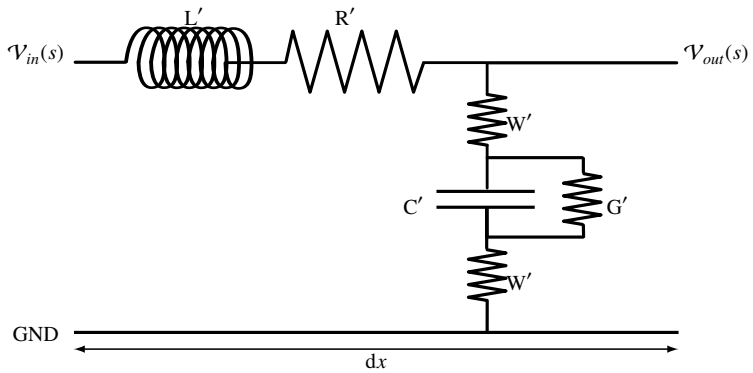


Figure 3.11: Advanced TML cable model with inductive, Ohmic resistive conductor and finite resistance of the dielectric.

From this model the transfer function can be derived by setting up the PDE with boundary conditions, e.g. introducing termination [20]. For terminated TML with load impedance Z_L, the transfer function is

given by equation 3.25.

$$\mathcal{T}(s) = \frac{Z_L}{\sinh(\kappa(s) \cdot l) + Z_L \cdot \cosh(\kappa(s) \cdot l)} \tag{3.25}$$

with

$$\kappa(s) = \sqrt{\mathrm{W} \cdot \frac{\mathrm{LC} \cdot s^2 + (\mathrm{GL} + \mathrm{RC}) \cdot s + \mathrm{GR}}{2\mathrm{C} \cdot s + \mathrm{W}(1 + \frac{2\mathrm{G}}{\mathrm{W}})}}. \tag{3.26}$$

For this model we assume as the initial condition a uniformly distributed potential over the conductor and moreover $\Phi(x) = 0$. The form of equation 3.25 is independent of the specific topology of the model and only defined by the initial and boundary conditions. The complex function κ contains the information of the frequency behaviour. Equation 3.26 holds only for frequencies lower than

$$\omega_{Skin} = \frac{1}{\mu\sigma \cdot r^2} \tag{3.27}$$

where μ, σ and r are the absolute permeability, conductivity and radius of the conductor material. This frequency is defined by the Skin depth being equal to the radius of the conductor. Solving the diffusion equation 3.11 in the complex frequency domain, the specific resistance R' can be rewritten as $R'(s)$,[8]

$$\mathrm{R}' \to R'(s) = \frac{k_0}{\frac{2r}{\delta_{\mathrm{Skin}}(s)} - 1} \cdot s = \frac{k_0}{k_1 \cdot \sqrt{s} - 1} \cdot s = L'(s) \cdot s$$

with $k_0 = \mu \cdot (l \cdot \pi)^{-1}$ and $k_1 = 2r\sqrt{\mu \cdot \rho^{-1}}$, where r, ρ and μ represent the radius of the conductor, the resistivity ($1.68 \times 10^{-8}\,\Omega\mathrm{m}$) and absolute permeability of copper ($1.26 \times 10^{-6}\,\mathrm{Hm}^{-1}$) respectively. R' is constant for $\omega < \omega_{Skin}$ but increases with higher frequency as shown in figure 3.12. κ can be rewritten as

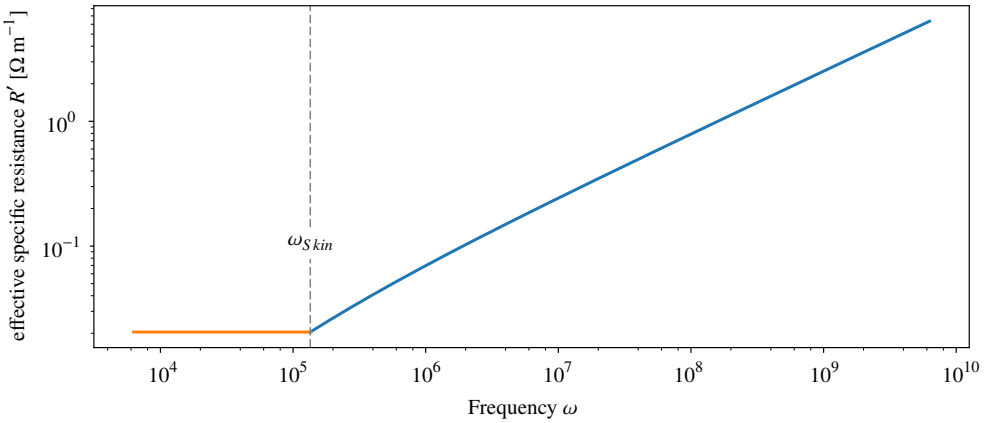


Figure 3.12: Effective specific resistance $|R'(s)|$ of copper with radius 511 μm plotted against frequency ω. Below ω_{Skin} the specific resistance remains constant.

[8] The Skin effect is only considered for the longitudinal resistance R'. It also affects W' and G'. We assume that W'^{-1} and G'^{-1} are large compared to R'. This is a valid assumption since the Ohmic loss should be minimal for high-bandwidth TML.

$$\kappa(s) = \sqrt{\mathrm{W}' \cdot \frac{\mathrm{C}'(\mathrm{L}' + L'(s)) \cdot s^2 + \mathrm{G}'(\mathrm{L}' + L'(s)) \cdot s}{2\mathrm{C}' \cdot s + \mathrm{W}'\left(1 + \frac{2\mathrm{G}'}{\mathrm{W}'}\right)}} = \sqrt{\mathrm{W}' \frac{\mathrm{C}' \cdot s^2 + \mathrm{G}' \cdot s}{2\mathrm{C}' \cdot s + \mathrm{W}'\left(1 + \frac{2\mathrm{G}'}{\mathrm{W}'}\right)} \cdot \mathcal{D}'(s)} \tag{3.28}$$

with $\mathcal{D}'(s) = \mathrm{L}' + L'(s)$.[9] The change of the initial equivalent circuit is shown in figure 3.13 to 3.14.

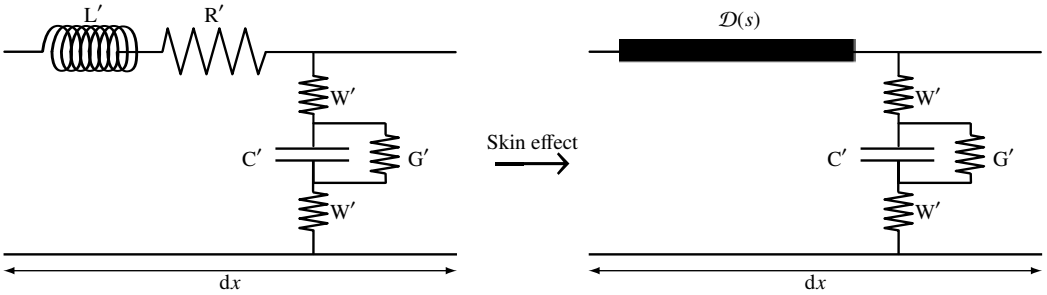


Figure 3.13: Equivalent circuit for an advanced cable model without Skin effect.

Figure 3.14: Equivalent circuit for an advanced cable model with Skin effect.

There is one special case to be mentioned in which $\kappa(s)$ can be simplified for Very-Large-Scale-Integration (VLSI) designs. For short metal traces on chip the serial inductance L and the leakage resistances W and G can be neglected. Thus a RC model is convenient with $\kappa(s) = \sqrt{\mathrm{RC}s}$.

To obtain the frequency dependent attenuation the amplitude $\mathcal{A}$ of the transfer function 3.25 has to be calculated. The amplitude of the transfer function with boundary conditions for terminated end $Z(x = l) = Z_L = Z_0$ is given by equation 3.29. The corresponding differential TML setup is depicted in figure 3.15.

$$|\mathcal{T}(s)|_{term}(\omega)|_{\alpha=0} = \sqrt{\frac{2 \cdot {Z_L}^2}{\left(1 + {Z_L}^2\right)\cosh(2\rho(\omega) \cdot l) + \left({Z_L}^2 - 1\right)\cos(2\epsilon(\omega) \cdot l) + 2{Z_L}^2 \sinh(2\rho(\omega) \cdot l)}} \tag{3.29}$$

$$\rho(\omega, \alpha = 0) = \mathrm{Re}\,\kappa(s), \quad \epsilon(\omega, \alpha = 0) = \mathrm{Im}\,\kappa(s) \tag{3.30}$$

In the open-ended case $\lim_{Z_L \to \infty} |\mathcal{T}(s)|_{term}$ equation 3.29 results in

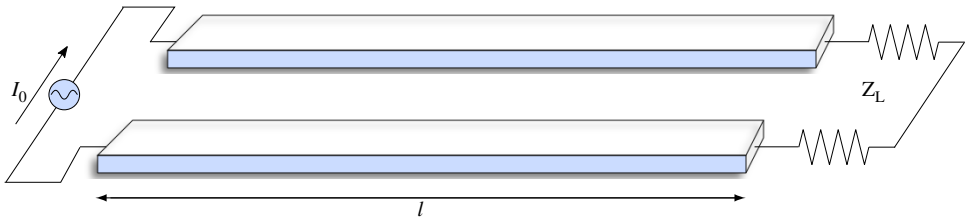


Figure 3.15: Differential TML with termination impedance Z_L.

$$|\mathcal{T}(s)|_{open}(\omega)|_{\alpha=0} = \sqrt{\frac{2}{\cosh(2\rho(s) \cdot l) + \cos(2\epsilon(s) \cdot l) + 2\sinh(2\rho(s) \cdot l)}} \tag{3.31}$$

[9] $\mathcal{D}'(s)$ has units of Hm^{-1} and can be interpreted as a frequency dependent inductance.

The characteristic impedance Z_0, according to equation 3.6, 3.7 and 3.28 yields

$$Z_0 = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{\mathcal{D}(s) \cdot s}{\frac{2}{\mathrm{W}'} + \mathrm{G}' + \mathrm{C}' \cdot s}} = \sqrt{\frac{\mathrm{L}' + L'(s)}{\frac{2}{\mathrm{W}'s} + \frac{\mathrm{G}'}{s} + \mathrm{C}'}} \xrightarrow[\alpha \to 0]{\mathrm{Im}(s) \to \infty} \sqrt{\frac{\mathrm{L}}{\mathrm{C}}} \tag{3.32}$$

Figure 3.16 shows the attenuation and the characteristic impedance versus frequency, equation 3.29 and

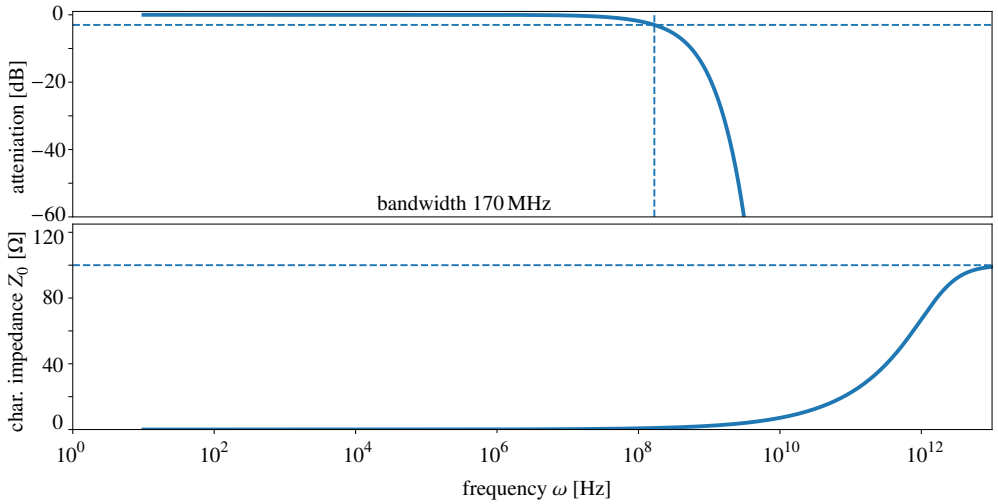


Figure 3.16: Example of the frequency dependent attenuation (top) and characteristic impedance (bottom) of the terminated TML model described by equation 3.29 with $Z_L = Z_0 = 100\,\Omega$ and length $l = 15\,\mathrm{m}$. Dashed lines (top) indicate the $-3\,\mathrm{dB}$ threshold for the bandwidth definition. Dashed line (bottom) is the $100\,\Omega$ marker.

3.32 for realistic cable properties with $Z_0 = 100\,\Omega$ and 15 m length. The cable is terminated with Z_0. Assuming a data stream with $1.6\,\mathrm{Gbits}^{-1}$. The base frequency is 800 MHz. If the data stream is 8b10b encoded, the number of consecutive same-valued bits is 5 and therefore the minimum effective frequency 160MHz. From figure 3.16 we read for the base frequency 800 MHz an attenuation of $-14.62\,\mathrm{dB}$ and for the lowest frequency 160 MHz, due to 8b10b encoding, $-2.87\,\mathrm{dB}$. In order to minimise the introduced inter-symbol interference one can add pre-emphasis on the signal to compensate the approximate 10 dB difference in amplitude.

Summary This parametrized cable model serves to obtain the characteristics of the Infiniband cables. The frequency behaviour of the cables, especially the bandwidth, is of importance for the correct choice with respect to signal integrity in the full TML system. Therefore studies of different cable geometries, i.e length and conductor diameter, have been performed and presented in section 6.2.

CHAPTER 4

The Data Handling Processor

The Data Handing Processor (DHP) is manufactured in 65 nm Complementary-Metal-Oxid Semicondutor (CMOS) technology and measures $2 \times 4\,\mathrm{mm}^2$ in size. The 65 nm CMOS process is an industrial standard since 2006 and therefore well under control. In contrast to the 10 nm state-of-the-art technology used in 2017/2018 for System-on-Chip (SoC) purposes the 65 nm technology is well known to be radiation hard up to TID ≤ 1 MGy [21][22]. The yield of functionally working chips (DHP) is approx. 98% (600 tested chips with a total processed area of $72\,\mathrm{cm}^2$), see section 4.3. The standard Static-Random-Access-Memory (SRAM) and register-memory cells are tolerant to single-event upsets (SEU) to a measured single bit cross-section of $9.7 \times 10^{-14}\,\mathrm{cm}^2$ (SRAM) and $6.4 \times 10^{-15}\,\mathrm{cm}^2$ (register) respectively [23].

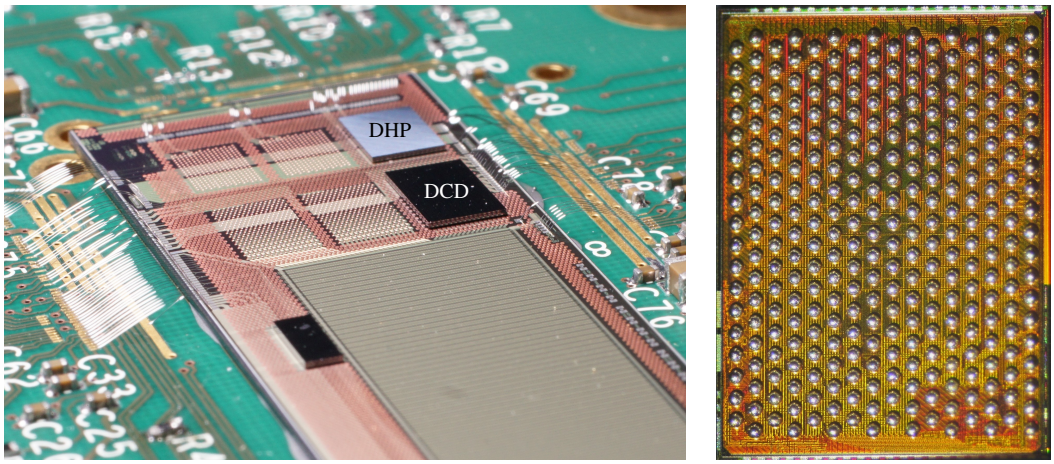


Figure 4.1: End-of-Stave (EOS) region of the PXD6 prototype with one pair of DHP and DCD (left). Bump bonds for electrical connection to the metallisation of the all silicon substrate of the PXD module (right).

4.1 Functional overview

The next paragraphs summarise the functional blocks of the DHP. The focus is on the data handling and communication with the on-module chips, DCD [16], the Switcher and the back-end system, e.g. DHE. For further information on the DHP read [24].

Configuration As an on-module controller steered by the back-end system, the DHP implements a configuration register. This register is a part of the full **Joint-Test-Action Group** (JTAG) chain [25]. The JTAG chain is a IEEE 1149.1 standard methodology to test and configure hardware and is used as the **Slow Control Environment**. The registers implemented are shift-register like and the hardware is daisy-chained. Data written into the registers triggers data to be read out. Thus checking for right configuration can be easily done by writing twice to the register. The JTAG chain on module is shown in figure 4.2. All on-module chips are connected in series via the JTAG chain. Configuration data, namely Test-Data Input (TDI), is sent by the back-end system and loaded into the dedicated registers of the chips. The present data in the registers are sent back via the Test-Data Output (TDO). The Test-Mode Select (TMS) signal is used to select the chip which configuration is aimed to be changed. The common clock, namely Test Clock (TCK), is used as the reference for the Slow Control. The configuration registers of

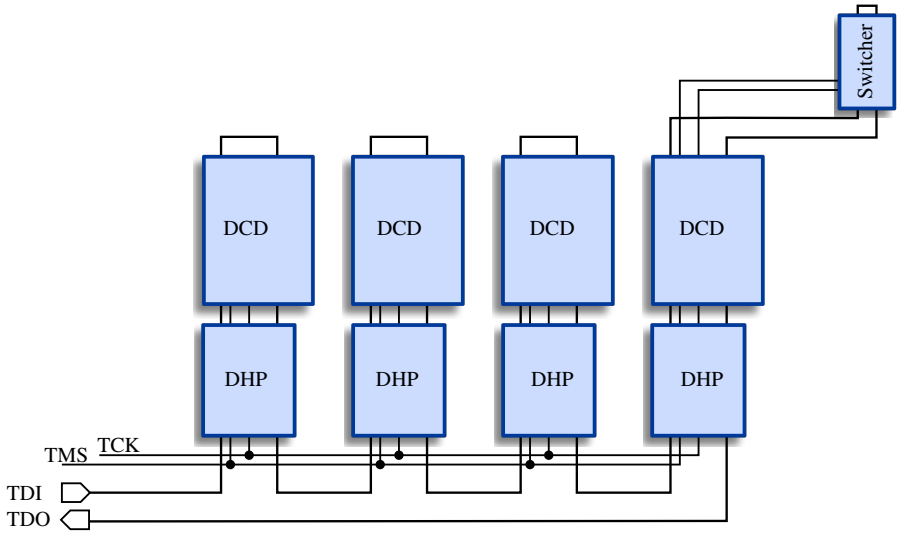


Figure 4.2: JTAG block diagram with four DHP- DCD pairs and one Switcher (indicating six Switcher in series). Configuration data TDI is send to the dedicated chip which is selected via TMS. TCK clocks the configuration registers of the chips.

the DHP have Hamming code implemented, a linear error-correcting code, to mitigate SEU [24]. The DHP contains two separate configuration registers 'global' and 'core' for analogue and digital purposes respectively. The **'global' register** incorporates settings for steering DACs, especially the currents for the LVDS tranceivers and CML driver, and global timing settings defining the communication between the on-module chips. The **'core' register** incorporates settings for the data processing and DHP internal digital synchronisation.

Memories The memories within the DHP are SRAM-cell blocks of 1024×256 bits and 1024×128 bits. There are four logical memories implemented, summarised in table 4.1. For each memory an eight-state state machine is used to read and write the data to the memory in order to refresh the content. The total size of the SRAM memories is 304 kB.

The **raw-data memory** stores 256 ADC values per address. The 9 bit address space can store ADC values that represent 512 gates of the matrix. The PXD9 has a total frame length of 192 gates, thus approx. 2.7 full frames can be stored. Therefore hits are buffered , in order to compensate for the latency between the physics event and the corresponding trigger. Two memory address pointers, read and write, are implemented. A latency value can be programmed in the 'core' register that defines the difference of

Memory	raw-data	pedestal	offset	switcher
Size [kB]	128	128	32	16

Table 4.1: Memories and their sizes within the DHP.

the values within the pointers.

The **pedestal memory** stores the ADC values of dark frames. Frames which have not been exposed to a radiative environment, e.g. active beam in the accelerator machine. With these pedestal data, fluctuations of drain currents from DEPFET pixel to pixel can be accounted for and compensated. The pedestal memory is logically divided into two sub block. A dedicated bit can be set in the configuration register to enable one of the two blocks. The memory size for the pedestal is equal to the raw data memory.

The **offset memory** stores the 2 bit values for adjusting the dynamic range of the ADC within the DCD. With these adjustments pedestal compression can be achieved. The values for the pedestals might vary over the full 8 bit range ($0-255$), thus no margin is left for real hit values, that lie higher than the pedestal distribution [26].

The **switcher memory** stores the sequence which is applied to the switcher to enable the DEPFET voltages. This sequence is important to operate the detector safely. The switcher memory is therefore sub divided in two logical blocks. The first block stores the normal-operation sequence. The second block is enabled via the steering signal *veto*. 4×32 bit words are read from the switcher memory storing the 32 bit sequences for all four switcher signals *clock*, *serIn*, *gate* and *clear*. The level sensitive *veto* signal enables the second block that stores the sequence for blinding the matrix against high irradiation doses induced by background.

External control The Back-end-read-out system, called Data Handling Engine (DHE) steers and clocks the DHP via the *trigger line* and the reference clock *gck* respectively. Four control signals, *rst*, *trg*, *mem_dump* and *veto*, are transmitted via Manchester coding over the trigger line. The signals are four-times time-multiplexed, thus one command has a length of 8 bit. A level sensitive global reset (*rst*) is subdivided into two states. A short *rst*, one command length of 8 *gck* cycles, reinitiates the framing block and the gigabit-serial link. A long *rst*, more than one command length, reinitiates the processing core with all state machines. Signal *trg* and *mem_dump* are used if zero suppressed data[1] or (partially) memory read-out[2] are needed. In order to protect the DEPFET pixel during beam injection into the storage rings that causes high background, e.g. Touschek, beam-gas scattering, Bhabha, etc., the *veto* flag enables the veto mode [15]. This mode switches to a Switcher sequence which is supposed to proect the charge located in the internal gate. Additional charge generated by background at injection are directly cleared by enabling a clear potential and charges are not accumulate in the internat gate [27].

ASIC interconnect The main purpose of the DHP is receiving and transmitting data from and to the periphery of the PXD. The radiation hard integrated circuits are located in the radiation-exposed volume

[1] Zero suppressed data corresponds to data containing hit information only. The common mode is subtracted and the true signal values are packed and send [24].

[2] Memory dumps are raw data read outs to obtain pedestal frames. These frames are taken in the absence of bunch crossings at the interaction point to extract information about absolute and time variation of e.g. leakage currents inside the DEPFET pixels. The pedestal information can be uploaded into the DHP pedestal memory to subtract from the total pixel value while zero suppressed read out is active.

while the back-end is shifted outside of this sensitive volume. The on-module chips are steered and synchronised by the DHP internal generated synchronisation signals.

- *fsync* (frame-synchronisation)
  - aligns the raw-memory write-pointer and the switcher memory read-pointer.
  - its period is programmable.
  - periodically resets the raw-memory write-pointer and the switcher memory read-pointer to zero.
- *row2sync* (row-to-synchronisation)
  - triggers the data conversion within the DCD.
  - aligns data conversion start (DCD) and gate selection (Switcher).

The functional block diagram is shown in figure 4.3.

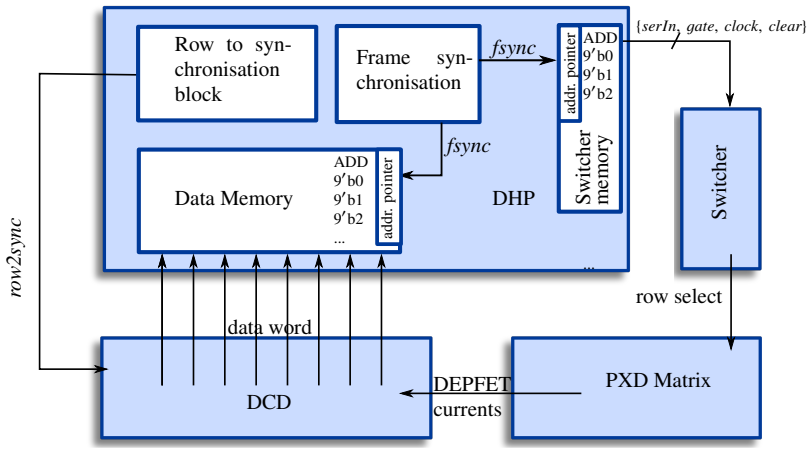


Figure 4.3: Functional block diagram of the control signals which are generated inside the DHP for the peripheral ASICS. The frame-synchronisation logic block handles the gate selection on the matrix and the corresponding memory location on the chip while the row-to-synchronisation logic block steers the DCD conversion.

The *fsync* is a periodically generated signal used to synchronise the raw-data memory-address pointer and the corresponding switcher memory read-pointer. Thus data of the selected gate on the matrix is stored on the proper memory location. The period of the *fsync* signal is programmable inside the DHP to adjust for different matrix sizes. The four differential signals are sent to the Switcher, namely *serIn*, *clock*, *gate* and *clear*, see figure 4.4. These timing signals define the sequence of the voltages that are applied to the DEPFET pixels. The *clock* signal is used to step through the matrix gate by gate, called rolling-shutter mode [27].[3] The *serIn* signal is used to reset the gate position selected by the Switcher, thus *fsync* and *serIn* have the same period to avoid interferences.

The second synchronisation signal *row2sync* triggers the data conversion within the DCD and resets it if the chip is running out of sync [16]. The DHP is sampling the digitised drain currents from the DCD. The interface of both chips is presented in figure 4.5. The analogue-digital converters (ADC) of the DCD

[3] Contrary to the ATLAS pixel detector the PXD read out scheme works sequentially. The pixel values are digitized and read gate after gate.

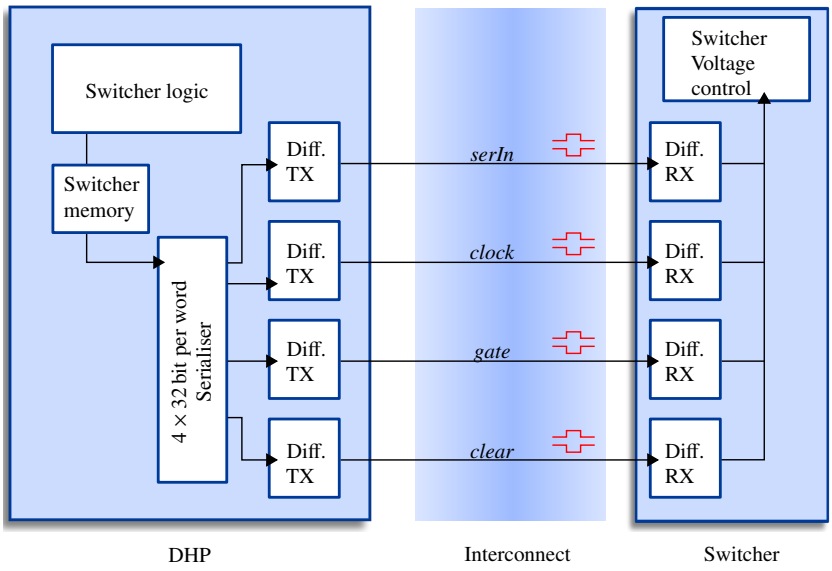


Figure 4.4: Block diagram of the interconnection of the Switcher and DHP. The steering signals *serIn*, *clock*, *gate* and *clear* are sent differentially to the Switcher enabling the DEPFET voltages according to the sequence stored in the switcher memory.

digitise the drain current with a resolution of 8 bit. Eight words are simultaneously transmitted to the DHP via 8 buses, i.e. 8×8 bit = 64 bit lines, with a bit rate of 320 Mbps. In order to reduce the amount

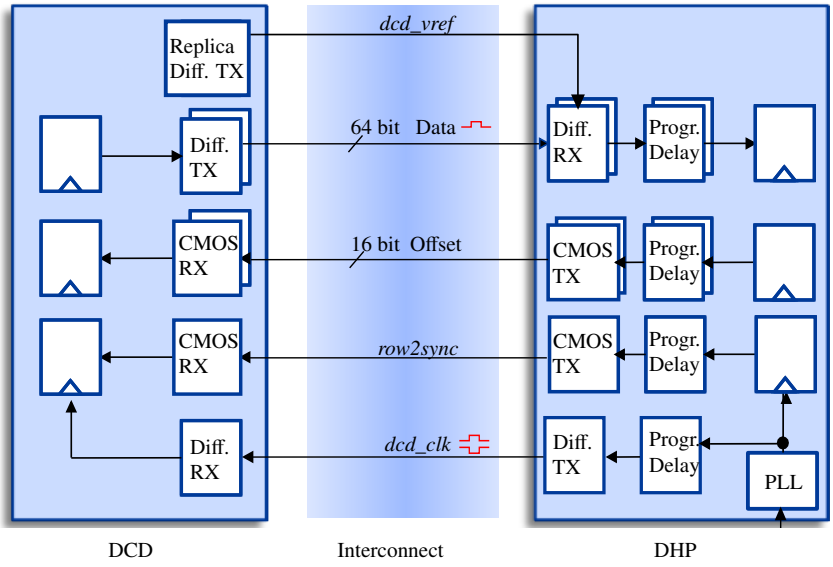


Figure 4.5: Block diagram of the interconnection of DCD and DHP.

of electrical connections between the DCD and DHP only one of the LVDS TX ouputs are connected for each bus. Because of this the differential LVDS receivers of the DHP needs the reference threshold of a replica of the differential transmitter of the DCD [16]. The DCD is clocked by a 320 MHz reference clock (*dcd_clk*) generated inside the phase-locked loop (PLL) of the DHP. Adjustment of the dynamic range of the DCD is possible by 2 bit words that are sent from the DHP offset memory to the DCD via 8 buses,

i.e. 16 bit line [26]. Since the data words are sent in parallel the sampling point (point within the unit interval) of the receivers have to be adjusted in order to compensate relative phase shifts of single bits. This can be done by programmable delay elements implemented via inverter chains. The propagation time of the inverters defines the delay. 4 bit registers are available for each delay element in the 'global' configuration register.

The frequency of the rolling-shutter mode is approx. 50 kHz. This translates into a conversion window of approx. 100 ns per gate. One complete gate is digitised by the DCD within 32 *dcd_clk* cycles. The deserialiser of the DHP crosses the *dcd_clk* and *gck* domain by four times time-multiplexing, thus 8 *gck* clock cycles are needed for one gate to be stored.

Data Handler The raw-data memory of the DHP is constantly refreshed by new pixel data according to the rolling shutter mode of the PXD detector. The triggering scheme is shown in figure 4.6. Each pixel data set belonging to one gate (256 bytes) is digitised by the DCD within 32 DCD clock cycles and stored as one word in the raw data memory of the DHP. Corresponding pedestals can be stored in the pedestal memory. The position of the active gate and the storage address of the raw data memory can be aligned. This can be achieved by two programmable 'latencies' with resolutions 4 and 2 *dcd_clk* cycles. If an event occurs an active *trg* is send via the *trigger line* to the DHP. To compensate for the delay between the event and the corresponding triggering a 'latency' can be programmed within the DHP. This latency is constant and is defined once. The triggering mechanism is shown in figure 4.6. An incoming *trg* word is decoded within 8 *gck* clock cycles. The trigger flag enables the data processing chain. The processing chain enables the zero-suppression mode while the trigger signal is high. Thus zero-suppression is level sensitive to the trigger signal. Starting from the active memory address the data is sequentially fed into the Data Processing block. The frame size, i.e. the total number of gates read, is programmable. The data processing block consists of the common mode computation and the hit finder. The common mode is computed by the double sparse algorithm [24]. The hit finder compares the pre-processed data against a programmable threshold. In order to subtract pedestal values from the raw data the pedestal memory of the DHP is used. Additionally a global pedestal can be programmed and subtracted. The resultant data value is proportional to the signal strength of the corresponding pixel. Data values exceeding the programmable threshold are marked as hits. All hits are packed and framed as shown in the figure 4.7. The first 16 bit word contains information of the row ID and the corresponding 5 bit CM value. The second word contains the column ID and the corresponding hit value (ADC value). The next words represent the further hits within the Row ID. This repeats for all row IDs which contain hits.

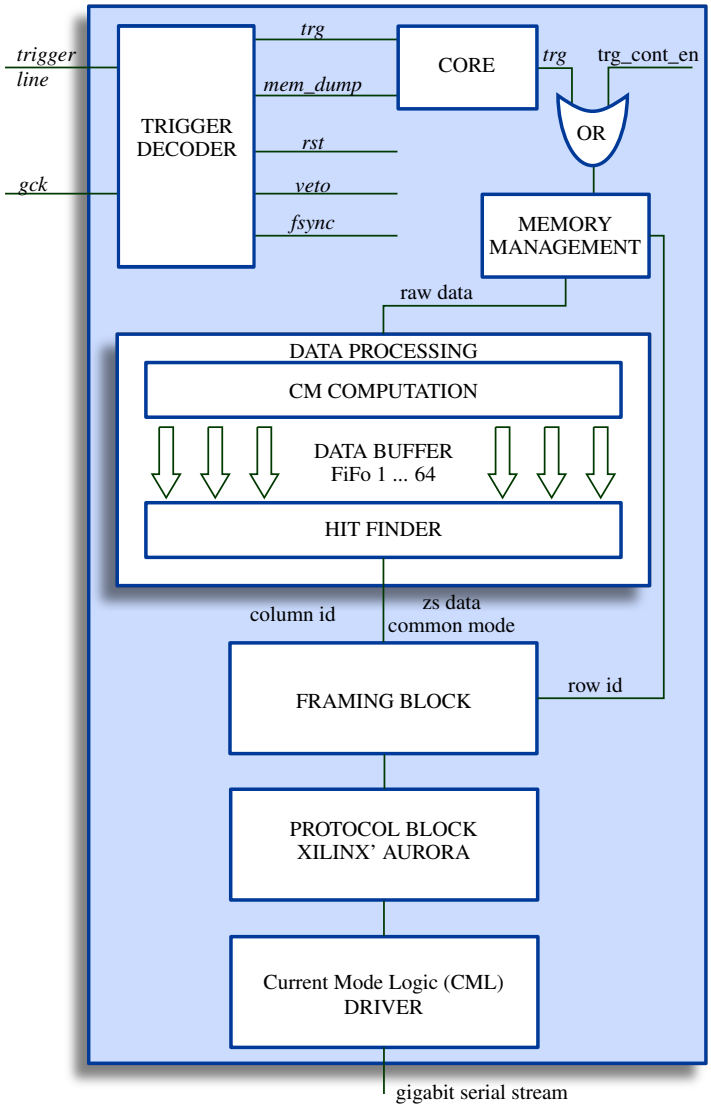


Figure 4.6: Triggering scheme and data flow inside the DHP. Trigger enables the data processing chain and hits are packed within frames that are serialised and send with the Serial driver.

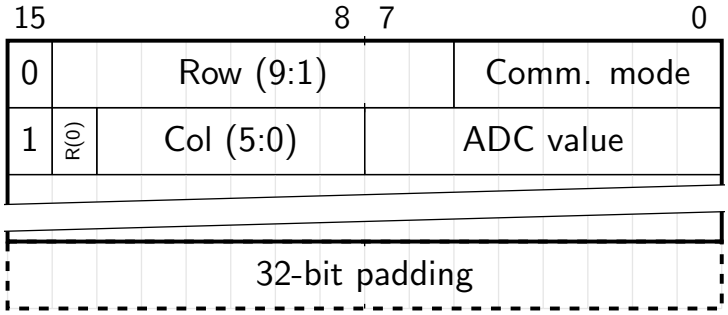


Figure 4.7: Frame representation of the packed data sent by the DHP.

4.2 Characterisation of DHP data processing

4.2.1 Queue model for Hit finder

In order to reduce the ~ 20 Gbps data rate coming from the DCD, the DHP has to perform a data reduction of factor ~ 16.[4] The reduction scheme is implemented via zero suppressed data output. Only data corresponding to hits are sent. The hit finder and the common mode computation of the single matrix gates are discussed in [24]. One row of data corresponding to one quarter of the geometrical row of the matrix, i.e. 64 data words, is fed in parallel into the 64 FiFos. Hence H hits in the row occupies H FiFos in the Buffer simultaneously. The achievable hit extraction rate H_0 is designed to be 2 hits per row, resulting in a maximum hit occupancy of 3%. This number is essential as higher occupancy directly results in possible data loss in the processing chain of the DHP by buffer overflow.

Here we focus on the performance of the data reduction and therefore a top layer model is presented, see figure 4.8. Due to the input data rate ν the 64 FiFos[5](buffer) are filled. Depending on the number of

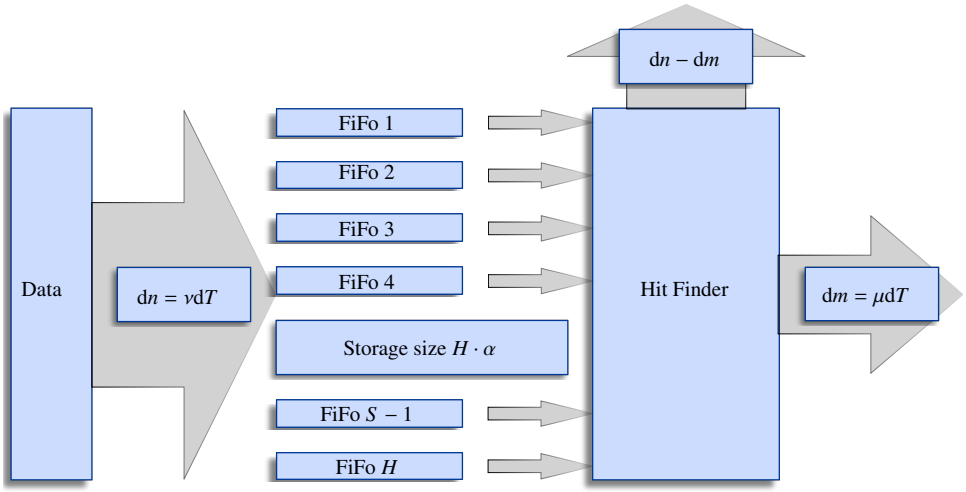


Figure 4.8: Data flow model of the hit finder implemented in the DHP. Data loss dn − d$m$due to imbalanced data input rate ν and output rate μ.

hits per row H the total number of hits stored is variable. We assume the worst case scenario, namely all hits of all incoming rows are placed at the same column (fed into the same FiFo). Thus one FiFo is filled after α rows, where α is the depth of the FiFo. The total storage size is $H \cdot \alpha$. The output rate of the hit finder is μ and the data rate related to lost data by buffer overflow is the difference of input and output data rate $\nu - \mu$. The equilibrium condition, i.e. no data loss, is met, if the difference of the number of inserted n and removed m hits per row is equal to the total number of hits in the buffer.

$$\mathrm{d}n - \mathrm{d}m = H \cdot \alpha \tag{4.1}$$

with $\mathrm{d}m = (\nu \cdot \Theta(H_0 - H) + \mu \cdot \Theta(H - H_0))\,\mathrm{d}T$, where H_0 is the maximum number of hits that can be removed, H the number of hits, Θ the Heaviside function and ν, μ the data rate of the hit finder output without and with data loss. The complete relation between the time without data loss T and the number

[4] This number results from the effective maximum data rate output of the DHP, namely $8/10 \cdot 20\mathrm{GCK} = 1.24$ Gbps - 8b10b encoding. Thus reduction factor $20/1.24 \sim 16$.

[5] FiFos is the acronym of First-in-First-out and can be implemented as a shift register.

of hits H can be written as

$$T(H;\alpha,\nu,m) = \frac{H \cdot \alpha}{n-m} \tag{4.2}$$

To verify this model and to extract the maximal hit removal H_0, in order to compare it to the designed value of 2 hits per row (2 clock cycles), the time without data loss T is recorded depending on the number of hits per row H and plotted in figure 4.9. In case of two hits per row or less $H \leq 2$ no errors occur, and thus no data loss is present in the system. With increasing number of hits per row the error rate increases and the time without errors decreases. The minimal time asymptotically approaches the time corresponding to the FiFo depth α. The fit of the top layer model 4.2 is shown in figure 4.10. The best fit, least squares, is only valid for number of hits per row $H > 6$. The fitted parameters deviate from the

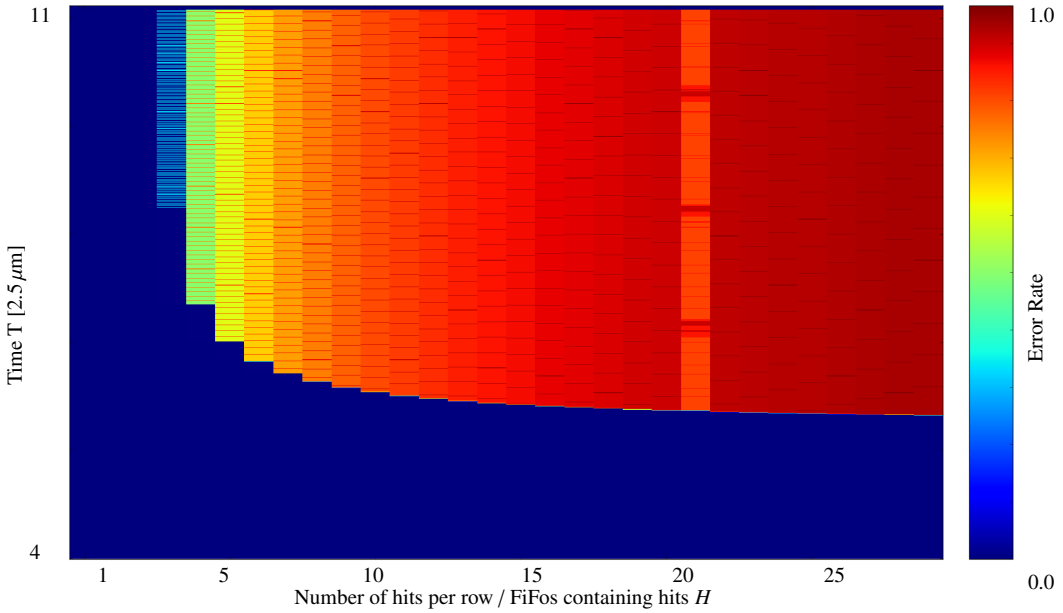


Figure 4.9: Error rate as a function of the number of hits in the FiFo array of the hit finder. For more than two hits per row the FiFo depth is not sufficient to temporally store the data.

designed ones. This has two implications;

1. The top layer model is not sufficient to describe the implementation of the fit removal in the DHP.

2. The deviation is simply reflected by quantisation error of the variable space (T, H)

The model implies a steady state condition for the FiFo depth α. This is not true for a dynamic system since the effective FiFo depth is enlarged by assuming that for each removed hit per cycle a new hit can be inserted and therefore the effective FiFo depth is dependent on the number of FiFos simultaneously containing hits,

$$\alpha_{\text{eff}} = \alpha_{\text{design}} \left(1 + \left(\text{ceil}\left(\frac{H}{H_0}\right)\right)^{-1}\right)$$

Using the above correction for the FiFo depth one can show that the fit resembles the data to a precision

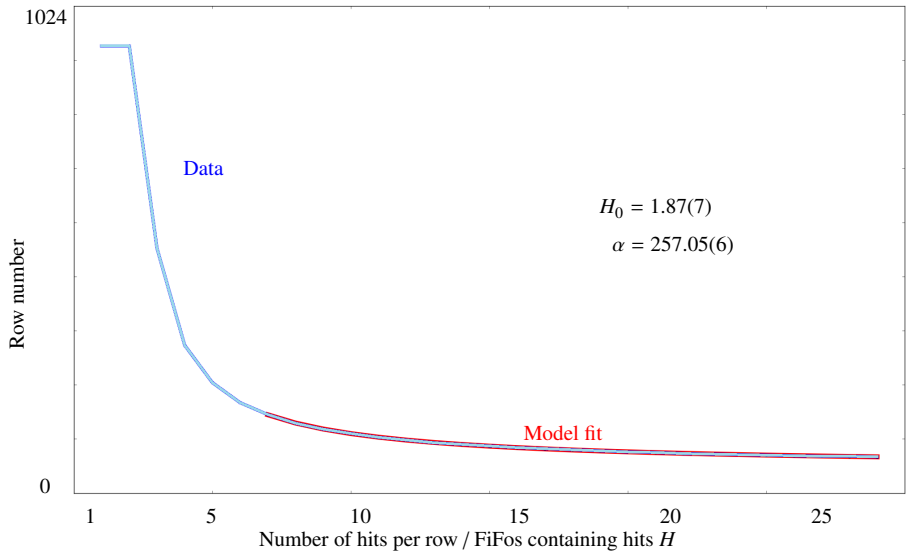


Figure 4.10: Fit of the top layer model to the measured data. The model describes the data for hits per row larger than 6 in a sufficient good approximation.

of less than 1%, see figure 4.11. The complete relation is

$$T(H;\alpha_{\text{design}},H_0) = \frac{H\alpha_{\text{design}} \cdot \left(1 + \frac{1}{\text{ceil}\left(\frac{H}{H_0}\right)}\right)}{n - (n \cdot \Theta(H_0 - H) + m \cdot \Theta(H - H_0))}. \tag{4.3}$$

The extracted parameter (H_0, α_{design}) show still some deviations apart from the fact that the corrected dynamic FiFO size has been introduced. The reason for this deviation is the common mode calculation. The common mode is calculated for each row. Thus hit distribution over many rows will demand more calculations. In addition the common mode calculation adds one additional clock cycle to the total computation [28]. This reduced the effective maximum hit removal rate H_0. The dynamics of the system increases the effective FiFo depth α. Table 4.2 shows the comparison of designed and effective parameters for the hit finder implementation of the DHP. The effective buffer depth is enlarged by two hits that is expected because of the hit extraction rate of approx. 2 per row. The DHP is therefore capable to cope

	designed	fitted (effective)
H_0	2	1.83(5)
α	256	258.05(3)

Table 4.2: Comparison of the designed hit removal rate H_0 and FiFo depth α with the effective parameters extracted via the top layer model fit.

with a continuous occupancy of up to 3%.

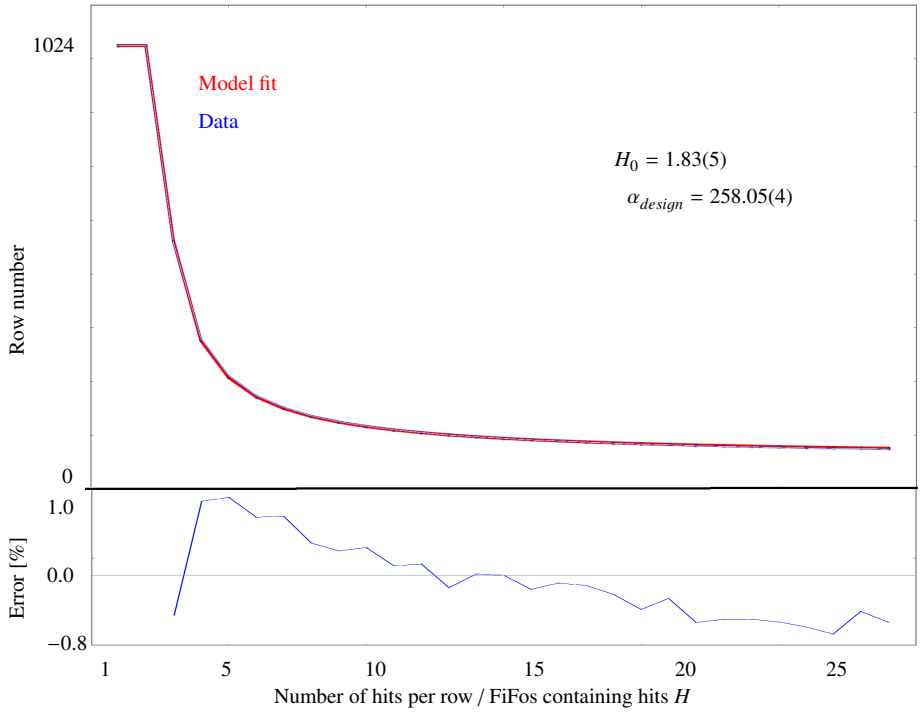


Figure 4.11: Fit of the top layer model with effective FiFo α_{eff} depth to the measured data.

4.2.2 Characterisation of DHP CML driver

The driving capability of the DHP is defined by its Current Mode Logic Driver (CML TX). This driver consists of a two stage differential driver as shown in figure 4.12. The first stage consists of two 50 Ω pull-up resistors and two NMOS transistors. The signal to be transmitted is first amplified by a differential pre-amplifier (not shown). The differential signal $(S, \bar{S})$ is connected to the two input gates of the first stage. The complementary switching of the NMOS transistors enables the current, which is defined by a current sink I_B, to flow trough the TML and the 100 Ω termination resistor at the far end of the TML, i.e. located close to the receiver. The voltage drop at the termination resistor defines the output swing of the differential output signal. The second stage is a copy of the first stage, but has two major differences,

1. The drain potential of the NMOS transistors are connected to the output of the first stage (TX_N, TX_P).

2. The signals connected to the two input gates of the second stage are delayed with respect to $(S, \bar{S})$, denoted as $(S_\tau, \bar{S}_\tau)$, and connected oppositely.

The common mode is defined by CM = $^1/_2 \cdot (V_{hi} - V_{lo})$ where the high/low potential denotes the high/low potential at the termination resistor and therefore the output voltage swing.

To reveal the working principle of the pre-emphasis driver, the time domain waveform is shown in figure 4.13. The parameters I_B, I_{BD} and τ are programmable via registers in the DHP. The shape of the output waveform resembles the amplification of the high frequency part (edges) of the signal spectrum. The low frequency part (plateau) is attenuated. This is the implementation of the pre-emphasis in the DHP. τ defines the frequency range in which the signal is amplified by the strength $^{I_{BD}}/_2$ [21].

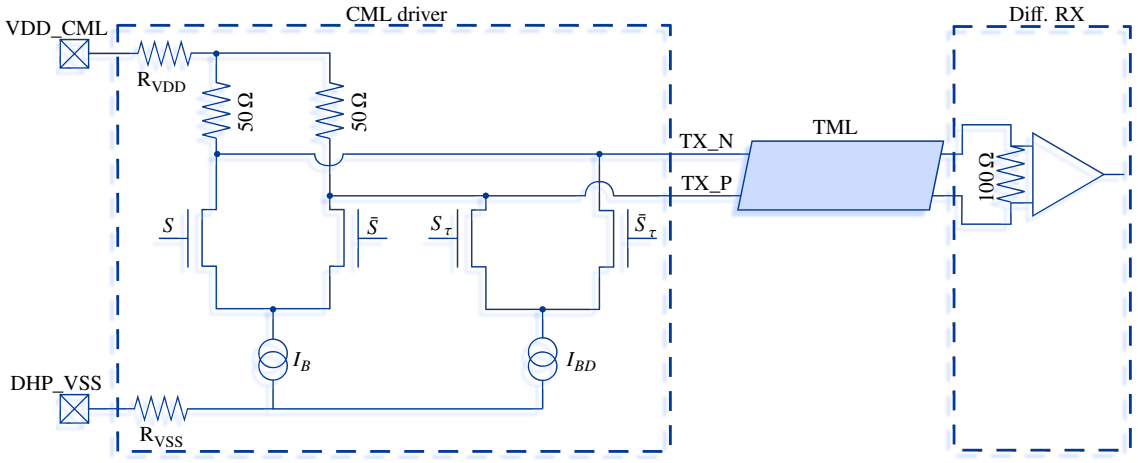


Figure 4.12: Simplified schematics of the CML driver with main and pre-emphasis stage.

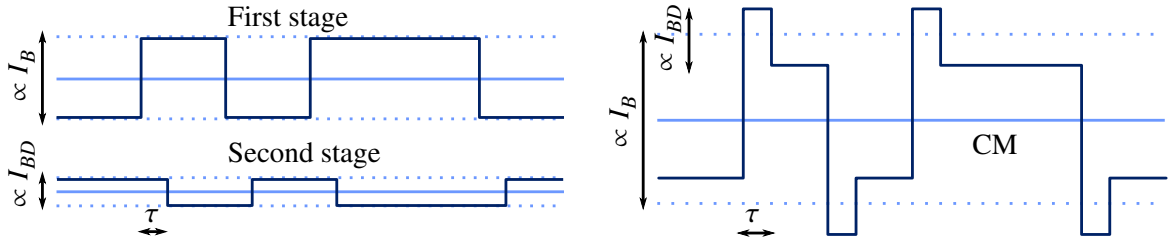


Figure 4.13: Working principle of the CML driver in the time domain (left). Time domain waveform of the CML driver output TX_N / TX_P with enabled pre emphasis (right).

Detailed schematics An in-depth schematic, equivalent to the real implementation of the CML driver, is depicted in figure 4.14. The main driver consists of the input transistors MØ and M1 and the current mirror M2M3, consisting of M2 and M3, with a mirror ratio of 1 : 20. The current set by DAC 'BIAS' defines the source-drain current of M3, thus the source-gate voltage adjusts according to the output current. This current is mirrored with a factor 20 to M2. Due to the topology of the driver, the maximum expected source-drain I_{ds} current of M2 is limited to roughly 19 mA.[6] The current mirror M67 of the pre-emphasis stage has a ratio of 1 : 2 and is steered by the DAC 'BIASD'. The biasing circuit within the DHP is designed by the University of Barcelona. The unit cells, referenced as 'UBDAC', provide a current output of 1 μA per bias setting. The cell is powered by DHP_VDD and has a linear output characteristic for the full 8 bit range of the current steering DACs.

Biasing scheme of DHP CML driver The biasing scheme of the current mirror M2M3 is show in figure 4.15. Current mirror M6M7 for the pre-emphasis part is biased in the same way. The maximum output current of the UBDAC cell is 255 μA and programmable via the JTAG interface. This current is multiplied by two current mirrors with ratios 1 : 4 for M10M11 and 1 : 3 for M8M9 resulting in a total multiplication of 12 and a total current of 3.06 mA biasing the current mirror M2M3 of the main stage of the CML driver. In order to access the the drain potential of the steering NMOS transistor M3 of the main current mirror M23 a test point, named CML_ITX, has been introduced in the design. Such test

[6] M2 is working in the saturation region $V_{ds} > V_{ov} = V_{gs} - V_{thr} > 0$ where V_{ov} is called the overdrive. In this case I_{ds} is independent of V_{ds}. I_{ds} passes, if the output is properly terminated with 100 Ω, a total resistance of (50 ‖ 150) Ω = 37.5 Ω. Assuming a threshold voltage of 480 mV for the PMOS a minimum $V_{ds} = V_{thr} = 480$ mV is required that results in a maximum current output $I_{ds} = \frac{VDD\_CML - 0.48\,\mathrm{V}}{37.5\,\Omega} = 19.2$ mA.

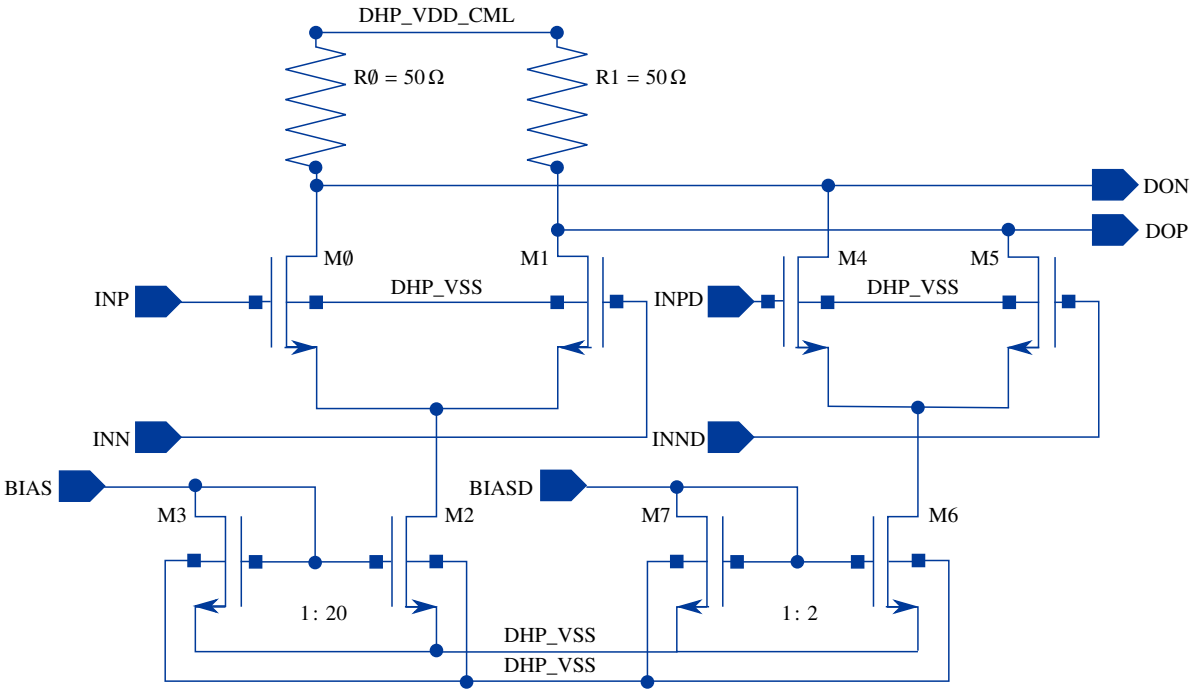


Figure 4.14: Transistor level schematics of the Current Mode Logic driver with DACs for the main stage, BIAS, and the pre-emphasis stage, BIASD.

points have also been introduced for the pre-emphasis stage (CML_ITXD) and the PLL (PLL_ILS), see figure 4.16. External pads are always connected to an electrostatic discharge (ESD) protection circuit consisting of diodes opening if voltages are applied to the pad that exceeds the supply voltage of the circuit, i.e. DHP_VDD_CML = 1.2 V. Any induced charge will flow through the diodes and protect the internal circuit. In DHP v1.1. the output of the multiplication circuit is wrongly connected to the main current mirror as shown in figure 4.15 (red connection line). In this case the steering current has to pass the ESD resistor (199 Ω). For DHP v1.2 the test pad connection has been corrected.

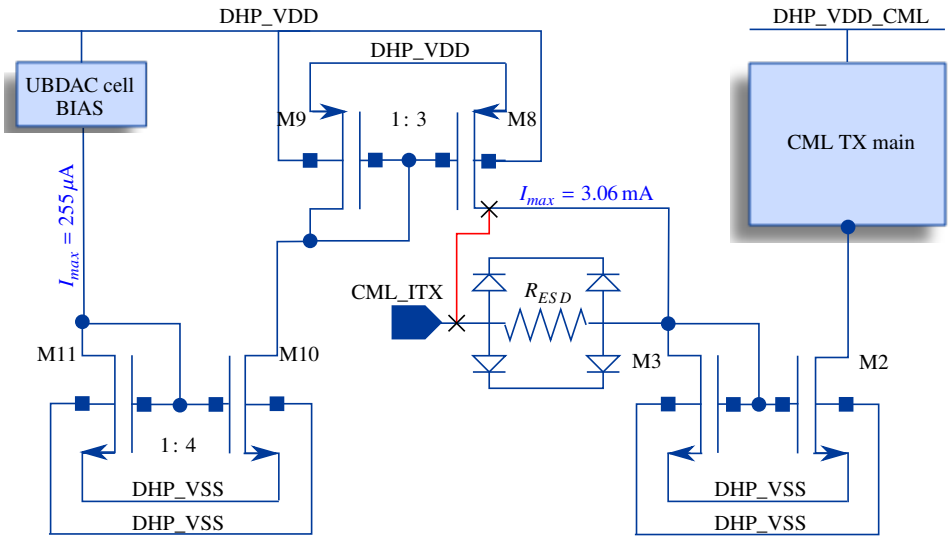


Figure 4.15: Biasing scheme of the main stage of the CML driver with UBDAC cell and multiplication stage.

Complete biasing scheme The CML block is placed on chip closely to the PLL block as shown in figure 4.16. The PLL and CML block is connected in series to the DHP_VSS line that represents the reference potential within the chip. The external DHP_VSS pad is connected to the DHP_VSS plane. The connection to the PLL and CML block is realised with vias that connect different layers within the chips. The ohmic resistance of one via is roughly 5 Ω. Proper biasing of the blocks therefore should have less than 5 Ω parasitic resistance, as indicated with R_{ILS}, R_{ITX} and R_{ITXD} in figure 4.16. Both blocks are biased by DHP_VDD_CML. Current drawn from DHP_VDD_CML causes, in case of non negligible parasitic resistances, the DHP_VSS potential to rise. This has a severe impact on the steering current mirrors of the CML block. For DHP v1.2 the connection to DHP_VSS has been improved in order to minimize the parasitic resistances. To understand the impact of the ESD resistor and the parasitic resistances of the DHP_VSS line a block diagram is shown in figure 4.17. It shows the PMOS M8 and NMOS M3 transistor connected in series with the parasitic resistances on the DHP_VSS line and the ESD resistor. The saturation voltages for the transistors of the 65 nm technology is roughly 480 mV and

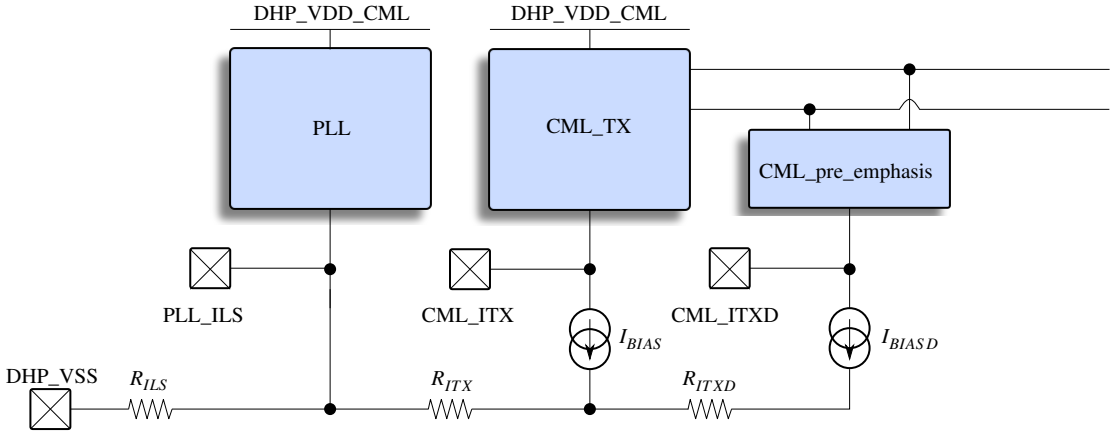


Figure 4.16: Block diagram of the DHP_VSS connecting scheme of the PLL and CML block.

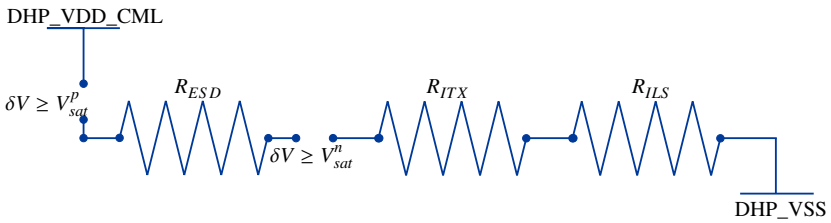


Figure 4.17: Equivalent biasing circuit diagram with parasitic resistances.

400 mV for P- and NMOS transistors respectively. Thus one can write for the maximal current allowed to be sunk is,

$$I^{max}(R_{ITX}, R_{VSS}) = \frac{\text{DHP\_VDD} - (V^p_{sat} + V^n_{sat})}{R_{ESD} + R_{ITX} + R_{VSS}} = \frac{0.32\,\text{V}}{199\,\Omega + R_{ITX} + R_{ILS}} \tag{4.4}$$

In case of DHP v1.1 the maximum current, if negligible parasitic resistance is assumed, i.e. $R_{ITX} = R_{ILS} = 0$, is 1.6 mA. Per design the maximum output current of the multiplication stage is 3.06 mA. The limitation is introduced by the ESD resistor. In case of DHP v1.2, where the ESD resistor is not connected in series anymore, the maximum current is only limited by the maximum output current of the multiplication stage, i.e. 3.06 mA. If parasitic resistances are not negligible the situation becomes worse

and the maximum current drops. To investigate R_{ILS} and R_{ITX} the pre-emphasis stage has been used as a current source.

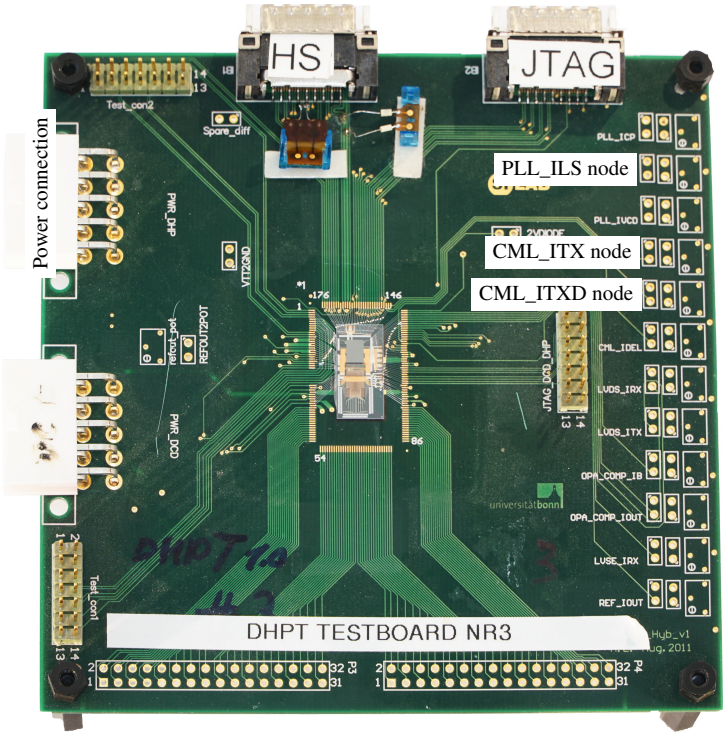


Figure 4.18: DHP test board for general purpose characterisation. Test nodes for measuring potentials of the CML driver are foreseen (right side).

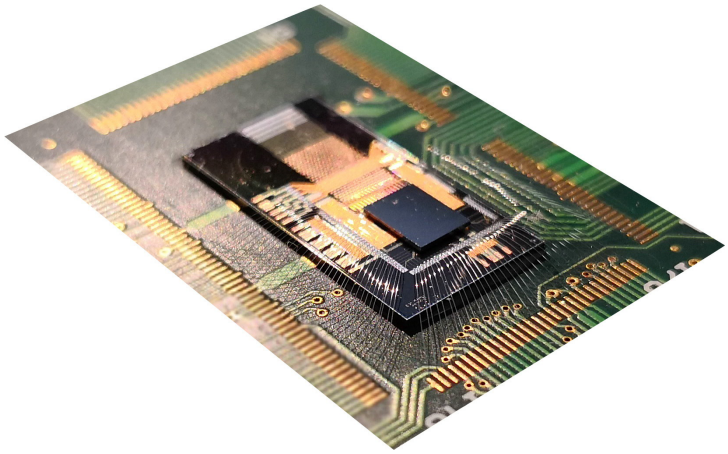


Figure 4.19: Wire-bond adapter with a bumb-bonded DHP v1.2. Wire-bonds connect the DHP with the test board.

Test system and results To test and verify the parasitic resistances a general purpose PCB for DHP testing has been used, see figure 4.18. A single DHP v1.2 is bump-bonded onto a silicon wire-bond adapter to connect via small (apprx. 100 μm thick) wire bonds to the PCB. The back-end of this system is a Xilinx ML-505 Evaluation board which embeds a Virtex-5 Filed-Programmable-Gate-Array (FPGA).

The FPGA has some functional parts of the DHE emulated. The fast *trigger line* as well as the slow control is established via the ML-505. The Interface used between PC and ML-505 is a Ethernet connection with UDP protocol. The configuration registers of the DHP have been constantly rewritten with new values for the pre-emphasis settings of the CML driver, settings 0 to 255. In order to extract the resistances the test nodes shown in figure 4.18 have been used to measure the potential. The currents drawn from the respective power rails have been measured. The resistances are given by Ohm's law and define the slope of the linear dependency, see figure 4.20. A linear fit with errors, on both, the currents and voltages, has been used to extract the slope that is a direct measure of the resistances between the test node and the external DHP_VSS pad. The maximal current draw by the two versions differs by a factor of approx. 2.5. The parasitic resistances are summarised in table 4.3. From the resistance values one can calculate the maximum current flow, see equation 4.4, in the multiplication stage.

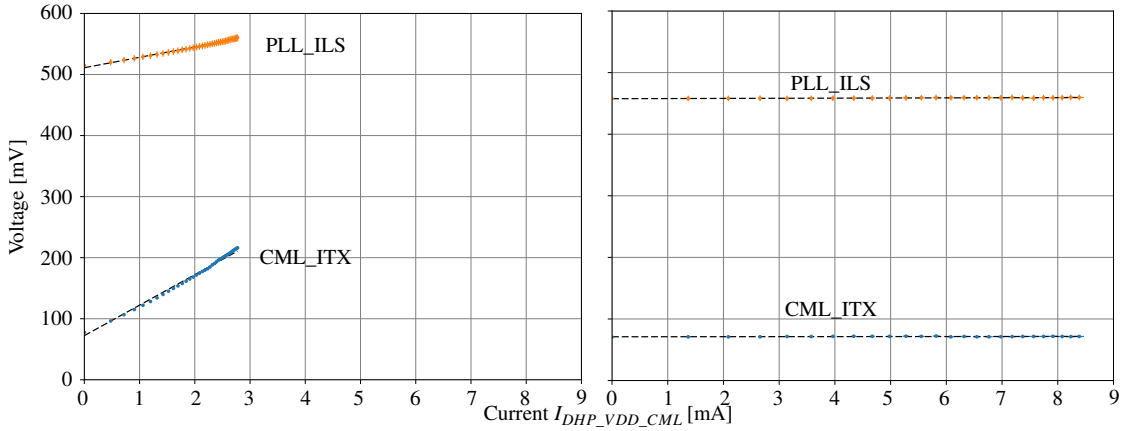


Figure 4.20: Voltage measurements at the nodes PLL_ILS and CML_ITX for DHP v1.1 (left) and DHP v1.2 (right). The slope of the voltage with respect to the current $I_{DHP\_VDD\_CML}$ is a direct measure of the parasitic resistance on the DHP_VSS line shown in figure 4.16.

DHP version	R_{ILS} [Ω]	$R_{ILS} + R_{ITX}$ [Ω]	R_{ITX} [Ω]	I_{max} [mA]
v1.1	17.1(2)	49.9(6)	32.8(6)	1.3 mA
v1.2	0.2(3)	0.6(3)	0.4(0)	3.06 mA

Table 4.3: Summary of the parasitic resistances of the DHP_VSS line and the maximum output current, according to equation 4.4, of the multiplication stage for DHP version v1.1 and v1.2.

As discussed earlier the wrongly connected ESD resistor cannot be the only cause to drive the multiplication stage out of saturation. Adding a DHP_VSS potential shift due to parasitic resistances it is indeed possible to shut off the current mirrors. In order to understand the implications of the presence of the parasitic resistances the current gain of the multiplication stage has been measured and plotted for both DHP versions, see figure 4.21.

In case of version v1.1 the gain of the multiplication stage decreases from 13.04(7) $^{\mu A}/_{DAC}$ to 3.79(2) $^{\mu A}/_{DAC}$. That is a drop of roughly 71%. The expected gain is $G_{M10M11} \times G_{M8M9} = 4 \times 3 = 12\,^{\mu A}/_{DAC}$ if both current mirrors are saturated. The second current mirror is driven out of saturation resulting in only a total gain of roughly $4\,^{\mu A}/_{DAC}$. This corresponds to the measured gain within a deviation of less than 10% compared to the designed values. The maximum current steered by the multiplication stage is 1.595(1) mA. This

deviates from the prior calculated maximum current of 1.3 mA using the parasitic resistances. One explanation of this discrepancy is originated by the saturation voltage of the P- and NMOS transistors used in the equivalent circuit, figure 4.17, which might be overestimated. Assuming $V_{sat}^{P} + V_{sat}^{N} = 0.8V$ the maximum output current is 1.61 mA. Since the saturation voltages are not exactly known due to the concealment of the manufacturer, a more precise estimation is not possible [29]. Process variations also might be a source of the deviation. Any wafer being processed underlie natural process variable fluctuations, like doping concentrations and therefore also fluctuations of switching characteristics of transistors. The maximum voltage swing at the termination resistor for DHP v1.1 is 243.15(1) mV. For v1.2 the gain drops from 16.2(1) $\mu A/_{DAC}$ to 10.82(3) $\mu A/_{DAC}$. This is a drop of 49.5%. The maximum current is 3.154(8) mA.

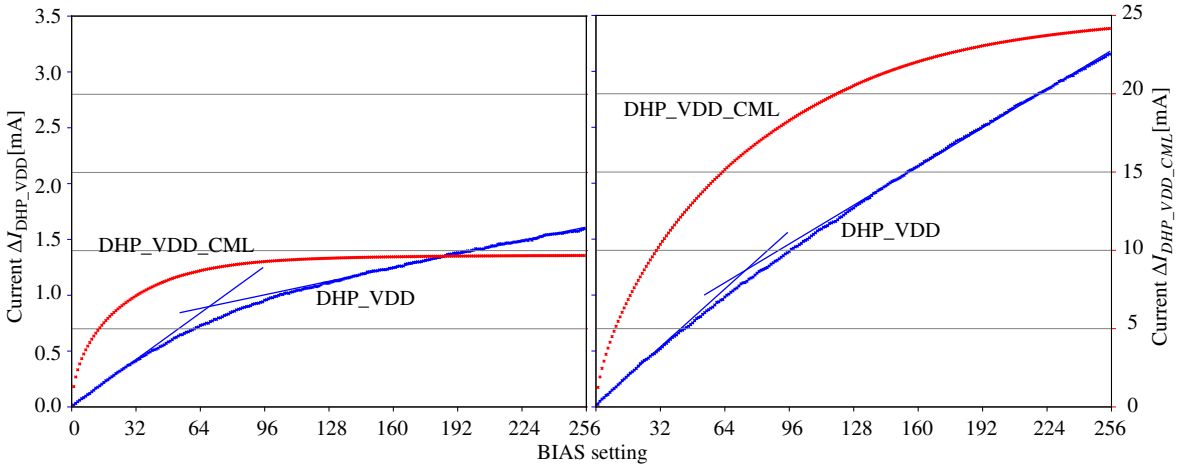


Figure 4.21: Current draw on DHP_VDD (blue) and DHP_VDD_CML (red) with respect to BIAS settings for DHP v1.1 (left) and DHP v1.2 (right). The slope of I_{DHP_VDD} with respect to the BIAS setting represents the gain of the current multiplication stage.

Comparing both plots in figure 4.21 one can deduce that the change in the ESD resistor connectivity and the minimisation of the parasitic resistances on DHP_VSS improves the driving capability of the CML driver. The maximum current of the main stage improved by a factor of 2.4 from 9.686(1) mA to 24.168(8) mA that relates to a output swing of 243.15(1) mV and 604.2(7) mV, respectively. The summary of the improvements of the CML driver from version v1.1 to v1.2 is shown in table 4.4.

DHP version	$I_{\text{main stage}}^{\max}$ [mA]	$V_{\text{output}}^{\max}$ [mV]
v1.1	9.686(1)	243.15(1)
v1.2	24.168(8)	604.2(7)

Table 4.4: Summary of the improvements of the CML driver current strength from DHP version v1.1 to v1.2.

Limits of the CML driver The topology of the CML driver has a major disadvantage. The dynamic range of the driver is defined by the supply voltage VDD_CML and the total series resistance. The total series resistance is 37.5 Ω. As discussed in the previous paragraphs, the maximum current drawn by the main stage is approx. 19 mA. If highest overall amplitude is foreseen and on top pre-emphasis is enabled, the CML driver is operated outside of its dynamic range. This has the following implications;

- The total current $I_B + I_{BD} < 19\,\text{mA}$
- If $I_B \approx 19\,\text{mA}$, no current can be added

Figure 4.22 shows recorded waveforms of the output of the CML driver of a DHP v1.2 for two cases of I_B. In the first case (left plot) maximum I_B is enabled and thus maximum overall amplitude is achieved. To show the limitations of the CML driver two waveforms are shown. The first without pre-emphasis enabled (blue), the second (orange) with enabled pre-emphasis. No enhancement of the high-frequency part is present. Only the attenuation of the low-frequency part is achieved. The second case (right plot) shows medium I_B. The two waveforms indicate no pre-emphasis enabled (blue) and maximum pre-emphasis enabled (orange). The high-frequency part is enhanced and the low-frequency part is attenuated. This limitation brings up different usage-scenarios;

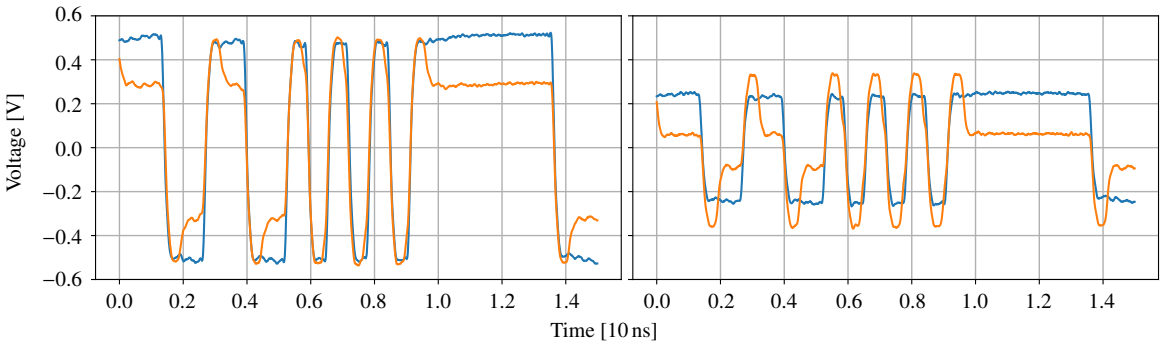


Figure 4.22: CML driver output of DHP v1.2 with pre-emphasis limitations. Signal is terminated and probed after 5 mm of diff. copper traces with $Z_0 = 100\,\Omega$ and 8 GHz active differential probe. Two scenarios are shown. With (blue) and without (orange) enabled pre-emphasis for maximum (left) and medium (right) I_B. For the medium case, enabled pre-emphasis enhance the high- and attenuates the low-frequency part.

1. If signals with high inter-symbol interference are transmitted use $\tau \approx$ bit-width.
   - If low-bandwidth TML is in use, spectrum shaping of data signal is more important than overall amplitude. Thus a medium I_B should be used to mitigate inter-symbol interference.
   - If medium-bandwidth TML is in use, spectrum shaping of data signals is of less interest. Thus a higher I_B should be used.

3. If a clock signal is transmitted use $\tau <<$ bit-width. Use medium I_B to achieve high spectrum reshaping to increase the slew rate of the clock signal.

For the purpose of sending data streams with 8b10b encoding τ should be approx. the bit-width. Figure 4.23 shows the waveforms for all four settings of τ.

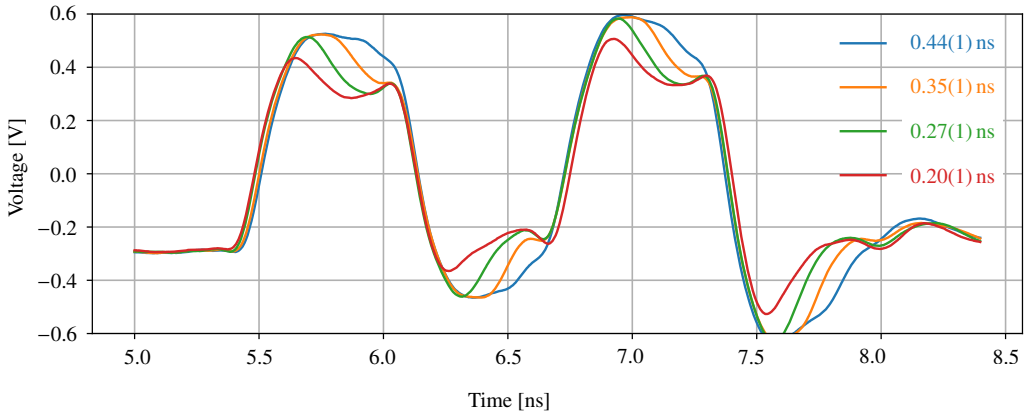


Figure 4.23: DHP CML driver output with all four pre-emphasis delay settings τ.

4.3 Mass Testing of DHPT 1.2

This section comprises an additional item in the chain of qualifying the signal integrity of the whole PXD chain: The indemnification of the functional quality and driving capability of each single DHP assembled on the modules inserted in the PXD. Therefore a verification environment has been developed according to the Universal Verification Methodology (UVM)[7] [30] to test the final DHP v1.2.

4.3.1 Verification environment

UVM sets guidelines to provide a robust framework for verification purposes. The Standard set up consists of constraints, tests and checker. The constrains are set due to the specification and the operation conditions and is therefore known a priori. The tests are sets of algorithms that are performed on the chip in order to test the functional behaviour. The last of the triplet is the checker. It logs the outcome of the tests and controls test parameters on run time. The environment is constantly checking if the

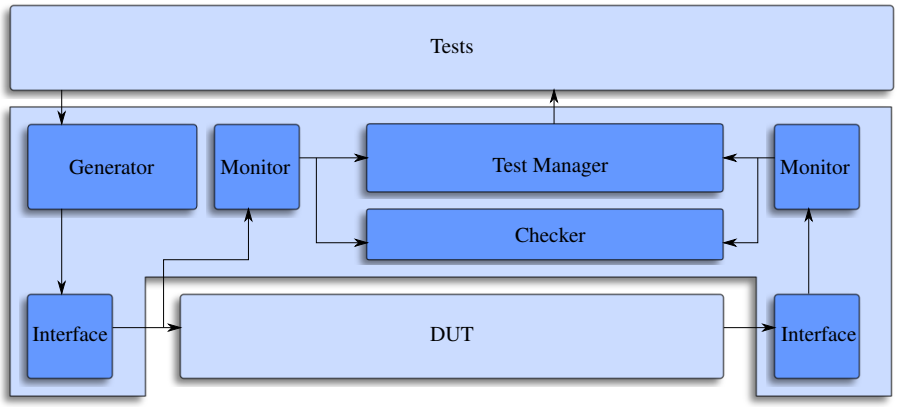


Figure 4.24: Standard verification environment setup according to UVM. Arrows indicate manipulation/feedback.

[7] UVM is a standard for digital verification and is used for pre silicon tests. It is not aimed to be used for mass production test, although it provides suitable guidance of how to set up a mass production environment.

behaviour is expected, i.e. the correct response to a given stimulus according to the specifications. This environment consists of two main layers, the hardware and software layer as shown in figure 4.25. Both layers consist of different implemented entities. The hardware layer contains the host pc with operating system 'Scientific Linux 7' and the needle card (plus probe station). The software layer on the other hand is the EPICS based and via python controlled read-out system. The interface between hardware and software layer is realised with the BASIL framework [31]. This framework is mainly developed and maintained by the Silicon Laboratory SILAB members of the Physics Institute of the University of Bonn. It incorporates Verilog based firmware and Python based driver implementations to easily set up a FPGA based test environment.

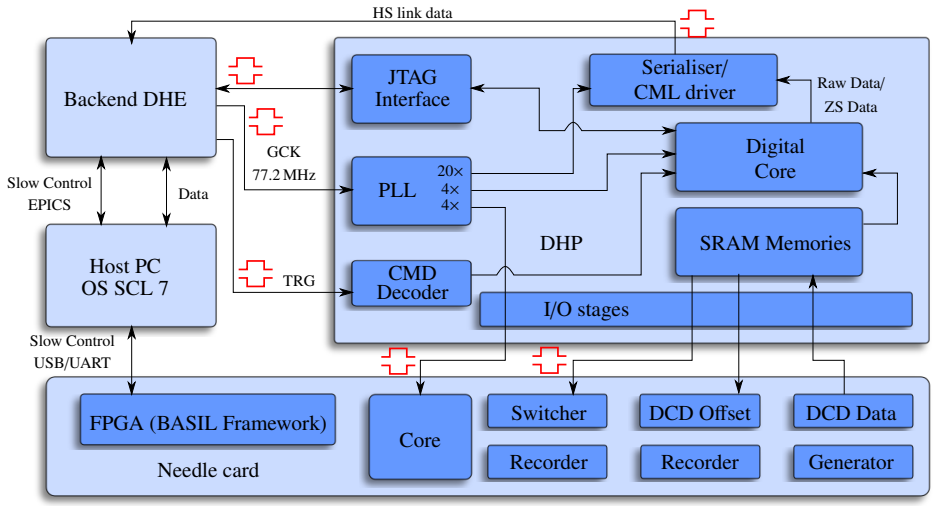


Figure 4.25: Functional block diagram of the mass production environment. Differential signals are marked with a red waveform.

Hardware To physically connect to each DHP chip a dedicated 4-layer PCB with cantilever needles in the center has been designed by the designers. This PCB, called needle card, contains a Spartan 6 FPGA board from Xilinx and a USB to UART controller chip. The needle card acts as an DCD and Switcher emulator. The needles are made out of tungsten compound and have a series resistance of approx. 1 Ω per needle. Since no voltage sensing is implemented the series resistance of the needles have to be taken into account for any voltage drop. The needles are aimed to contact the bump bonds of the DUT as depicted in figure 4.26. The top and bottom view of the needle card is shown in figure 4.27 and 4.28, respectively.

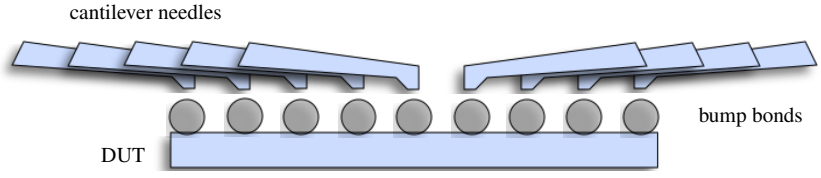


Figure 4.26: Optical alignment of the cantilever needles and the bump bond matrix.

The connectors in the upper side of figure 4.27 from left to right are; micro-USB, Infiniband (High Speed Signals), Infiniband (Slow Control - JTAG) and power. Voltage regulators are positioned on the right side to regulate the voltages. It can be chosen to bridge the regulators to directly apply the power supply

voltage to the chip.[8] The FPGA is placed at the bottom side. Debug pins are available at the left side to probe signals. The hole for optical control of the cantilever needles is positioned in the center. In figure 4.28 the wiring from the fanout vias of the needle card to the cantilever needle ring, called spider, is shown. A connected chip is shown in figure 4.29 as seen through a microscope via the hole. This visual control is used to allow the observation of the needle card and the DUT during the connection phase, especially during the alignment process of the needles with the bump bond positions.

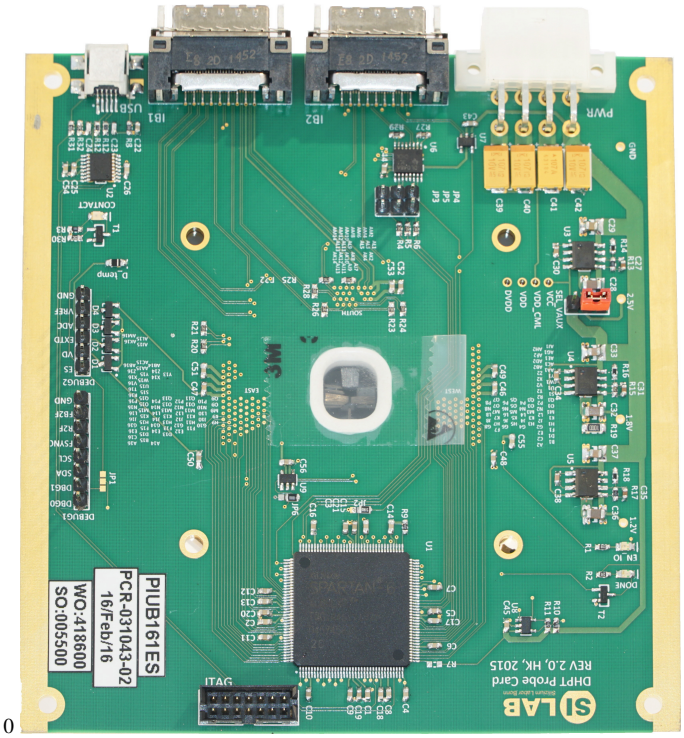


Figure 4.27: Top view of the needle card used for mass testing of the DHP. Connectors for the host PC and the back-end system are placed at the top side. The hole for visual inspection of the connecting DUT is located in the center.

The back-end system consists of the Data Handling Engine DHE and the host PC. The DHE steers the *trigger line* and receives the output data of the DHP. A Virtex-5 Xilinx FPGA is the processing unit of the DHE. The DHE is connected to the host PC and controlled over the EPICS system.

Firmware and Software The firmware block diagram implemented in the Spartan 6 FPGA on the needle card is shown in figure 4.25. The firmware consists of

- UART controller
- Sequencer
- Recorder
- Triggering logic
- Memories

[8] This results in unsensed voltages.

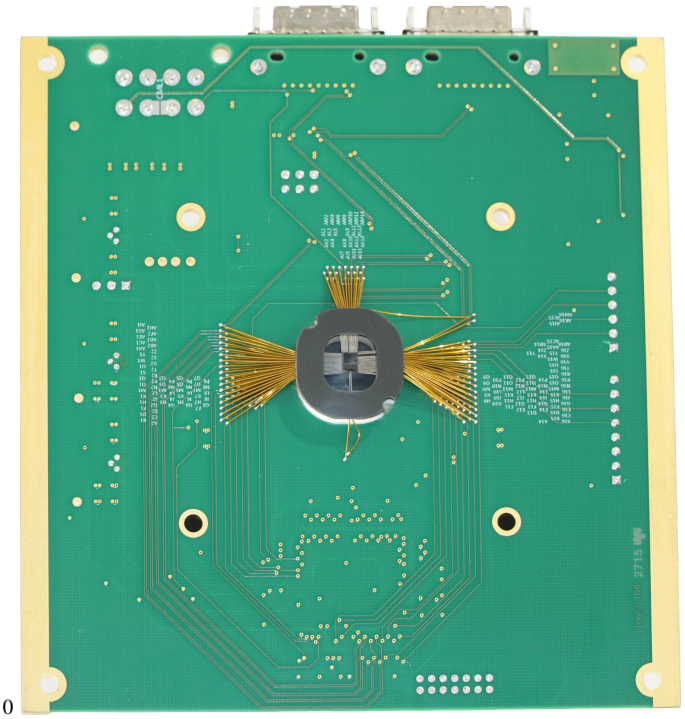


Figure 4.28: Bottom view of the needle card used for mass testing of the DHP. Wiring from the fanout vias to the cantilever spider in the center.

Figure 4.29: Top view of the needle spider inside the cut-out of the PCB. A DHP v1.1 is aligned and connected.

The UART (Universal Asynchronous Receiver Transmitter) controller protocol is given by a four-state state machine. First, send to the controller the control word for receiving the memory location. Second, send the memory address. Third, send the length of the data to be sent. Four, send the data. Data can be

written into the memories. Data can be written into the dedicated memories for the emulation of the DCD. Emulating pixel and offset data can be done by uploading test patterns into the memory of the Spartan 6 FPGA. Sequencers are used to send data from the memories to the DHP. Receivers are recording data from the DHP.

4.3.2 Tests algorithms

The DUT is manually connected and powered on. The chip internal default values are initialised at power up.

[1] Power Consumption The power consumption of the DUT is measured with a dedicated power supply. The currents for DHP_VDD and DHP_DVDD are sampled and checked. The condition for passing the test is,

$$120\,\text{mA} < I_{DHP\_VDD} < 150\,\text{mA}$$
$$30\,\text{mA} < I_{DHP\_DVDD} < 50\,\text{mA}$$

at DHP_VDD = 1.2 V and DHP_DVDD = 1.8 V.[9] The margin originated from the unknown voltages on chip, due to the missing sense lines. The Ohmic resistance of the tungsten cantilever needles causes a voltage drop of roughly 20 mV resulting in a current change of $\sim 5 - 10$ mA. Due to missing voltage sensing, voltage correction is applied by software.

[2.1] JTAG Interface The project-common framework provides a JTAG boundary scan to search for devices within the JTAG chain. This scan is used to detect the DUT by reading the DHP_ID which is hard coded within the DHP. The test passes if the DUT is correctly detected.

[2.2] JTAG Registers After the JTAG boundary scan, each single bit in the JTAG registers are toggled, except the registers corresponding to the biasing of the LVDS driver and receivers[10]

[3] Memory Tests All SRAM memory cells (dedicated to DCD data, pedestal, switcher and DCD offset) are toggled and a checker board pattern is uploaded to detect stuck bits. In addition two random bit patterns are uploaded.

[4] I/O Streams All inputs/outputs of the DHP are tested. The I/Os are dis-/enabled and test data are transmitted. Checking for correct enabling, disabling and data record is performed. The delay elements of the data I/Os are swept to find correct phase relation of the parallel sent bits of the DCD-DHP interconnect.

[5] HS Link Stability CML driver parameters are set to optimal settings and stability of the link is checked. 1000 full raw-data memory read-outs of the DHP are performed.

[9] The measured currents at DHP test- and Hybrid5 boards justify the limits within the current consumption test.

[10] Overwriting those registers with zeros causes the LVDS driver/receivers to fail and a power cycle is needed to establish JTAG communication again.

[6] Memory Dump Different sizes of raw-memory read-outs are performed with different test pattern. Data is uploaded in test-mode of the DHP. This mode enables a persistent state of the raw-data memory. Data is not continuously refreshed. The recorded data by the needle card is compared against the test pattern loaded into the DHP. If data matches, the test passes. This is done with multiple test patterns.

[7] Triggering - Zero Suppressed Data The full processing chain is tested via a test pattern containing well defined hits with a known common mode. The test data is uploaded into the raw-data memory of the DHP while being in test mode. Triggering is enabled and the data recorded. The defined hits and common mode are checked against the hits and common mode computed by the DHP. If this matches the test passes.

Figure 4.30: Box with 100 dies as received from the manufacturer.

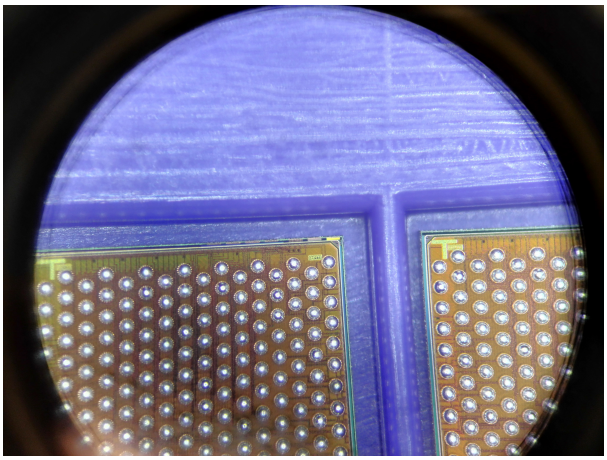


Figure 4.31: Bump bond inspection of DHP v1.1 via microscope.

4.3.3 Summary and conclusions

The mass testing procedure is reliable. Connection to the DUT via the cantilever needles is the crucial part. Bad contact can have several effects

- Bad powering. Higher resistances results into higher voltage drops in an unsensed system.
- Bad connection to JTAG pads. Configuration of the DHP fails.
- Bad connection to HS link pads. HS data not received correctly.
- Bad I/O connection. Switcher data or/and DCD data wrongly sampled.

Many potential effects resulting in a failing test are present. Bad connection can be caused by oxide generation on the bump bonds or by resistive residues on the tips of the cantilever needles. The tips can be cleaned by adhesive pads. These pads are placed like the DUTs and carefully contacted with the needles. The sticky pads remove the residues off the tips. The oxide on the bumps are harder to remove. The only way, without manipulating the bumps thermally, is to contact the bumps with the tips of the needle with higher pressure (overdrive). The pressure results in cracking of the oxide and thus decreasing the resistivity. Since for mounting the DHP on the PXD9 modules re-flow is used, i.e. the bump bonds melt and connect the DHP and module pads, the oxide is no issue for the later mounting procedure.

The number of DHP v1.2 tested up to January 2018 is 600. The **yield is > 98%**[11]. The high yield is due to two facts,

- The 65 nm technology is under proper control, i.e. **process parameters variations are small**.
- The chip area is approx. $12,\mathrm{mm}^2$. In 2008 semiconductor companies producing GPUs have used this technology for commercial usage. Those chips have sizes of up to approx. $324\,\mathrm{mm}^2$. The error ratio scales with larger area as process variations are more likely to occur for larger dimensions of the chip.

[11] This yield accounts also for chips damaged by the tester.

CHAPTER 5

Methods for Signal Integrity Measurements and Simulation Framework

5.1 Analogue measurements

Analogue methods focuses on the signal waveform and extracts parameters evaluating the signal quality with respect to data correctness. In order to minimize signal waveform distortions, reflections due to poor impedance-matched TML are investigated by Time Domain Reflectrometry (TDR) [32], [33].

Time Domain Reflectrometry

An incident step like waveform is injected into the near end of the TML. Impedance mismatches along the TML will cause local reflections that are sampled at the injection terminal. The local reflections are attenuated due to the lossy TML, and therefore have less impact on the near end. Since the method relies on reflections the far end of the TML has to be open or shorted, $Z \to \infty$ or $Z \to 0$, respectively.

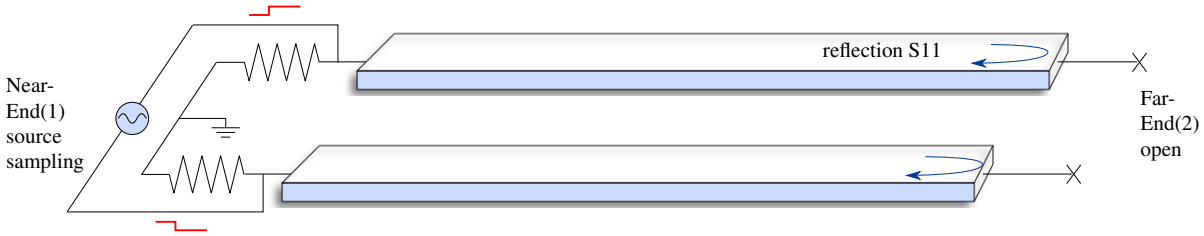


Figure 5.1: Two terminal TDR set up for differential TML. The near end of the TML is connected to a source- and sampling circuit. The far end is kept open for full reflection.

The reflection coefficient is defined as

$$\mathcal{R} = \frac{Z_L(x) - Z_0}{Z_L(x) + Z_0} = \frac{r-1}{r+1} = \frac{V_{refl}}{V_{inc}} \tag{5.1}$$

where $Z_L(x)$ is the impedance at point x along the TML, Z_0 the characteristic impedance, V_{inc} and V_{refl} the incident and reflected signal, respectively. r represents the ratio $Z_L(x) \cdot Z_0^{-1}$. The TDR method is used to estimate the amplitude of the locally reflected signal and therefore to decide if the impedance mismatches are severe and design changes are needed. If $Z_L(x)$ differs by a factor 2 or 0.5, the relative reflection of the incident signal is $|\mathcal{R}| \approx 0.33$. 'Severe' mismatches cause dips or bumps within the

waveform by destructive, i.e. $\mathcal{R} \in (-1, 0)$ and $r \in (0, 1)$, or constructive, i.e. $\mathcal{R} \in (0, 1)$ and $r \in (1, \infty)$, interferences, respectively. Unintended crossing of the threshold, which is defined by the receiver, triggers unwanted states that is especially problematic for clock lines.

Figure 5.2 shows an example of a short TML with a via connecting the top with the middle layer of the PCB.

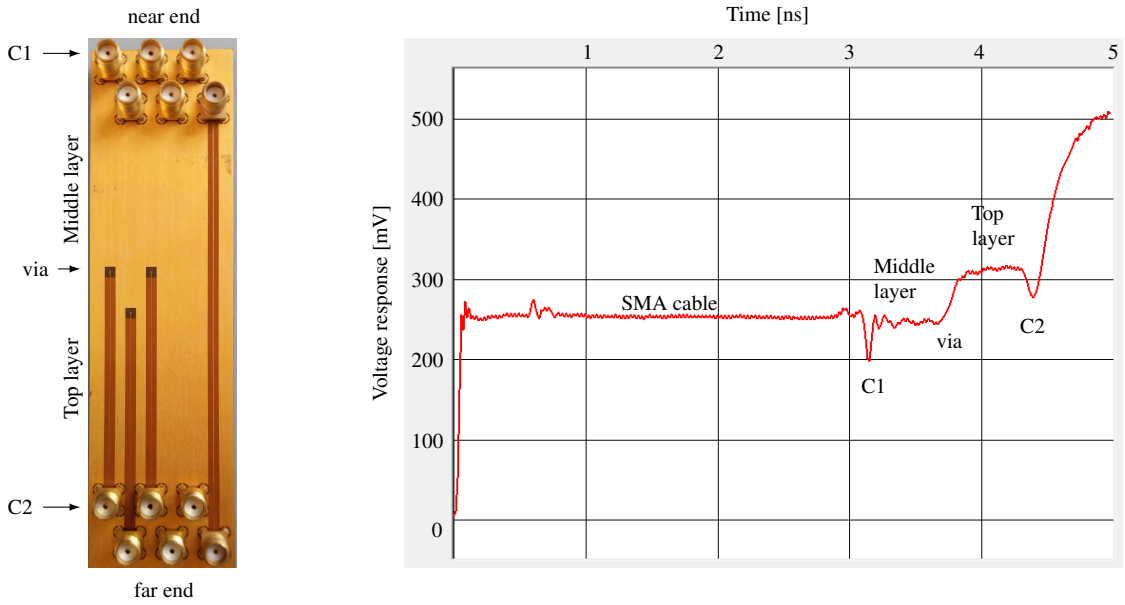


Figure 5.2: Example of TDR measurements. TML with a via connecting the middle and top layer (left picture, left trace). The via shows an inductive response, i.e. increment of the impedance and thus positive reflection.

Scattering Parameters

A more general method extracting reflection and transmission coefficients from any TML is called scattering parameter (s-parameter) extraction [34]. This method, in contrast to the TDR method, uses the near and far end shown in figure 5.3. A step like waveform is injected in one side. The reflected and transmitted parts are sampled at the corresponding other side. The s-parameter s11 and s22 refers to the reflections defined by the reflection coefficient $\mathcal{R}$. s21 and s12 are the transmission related parts defined by the transmission coefficient $\mathcal{T}$ with $\mathcal{T} = 1 - \mathcal{R}$. The s-parameters contain information about

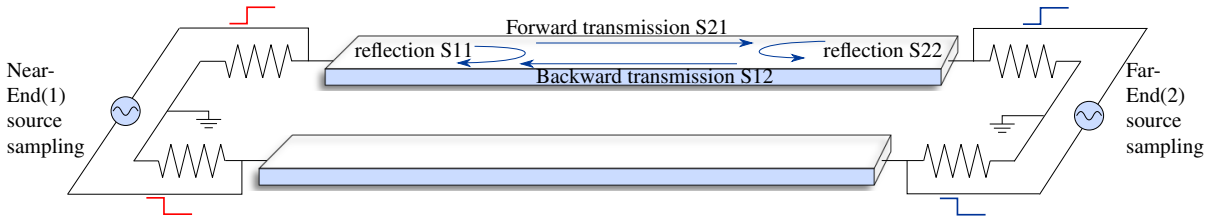


Figure 5.3: Four terminal scattering parameter and time domain reflectrometry setup for differential TML. Near and far end of the TML is connected to a source- and sampling circuit. Near and far end response of a test pulse is sampled and reflection and transmission amplitudes are measured.

attenuation and relative phase of the signal with respect to the frequency content. s21 represents the forward transmission of the TML. By extracting the scattering parameters design issues can be found and mitigated by revision of the design.

Eye Diagrams

As discussed in section 3.4 inter-symbol interference will introduce a common mode that varies with time, dependent on the waveform. As the bit pattern is more random like, the inter-symbol interference is more pronounced due to higher likelyhood of consecutive same-valued bits. A method called eye diagram is used to concentrate the time information of a long sequence as shown in [35]. A random bit pattern is sliced by unit intervals (UI) and the unit intervals are superimposed. The result is a waveform covering numerous transitions as shown in figure 5.4.

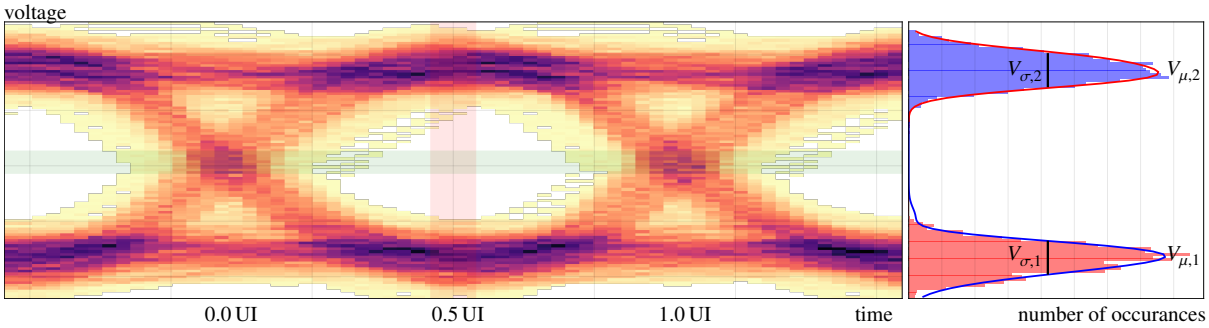


Figure 5.4: Simulated eye diagram with extracted parameters to obtain the vertical opening and the Q-factor. The waveforms (left) within the area at 0.5 UI are accumulated in the histogram (right). The colour of the histogram entry separates the bit values high (blue) and low (red). The horizontal (green shaded) and vertical (red shaded) color bands represent the histogram regions. Data within the vertical (red shaded) color band is mapped onto the right hand side histogram.

The eye diagram contains information about the vertical and horizontal opening and the jitter. The receivers clock-data recovery (CDR) circuit adjusts the sampling point at the centre of the unit interval (UI), see vertical (red shaded) region in figure 5.4. Any receiver requires a minimum separation of the low and high level. The voltage difference of these two levels and the noise at each of them can be summarised in the Q-factor. This factor represent the separation quality of the levels.

$$Q = \frac{V_{\mu,2} - V_{\mu,1}}{V_{\sigma,2} + V_{\sigma,1}} \tag{5.2}$$

It relates the plateau thickness to the overall amplitude of the signal. The thinner the plateau the lower the inter-symbol interference effect. The Q-factor is directly related to the analytical bit error rate defined by the complementary error function.

$$\mathrm{BER}(V_{thr}) = \frac{1}{2}\left(\mathrm{erfc}\left(\frac{|V_{\mu,1} - V_{thr}|}{V_{\sigma,1}}\right) + \mathrm{erfc}\left(\frac{|V_{\mu,2} - V_{thr}|}{V_{\sigma,2}}\right)\right) \tag{5.3}$$

The bit error rate therefore is defined by a given threshold. The histogram of the jitter at the zero crossing, i.e. at 0.0 UI and 1.0 UI, contains information about random (Gaussian shaped) and deterministic jitter, see figure 5.5.

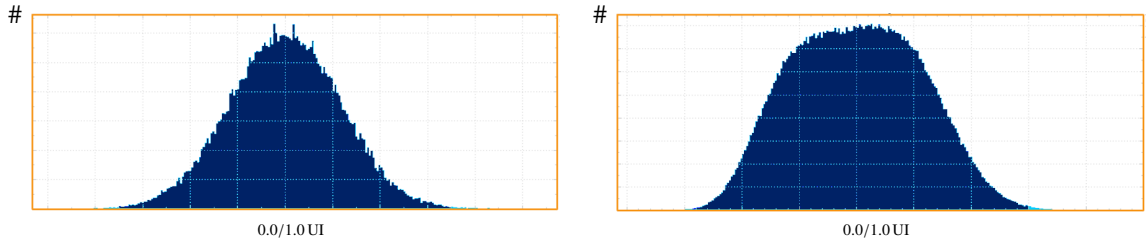


Figure 5.5: Histogram of the eye diagram at zero crossing. Gaussian like jitter (left) corresponds to random jitter due to thermal noise in the electronics. Deterministic jitter (right) caused by environmental effects or explicit data patterns.

The eye diagram itself contains also information about the probability of sampling wrongly one particular bit at a certain sampling point along the unit interval. This can be represented by the bath tub plot, see 5.6. It plots the probability of sampling the wrong value of a bit versus the horizontal sampling point. The probability to sample wrongly at the points 0.0 UI and 1.0 UI is per definition 0.5 as the waveform crosses the zero threshold.

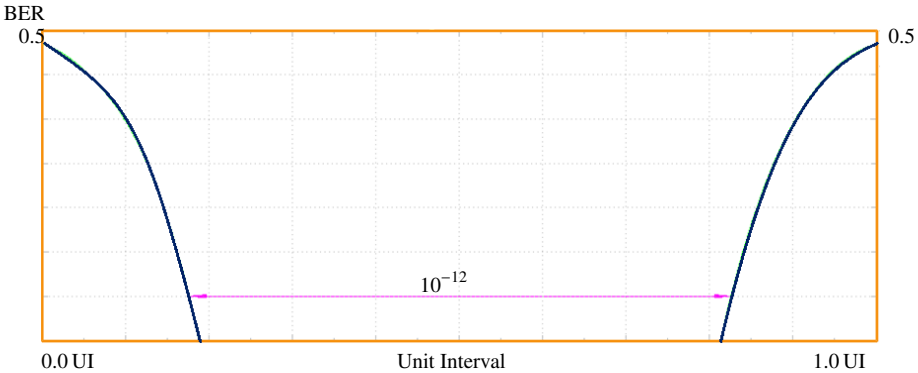


Figure 5.6: Bathtub plot showing the bit error rate as a function of the horizontal sampling point within a unit interval. The bit error rate is per definition 0.5 at the zero crossing, i.e. 0.0 UI and 1.0 UI.

5.2 Digital measurements

Bit Error Rate Test

A common standard in digital verification is the use of a n bit Linear Feedback Shift Register (LFSR). The LFSR generates a pseudo random bit pattern of a given periodicity. A seed sequence is loaded into the n bit LFSR. With each clock cycle the feedback is generated by a combinatoric of some of the intermediate bits. This generates a pseudo random bit sequence with a periodicity of $2^n - 1$ bits. The implementation is easy and is used in standard transceivers. The bit error rate (BER) can be calculated by sampling the bit stream from any transmitter and check against the standard n bit LFSR sequence, if implemented in the transmitter. Typically a BER of 10^{-15} and less for serial random-like bit streams are requested for safe operation in industry. By use of encoding mechanisms and protocols the BER, corresponding to random-like bit streams, can be lowered. A measurement of the BER is limited by the output data rate and thus the time needed for collection of sufficiently large numbers of bits. In industry large farms of device under test (DUT) are run in parallel and therefore increase the effective output data rate. This is not possible in small scale productions and in academic institutes with limited resources. In

order to qualify the BER with time constrains and few DUTs, the confidence level (CL) can be defined as,

$$\mathrm{CL} = 1 - \mathrm{e}^{-N\cdot\mathrm{BER}} \cdot \sum_{k=0}^{E} \frac{(N\cdot\mathrm{BER})^k}{k!}$$

where N is the number of bits transmitted, BER the target bit error rate and E the number of measured bit errors. N equals the product of data rate and measurement time. Table 5.1 shows for different target bit error rates, the time needed to sample one wrong bit with a confidence level of 95%. It is not feasible to perform large bias condition sweep tests for the CML driver of the DHP since for BER$< 10^{-12}$ more than one hour per bias condition is needed. The digital bit error rate test is therefore rather handy to

BER	Time $T[s]$
10^{-10}	30.5 s
10^{-12}	50.8 min
10^{-14}	84.7 h
10^{-15}	35.3 d
10^{-16}	0.97 a

Table 5.1: Time needed for different target bit error rates BER at a confidence level of CL95% to measure one bit error $E = 1$ for DHP (1.55 Gbps) driver testing. With total number of transmitted bits $N = 1.55\mathrm{e}9 \cdot T$.

quantify the link performance for optimal bias conditions found with eye diagram measurements than to sweep over a large range of bias conditions and repeat the measurement. For large parameter space of the bias conditions a different approach has been used that is discussed in the next section.

5.3 Simulation Framework

A general approach to quantify the driving capability of a given driver design is to obtain the eye diagram of the output waveform for a given cable model via 'Simulation Program with Integrated Circuit Emphasis' (SPICE) simulations. SPICE simulations are used at pre-silicon verification. With a dedicated cable model, i.e. extracted scattering parameter of a cable, the output waveform can be computed and performed according to design adjustments. This method is limited by the information given by the design. To validate the signal integrity of the TML system an approach has been used that incorporates as many information extracted by measurements as possible. The simulation framework used is explained in the following.

The simulation framework aims to resemble the real-world scenario as close as possible. For this reason all input data are taken from measurements. The input waveform, the waveform fed into the TML system, is either an arbitrary time series, i.e. simulated, or is measured by a high-speed oscilloscope. The TML system model is given by the scattering parameters. Figure 5.7 shows the block diagram of all inputs and outputs. The spectrum of the input waveform is computed by a standard Fast-Fourier-Transformation (FFT). The output of the FFT is complex and thus represents the amplitude and relative phase relation of the decomposed plane waves expansion. The scattering parameters represents the frequency dependent attenuation and the phase relation of the TML system. Both, the spectrum and scattering parameters, are in the frequency domain. Thus the input spectrum s_{in} and transmission coefficient $(\mathcal{A}(\omega), \Phi(\omega))$ can be multiplied for each frequency,

$$s_{\mathrm{out}}(\omega) = s_{\mathrm{in}}(\omega) \cdot \mathcal{A}(\omega) \cdot \mathrm{e}^{\mathrm{i}\cdot\Phi(\omega)} \tag{5.4}$$

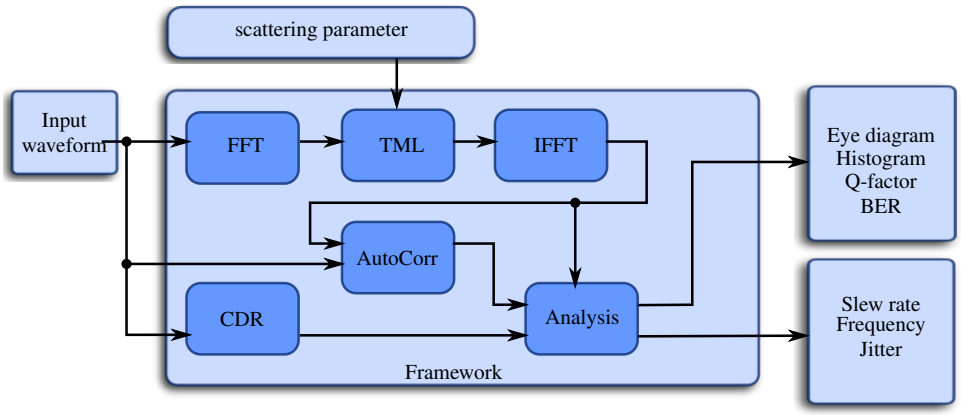


Figure 5.7: Block diagram of the Eye-diagram-simulation framework used to simulate eye diagrams for a given set of input waveforms and s-parameters (transmission coefficients).

where $\mathcal{A}(\omega)$ and $\Phi(\omega)$ are given by the s-parameter extraction and represent the attenuation and relative phase relation for a given frequency, respectively. The output spectrum s_{out} is transformed by a inverse FFT (IFFT) to obtain the output waveform of a given TML represented by the s-parameters. To extract the input waveform characteristics, e.g. frequency, a Clock-Data-Recovery module (CDR) is implemented. The input and output waveform is fed into an auto correlation (AutoCorr) module. This module computes the propagation time of the signal moving across the cable and aligns the input and output waveform for further analysis. The analysis module uses the information of the CDR and AutoCorr modules and the output waveform of the TML system. The information of the data frequency, given by the CDR, and the propagation delay, given by the AutoCorr, is used to slice the output waveform in unit intervals (UI) and superimpose them. The analysis provides the eye diagram, histograms, Q-factor, BER, slew rate, frequency, jitter and many more information. All simulated eyes and data are retrieved by this framework. For large parameter spaces with different input waveforms, i.e. different amplitudes, pre-emphasis strengths, etc, this framework can be used to compare different characteristics and find proper TML designs and/or input waveform modulations.

CHAPTER 6

Result of integrity studies

This chapter comprises the signal integrity studies of the components used for the TML system of the PXD detector. The single components are characterised and the results presented. The TML system is successively built and combined to obtain the full scale TML system.

6.1 Full scale TML system

The final characterisation of the full-scale TML system is shown in this chapter. Figure 6.1 shows the block diagram of the TML system for full characterised. In order to ensure proper signal integrity throughout the system two major paths have been characterised. The first is the clock path, namely the *gck* line. The reference clock *gck* is generated in a PLL of the DHE and sent to the PXD module. The second is the data path, namely high-speed link (HS link). Four HS links are present on each PXD module, transmitting the data streams of each DHP to the DHE.

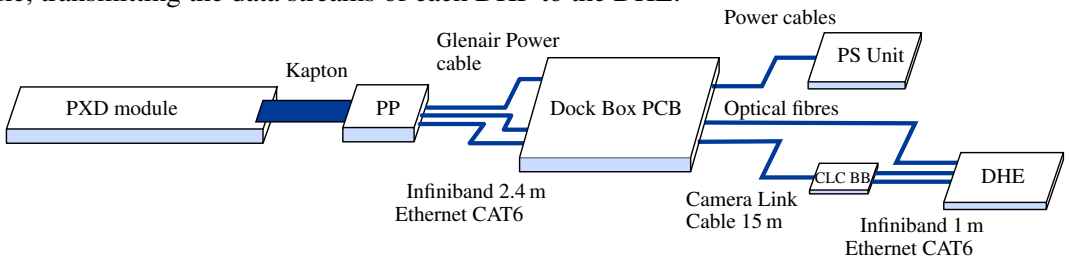


Figure 6.1: Block diagram of the full scale system as characterised within the scope of this thesis. Two major paths are of interest. The *gck* path, that is used to send the reference clock from the DHE over the camera-link cable (CLC) via the Dock Box (DB) to the PXD module. The HS data path, that conducts the gigabit serial data from the DHP on the module to the optical transmitter on the Dock Box (DB).

$$\begin{aligned} \textit{gck}\text{ line}: \quad & \text{DHE} \xrightarrow[1\,\text{m}]{\text{Infiniband}} \text{CLC Breakout Board (CLC BB)} \xrightarrow[15\,\text{m}]{\text{CLC}} \text{Dock Box (DB)} \\ & \xrightarrow[2.4\,\text{m}]{\text{Infiniband}} \text{Patch Panel (PP)} \xrightarrow[0.4\,\text{m}]{\text{Kapton}} \text{PXD} \\ \text{data path}: \quad & \text{PXD} \xrightarrow[0.4\,\text{m}]{\text{Kapton}} \text{Patch Panel (PP)} \xrightarrow[2.4\,\text{m}]{\text{Infiniband}} \text{Dock Box (DB)} \xrightarrow[15\,\text{m}]{\text{optical fibres}} \text{DHE} \end{aligned}$$

The interconnects are shown in figures 6.2 to 6.5. The flat-band Kapton is glued to the PXD module. Wire-bonds connect electrically the signal traces of the Kapton with the End-of-Stave (EOS) routing

of the module. The Kapton has an intermediate passive PCB for decoupling capacitors, see figure 6.2. These are used for power line filtering, that is needed to reduce noise on the supply lines and prevent short transient over-voltage of the DEPFET voltages to occur. Although the power supply of the modules handles over-voltage/current at the regulator site, the modules are approx. 15 m apart from the supply and high frequency modulations of the voltages cannot be regulated by the supply due to cable attenuation: The high frequency modulation is not sensed by the power supply. The Kapton is connected via a 100-pin Samtec connector to the patch panel. The patch panel is a small PCB. It is the interface of the Infiniband,

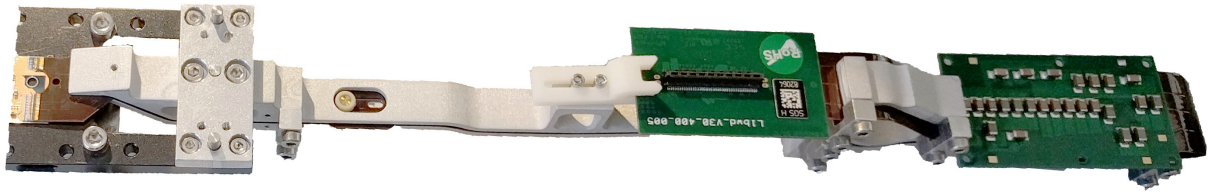


Figure 6.2: End-of stave region of the PXD module (left) wire-bonded to the Kapton. Aluminium support structure providing rigidity to the flexible Kapton. The intermediate PCB envelopes the Kapton. Vias connect the decoupling capacitors with the metal layer of the Kapton. The Samtec connector connects the Kapton to the patch panel.

Ethernet and power cable soldered on top of it to the Kapton. For soldering purposes the shield of the differential lines of the Infiniband cable is cut off by a few millimetres. This point is crucial because of varying mutual capacitance and inductance and thus changing locally the impedance.

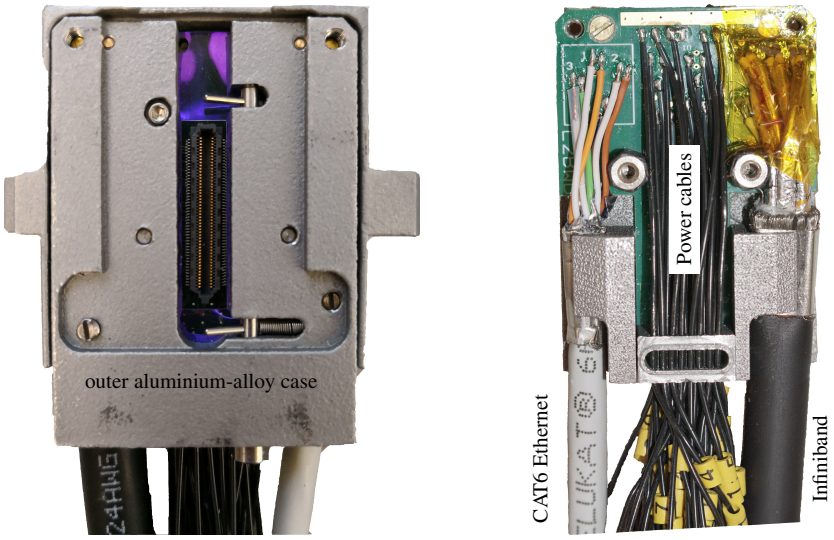


Figure 6.3: Patch panel close up. Female Samtec connector (left) connects the Kapton to the Patch Panel. CAT6, Infiniband and power cable are soldered on the Patch Panel (right). The inner shield of the differential Infiniband pairs are cut off for proper soldering.

The PXD module, Kapton and the patch panel are placed inside the sensitive volume of the PXD detector. In order to route the signals to the back-end outside of the sensitive volume a dock-box PCB is used as shown in figure 6.4. The cables from the patch panel are connected to the dock-box PCB. The high speed signals, e.g. DHP HS data, are transmitted via the Infiniband cable. The HS data are feed into an optical transmitter mounted on the dock-box PCB. The slow control signals, e.g. JTAG, are transmitted via the CAT6 cable and the power lines via the power cable. From the dock-box PCB the HS data are sent as optical signals to the back-end system via optical fibres. The slow control signals, *trigger*

line signal and *gck* signal are transmitted via a camera-link cable (CLC) to the back-end. In the scope of

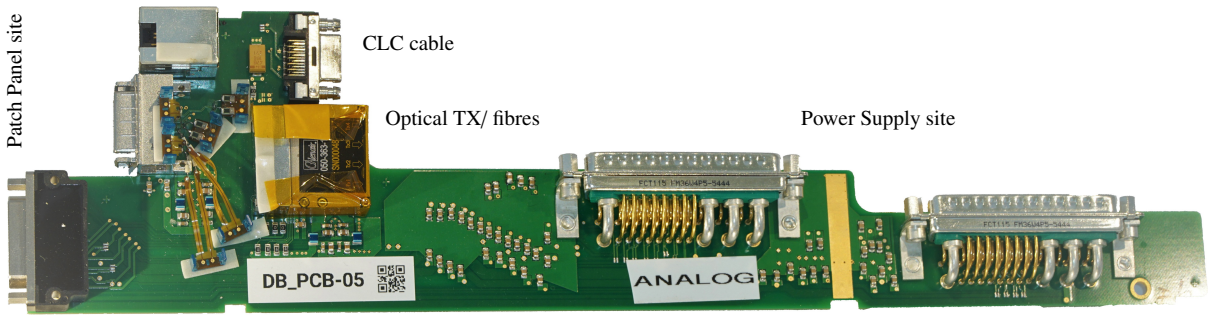


Figure 6.4: Dock Box PCB with power connectors and Infiniband interface. Infiniband, power and Ethernet cable are connected on the left and the signals are rerouted. HS links from the Infiniband are connected to the optical transmitter. Power is connected to the analogue and digital power connectors. Slow control data lines are connected to the camera-link cable (CLC) connector.

this thesis a dedicated camera-link cable break-out board has been used to match the interfaces of the CLC cable on the dock-box PCB and the Infiniband and Ethernet connectors of the DHE. In the final experiment, the dedicated CLC break-out board has been implemented into the Data Handling Interface (DHI).[1] The DHI handles the slow control signals while the DHE handles the HS data of the DHP. The

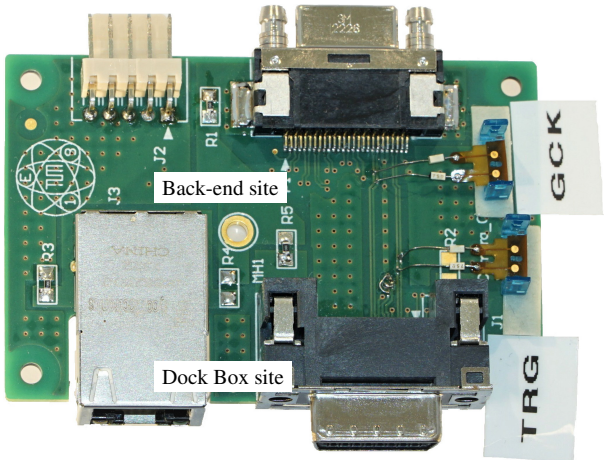


Figure 6.5: Camera-link cable break-out board with five pin power connector for supplying the optical transmitter on the Dock box. The power line is routed via the CLC. The CLC break-out board is the interface between the back-end connectors and the Dock box connectors.

number of connections/interfaces will affect the signal quality. The *gck* signal path incorporates eight such interfaces, i.e. EOS wire bonding, Patch Panel Samtec connection, Patch Panel soldering, Dock Box Infiniband connector, Dock Box CLC connector, CLC BB CLC connector, CLC BB Infiniband connector and DHE Infiniband connector. The HS data path goes only to the Dock Box and thus have five interfaces only. The next paragraph extensively discusses the properties of the Infiniband cables of various types.

[1] The DHI is at the time of the measurements still under construction and not available for testing.

6.2 Characterisation of Infiniband cables

The Infiniband cables under tests have eight differential pairs each. The copper core is silver plated to increase the surface conductivity and each pair itself is shielded. Table 6.1 shows the cable properties. From spatial constrains concerning services at the end caps of the Belle II detector, the used Infiniband cables have to be sufficiently thin, e.g. AWG28. The forward scattering parameters (transmission loss) of different cable lengths have been extracted by a four terminal measurement, see section **??**. The data is

Length l [m]	AWG	Diameter d [mm]	Cross section A [mm^2]	Impedance Z_0 [Ω]
1	28	0.321	0.081	100(5)
3	28	0.321	0.081	100(5)
5	28	0.321	0.081	100(5)
10	26	0.405	0.129	100(5)
15	24	0.511	0.205	100(5)

Table 6.1: Summary of the properties of the investigated Infiniband cables. All of them are designed to obtain $Z_0 = 100\,\Omega$.

presented in figure 6.6. The bandwidth has been extracted directly from the datasets, see figure 6.6 and from the analytic TML model from section 3.6,

$$\mathcal{A}(\omega) = \sqrt{\frac{2 \cdot {Z_L}^2}{\left(1 + {Z_L}^2\right)\cosh(2\rho(\omega)\cdot l) + \left({Z_L}^2 - 1\right)\cos(2\epsilon(\omega)\cdot l) + 2{Z_L}^2 \sinh(2\rho(\omega)\cdot l)}}$$
$$\rho(\omega) = \mathrm{Re}(\kappa_{\mathrm{Skin}})$$
$$\epsilon(\omega) = \mathrm{Im}(\kappa_{\mathrm{Skin}})$$

with fit parameters W′, G′ and C′,

$$\kappa_{\mathrm{Skin}}(s; \mathrm{W}', \mathrm{G}', \mathrm{C}') = \sqrt{\mathrm{W}' \frac{\mathrm{C}' \cdot s^2 + \mathrm{G}' \cdot s}{2\mathrm{C}' \cdot s + \mathrm{W}'\left(1 + \frac{2\mathrm{G}'}{\mathrm{W}'}\right)} \cdot \mathcal{D}'(s)} \quad \text{and} \quad \mathcal{D}'(s) = \mathrm{L}' + \frac{k_0}{k_1 \cdot \sqrt{s} - 1}$$

with $k_0 = \mu \cdot (l \cdot \pi)^{-1}$ and $k_1 = 2r\sqrt{\mu \cdot \rho^{-1}}$, where r, ρ and μ represent the radius of the conductor, the resistivity ($1.68 \times 10^{-8}\,\Omega$m) and absolute permeability of copper ($1.26 \times 10^{-6}\,\mathrm{Hm}^{-1}$) respectively. The fit parameters are chosen to be the specific conductances W′, G′ and capacitance C′. L′ is defined by the characteristic impedance and the specific capacitance, i.e. $\mathrm{L}' = Z_0^2 \cdot \mathrm{C}' = 10^4\,\Omega \cdot \mathrm{C}'$. Due the Skin effect R′ has been replaced by $\mathrm{R}' \to R'(s) = \frac{k_0}{k_1 \cdot \sqrt{s}-1} \cdot s$. The quality ($\chi^2/\nu$) of the fit and the extracted bandwidths are shown in table 6.2. The bandwidth are extracted from the data set and from the fit model. The error on the bandwidth (data set) is due to the sampling of the step-like function used for the s-parameter extraction, namely 25 ns → 40 MHz. The comparison of the bandwidth from the data-set and from the fit shows that the model works for cable lengths $l > 1$ m. For the one metre cable the relative deviation is approx. 15%. The parameters W′, G′ and C′ are summarised in table 6.3. The errors on the parameters are given by the fit and are of the order of the values. They show that the data set or the model is not sufficient to extract the parameters with a high precision. The trend of the values shows, that the parameters W′, G′ and C′ increases with higher cable lengths. These parameters are total values and

thus depend on the cable length itself. The extracted capacitances are plotted against the cable length in

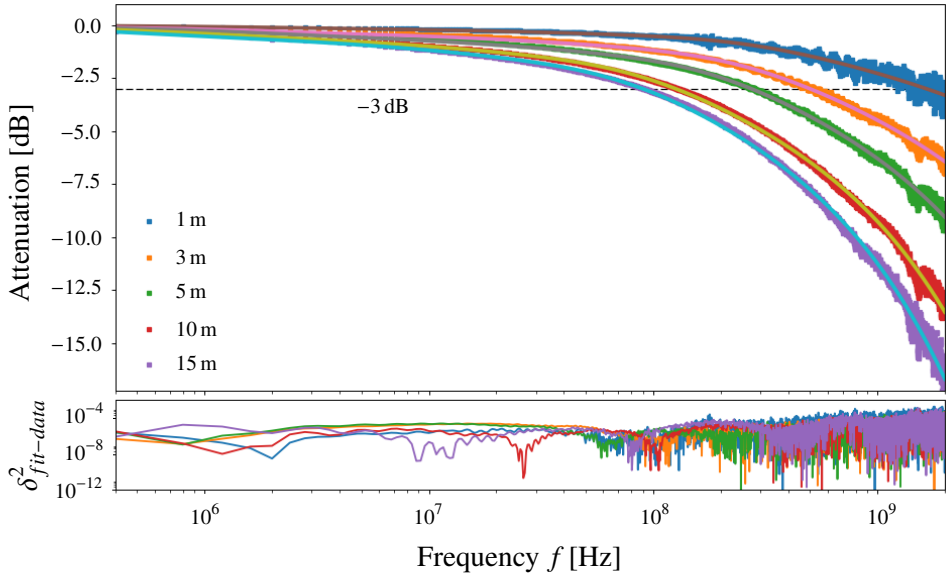


Figure 6.6: Transmission loss for different lengths of Infiniband cables shown in the top plot. Analytic model fitted to the data denoted by continuous lines. Bandwidth threshold −3 dB denoted by the dashed horizontal line. Squared deviation of fit and data are shown in the bottom plot.

Length l [mm]	AWG	$\frac{\chi^2}{\nu}$	Bandwidth [MHz] from data	Bandwidth [MHz] from fit
1	28	0.939	1230(40)	1659
3	28	0.992	489(40)	501
5	28	0.995	282(40)	275
10	26	0.965	129(40)	126
15	24	0.996	92(40)	90

Table 6.2: Extracted and measured bandwidths. χ^2/ν represents the quality of the fit. The error is defined by the resolution of the frequency range used in the measurement.

Length l [mm]	AWG	W_{fit} [(mΩ)$^{-1}$]	G_{fit} [(mΩ)$^{-1}$]	C_{fit} [pF]
1	28	1.7(3)	0.6(8)	5(4)
3	28	3.2(3)	1.3(3)	11(7)
5	28	3.6(3)	1.8(5)	18(12)
10	26	3.5(3)	2.0(8)	40(33)
15	24	3.7(3)	2.4(9)	53(46)

Table 6.3: Summary of the extracted parameters. Errors given by the fit.

figure 6.7. To compare the extracted values, the theoretical characteristic self capacitances according to

equation 3.15 are plotted as well in figure 6.7:

$$\frac{C_{self}}{l} = \frac{\pi \epsilon_0 \epsilon_r}{\operatorname{arccosh}\left(\frac{2a}{r}\right)} \tag{6.1}$$

with separation of the conductors of the differential pair $a = 1$ mm and the conductors radii $r = {}^{d}/_{2}$ from table 6.1. The extracted values are underestimated according to the comparison. Additionally, the mutual capacitance due to coupling of different differential pairs, are not included. The mutual capacitance adds on top of the theoretical self capacitance. Thus the total theoretical capacitance increases and the deviation to the extracted ones increases. The extracted values deviate by 34.8% up to 57.8% from the theoretical values. This is expected, since the fit quality χ^2/ν shows that either the data set is noisy or the cable model is not sufficient. The major problem of extracting reasonable cable properties from a model are second order effects. These effects, e.g. mutual capacitances, inductances, introduce deviations not included in the model. Additionally, the extracted forward scattering parameter contains the transfer function of the fixture that has been used to connect the Infiniband cables to the Digital Serial Analyser. This parasitic transfer function is not mapped onto the analytical model and thus the measured frequency response does not resemble the exact model. The impact of the Skin effect on the interconnects are discussed in detail in [36]. Although the parameter extraction is not sufficiently precise, the model can still be used for simulation purposes as shown in the next section. In order to optimise the bias parameters

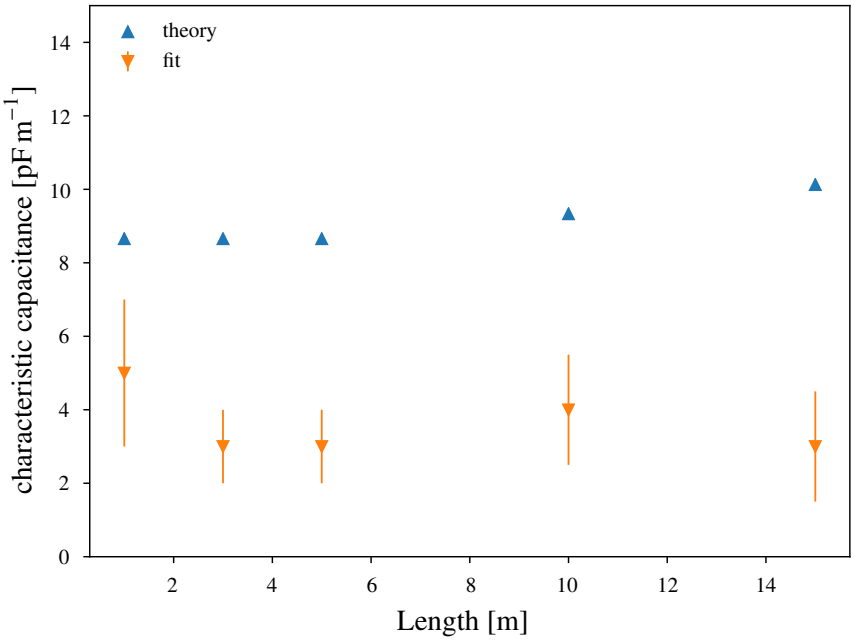


Figure 6.7: Comparison of theoretical and extracted specific capacitances for all presented cable lengths. Values of characteristic capacitances foreseen by theory exceed the extracted ones. The mutual capacitances are not taken into account in the analytical model.

of the CML driver, discussed in section 4.2.2, a simulation framework has been written. The simulation includes the forward scattering parameter and real waveforms at the direct output of the CML driver of a DHP v1.2 on a dedicated DHP test board as shown in section 4.2.2. Using this simulation tool investigations of the signal integrity has been conducted and parameter scans with best bias settings have been performed.

Eye diagram measurements and simulations

To validate the simulation quality and prove that the model, as discussed earlier, resembles real measurements eye diagrams of different Infiniband cables have been measured and the scattering parameters extracted to simulate the eye diagram. Figure 6.8 shows eye diagrams of three Infiniband cables of different lengths and conductor diameters. The simulated vertical eye opening deviates within a precision of $\leq 10\%$ by an error of 10 mV (histogram bin width) on the simulated eye and approx. 10 mV on the measured eye. The measured eye corresponds to the average minimal separation of the voltage levels at 0.5 UI of a sample of one million transitions recorded by a high-bandwidth oscilloscope. The direct comparison of the three cables are shown in table 6.4. The error on the vertical eye opening and on the sigma of the plateau thickness drives the error of the Q-factor. The higher Q the better the separation of the levels. The deviation of the vertical eye opening as well as the Q-factor is approx. 10%. This is a reasonable precision for relative values and thus sufficient to obtain parameter regions which are best. As discussed in section 4.2.2, the pre-emphasis width τ for pseudo-random data with low-bandwidth cables, i.e. high inter-symbol interference, is best, if τ is equal to the bit width. Thus only two parameters are free to choose, i.e. overall amplitude and the pre-emphasis strength. To obtain the vertical eye opening, a region enclosing the center of the unit interval 0.5 UI is used to histogram the eye and extract the range without any entries, see figure 6.9 right. The simulated vertical eye opening scanned over the full bias range, using the forward scattering parameter with AWG24 15 m Infiniband cable, is presented in figure 6.10. The highest vertical eye opening is achieved by a moderate main stage current and the maximal pre-emphasis strength. These settings are expected as for higher main stage current the current mirrors of the CML driver are driven out of saturation and thus are not able to supply more current. The spectrum shaping of the initial signal, i.e. DHP output, is in this case more important than the overall amplitude. The optimal setting is $(a, b) = (120, 245)$[2] with a vertical eye opening of 165 mV, see figure 6.8 (bottom right).

(length [mm] - AWG)	vertical eye opening [mV]		Q-factor	
	measured	simulated	measured	simulated
(1,000 - 28)	656(2)	620(10)	3.02(8)	3.6(6)
(10,000 - 24)	225(2)	202(10)	1.37(3)	1.3(2)
(15,000 - 24)	172(2)	165(10)	0.93(1)	0.91(6)

Table 6.4: Summary of the eye diagram parameters of three different cable geometries and comparison with the simulations.

The second figure of merit is the bit error rate (BER). The analytic BER presented in section 5 exploits the quantities of the Gaussian distribution used to evaluate the lower and upper band of the eye diagram. The BER versus the bias parameters are shown in figure 6.11. A BER of 10^{-16} can be achieved. The optimal bias parameter with respect to vertical eye opening and BER differ. There is no one-by-one correlation between vertical eye opening and BER. The vertical eye opening does not include information about the strength of the inter-symbol interference effect introduced by the low bandwidth cable. This information is either embedded in the Q-factor or can be expressed by the BER. The BER on the other hand does not include absolute information, e.g. vertical opening, see equation **??**. Since differential receivers need a minimal absolute separation of the low and high level, the vertical eye opening is more

[2] These bias settings correspond to the main $a \propto I_B$ and pre-emphasis $b \propto I_{BD}$ stage of the CML driver.

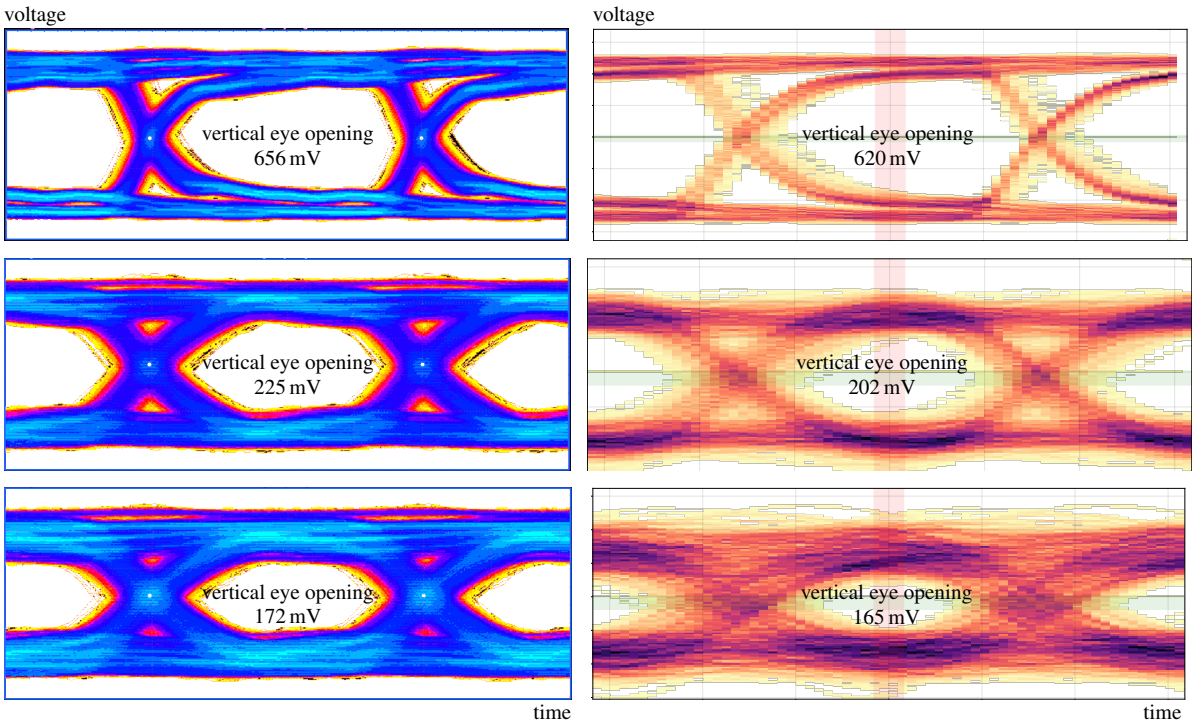


Figure 6.8: Eye diagram of the HS link with pseudo random bit pattern via 1 m AWG28 (top), 10 m AWG24 and 15 m AWG24 (bottom) Infiniband cable at 1.52 GHz (DHP v1.2). Measured eyes on the left, simulated eyes on the right.

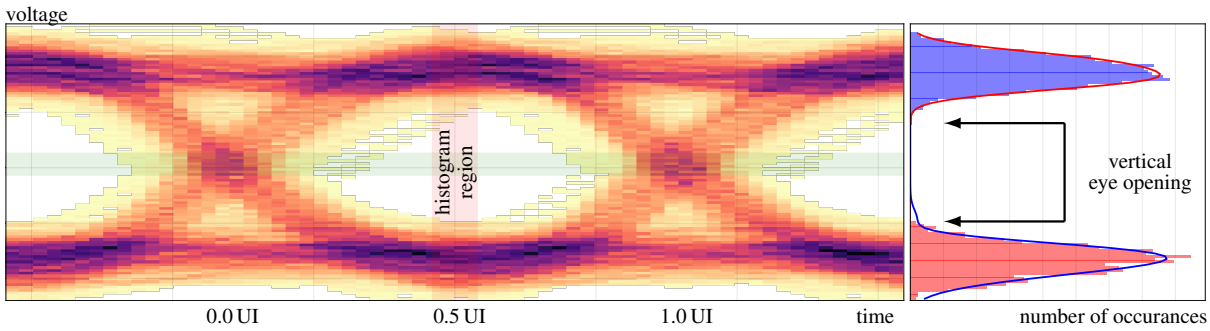


Figure 6.9: Example of a simulated eye diagram for a specific bias parameter set to obtain the vertical opening. Histogram (right) used to extract the region without entries that defines the vertical eye opening.

suited to evaluate a TML system.

Figure 6.12 shows the highest vertical eye opening achieved with optimal bias parameters versus the cable length of the Infiniband cables. Measured and simulated data are shown. In addition the full scale TML system is included as described at the beginning of the chapter. The full scale TML system performs slightly better than a 10 m Infiniband cable. As a reminder, the full scale TML includes the Kapton, PP, 2.4 m Infiniband cable and the DB PCB. The full scale TML system is much shorter in length, i.e. 40 cm Kapton and 2.4 m Infiniband, but incorporates five connectors, where impedance mismatches and transfer functions of the connectors degrade the forward transmission coefficient. The minimal level separation for the electro-optical transceiver on the DB PCB is 250 mV[37]. This is a value provided by the manufacture and is not a hard threshold. It is recommended to provide the minimum separation as requested to operate the system within the specification. With the full scale TML system a vertical eye opening of approx. 230 mV is achievable. This is 8% below the recommended value.

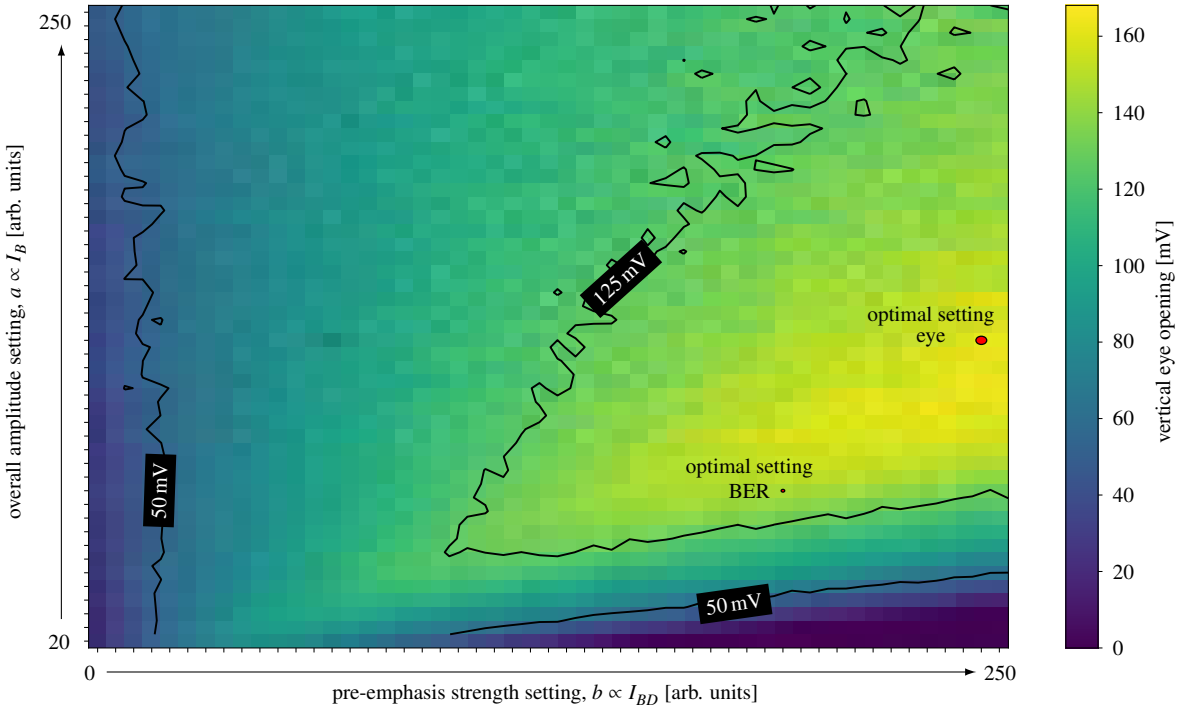


Figure 6.10: Simulated vertical eye opening versus bias parameters for AWG24 15 m long Infiniband cable. Optimal setting with respect to the eye opening $(a, b) = (120, 245)$. The contour lines indicate region of more than 50 mV and 125 mV.

Remark: During the time the DHP existed in version 1.1 the full scale TML system has foreseen the Kapton, PP and 15 m Infiniband cable solution. This solution has been rejected since the DHP v1.1 is not capable of driving the 15 m Infiniband cable, see section 4.2.2. The first attempt to connect the PXD module via Kapton, PP and Infiniband cable directly to the back-end system and use the differential receiver of the dedicated FPGA with a minimum level separation of 125 mV therefore has been revised and the back-up solution with a electro-optical transceiver was developed. This solution has higher requirements with respect to the level separation, i.e. min. 250 mV compared to min; 125 mV for the FPGA solution. With the newest DHP version the first attempt (15 m Infiniband cable to FPGA receivers) is preferred over the full scale TML system, as seen in figure 6.12. Since the TML system topology has been finalised at the time the latest DHP version has been developed, for safety reasons, the second approach made it into the final PXD system.

Figure 6.13 shows the relative parameter space, exceeding two given thresholds for different cable lengths and the full scale TML system, defined by

$$p_{thr} = \frac{\text{\# of bias points with vertical eye opening } > \text{thr}}{\text{total \# of bias point}}$$

Two thresholds for the **simulated minimal vertical eye opening** have been used. The first threshold is 125 mV of the differential receiver of the FPGA embedded in the DHE, the second is 250 mV of the electro-optical transceiver. The errors indicate variation of 10% of the relative parameter space. For cable lengths up to 5 m for both thresholds more than 80% of the CML driver parameter space is available. For longer cables the relative parameter space drops significantly to 30% for the lower threshold and to 0% for the higher threshold at 5 m. The relative parameter space is approx. 75% and 20% for the full scale

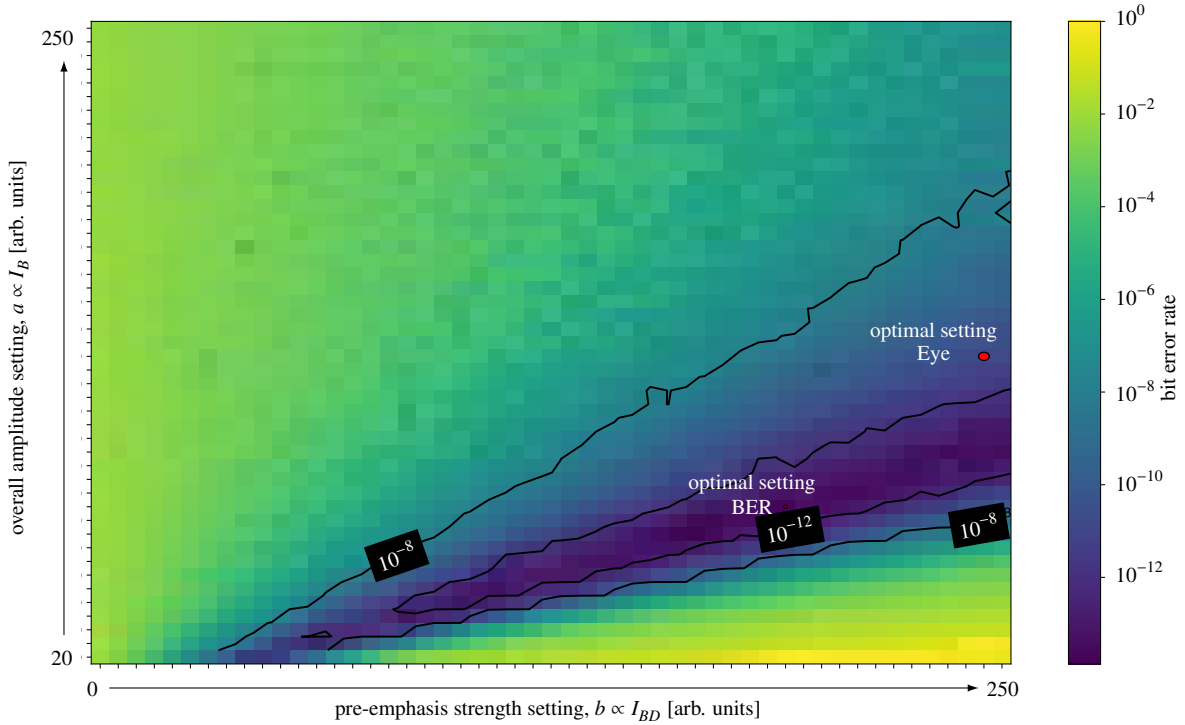


Figure 6.11: Simulated BER versus bias parameters for AWG24 15 m long Infiniband cable. Optimal setting with respect to the min. BER $(a, b) = (60, 205)$. The contour lines indicate region of less than 10^{-8} and 10^{-12}.

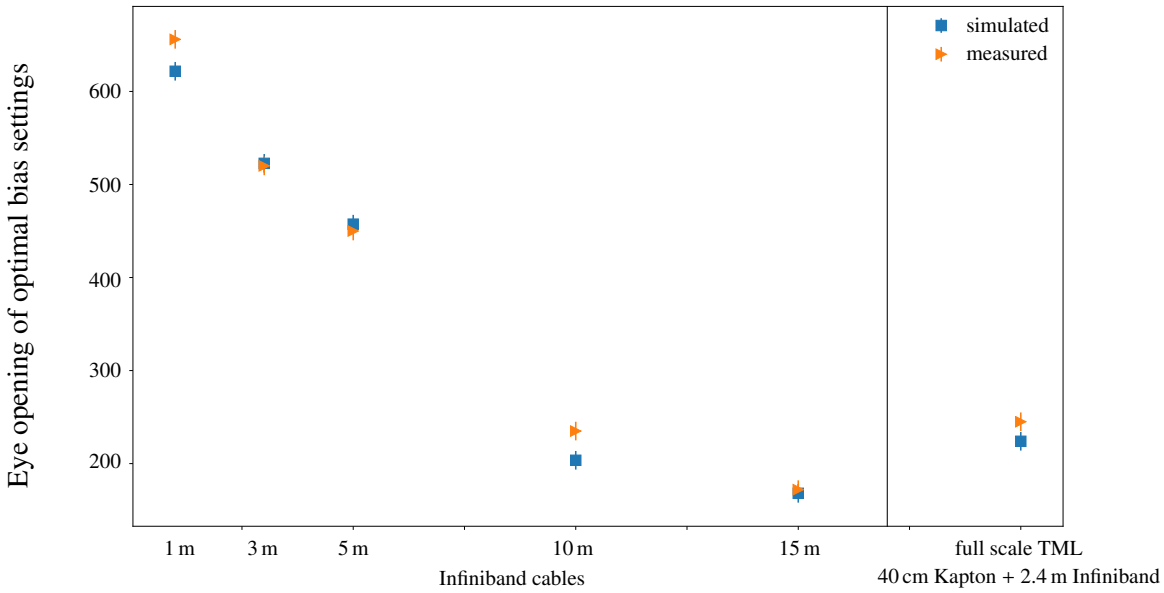


Figure 6.12: Comparison of measured and simulated optimal eye opening for different lengths of Infiniband cable and full scale TML system.

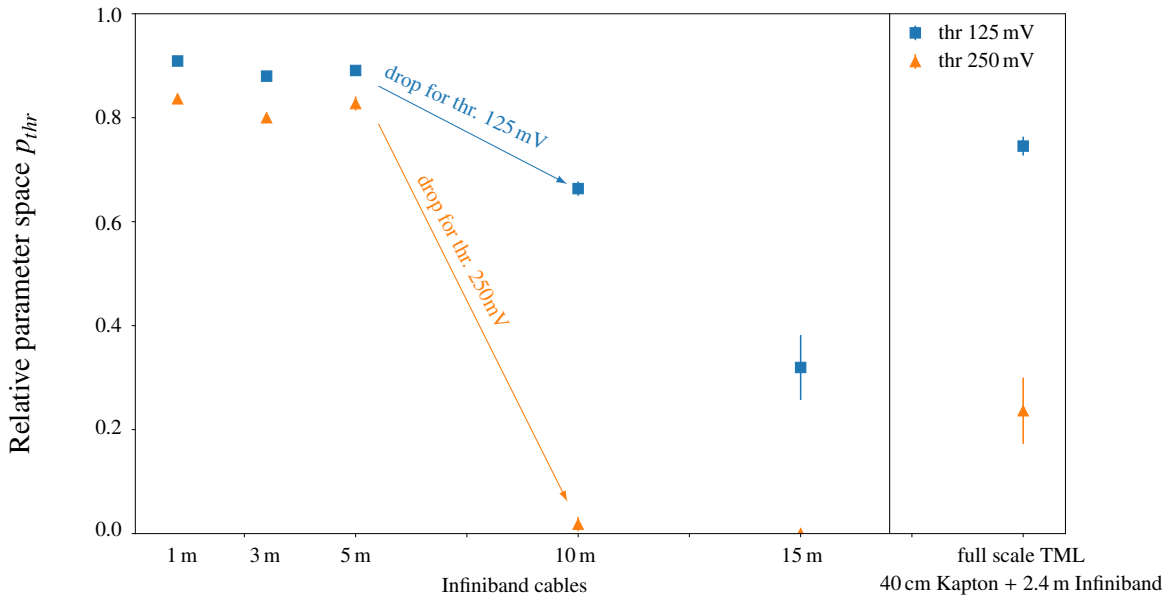


Figure 6.13: Relative number of CML bias points, whose corresponding simulated vertical eye opening exceeds the threshold of the two possible approaches, differential FPGA receiver (125 mV) and optical receiver (250 mV).

TML system at the lower and higher thresholds, respectively.

6.3 Characterisation of the End-of-Stave region and flat-band Kapton

The first item of the full scale TML, seen from the PXD module for sending the HS link data, is the EOS of the PXD module and the flat band Kapton shown in figure 6.14. The densely routed high speed signals on the EOS are connected via wire bonds with the flat band Kapton. Due to the high amount of connections, e.g. wire bonds, and the varying trace geometry on the Kapton investigations of impedance mismatches are essential to validate the integrity of the system.

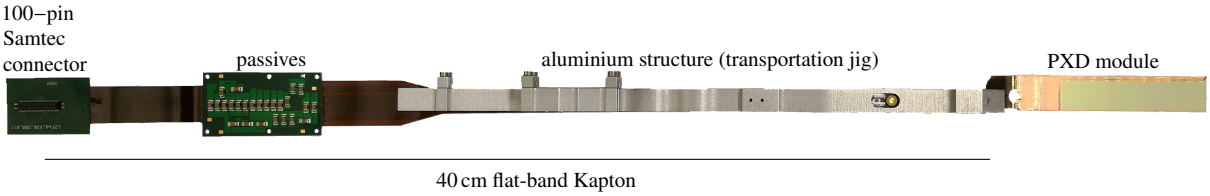


Figure 6.14: Flat-band Kapton attached to the PXD module. Passive decoupling capacitors are placed on an intermediate PCB that wraps the flat-band Kapton. The aluminium structure acts as stress release and protects the wire-bonds against pull forces.

The EOS region is shown in figure 6.15. The module under test does not feature ASICs on it, it is a bare module. The gold pads of the Kapton are used to bond wires to them and connect the metallisation of the EOS. The aluminium support structure has no electrical function. The wire bonds introduce impedance mismatches close to the EOS. For the HS data path this is a crucial spot, since it is the closest to the DHP. To validate that the HS data signals do not suffer from reflections and thus possible bit errors, a time domain reflectrometry measurement has been conducted.

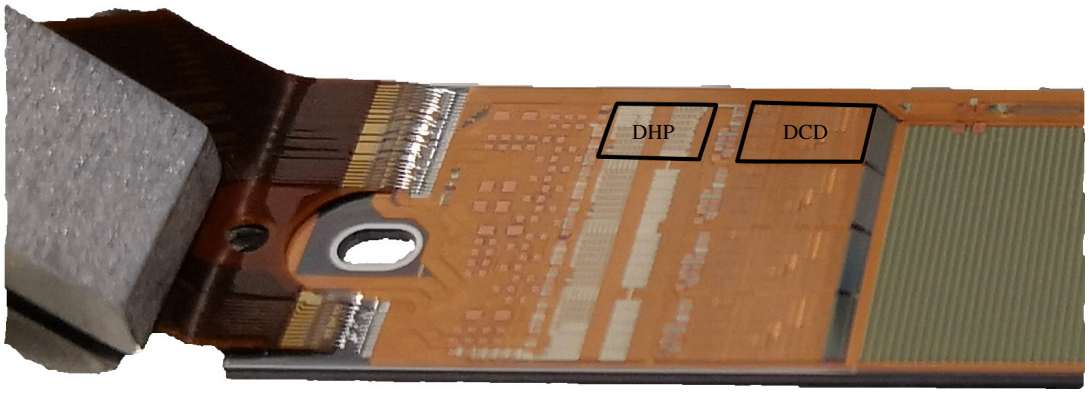


Figure 6.15: Close-up of the EOS of the PXD module. The flat-band Kapton is glued onto the bare silicon. The wire-bond connect electrically the module and the flat-band Kapton. The metallisation is below the visible copper layer. Soldering pads for passives are placed close to the chip location.

TDR measurements

The set-up to measure the reflections of the EOS region, the Patch Panel and the connections the approach shown in figure 6.16 has been used. A dedicated SMA-to-Infiniband break-out board has been used to connect the DUT to the Digital Serial Analyser (DSA). The DSA provides a step-like signal on the input terminal and samples the reflected signal simultaneously. This set-up connects the input terminal

on the opposed side of the EOS region. This has one major drawback. The incident signal has to pass the Infiniband cable and thus is attenuated. The signal amplitude at the EOS region is therefore smaller than the incident one. The reflection at the EOS itself is attenuated and thus the measured voltages used to compute the reflection coefficients do not match the real amplitudes. To mitigate this effect the forward transmission coefficient measured in the previous section is used to compute the actual signal amplitude at the EOS region. With this approach the attenuation introduced by the Infiniband cable can be compensated.

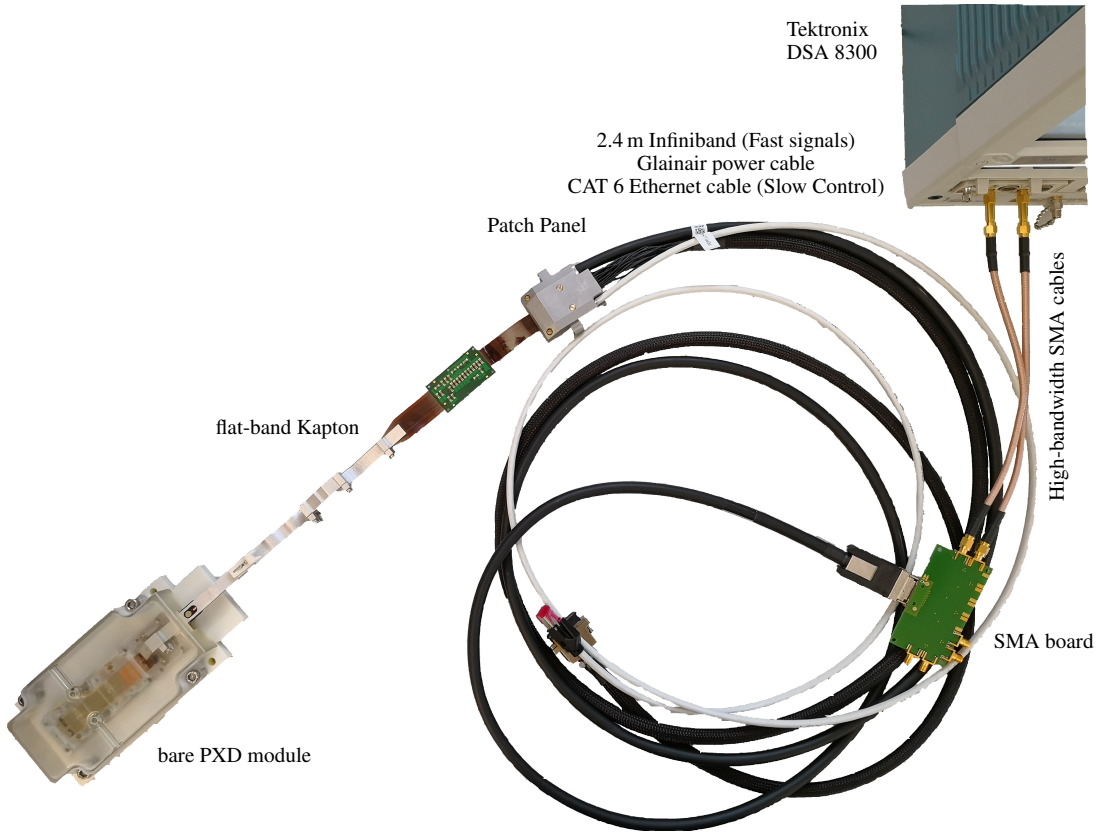


Figure 6.16: Close-up of the EOS of the PXD module. The flat-band Kapton is glued on the bare silicon. The wire-bond connect electrically the module and the flat-band Kapton. The metallisation is below the visible copper layer. Soldering pads for passives are placed close to the chip location

Figure 6.17 shows the incident step with the reflected one for un-/connected DUT. In the unconnected case, only the SMA-to-Infiniband break-out board introduces a propagation delay of the signal. The step is reflected with full amplitude after approx. 4.5 ns of the incident step. The spikes seen close at the spot where total reflection occurs are reflections due to the SMA-to-Infiniband break-out board, especially due to the connectors. In the second case the signal propagates up to 30 ns after the incident step. The reflected step has the characteristic low-bandwidth rising of a low bandwidth TML. The spikes at approx 23 ns and 30 ns after the incident step are reflections at the Patch Panel interconnects and the EOS wire-bonds, respectively. The Patch Panel interconnects are shown in detail in figure 6.3. The Samtec connector (left) and the soldering (right) of the Infiniband cable wires introduces impedance mismatches causing the reflections. Especially the soldering spots are sensitive to noise and impedance mismatches. At these spots the differential pairs are bare and the shields are removed for soldering purposes. The impedance along the DUT are calculated, see equation 5.1, and presented as a close-up

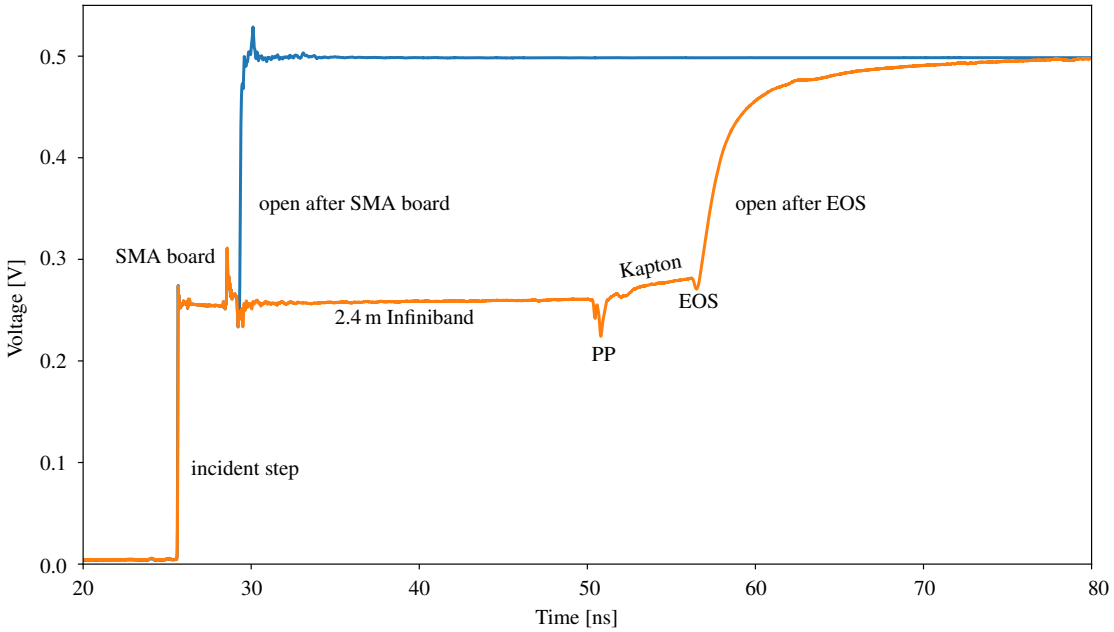


Figure 6.17: Time Domain Reflectrometry measurement of the bare module with attached Kapton, Patch Panel and 2.4 m Infiniband cable. Reference reflection without the DUT (blue) and with DUT (orange).

in figure 6.18. It shows the part of the DUT without the Infiniband cable. The reference impedance is $Z_0 = 100\,\Omega$. The dashed line represents the corrected impedance after compensating for the Infiniband cable attenuation. The connection to the Patch Panel via the Samtec connector and the soldering of the wires are clearly visible and introduce a local increase in capacitance. As $Z_0 = \sqrt{L/c}$, connectors and changes in interfaces lower the impedance by increasing the capacitance locally. The passive decoupling and filter capacitances on the intermediate PCB of the Kapton, as well as the EOS also introduces some lowering of the impedance. The maximum reflection is less than 16% of the incident step. The overall rising of the impedance is originated by the DC resistance of the Kapton [38]. Additionally to the low reflection of 16%, the time scale of the reflections are less than 280 ps. The HS data paths of the four DHP are similar with respect to impedance mismatches. To evaluate the relative reflection amplitudes and the characteristic widths of the reflections, the comparison between the *gck* line and the HS data path is shown in table 6.5. Relating the reflections to the signal characteristics, it is evident that the

Path	Bit width [ns]	Amplitude [mV]	Reflection width [ns]	rel. Reflection amplitude
gck	13.12	N/A	0.28	0.16
HS data	0.656	250	0.23	0.14

Table 6.5: Summary of the Signal characteristics and the reflections on the *gck* and HS data path.

impedance mismatches have no sever impact on the signal integrity of the system. Nevertheless, for the HS data path the margin of the achievable, with respect to the required, minimum vertical opening of 250 mV shown in figure 6.12 is small and therefore any reflections should be mitigated. Proper soldering and connection via the Samtec connector are essential, since these two spots are the most sensitive to impedance mismatches.

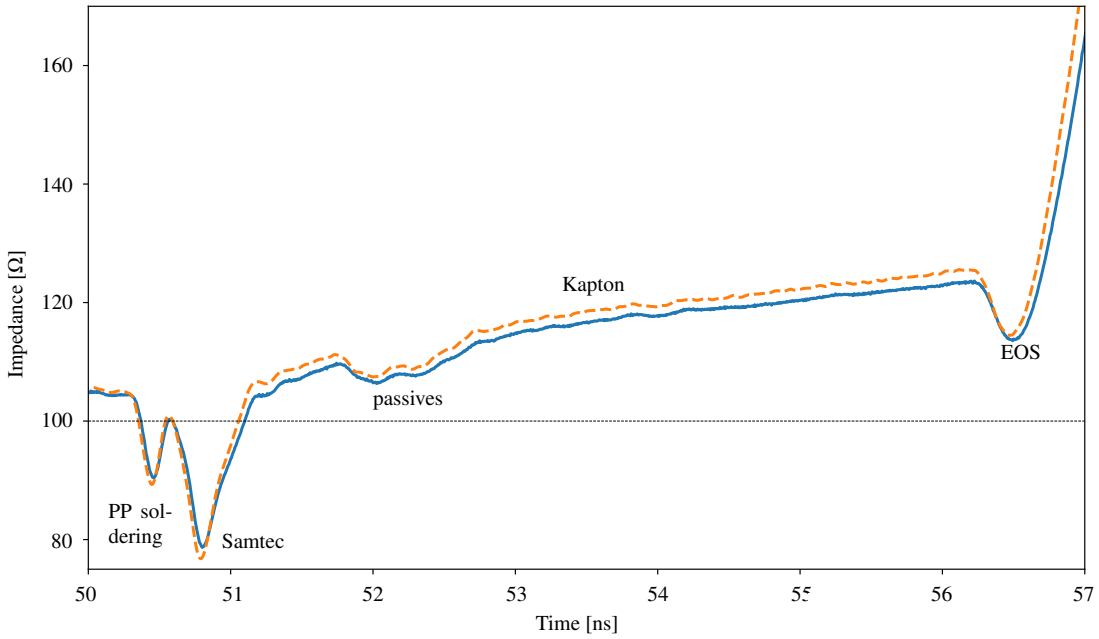


Figure 6.18: Impedance along the DUT. Close-up of the Patch Panel, Kapton and EOS region. Reference impedance indicated by the 100 Ω-line. Interfaces identified by locally increased capacitance introducing dips in the impedance profile. Impedance profile calculated from raw reflected signal (blue) and Infiniband compensated (orange, dashed) are shown.

6.4 *gck* slew rate measurements

On the other hand, impedance mismatches are not the only issue degrading the quality of the signal. For the HS data, a clean reference clock is needed. Low noise, low phase jitter and high slew rates $^{dV}/_{dt}$ are important. The reference clock of the DHP is received at the LVDS receiver. The *gck* rising edge triggers the logic. If the steepness of the rising edge, i.e. the slew rate, is low, the point the logic triggers highly depends on the noise on the threshold. This results in higher jitter. Higher jitter closes the eye diagram such that the horizontal and vertical[3] opening decreases. The horizontal opening is essential for the receivers sampling point. A receiver itself adjusts to sample in the center of the unit interval but due to random jitter a margin around the center is still needed. To validate the slew rate of the *gck* as close as possible to the PXD module, the *gck* signal is sampled at the Dock Box PCB, see figure 6.19. High speed probes are soldered on the PCB to sample the signals with a high-bandwidth oscilloscope (8 GHz). There are three flavours of the CLC break-out board.

1. Passive PCB - just changes the interface.
2. Active PCB with differential amplifier.
2. Active PCB with CMOS driver - changing the LVDS levels to full CMOS.

The first flavour is a passive PCB with re-routing of the signal traces. The second has an active component to amplify the differential *gck* signal and add pre-emphasis with a dedicated RC device, see schematics in figure 6.20. The differential input signal, e.g. *gck*, is fed into a differential amplifier. The common mode

[3] This is especially true, if the slew rate of the signal is small. A diamond shape can be inserted into the eye diagram such that the vertical distance of the diamond shape decreases if the horizontal one does.

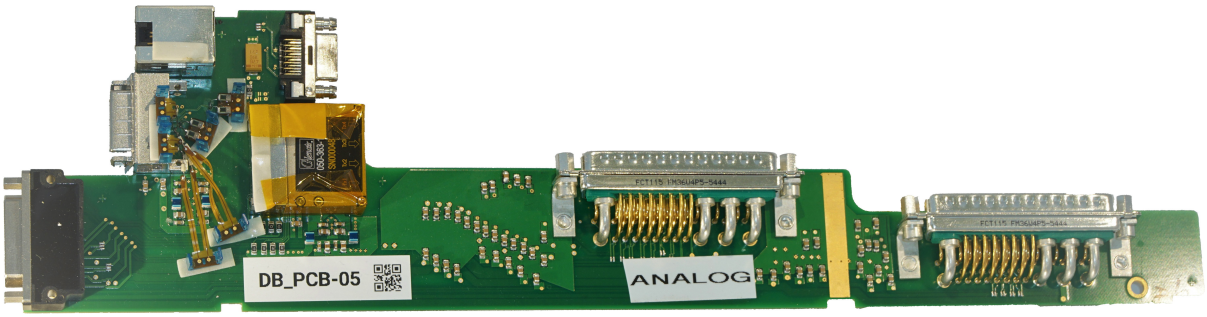


Figure 6.19: Dock Box PCB with soldered high-speed probes (close to the left connector) to sample the *gck* signal after passing 15 m CLC cable. The Dock Box PCB is the closest component to the pxd module where probing is still possible without manipulating the Patch Panel.

is fixed by a resistive voltage divider at the output node close to the pre-emphasis stage, see black box in figure 6.20. The third flavour has a CMOS driver implemented. It converts the differential input to a full CMOS signal with higher amplitude and pre-emphasis, see schematics 6.21. The pre-emphasis stage is similar to the second flavour, see black box in figure 6.21. The pre-emphasis stage in both cases is a RC pair added to each output lines to boost the high frequency part of the signal. The performance of all

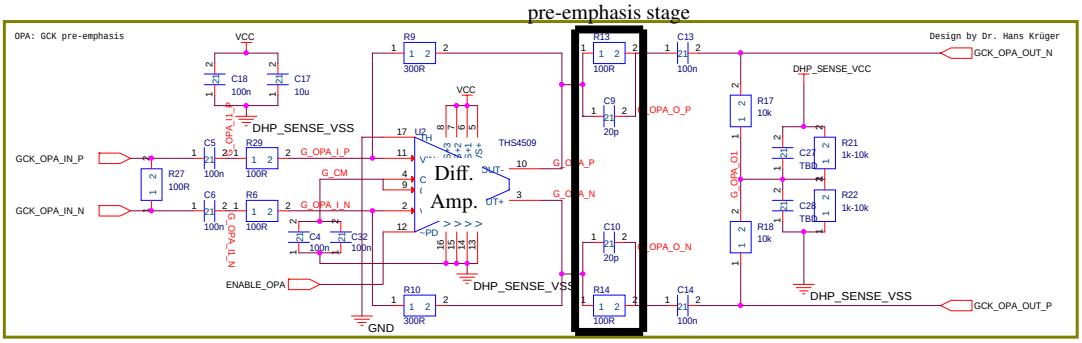


Figure 6.20: Active CLC break-out board with differential amplifier and pre-emphasis stage (black boxes) on each output lines.

three flavours are shown in figure 6.22. Using the passive PCB, the *gck*, after passing 15 m CLC to the Dock Box, has a slew rate of approx. 0.16 $^{V}/_{ns}$. Using the active boards the slew rate increases by a factor 4.37 to approx. 0.7 $^{V}/_{ns}$. The CMOS PCB performs best while the differential amplifier PCB has some oscillations. These oscillations occur due to the return current path on the PCB and could be fixed by careful revision of the PCB design. The close-up of the rising edge is shown in figure 6.23. The slew rate is defined as the rate at the common mode of the signal.

A comparison of simulated slew rates with the forward scattering parameter of the full *gck* path and the measured ones yields the following picture 6.24. The slew rate of the *gck* after 15 m Infiniband cable is higher than the CLC system with passive CLC break-out board. The active PCB is comparable to 10 m Infiniband cable. A list of all simulated and measured values are presented in table 6.6.

With a simple receiver model the rms jitter is inversely proportional to the slew rate

$$\text{jitter}^{\text{rms}}_{\text{SR}}\ [\text{ns}] = \frac{\text{noise on the threshold level}^{rms}\ [\text{V}]}{\text{SR}\ [^{\text{V}}/_{\text{ns}}]}$$

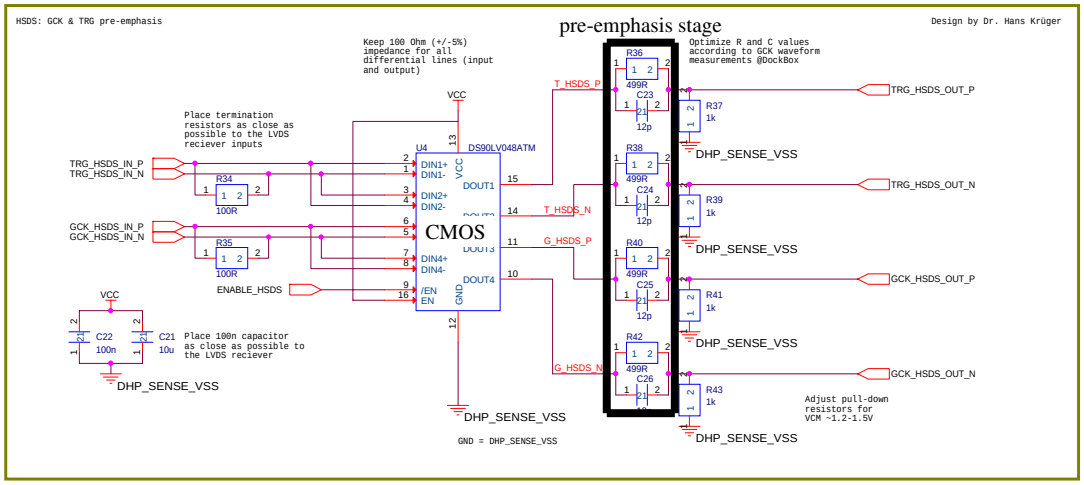


Figure 6.21: Active break-out board with CMOS driver and pre-emphasis stage (black boxes) on each output lines.

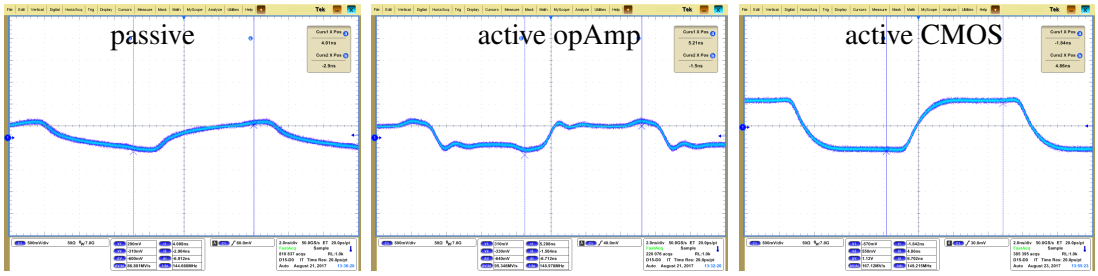


Figure 6.22: *gck* signal after 15 m camera link cable. Passive CLC break-out board (left), active differential amplifier board (center) and CMOS board (right).

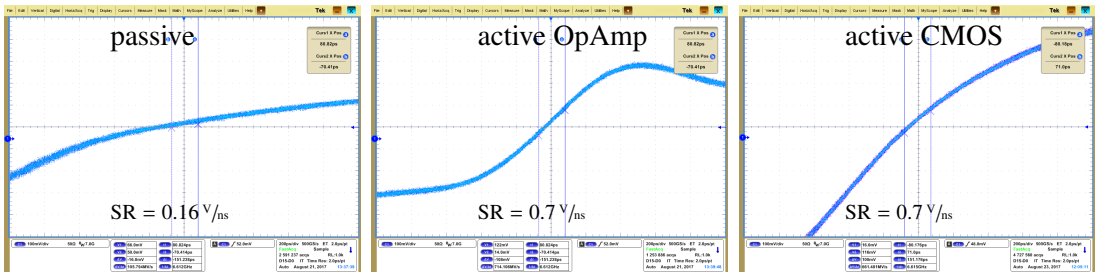


Figure 6.23: Rising edge of the *gck* signal after 15 m camera link cable. Passive CLC break-out board (left), active differential amplifier board (center) and CMOS board (right).

The noise of the receiver is dominated by thermal and shot noise. These originate by fluctuations of the number of charge carriers and its velocities, respectively. Using this simple relation and simulating the vertical eye opening by adding the jitter introduced by the slew rate one can show that for the system the minimal acceptable slew rate is approx. $0.2\,^{V}/_{ns}$, see figure 6.25. In this simulation a noise on the receiver threshold of 5 mV has been used.[4] The additional jitter at the zero crossing of the eye decreases to a minimal value of approx. 30 ps for higher slew rate $> 0.5\,^{V}/_{ns}$. The unit interval (bit width) of the

[4] Thermal noise is the dominant noise source for threshold fluctuations [39]. The gate of a transistor couples capacitively with the channel. This 'capacitor' suffers from thermal noise and thus change the switching characteristics.

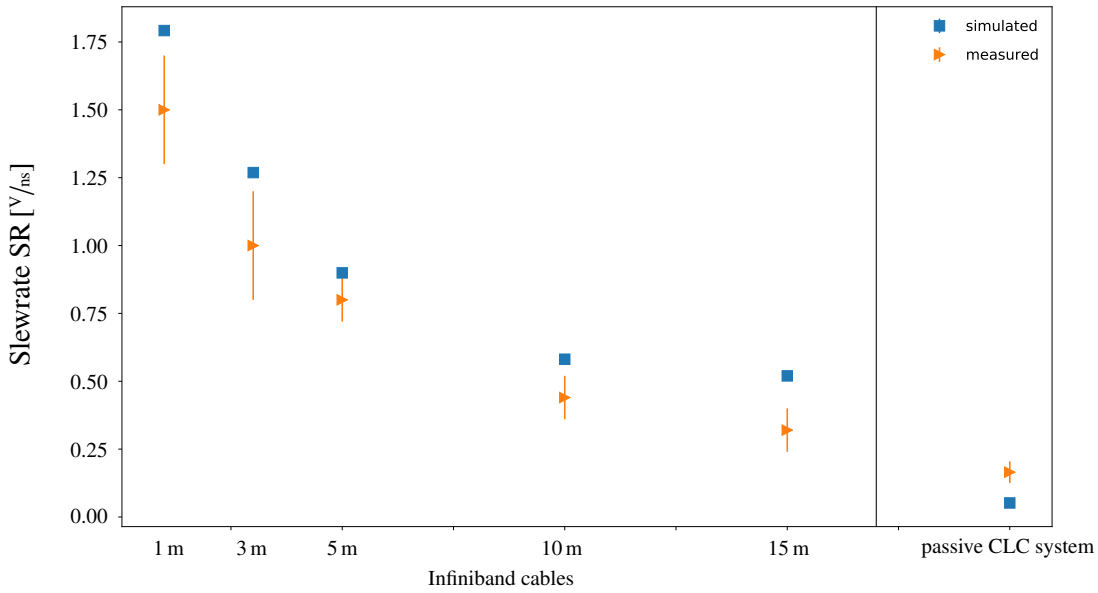


Figure 6.24: Comparison of slew rates of the *gck* signal with different cables. Infiniband cables from 1 m up to 15 m and the 15 m CLC with passive CLC break-out board.

TML	Infini. 1 m	Infini. 3 m	Infini. 5 m	Infini. 10 m	Infini. 15 m	passive CLC system 1 m + 15 m + 3 m
SR_{sim} [V/ns]	1.7919(6)	1.2687(5)	0.8993(3)	0.5812(4)	0.5197(1)	0.05159(6)
SR_{meas} [V/ns]	1.5(2)	1.0(2)	0.8(2)	0.44(8)	0.32(8)	0.165(2)

Table 6.6: Simulated and measured slew rates of the *gck* signal for various lengths of Infiniband cable and the passive CLC system.

1.52 GHz-HS data stream is 656 ps. For slew rates below 0.1 V/ns the additional jitter increases by 20% of the bit width, namely > 130 ps. With the active CLC break-out board it is possible to achieve higher slew rates than 0.5 V/ns. From figure 6.12 (section 6.2) one reads a vertical eye opening of approx. 230 mV. This value has been measured by using the passive CLC break-out board. By using the active one an improvement in vertical eye opening of approx. 10% can be achieved. The additional jitter can be reduced to 5% of the bit width.

Remark: It shall be remembered that the assumption that the receiver obeys the simple relation shown above is retrieved from a simple model. In praxis it is far more complicated and a spice model simulation with the receiver implementation is needed to verify the statement. This simulation is outside of the scope of this thesis.

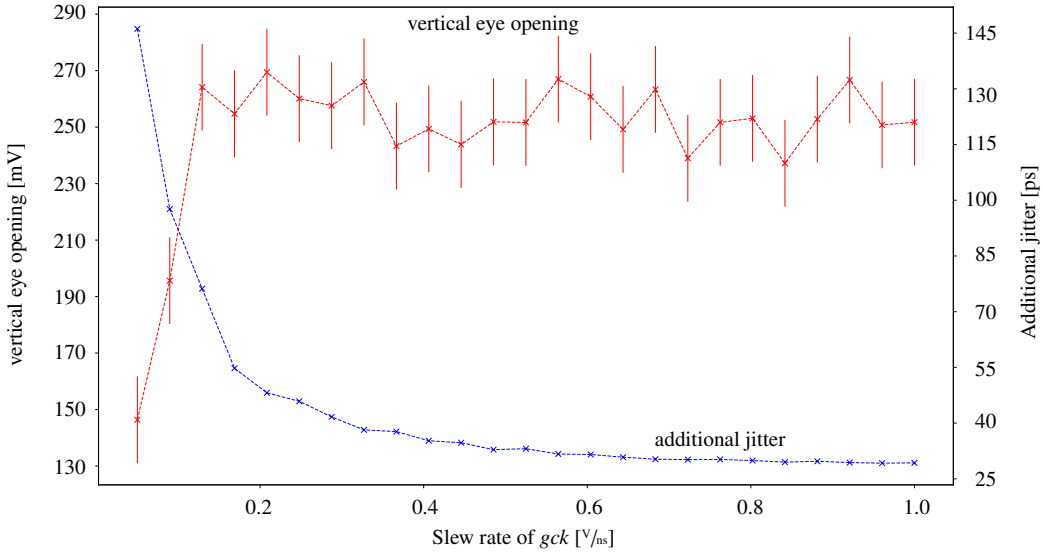


Figure 6.25: Vertical eye opening and additional random jitter of the simulated eye diagram of the full scale TML system and its dependence on the *gck* slew rate. The total jitter consists of the jitter introduced by the slew rate and the intrinsic jitter of the *gck* signal.

6.5 Combined tests: Full scale TML system with active CMOS CLC break-out board

Finally the **simulation** with final optimisation can be performed. The active CLC break-out board is used. The HS data signal is probed on the dedicated DHP test board and feed into the simulation with the final forward scattering parameter for the full scale TML system. The optimal CML working point ($a = 100, b = 235$) with respect to the vertical eye opening is presented in figure 6.26. A maximum simulated vertical eye opening of approx. (290 ± 10) mV can be achieved. Compared to the system with a passive CLC break-out board and smaller slew rate of the *gck* signal, the vertical eye opening increased by an absolute value of 60 mV - an increment of approx. 26%. Figure 6.27 shows the analytically extracted BER versus the bias parameters. The analytical BER is simulated to be $< 10^{16}$. Since the simulation relies on sampled waveform of finite length, which implies a limited number of bits, the simulated BER is not an exact value and has to be related to a confidence level. In this case the number of bits (limited by the internal memory of the oscilloscope used to sample the waveform) does not allow a higher confidence level than approx. 76%. Therefore the digital bit error rate test has been run over 240 hours. It has been stopped at BER $= 2.3 \times 10^{-15}$ without a single bit error at a confidence level of 95%. The **measured** eye diagrams for the full scale TML system with passive and active CLC break-out board are shown in figure 6.28 and 6.29, respectively. The vertical eye opening of the passive system is approx. 230 mV. With the active system an opening of approx. 270 mV can be achieved. This is 20 mV less than the simulated vertical opening ($\sim$ 7% less). The Q-factor increases from 1.54(7) (passive) to 2.19(7) (active). The Q-factor of both systems are summarised and compared in table 6.7 with the Q-factor of the Infiniband cables discussed in section 6.2. Recalling figure 6.12 one can conclude that the active system competes with a 7 m to 8 m Infiniband cable in terms of vertical eye opening and separation quality (Q).

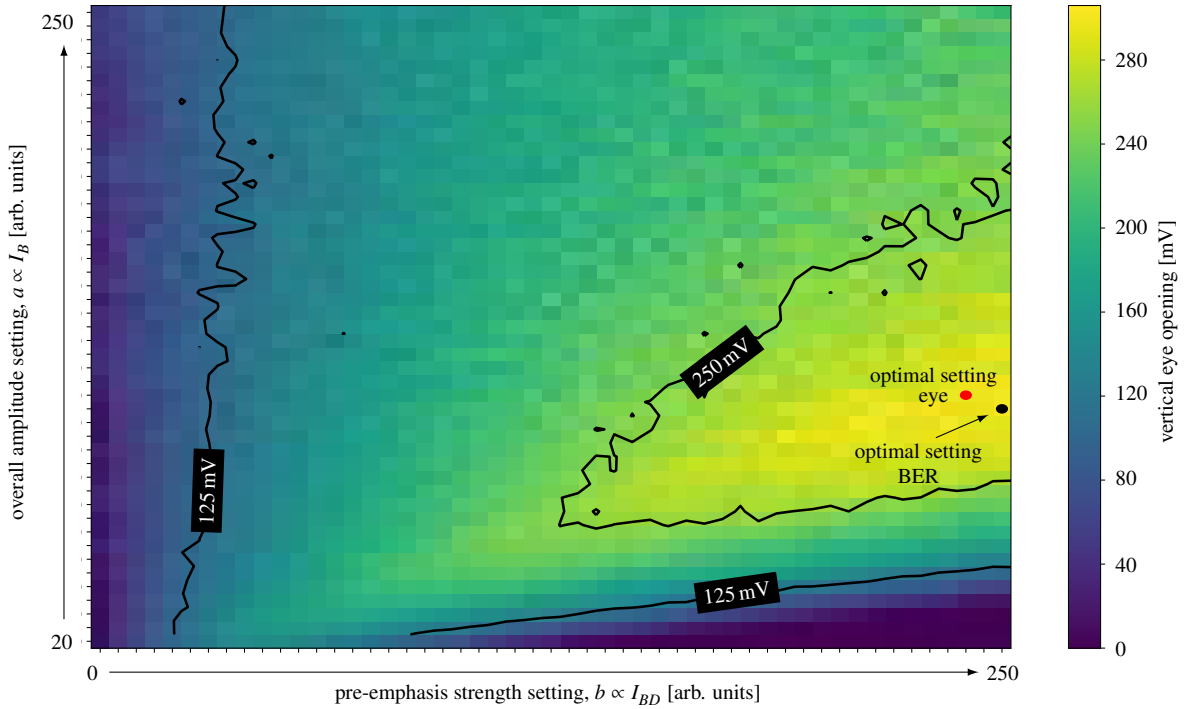


Figure 6.26: CML parameter scan for the full scale TML system with active CMOS CLC break-out board and extracted vertical eye opening (colour code). Optimal working point with respect to vertical eye opening and BER shown.

TML System	measured vertical eye opening [mV]	Q-factor
Infiniband l = 1 m, AWG28	656(2)	3.02(8)
Infiniband l = 10 m, AWG24	225(2)	1.37(3)
Infiniband l = 15 m, AWG24	172(2)	0.93(1)
passive TML system	230(10)	1.54(7)
active TML system	270(10)	2.19(7)

Table 6.7: Comparison of the vertical eye opening and Q-factor between Infiniband cable and passive/active full scale TML system.

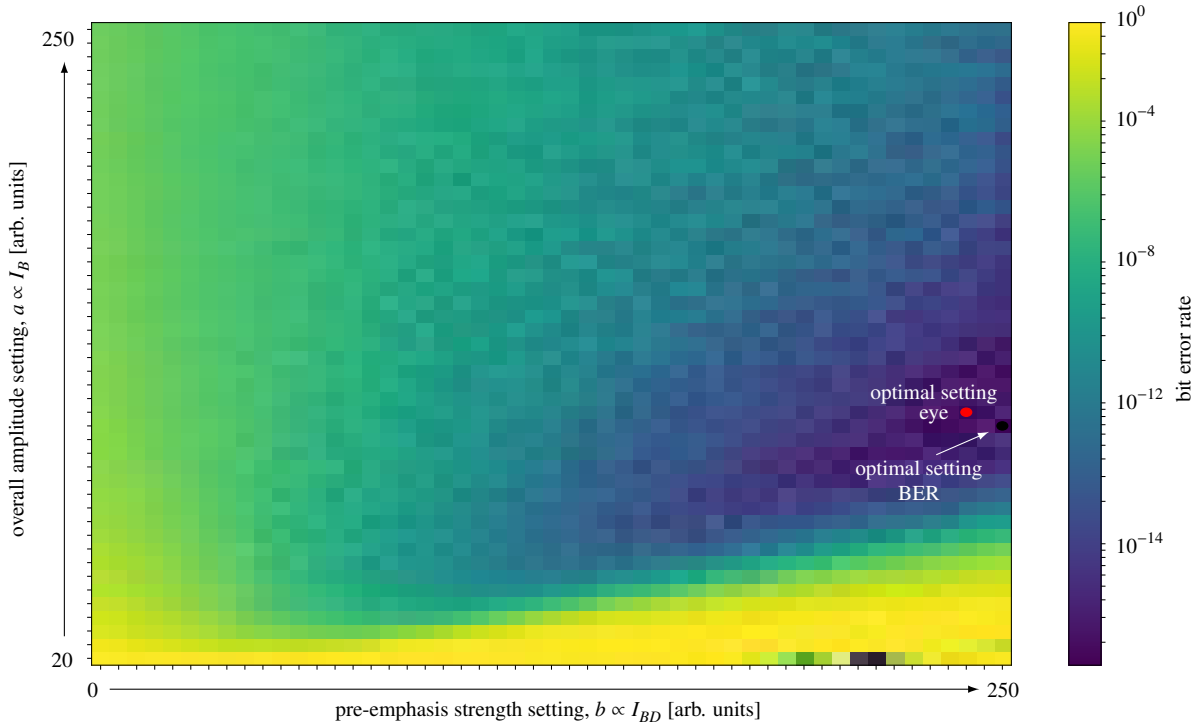


Figure 6.27: CML parameter scan for the full scale TML system with active CMOS CLC break-out board and extracted bit error rate (colour code). Optimal working point with respect to vertical eye opening and BER shown.

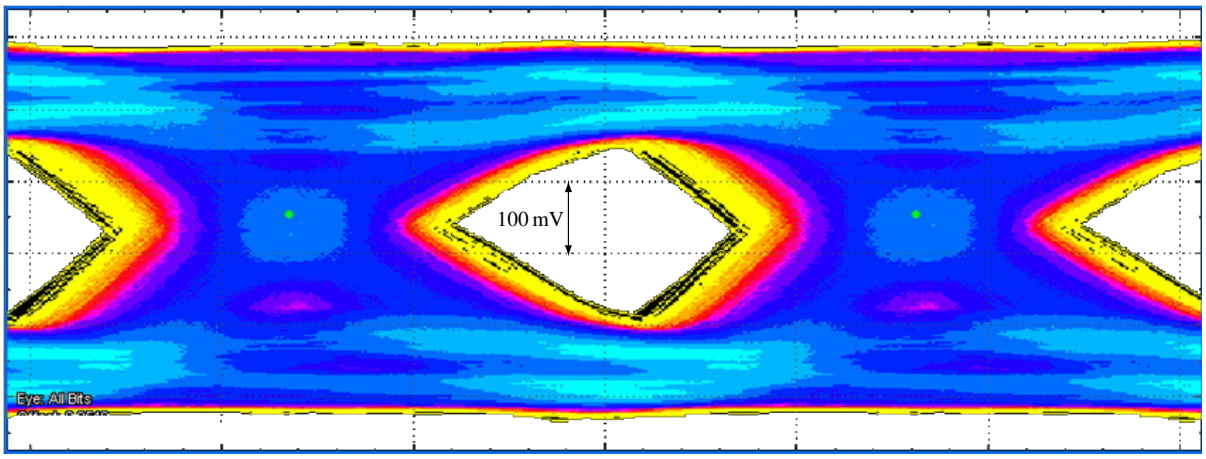


Figure 6.28: Measured eye diagram for optimal bias settings ($a = 100, b = 235$) with passive CLC break-out board.

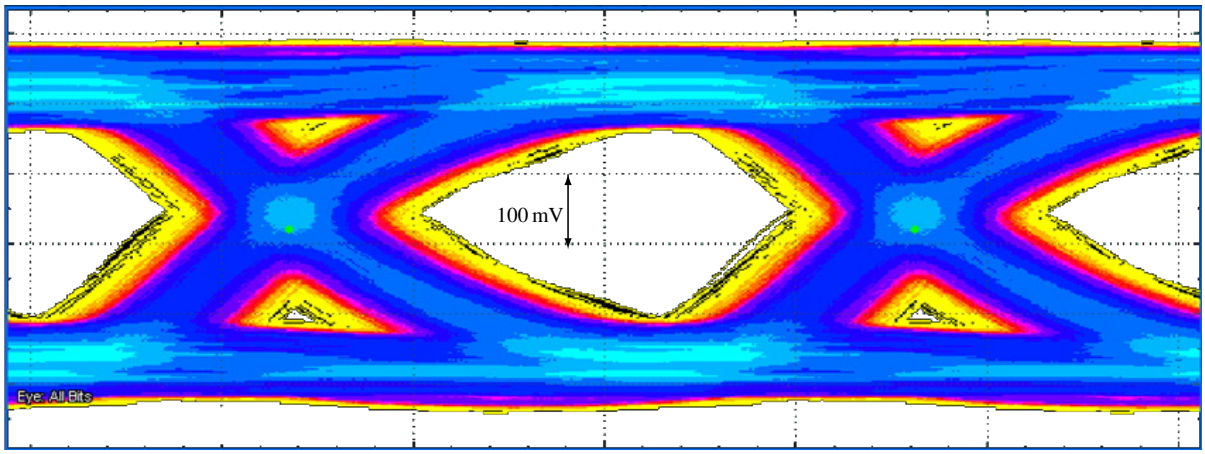


Figure 6.29: Measured eye diagram for optimal bias settings ($a = 100, b = 235$) with active CLC break-out board.

6.6 Full scale TML system: Proof of Principle at KEK

The full scale TML system with active CMOS CLC break-out board and the final PXD module works reliably in the lab environment with respect to data integrity. The link established by the back-end system is stable over weeks of operation. The PXD modules assembled in the PXD detector at the KEK facility on the other hand show some link instability. These instabilities correlate with the powering of the DCD on the module. At the current phase of the detector operation a known problem with the voltage sensing on the modules is present. A proper sensing is therefore not possible. This introduces an unknown situation of the applied voltages on the DHP. Since the powering of the on-module ASICs is not independent, i.e. common ground potential, changes in current consumption of the DCD shifts the ground potential of the DHP and thus changes the CML bias currents. This situation is mitigated by applying higher voltages at the regulators of the power supply of the system. Any voltage drop, that is not compensated by proper sensing, will not affect the CML driving capability as far as the core voltage applied at the DHP is not less than the nominal 1.2 V. For the physics phase operation the sensing problem will be solved and link stability should not be an issue. Within the final experiment, the active component of the CLC break-out board is implemented in the DHI and thus no dedicated PCB is needed.

CHAPTER 7

Conclusion and Discussion

The goal of this thesis is to investigate the data processing and driving capability of the Data Handling Processor of the PXD. Furthermore the signal integrity has been studied and the design of the transmission line system optimised for of the PXD. The Hit finder of the DHP, that is essential for the zero-suppression mode, copes with constant 2.86% occupancy of the PXD module with a effective hit extraction rate of 1.83(5) hits per data row. The simulated occupancy of 3% for the ASIC region within the detector has been simulated by the collaboration and is competitive with the results found with the thesis. The simulated occupancy states the maximal occupancy while particle injection takes place. The serial driver of the DHP, i.e. the CML driver, has been improved over the chip generations, generating a differential amplitude from 243.15(1) mV to 604.2(7) mV for version v1.1 and v1.2, respectively. With this improvement the differential output amplitude of the data signal, taking the full scale transmission line into account, exceeds the min. requirement of the optical converter by 40 mV. The bit error rates of less than 3×10^{-15} at a confidence level of 95% with a vertical eye opening of approx. 290 mV is achievable.

The full scale TML system has been qualified, characterised and tested. Scattering parameters have been extracted and an analytical model constructed to show that the assumptions used, to optimise the bias parameters of the CML driver via the developed simulation framework, is consistent with measurements. For the full scale transmission line, bias parameters for the overall amplitude a and the pre-emphasis strength b has been found in the region of $(a, b) = (100, 235)$. The parameter space, introducing sufficient high vertical eye openings, is roughly 20% of the total parameter space of the CML driver. The impedance mismatches along the transmission line system is less than 16% and therefore not sever.

The slew rate of the reference clock *gck*, at the far-end, i.e. PXD module, has been measured to be insufficiently low, i.e. $0.16\,{}^{\mathrm{V}}/_{\mathrm{ns}}$. Two flavours of active boards, introducing pre-emphasis on the *gck* signal at the near-end, i.e. DHE, have been introduced to increase the slew rate by a factor of approx. $4 - 5$ to approx. $0.7\,{}^{\mathrm{V}}/_{\mathrm{ns}}$. This results into a decrease of the jitter on the data signal of approx. 40 ps. The CMOS flavour has been chosen over the differential amplifier, to be implemented into the back-end system of the PXD because of its robustness against oscillations.

The mass testing of each single DHP mounted onto the PXD modules has been performed with a yield of proper working chip of approx. 98%, that is $70.56\,\mathrm{cm}^2$ out of $72\,\mathrm{cm}^2$ of processed area. This high values originates from the well controlled 65 nm process that is used for the DHP.

For the future the concept of a multi chip solution should be revised. The System-on-Chip approach, i.e. including converters and steering functionalities, could be an option. The read-out electronics, i.e. DCD and DHP, can be integrated into a single ASIC. Since the analogue-to-digital converters are most power consuming, cooling and powering are the most limiting factor using monolithic approaches such used in

the PXD. The transmission line system is sensitive to successively changed interfaces, that introduces connectors. These connectors highly degrade the signal integrity by impedance mismatches. Copper based transmission line systems face limits as signals exceed sup-gigabit data rates. Optical transmission on the other hand is not suitable in high radiation environments, since the optical properties of the fibres, especially the coating, degrades with higher irradiation. New technologies and approaches are needed to circumvent the limits of copper based transmission line systems in sup-gigabit data rate systems.

CHAPTER 8

Decomposition of κ for TML model

In order to model the TML the real and imaginary part of the complex function κ, that contains the characteristics of the particular model under test, have to be calculated. Therefore the decomposition is shown in more detail here. Furthermore the mathematical characteristics of κ is shown. Figure 8.1 shows the model under test.

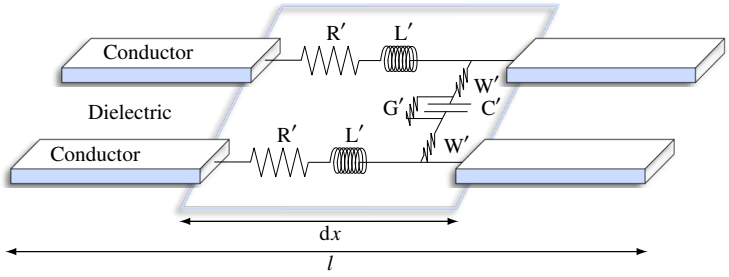


Figure 8.1: Differential cable model for the analysis of the complex function $\kappa(s)$.

The amplitude of the transfer function for the terminated case $Z_L = Z_0$ is given in 8.1

$$\mathcal{A}(\omega) = \sqrt{\frac{2 \cdot {Z_L}^2}{\left(1 + {Z_L}^2\right)\cosh(2\rho(\omega) \cdot l) + \left({Z_L}^2 - 1\right)\cos(2\epsilon(\omega) \cdot l) + 2{Z_L}^2 \sinh(2\rho(\omega) \cdot l)}} \tag{8.1}$$

κ manifests in two distinct forms dependent on the frequency range. Below and above the frequency in which the Skin depth is equal to the radius of the conductor,

$$\omega_{\text{Skin}} = \frac{1}{\mu\sigma \cdot r^2} \tag{8.2}$$

with the absolute permeability μ, conductance σ of the material and the radius r, the effective cross section of the conductor is constant.

Case $\omega < \omega_{\text{Skin}}$: κ can be written in the form of equation 3.26

$$\kappa(s) = \sqrt{\text{W}' \cdot \frac{\text{L}'\text{C}' \cdot s^2 + (\text{G}'\text{L}' + \text{R}'\text{C}') \cdot s + \text{G}'\text{R}'}{2\text{C}' \cdot s + \text{W}'(1 + \frac{2\text{G}'}{\text{W}'})}}. \tag{8.3}$$

The identity

$$\sqrt{a+\mathrm{i}b} = \pm\left(\sqrt{\frac{a+\sqrt{a^2+b^2}}{2}} + \mathrm{i}\,\mathrm{sgn}(b)\sqrt{\frac{-a+\sqrt{a^2+b^2}}{2}}\right), \quad a,b \in \mathbb{R} \tag{8.4}$$

can be used to decompose the square root of a complex function into the representation of the real and imaginary part. Henceforth we will restrict ourselves to the positive valued solution of the decomposition 8.4 such that

$$\kappa(s) = \sqrt{\tilde{\rho}+\mathrm{i}\tilde{\epsilon}} = \sqrt{\frac{\tilde{\rho}+\sqrt{\tilde{\rho}^2+\tilde{\epsilon}^2}}{2}} + \mathrm{i}\,\mathrm{sgn}(\tilde{\epsilon})\sqrt{\frac{-\tilde{\rho}+\sqrt{\tilde{\rho}^2+\tilde{\epsilon}^2}}{2}} = \rho + \mathrm{i}\,\mathrm{sgn}(\tilde{\epsilon})\epsilon \tag{8.5}$$

with

$$\rho = \sqrt{\frac{\tilde{\rho}+\sqrt{\tilde{\rho}^2+\tilde{\epsilon}^2}}{2}}, \qquad \epsilon = \sqrt{\frac{-\tilde{\rho}+\sqrt{\tilde{\rho}^2+\tilde{\epsilon}^2}}{2}}$$

The goal is to write equation 8.3 in the form of equation 8.5 and use the real and imaginary part. We define $T = \mathrm{W}'\left(1+\frac{2\mathrm{G}'}{\mathrm{W}'}\right)$ and $M = \mathrm{G}'\mathrm{L}' + \mathrm{R}'\mathrm{C}'$ and write $\kappa(s)^2$ as

$$\kappa(s)^2 = \mathrm{W}' \cdot \frac{\mathrm{L}'\mathrm{C}'s^2 + Ms + \mathrm{G}'\mathrm{R}'}{2\mathrm{C}'s + T} \cdot \frac{2\mathrm{C}'\overline{s} + T}{2\mathrm{C}'\overline{s} + T} = \mathrm{W}' \cdot \frac{\boxed{\mathrm{A}}}{\boxed{\mathrm{B}}} \tag{8.6}$$

by multiplying a smart one. The denominator $\boxed{\mathrm{B}}$ is real valued and can be written as

$$\boxed{\mathrm{B}} = (2\mathrm{C}'s + T)(2\mathrm{C}'\overline{s} + T) = 4\mathrm{C}'^2\omega^2 + 4\mathrm{C}'^2\alpha^2 + 4\mathrm{C}'T\alpha + T^2 \tag{8.7}$$

by using $s = \alpha + \mathrm{i}\omega$. Calculating the nominator $\boxed{\mathrm{A}}$ yields,

$$\boxed{\mathrm{A}} = (\mathrm{L}'\mathrm{C}'s^2 + Ms + \mathrm{G}'\mathrm{R}')(2\mathrm{C}'\overline{s} + T) = 2\mathrm{L}'\mathrm{C}'^2 s^2\overline{s} + \mathrm{L}'\mathrm{C}'Ts^2 + 2\mathrm{C}'Ms^2 + MTs + 2\mathrm{C}'\mathrm{G}'\mathrm{R}'\overline{s} + \mathrm{G}'\mathrm{R}'T \tag{8.8}$$

$$= 2\mathrm{L}'\mathrm{C}'^2\alpha^3 + 2\mathrm{L}'\mathrm{C}'^2\omega^2\alpha + (\alpha^2+\omega^2)(\mathrm{L}'\mathrm{C}'T + 2\mathrm{C}'M) + MT\alpha + 2\mathrm{C}'\mathrm{G}'\mathrm{R}'\alpha + \mathrm{G}'\mathrm{R}'T \tag{8.9}$$

$$+ \mathrm{i}\cdot\left(-2\mathrm{L}'\mathrm{C}'^2\alpha^2\omega - 2\mathrm{L}'\mathrm{C}'^2\omega^3 + MT\omega - 2\mathrm{C}'\mathrm{G}'\mathrm{R}'\omega\right) \tag{8.10}$$

For the off resonance case $\alpha = 0$[1] equation 8.6 yields by applying equation 8.7 to 8.10,

$$\mathrm{W}' \cdot \frac{\boxed{\mathrm{A}}}{\boxed{\mathrm{B}}} = \frac{\mathrm{W}'}{4\mathrm{C}'^2\omega^2 + T^2}\left((\mathrm{L}'\mathrm{C}'T + 2\mathrm{C}'M)\omega^2 + \mathrm{G}'\mathrm{R}'T + \mathrm{i}\cdot\left(-2\mathrm{L}'\mathrm{C}'^2\omega^3 + (MT - 2\mathrm{C}'\mathrm{G}'\mathrm{R}')\omega\right)\right) \tag{8.11}$$

[1] Henceforth $\alpha = 0$ will be assumed but not explicitly written in the equations. If needed it will be written in the context of the derivation.

We can identify $\tilde{\rho}$ and $\tilde{\epsilon}$ as

$$\tilde{\rho}(\omega) = \frac{\mathrm{W}'}{4\mathrm{C}'^2\omega^2 + T^2}\left((\mathrm{L}'T + 2M)\mathrm{C}'\omega^2 + \mathrm{G}'\mathrm{R}'T\right) \tag{8.12}$$

$$\tilde{\epsilon}(\omega) = \frac{\mathrm{W}'}{4\mathrm{C}'^2\omega^2 + T^2}\left(-2\mathrm{L}'\mathrm{C}'^2\omega^3 + (MT - 2\mathrm{C}'\mathrm{G}'\mathrm{R}')\omega\right) \tag{8.13}$$

Last step is to calculate $\rho(\omega)$ and $\epsilon(\omega)$ by using the identity 8.4. For that we compute $\sqrt{\tilde{\rho}(\omega)^2 + \tilde{\epsilon}(\omega)^2}$. We define the constants $T_1 = \mathrm{L}'T + 2M$ and $T_2 = MT - 2\mathrm{C}'\mathrm{G}'\mathrm{R}'$ present in equation 8.12 and 8.13 and write

$$\sqrt{\tilde{\rho}(\omega)^2 + \tilde{\epsilon}(\omega)^2} = \frac{\mathrm{W}'}{4\mathrm{C}'^2\omega^2 + T^2}\sqrt{\left(\mathrm{C}'T_1\omega^2 + \mathrm{G}'\mathrm{R}'T\right)^2 + \left(T_2\omega - 2\mathrm{L}'\mathrm{C}'^2\omega^3\right)^2} \tag{8.14}$$

Such that

$$\rho(\omega) = \sqrt{\frac{\mathrm{W}'}{4\mathrm{C}'^2\omega^2 + T^2}} \cdot \sqrt{\left(\mathrm{C}'T_1\omega^2 + \mathrm{G}'\mathrm{R}'T\right) + \sqrt{\left(\mathrm{C}'T_1\omega^2 + \mathrm{G}'\mathrm{R}'T\right)^2 + \left(T_2\omega - 2\mathrm{L}'\mathrm{C}'^2\omega^3\right)^2}} \tag{8.15}$$

$$\epsilon(\omega) = \sqrt{\frac{\mathrm{W}'}{4\mathrm{C}'^2\omega^2 + T^2}} \cdot \sqrt{-\left(\mathrm{C}'T_1\omega^2 + \mathrm{G}'\mathrm{R}'T\right) + \sqrt{\left(\mathrm{C}'T_1\omega^2 + \mathrm{G}'\mathrm{R}'T\right)^2 + \left(T_2\omega - 2\mathrm{L}'\mathrm{C}'^2\omega^3\right)^2}} \tag{8.16}$$

with

$$T = \mathrm{W}'\left(1 + \frac{2\mathrm{G}'}{\mathrm{W}'}\right), \quad M = \mathrm{G}'\mathrm{L}' + \mathrm{R}'\mathrm{C}', \quad T_1 = \mathrm{L}'T + 2M, \quad T_2 = MT - 2\mathrm{C}'\mathrm{G}'\mathrm{R}'$$

In equation 8.5 the sign of $\tilde{\epsilon}$ has to be taken into account. The sign switches at the frequency

$$\omega_0 = \sqrt{\frac{T_2}{2\mathrm{L}'\mathrm{C}'^2}}$$

see equation 8.14. Thus κ has two solutions

$$\kappa(s) = \begin{cases} \rho(\omega) + \mathrm{i}\cdot\epsilon(\omega) & , \omega < \omega_0 \\ \rho(\omega) - \mathrm{i}\cdot\epsilon(\omega) & , \omega > \omega_0 \end{cases} \tag{8.17}$$

with a positive and negative imaginary part depending on the frequency range. Due to the symmetry of the amplitude $\mathcal{A}(\omega)$, see equation 8.1, of the transfer function with respect to $\epsilon(\omega)$, the sign of $\tilde{\epsilon}$ has no influence on the form of equation 8.1. The imaginary $\epsilon(\omega)$ and real $\rho(\omega)$ part of $\kappa(s)$ are shown in figure 8.2 for different rations of $\frac{\mathrm{W}'}{\mathrm{G}'}$. For the DC case, i.e. $\omega = 0$, $\rho(\omega = 0) = \mathrm{R}' \cdot \left(\frac{1}{\mathrm{G}'} + \frac{2}{\mathrm{W}'}\right)^{-1}$ and $\epsilon(\omega = 0) = 0$ (Figure 8.2 has logarithmic scale! See equation 8.16). Furthermore the attenuation of the TML for $\omega = 0$ is

$$\mathcal{A}(\omega = 0; l) = \sqrt{\frac{2 \cdot {Z_L}^2}{\left(1 + {Z_L}^2\right)\cosh\left(2\frac{\mathrm{R}'\mathrm{G}'\mathrm{W}'}{\mathrm{W}'+2\mathrm{G}'} \cdot l\right) + \left({Z_L}^2 - 1\right) + 2{Z_L}^2\sinh\left(2\frac{\mathrm{R}'\mathrm{G}'\mathrm{W}'}{\mathrm{W}'+2\mathrm{G}'} \cdot l\right)}}$$

Figure 8.3 shows the amplitude $\mathcal{A}(\omega)$ at $\omega = 0$ of the model versus cable length l. This is due to the scaling factor $\frac{\mathrm{R}'\mathrm{G}'\mathrm{W}'}{\mathrm{W}'+2\mathrm{G}'} \approx 6.667 \times 10^{-9}\ \mathrm{m}^{-1}$. For small arguments of the hyperbolic functions $\cosh(x \approx 0) \approx 1$ and $\sinh(x \approx 0) \approx x$. Under the assumption $2\frac{\mathrm{R}'\mathrm{G}'\mathrm{W}'}{\mathrm{W}'+2\mathrm{G}'} \cdot l << Z_L^2$ one can show,

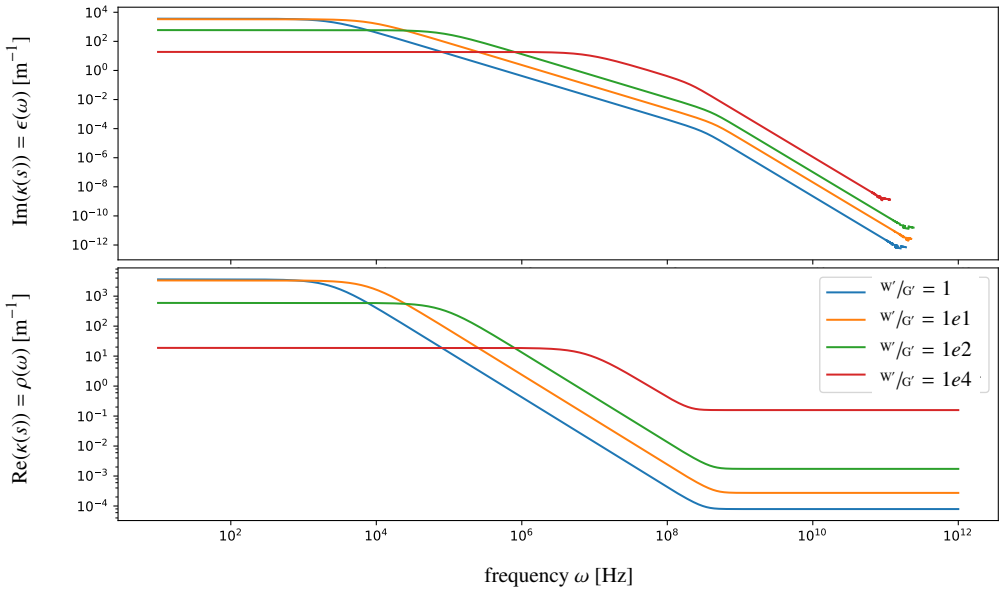


Figure 8.2: Imaginary and real part of the complex function κ versus frequency ω.
Parameters: $\{G' = 10^{-6}, C' = 10^{-10}, R' = 0.01, L' = 10^{-8}\}$ (Units omitted).

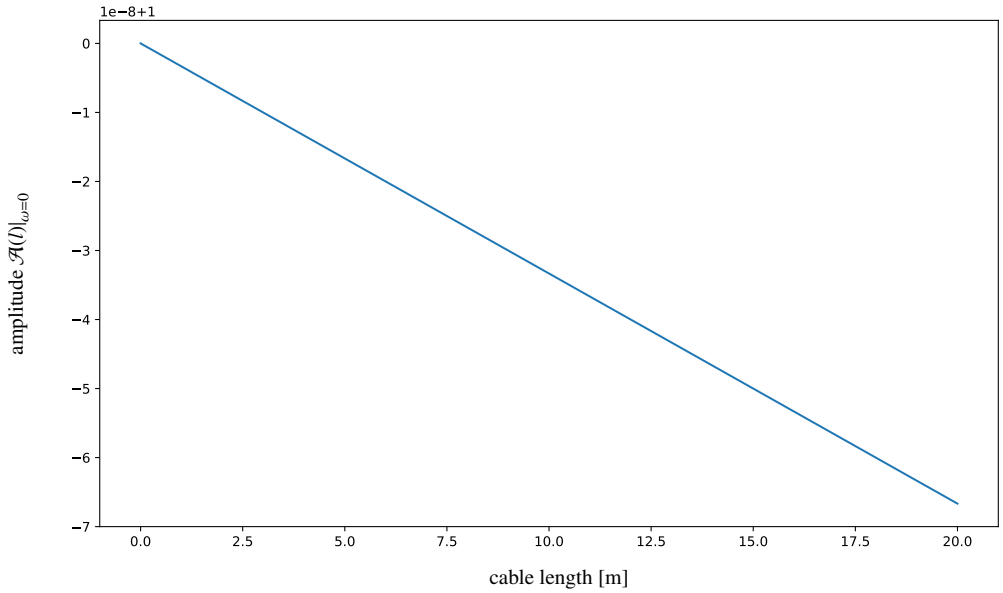


Figure 8.3: Amplitude $\mathcal{A}(\omega)$ at $\omega = 0$ of the model versus cable length l.
Parameters: $\{G' = 10^{-6}, C' = 10^{-10}, R' = 0.01, L' = 10^{-8}\}$ (Units omitted).

$$\mathcal{A}(l)|_{\omega=0} = \frac{1}{1 + 2\frac{R'G'W'}{W'+2G'} \cdot l} \tag{8.18}$$

Case $\omega > \omega_{\text{Skin}}$: For frequencies above $\omega_{S\,kin}$ the form of κ changes and we recall,

$$\kappa_{\text{Skin}}(s) = \sqrt{\mathrm{W}' \frac{\mathrm{C}' \cdot s^2 + \mathrm{G}' \cdot s}{2\mathrm{C}' \cdot s + \mathrm{W}'(1 + \frac{2\mathrm{G}'}{\mathrm{W}'})} \cdot \mathcal{D}(s)} = \sqrt{\tilde{\rho} + \mathrm{i}\tilde{\epsilon}} = \rho + \mathrm{i}\epsilon \tag{8.19}$$

We define $T = \mathrm{W}'(1 + \frac{2\mathrm{G}'}{\mathrm{W}'})$ and write

$$\kappa_{\text{Skin}}(s)^2 = \mathrm{W}' \frac{\mathrm{C}' \cdot s^2 + \mathrm{G}' \cdot s}{2\mathrm{C}' \cdot s + T} \cdot \mathcal{D}(s) \cdot \frac{2\mathrm{C}' \cdot \overline{s} + T}{2\mathrm{C}' \cdot \overline{s} + T} = \mathrm{W}' \cdot \mathcal{D}(s) \cdot \frac{\boxed{\mathrm{A}}}{\boxed{\mathrm{B}}} = \tilde{\rho} + \mathrm{i}\tilde{\epsilon} \tag{8.20}$$

by multiplying a smart one with $\boxed{\mathrm{A}}$ and $\boxed{\mathrm{B}}$ being the nominator and denominator, respectively. Comparing the physical units of the equation one finds $[\boxed{\mathrm{B}}] = (\Omega m)^{-2}$ and $[\boxed{\mathrm{A}}] = \mathrm{Hz}(\Omega\mathrm{m})^{-2}$. The denominator $\boxed{\mathrm{B}}$ is equal to the case with absence of the Skin effect, see equation 8.7,

$$\boxed{\mathrm{B}} = 4\mathrm{C}'^2\omega^2 + 4\mathrm{C}'^2\alpha^2 + 4\mathrm{C}'T\alpha + T^2 \tag{8.21}$$

For the nominator $\boxed{\mathrm{A}}$ one finds,

$$\boxed{\mathrm{A}} = \left(2\mathrm{C}'(\mathrm{C}'\alpha + 2\mathrm{G}') + \mathrm{C}'\mathrm{W}'\right)\omega^2 + 2\left(\mathrm{C}'^2\alpha^3 + \mathrm{C}'(2\mathrm{G}' + \mathrm{W}')\alpha^2 + \mathrm{G}'^2\alpha\right) + \mathrm{G}'\mathrm{W}'\alpha \tag{8.22}$$

$$+ \mathrm{i} \cdot \left(-2\mathrm{C}'^2\omega^3 + (-2\mathrm{C}'^2\alpha^2 + \mathrm{G}'\mathrm{W}' + 2\mathrm{G}'^2)\omega\right) \tag{8.23}$$

The next step is to decompose $\mathcal{D}(s)$ into its real and imaginary part. For that we recall the form of $\mathcal{D}(s)$,

$$\mathcal{D}(s) = \mathrm{L}' + L(s) = \mathrm{L}' + \frac{k_0}{k_1\sqrt{s} - 1} = \frac{\mathrm{L}'(k_1\sqrt{s} - 1) + k_0}{k_1\sqrt{s} - 1} \tag{8.24}$$

with material constants k_0 and k_1. The nominator and denominator of equation 8.24 can be multiplied by the complex conjugate of the denominator, i.e. $k_1\sqrt{\overline{s}} - 1$,

$$\mathcal{D}(s) = \mathrm{L}' + L(s) = \mathrm{L}' + \frac{k_0}{k_1\sqrt{s} - 1} = \frac{\mathrm{L}'(k_1\sqrt{s} - 1) + k_0}{k_1\sqrt{s} - 1} \cdot \frac{k_1\sqrt{\overline{s}} - 1}{k_1\sqrt{\overline{s}} - 1} = \frac{\boxed{\mathrm{C}}}{\boxed{\mathrm{D}}} \tag{8.25}$$

$\boxed{\mathrm{D}}$ yields,

$$(k_1\sqrt{s} - 1)(k_1\sqrt{\overline{s}} - 1) = k_1^2\sqrt{\alpha^2 + \omega^2} + 1 - k_1\left(\sqrt{s} + \sqrt{\overline{s}}\right) \tag{8.26}$$

Using the identity 8.4 one can write

$$\sqrt{s} = \pm(S_+ + \mathrm{i} \cdot S_-), \qquad \sqrt{\overline{s}} = \pm(S_+ - \mathrm{i} \cdot S_-) \tag{8.27}$$

$$S_\pm = \sqrt{\frac{\pm\alpha + \sqrt{\alpha^2 + \omega^2}}{2}} \tag{8.28}$$

and thus

$$\boxed{\mathrm{D}} = k_1^2\sqrt{\alpha^2 + \omega^2} + 1 - k_1\left(\pm(S_+ + \mathrm{i} \cdot S_-) \pm (S_+ - \mathrm{i} \cdot S_-)\right) \tag{8.29}$$

There are four solutions, namely

$$\sqrt{s} + \sqrt{s} = \begin{cases} \pm 2S_+ \\ \pm 2\mathrm{i}S_- \end{cases} \tag{8.30}$$

To obtain a real-valued expression of the denominator $\boxed{\mathrm{D}}$ only the real solutions are of interest. Equation 8.29 yields,

$$\boxed{\mathrm{D}} = 1 + k_1^2\sqrt{\alpha^2+\omega^2} - 2k_1(\pm S_+) \tag{8.31}$$

The positive solution $+S_+$ yields $\boxed{\mathrm{D}} \leq 1$ for $k_1 << 1$[2] and thus $|L(s)| \geq 0$. This is the physical relevant solution because $\mathrm{L}' + L(s)$ represents the increased total inductance by the Skin effect. Using the positive, real-valued solution of equation 8.29 $\mathcal{D}(s)$ can be written as,

$$\mathcal{D}(s) = \mathrm{L}' + \frac{k_0\left(k_1(S_+ - \mathrm{i}S_-) - 1\right)}{k_1^2\sqrt{\alpha^2+\omega^2} + 1 - 2k_1S_+} = \mathrm{L}' + \frac{k_0\left(k_1S_+ - 1\right)}{k_1^2\sqrt{\alpha^2+\omega^2} + 1 - 2k_1S_+} - \mathrm{i}\cdot\frac{k_0k_1S_-}{k_1^2\sqrt{\alpha^2+\omega^2} + 1 - 2k_1S_+} \tag{8.32}$$

Now we combine the expression of $\boxed{\mathrm{A}}$, $\boxed{\mathrm{B}}$ and $\mathcal{D}(s)$ from equation 8.23, 8.21 and 8.32, respectively. The result is,

$$\frac{\boxed{\mathrm{A}}}{\boxed{\mathrm{B}}}\cdot\mathcal{D}(s) = \frac{\mathrm{Re}(\boxed{\mathrm{A}}) + \mathrm{i}\cdot\mathrm{Im}(\boxed{\mathrm{A}})}{\boxed{\mathrm{B}}}\cdot\left(\mathrm{Re}(\mathcal{D}(s)) + \mathrm{i}\cdot\mathrm{Im}(\mathcal{D}(s))\right) \tag{8.33}$$

$$= \frac{\mathcal{R}_1\cdot\mathcal{R}_2 - \mathcal{I}_1\cdot\mathcal{I}_2 + \mathrm{i}\cdot(\mathcal{I}_1\cdot\mathcal{R}_2 + \mathcal{R}_1\cdot\mathcal{I}_2)}{4\mathrm{C}'^2\omega^2 + 4\mathrm{C}'^2\alpha^2 + 4\mathrm{C}'T\alpha + T^2} \tag{8.34}$$

with

$$\mathcal{R}_1 = \mathrm{Re}(\boxed{\mathrm{A}}) = \left(2\mathrm{C}'(\mathrm{C}'\alpha + 2\mathrm{G}') + \mathrm{C}'\mathrm{W}'\right)\omega^2 + 2\left(\mathrm{C}'^2\alpha^3 + \mathrm{C}'(2\mathrm{G}' + \mathrm{W}')\alpha^2 + \mathrm{G}'^2\alpha\right) + \mathrm{G}'\mathrm{W}'\alpha$$

$$\mathcal{I}_1 = \mathrm{Im}(\boxed{\mathrm{A}}) = \left(-2\mathrm{C}'^2\omega^3 + (-2\mathrm{C}'^2\alpha^2 + \mathrm{G}'\mathrm{W}' + 2\mathrm{G}'^2)\omega\right)$$

$$\mathcal{R}_2 = \mathrm{Re}(\mathcal{D}(s)) = \mathrm{L}' + \frac{k_0\left(k_1S_+ - 1\right)}{k_1^2\sqrt{\alpha^2+\omega^2} + 1 - 2k_1S_+}$$

$$\mathcal{I}_2 = \mathrm{Im}(\mathcal{D}(s)) = -\frac{k_0k_1S_-}{k_1^2\sqrt{\alpha^2+\omega^2} + 1 - 2k_1S_+}$$

$$T = \mathrm{W}'\left(1 + \frac{2\mathrm{G}'}{\mathrm{W}'}\right)$$

[2] The constant $k_1 = 2r\sqrt{\mu\sigma} \approx \mathcal{O}(r)$ with radius r, absolute permeability μ and conductivity σ of copper is of order of the radius dimension.

Now with equation 8.34 the decomposition of $\kappa_{\text{Skin}}(s)^2$ for the off resonance limit, i.e. $\alpha \to 0$, can be performed and $\tilde{\rho}$ and $\tilde{\epsilon}$ identified as,

$$\tilde{\rho}(\omega) = \frac{\mathrm{W}'}{\left(4\mathrm{C}'^2\omega^2 + T^2\right)\left(k_1^2\omega + 1 - k_1\sqrt{2\omega}\right)}\left(\tau_3\omega^3 + \tau_2\omega^2 + \tau_1\omega^{\frac{5}{2}}\right) \tag{8.35}$$

$$\tag{8.36}$$

with

$$\tau_1 = k_1\left(2\mathrm{G}' + T\right)\mathrm{C}'\left(\frac{k_0}{\sqrt{2}} - \sqrt{2}\mathrm{L}'\right) \tag{8.37}$$

$$\tau_2 = \left(2\mathrm{G}' + T\right)\mathrm{C}'\left(\mathrm{L}' - k_0\right) \tag{8.38}$$

$$\tau_3 = \left(2\mathrm{G}' + T\right)\mathrm{C}'k_1^2\mathrm{L}' \tag{8.39}$$

and

$$\tilde{\epsilon}(\omega) = \frac{\mathrm{W}'}{\left(4\mathrm{C}'^2\omega^2 + T^2\right)\left(k_1^2\omega + 1 - k_1\sqrt{2\omega}\right)}\left(\tau_9\omega^4 + \tau_8\omega^3 + \tau_7\omega^2 + \tau_6\omega + \tau_5\omega^{\frac{7}{2}} + \tau_4\omega^{\frac{5}{2}}\right) \tag{8.40}$$

$$\tag{8.41}$$

with

$$\tau_4 = k_1\left(\mathrm{G}'T\left(\frac{k_0}{\sqrt{2}} - \sqrt{2}\mathrm{L}'\right) + \frac{k_0}{\sqrt{2}}\left(2\mathrm{G}' + T\right)\mathrm{C}'\right) \tag{8.42}$$

$$\tau_5 = 2\left(\sqrt{2}\mathrm{L}' - \frac{k_0}{\sqrt{2}}\right)\mathrm{C}'^2 \tag{8.43}$$

$$\tau_6 = \mathrm{G}'T\left(\mathrm{L}' - k_0\right) \tag{8.44}$$

$$\tau_7 = \mathrm{G}'Tk_1^2\mathrm{L}' \tag{8.45}$$

$$\tau_8 = -2\mathrm{L}'\mathrm{C}'^2k_1^2 \tag{8.46}$$

Using the expressions for $\tilde{\rho}(\omega)$ and $\tilde{\epsilon}(\omega)$ the real and imaginary part of $\kappa_{\text{Skin}}(s)$ can be found to be

$$\rho(\omega) = \sqrt{\frac{\mathrm{W}'}{\left(4\mathrm{C}'^2\omega^2 + T^2\right)\left(k_1^2\omega + 1 - k_1\sqrt{2\omega}\right)}} \sqrt{\begin{pmatrix}\tau_1\\ \tau_2\\ \tau_3\end{pmatrix} \bullet \begin{pmatrix}\omega^3\\ \omega^2\\ \omega^{\frac{5}{2}}\end{pmatrix} + \sqrt{\left(\begin{pmatrix}\tau_1\\ \tau_2\\ \tau_3\end{pmatrix} \bullet \begin{pmatrix}\omega^3\\ \omega^2\\ \omega^{\frac{5}{2}}\end{pmatrix}\right)^2 + \left(\begin{pmatrix}\tau_9\\ \tau_8\\ \tau_7\\ \tau_6\\ \tau_5\\ \tau_4\end{pmatrix} \bullet \begin{pmatrix}\omega^4\\ \omega^3\\ \omega^2\\ \omega^1\\ \omega^{\frac{7}{2}}\\ \omega^{\frac{5}{2}}\end{pmatrix}\right)^2}} \tag{8.47}$$

$$\epsilon(\omega) = \sqrt{\frac{\mathrm{W}'}{\left(4\mathrm{C}'^2\omega^2 + T^2\right)\left(k_1^2\omega + 1 - k_1\sqrt{2\omega}\right)}} \sqrt{-\begin{pmatrix}\tau_1\\ \tau_2\\ \tau_3\end{pmatrix} \bullet \begin{pmatrix}\omega^3\\ \omega^2\\ \omega^{\frac{5}{2}}\end{pmatrix} + \sqrt{\left(\begin{pmatrix}\tau_1\\ \tau_2\\ \tau_3\end{pmatrix} \bullet \begin{pmatrix}\omega^3\\ \omega^2\\ \omega^{\frac{5}{2}}\end{pmatrix}\right)^2 + \left(\begin{pmatrix}\tau_9\\ \tau_8\\ \tau_7\\ \tau_6\\ \tau_5\\ \tau_4\end{pmatrix} \bullet \begin{pmatrix}\omega^4\\ \omega^3\\ \omega^2\\ \omega^1\\ \omega^{\frac{7}{2}}\\ \omega^{\frac{5}{2}}\end{pmatrix}\right)^2}} \tag{8.48}$$

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'Nel mezzo del cammin di nostra vita mi ritrovai per una selva oscura, ché la diritta via era smarrita.
Ahi quanto a dir qual era è cosa dura esta selva selvaggia e aspra e forte che nel pensier rinova la paura!
Tant' è amara che poco è più morte; ma per trattar del ben ch'i' vi trovai, dirò de l'altre cose ch'i' v'ho scorte.'

'In the middle of the journey of our life, I came to myself, in a dark wood, where the direct way was lost.
It is a hard thing to speak of, how wild, harsh and impenetrable that wood was, so that thinking of it recreates the fear.
It is scarcely less bitter than death: but, in order to tell of the good that I found there, I must tell of the other things I saw there.'

Dante Alighieri, La Comedia Devina

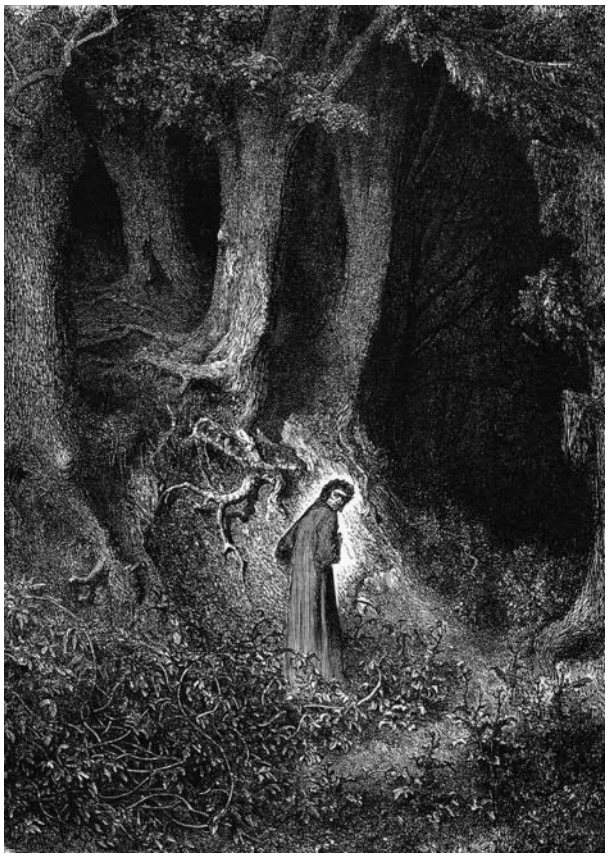

Illustration of Gustave Doré, 1861.

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