Characterization of final Belle II PXD production modules

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I hereby declare that this thesis was formulated by myself and that no sources or tools other than those cited were used.

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CHAPTER 1

Introduction

Particle physics deals with the fundamental particles and forces. To describe the interaction of these particles, a wide variety of models and mathematical theories have been developed. The standard model of particle physics is so far the most successful of these theories and contains all known fundamental particles and three of four known fundamental forces. It is based on the experimental observations of particle accelerators and their respective detectors.

Various experiments are performed to test the Standard Model. To investigate the puzzle of the imbalance of matter and antimatter, CP-violation in B-meson decays are investigated. CP-symmetry describes the invariance of a process under charge conjugation (C) and parity conservation (P). CP-violation was first observed in 1964 in a kaon decay system. It was not until 1972 that a scheme including the weak interaction was introduced by Kobayashi and Maskawa combining CP-violation with the Standard Model theory. Thereby a third quark family was predicted, the top and the bottom quark, which were not experimentally observed at that time. Due to charged-current interaction, the CP-violation and the flavor mixing could be integrated into the standard model using the Cabbibo-Kobayashi-Maskawa (CKM) formalism. In 2001, this theory has been validated at the Belle detector in Japan. [1, 2]

Despite the comprehensive Standard Model theory, fundamental questions in particle physics still remain open. For example, the Kobayashi-Maskawa model cannot explain the magnitude of the observed baryon asymmetry in the universe. To investigate the puzzle, the Belle II experiment at the SuperKEKB accelerator in Japan deals with CP-violation in B-meson decays. To continue research on physics beyond the standard model and to achieve higher precision in the measurement of rare processes. Consequently, a luminosity upgrade by a factor of 40 was performed at the KEKB to SuperKEKB and an upgrade of the Belle detector to the Belle II detector was needed, until 2018. A pixel detector (PXD) was added to the inner layer of the detector to achieve higher resolution on the vertices of the decay particles. [3]

Due to delays in the production only a part of the PXD detector was installed while data taking took place in 2019. The complete PXD geometry is planned to be incorporated in 2023. [4]

The present thesis focuses on the calibration, optimization and precision characterization of the PXD II modules, which are scheduled to be installed in the PXD detector during 2022. Each PXD module must be tested for full functionality after fabrication. In addition, operation parameters have to be tuned individually to achieve good detector efficiency. An optimization process on the modules is particularly important to ensure the homogeneity of the pixel response. To understand in more

detail the properties of the PXD module, two characteristic quantities, the transconductance g_m and the internal amplification g_q are investigated pixel by pixel in the PXD module. Furthermore the influence on the readout current of the digitization process is investigated.

In the chapters 2 and 3, an overview of the SuperKEKB and the Belle II detector is given. The main focus is on the PXD detector, its working principle and properties. In chapter 4 an overview of the laboratory characterization setup is given in which the modules are tested and characterized. A new dew point monitoring system was built and commissioned for the setup and described in detail. The main characterization steps of the PXD module are detailed in chapter 5. A study of the influence of the biasing voltages of the PXD module on the readout current follows in Chapter 6. The chapter 7 describes the measurement of DCD influence on the drain currents. Finally, the measurement of the DEPFET characteristics on pixel level is described in detail in chapter 8 and the absolute oxide capacity is determined.

CHAPTER 2

The Belle II Detector at the SuperKEKB collider

The Belle II Detector is located at the SuperKEKB circular asymmetric electron-positron collider, which is the upgrade of the former KEKB collider, at the KEK research complex in Tsukuba, Japan. SuperKEKB has a 40 times higher luminosity. To be able to measure such high collision rate, arising due to the higher luminosity, the former Belle detector is upgraded to the Belle II. To improve the vertex resolution, Belle II is equipped with two layers of silicon pixel sensors, located closest to the interaction point. The so called vertex detector consists of the inner PiXel Detector (PXD) and the strip vertex detector (SVD). In the following a short introduction to the SuperKEKB and physical properties are presented. An overview on the Belle II detector components and their placement is given.

2.1 SuperKEKB Collider

In figure 2.1 a schematic illustration of the SuperKEKB is given. Electrons are generated via the photoelectric effect, while the positrons are generated as secondary particles, via bremsstrahlung. The particles are accelerated over linear accelerators (linacs) and then injected into their respective storing rings: electrons into the High Energy Ring (HER) and positron into the Low Energy Ring (LER). Particle bunches are brought to the collision point, where the Belle II detectors records the collision events. [3, 5]

The SuperKEKB collider is a so-called B-factory, with a center-of-mass energy of 10.58 GeV. This energy describes exactly the $\Upsilon(4s)$ resonance. Mainly $\Upsilon(4s)$ mesons are produced, which further decay into $B\bar{B}$-meson with a branching fraction of more than 96 %. Since $\Upsilon(4s)$-mesons have a rather short decay time, they decay very close to the interaction point. Due to the asymmetry in the collider, the longer lived B-mesons (≈ 1 ps) are boosted along the beam axis. The vertices of the individual B-decays are displaced. This allows to identify the decay products of a single B-meson. A time dependence of the B-decays can be measured during the reconstruction of these vertices, which can be used to study the CP-violation of the B-mesons. The CP violation has been theoretically described in 2008 (Kobayashi, Maskawa), the measured level was insufficient to explain the full amount of the observed matter-antimatter asymmetry. With the luminosity upgrade to $L = 8 \cdot 10^{-35}\mathrm{cm}^{-2}\mathrm{s}^{-1}$, the B-physics studies can be investigated with much higher statistics. Uncertainties on the CP-violation can be reduced and the sensitivity to the beyond standard model contribution increased. In addition the Belle experiment so far found rare decays and CKM matrix elements were measured to higher

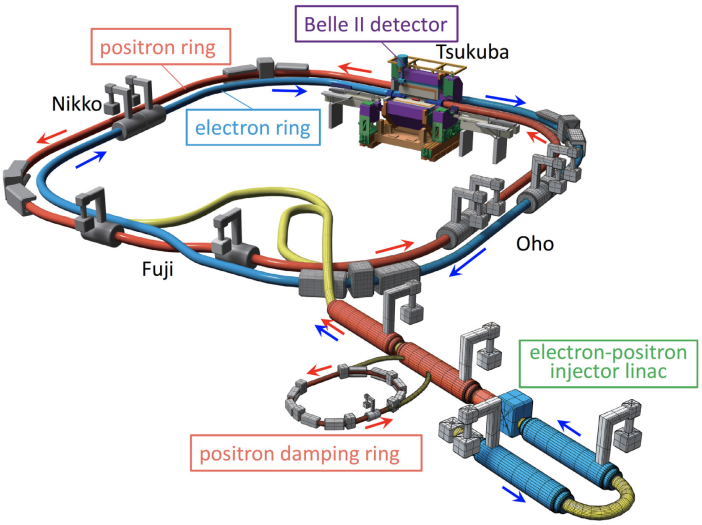


Figure 2.1: Schematics of SuperKEKB collider. Electrons and Positrons get accelerated in a linear accelerator, before injecting them into the storage rings HER and LER. They particle bunches collide at the interaction region inside the Belle II detector volume. [3]

precision. [6]

2.2 The Belle II detector

Due to the luminosity upgrade, the Belle II detector had to be improved. Despite higher occupancy leading to higher background, a fast readout and efficient operation was required. The detector should additionally withstand a higher radiation hardness. The upgraded detector was commissioned for the first time in 2018. The setup can be seen in figure 2.2. The detector consists of seven layers to cover all decay products and their physical properties. Since especially the B-meson pairs are investigated, the detector is aimed towards detecting the decay products of these. The seven sub-detectors allow determining the track, the particle type, the vertex and the energy of the decay products. The following information are taken from [5].

The *vertex detector* is the innermost sub-detector closest to the interaction region, which was redesigned during the detector update. It consists of the *Pixel Detector (PXD)*, which is surrounded by the *Strip Vertex Detector (SVD)* .

The innermost layer, the PXD, contributes to reconstruct the decay vertices of the B-mesons with a higher special resolution. Due to the adjustments of beam energies during the luminosity upgrade this pixel sensor technology was upgraded to be able to measure the evoked narrowed separation between the B-mesons vertices. It consists of two layers with radius of 14 mm and 22 mm. This work focuses on the PXD detector layer. It will be introduced in detail in chapter 3.

The mayor task of the SVD is to reconstruct the tracks of passing particles and determine their momenta. Furthermore it is able to reconstruct long-lived particles which decay outside of the PXD. It consists of four layers of double-sided silicon strip sensors. These are cylindrical arranged around the beam pipe with a radius of $38, 80, 115$ and $140\,\text{mm}$. The sensors consists of p- and n-doped semiconductor strips. When ionizing particles traverse, they create electron-hole pairs drifting to the

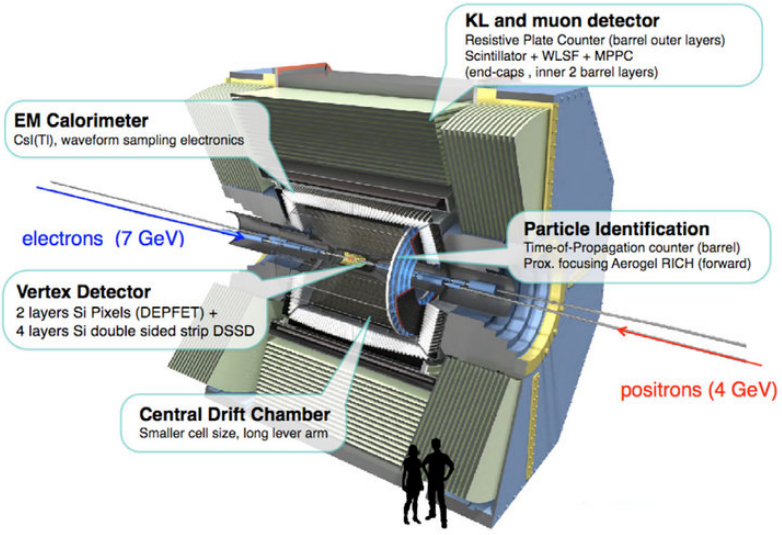


Figure 2.2: Schematics of the Belle II detector. It consists of seven sub-detector with the vertex detector closest to the interaction point, where electrons and positrons with asymmetric energy collide. [7]

p and *n* side. This gives a precise two dimensional spatial information of the decay particle track. Together with the PXD, they form the Vertex Detector of the Belle II detector. The combination of both parts gives a vertex reconstruction with a spatial resolution of $\sigma_z = 20\,\mu$m.

The layer surrounding the Vertex Detector is the *Central Drift Chamber (CDC)*, which measures charge particle trajectories. Resulting from these, the momentum can be determined by applying a magnetic field a measuring the radius of the resulting curved tracks. The energy loss of the decay particles inside the gas filled chamber provides additional information for particle identification. The chamber is equipped with field and sense wires and covers the detector volume from 16 to 113 cm radius from the interaction point. When a charged particle is traversing, it collides with gas-atoms and produces electron-ion pairs. Due to the sense and field wires, the primary electrons continue to ionize gas atoms and an avalanche gas amplification occurs. The electrons finally collected at the sense wires are proportional to the primary produced electrons. Thus the particle energy loss can be calculated.

Outside of the CDC volume the *Time-of-Propagation (TOP)* Counter is located. Together with the Aerogel Ring Imaging Counter (ARICH) it is the main device for particle identification. It consists of 16 quartz radiators with attached photomulitpliers. These are especially designed to detect the difference between kaon- and pion -mesons, which are decay modes of the *B*-meson. The measurement principle is based on the Cherenkov effect. The Cherenkov photons reflected internally under the Cherenkov angle in the quartz can lead to reconstruction and identification of the traversing particles with the help of their temporal and spacial information.

The *Aerogel Ring Imaging Cherenkov (ARICH)* Counter detector is used like the TOP detector for particle identification. The difference to the TOP measurement method is that the particles pass an aerogel radiator, where the cherenkov light hits a photo detector in a cone structure. The velocity of the traversing particles and thus the particle mass can be determined. This allows to separate lighter electrons, muons and pions with an energy below 1 GeV. In addition it also provides information on the discrimination between kaon- and pion-mesons.

The main task of the *Electromagnetic CaLorimeter (ECL)* is to measure photons with high efficiency. The third main product of the B-mesons is a π^0, which decays directly into two photons. The detector detects photons and electrons, their energy and angular coordinates. Furthermore, it detects K_L particles together with the K_L and muon detector. It consists of inner barrel crystals with photodetectors, which measures the light outcome by the electromagnetic interactions. With a radius of 1.25 m it is located at 2 m distance in forward and 1 m distance in backward direction to the interaction point.

As the name of the outer K_L *and Muon detector (KLM)* indicates, it is intended to detect the two particles, K_L and muons (hadron calorimeter). Due to the long lifetime of the muon and the low interaction with the other detector layers it travels much further than other particles. Together with the charged track from the CDC and their deposited energy in the KLM, the muon can be identified. Since K_L mostly decay into three pions, the track of previously produced pions within the CDC is an indicator to distinguish the two particles. The KLM is designed to bring most of the K_L to decay within the barrel layers. All layers are interspersed with 4.7 cm thick iron plates, which are used as the reflux yoke of the 1.5 T magnet enclosing all other sub detectors. They are also used as stopping material for K_L. When the K_L collides with an iron nucleus it leaves an hadronic shower signal with all of it's energy as a signature.

CHAPTER 3

The DEPFET Pixel Detector for Belle II

The Pixel Detector (PXD) is the the most inner layer for Belle II. It consists of monolithic pieces of silicon, meaning the sensor part and readout electronics are included. This makes a difference to the hybrid pixel detectors used for example in the ATLAS detector [9] (at LHC, Cern) where sensors and chips are separated. For the innermost layer of the Belle II detector it is crucial to have a low material budget for high precision tracking. Since Coulomb multiple scattering dominates for particles with low momentum (2 GeV), detectors with little material in the particle beam path are very important for momentum measurements. [8]

In the following the DEPFET pixel cells, their layout, working principle, and characteristics are explained. In addition, the readout chips and the module structure is presented.

3.1 DEpleted P-channel Field Effect Transistor

The DEpleted P-channel Field Effect Transistor (DEPFET) [10], illustrated in figure 3.1, consists of an high-resistivity n-type silicon bulk which provides the detector substrate. A p-channel Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) [11] is integrated on top of the detector substrate with source, gate and drain electrodes. Between a p^+ back-side contact and the source electrode a negative high voltage is applied to deplete the bulk by sideward depletion (depletion from both sides). At a distance of 1 µm to the external gate an additional deep n-well implant inside the detector substrate causes a potential minimum and works as an internal gate. [12]

When ionizing particles traverse the detector material electron-hole pairs will be generated. The produced electrons drift to the potential minimum (the internal gate) while the holes move to the p^+-contact. When the transistor is switched on a p-channel current (drain current I_D) from source to drain arises, which is controlled by the external gate. The accumulated electrons in the internal gate induce a mirror charge in the external gate that modulates the p-channel drain current I_D. The accumulated charge inside the internal gate increases therefore the p channel transistor drain current I_D. The change in the drain current I_D is measured by the drain contact.

The internal gate collects electrons until a positive voltage at the so called clear contact is applied (right figure 3.1). This forms an n-channel between the internal gate and the clear contact and all electrons accumulate at the internal gate are removed. The clear process is important to prevent a saturation of the internal gate and makes the detector sensitive to new signals. The deep p- well implantation below the clear gate prevents the clear gate to accidentally remove electrons during the

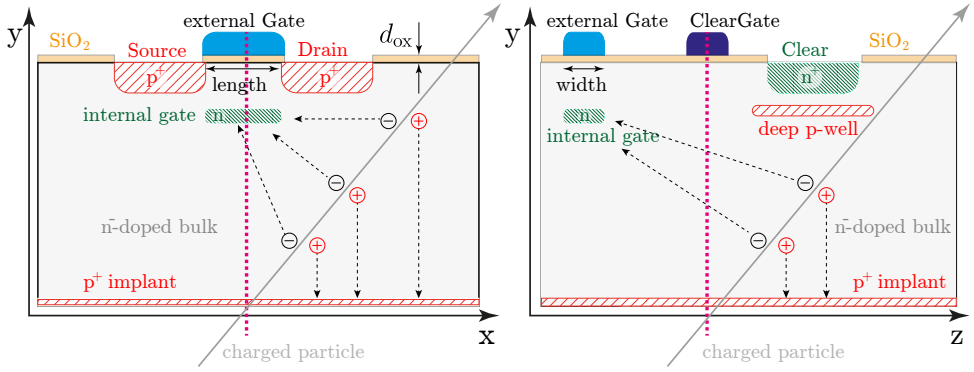


Figure 3.1: Cross section of a DEPFET pixel. On top of a n^- doped silicon bulk a MOSFET is implemented, which consists of the source, drain implants, and the external gate and the clear gate. An additional n-implantation below the external gate collects the signal electrons from electron-hole pairs created by a traversing particle. [13]

charge collection. [12]

3.1.1 Amplification

As described in [14] the drain current of a DEPFET pixel I_D is given by:

$$I_D = -\frac{W}{2L}\mu_h C_{ox}\left(f\frac{Q_{sig}}{WLC_{ox}} + V_G - V_T\right)^2. \tag{3.1}$$

Here, the width and length of the transistor is given by W and L. The mobility of the holes are stated with μ_h, the coupling factor describing how much the charge in the internal gate will be induced into the channel with f, the threshold voltage to turn on the FET with V_T, the gate voltage with V_G and the signal charge inside the internal gate with Q_{sig}. The oxide capacitance C_{ox} per unit area is defined as

$$C_{ox} = \frac{\epsilon_{ox}\epsilon_0}{d_{ox}}, \tag{3.2}$$

with ϵ_{ox} being the dielectric constant inside the oxide, ϵ_0 the vacuum permittivity and d_{ox} the width of the oxide layer (see figure 3.1). The gate oxide is the dielectric layer that separates the gate junction of a MOSFET from the source and drain implant. Further it acts as a conductive channel that connects the source and drain when the transistor is turned on. The current response ΔI_D to a single electron e^- collected in the internal gate is called internal amplification g_q [5]:

$$g_q = \frac{\Delta I_D}{e^-} = -\frac{f\mu_h}{L^2}\left[V_G - V_T + f\frac{Q_{sig}}{WL^3C_{ox}}\right] = f\sqrt{\frac{2\mu_h}{WL^3C_{ox}}\cdot I_D}. \tag{3.3}$$

Due to process variations the internal amplifications has a different order of magnitude for every pixel. Usually the values are around $400 - 600\,\mathrm{pA/e^-}$ [5].

The transconductance g_m of the DEPFET, which is also called the external amplification g_m, is a

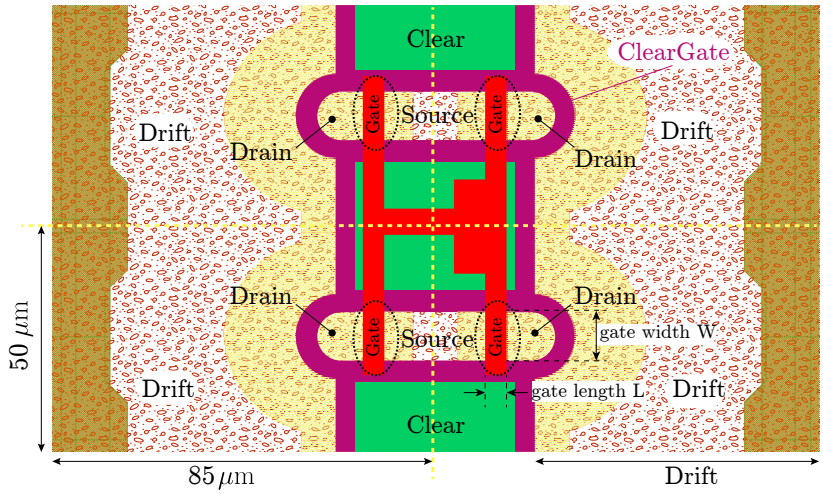


Figure 3.2: The layout of PXD9 DEPFET pixels is shown, where two pixel share a common source and clear implant. Four pixels are depicted and separated by the yellow dotted line. In purple the poly-silicon 1 (clear gate), in red the poly-silicon 2 (external gate), in green the n^+ implant (clear implant), in light yellow the n implant (also internal gate), in orange the additional drift implants and with the red pattern the p implant is depicted. [13]

quantity that characterizes the amplification of the transistor. It is defined as [14]

$$g_m = \frac{\delta I_D}{\delta V_G} = -\frac{W}{L}\mu_h C_{ox}\left(f\frac{Q_{sig}}{WLC_{ox}} + V_G - V_T\right) = \sqrt{\frac{2W\mu_h C_{ox}}{L}\cdot I_D}. \tag{3.4}$$

Investigation on the internal amplification g_q and the transconductance g_m are presented in section 8.

3.1.2 DEPFET Pixel Layout

A DEPFET matrix (the sensitive area) consists of DEPFET pixel cells in a 256 x 768 matrix for a so called PXD module. [5]

Every forth pixel is combined column-wise to the drain line. This is shown in figure 3.2, where the pixels are separated by a yellow dotted line. A double pixel cell is sharing a source implant and a clear implant (green). The clear implants surround the internal gate (light yellow) of each pixel. The clear gate region is separating the MOSFET including the source implant, the external gate (in red) and drain implant from the clear implant and surrounding drift region.

Two aluminum metal layers are placed on top. Figure 3.3 shows the pixel layout as before with 8 neighboring pixels with electrical contacts and metal layers included. The vertical blue lines represent the first aluminum layer (*alu1*). In this metal layer clear, drift, drift and source regions are connected by traces. On top, a second aluminum layer (*alu2*) is placed, which is depicted by the horizontal dark blue lines. The turquoise rectangles illustrate the contacts between the two aluminum layers while the black rectangles represent the contacts between the first aluminum layer and the silicon. The detailed layout of the sensitive region is relevant for the structure analysis in chapter 8.

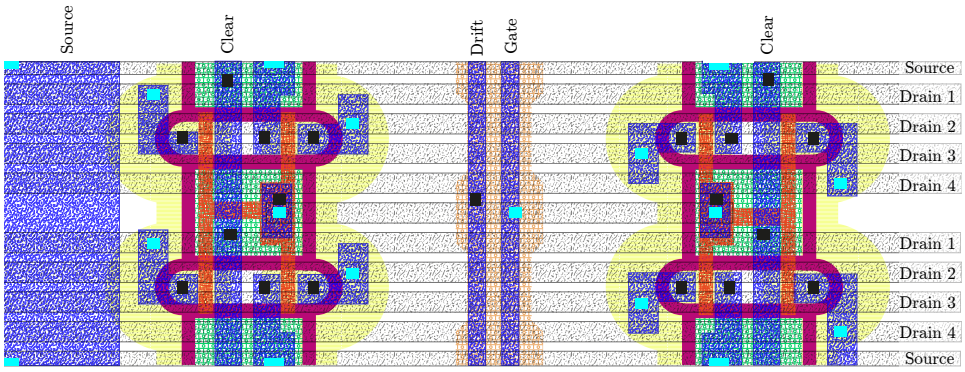


Figure 3.3: Layout of PXD9 DEPFET pixel with electrical connection and metallization. The color code is equal to figure 3.2. The horizontal light blue lines depict the first aluminum layer while the vertical dark blue lines show the second layer. The turquoise rectangular describes the connections between the two layers and the black ones illustrate the connections between the first layer and the silicon. [13]

3.1.3 Bulk Depletion

When a p-type semiconductor is connected to an n-type semiconductor a p-n junction is formed. A net negative charge is formed on the p-side of the p-n junction and a net positive charge on the n-side. The region near the junction where the flow of charge carriers decreases over time, resulting in empty charge carriers or many immobile charge carriers, is called the depletion zone. For the so-called sideward depletion (see figure 3.4) inside the DEPFET pixel an electrode is connected to the punch through contact on the front side (a p^+ implant). A negative backside bias voltage (hv) is applied. The larger the bias voltage, the more the depletion extents zone inside the bulk. From about hv = -35 V, the depletion zone reaches the backside and gets biased via the punch-through. bulk current (hv current) can be measured. From -60 V to -70 V the entire bulk is depleted. If now further negative voltage is applied, the bulk current saturates and the so-called *punch-through mechanism* appears again, which is depicted in figure 3.5. Through thermal created electron hole pairs and leakage current, holes are created which drift from the internal gate, the n^- bulk, to the backside. They then move in the direction of the source contact along the backside. Before crossing the bulk and reaching the p-source contact, the holes cross a small potential barrier. These holes are responsible for the additional punch-through current. The punch-through effect is discussed further in chapter 6.2.4. [14]

3.1.4 Readout Mechanism of a DEPFET Matrix

The equivalent circuit symbol for a DEPFET pixel is shown in figure 3.6(a). As shown in figure 3.2, all clear and gate lines of each row are connected. Every fourth pixel is combined column wise to the drain line. Thus, DEPFET pixel are enabled row-wise while the drain current is read out column-wise.

The matrix is read out in a four-fold rolling shutter system. The process is illustrated in figure 3.6(b). Accordingly, four pixel rows are read out simultaneously with the advantage that the readout time is faster by a factor of 4. Applying a negative voltage to the gate voltage, the transistors of the four DEPFET rows are switched on simultaneously. Further, the drain current is read out column by column. With help of clear voltage, which is again applied to four rows at the same time, the charge is removed from the internal gate after readout. The process is finished as soon as the gate-on

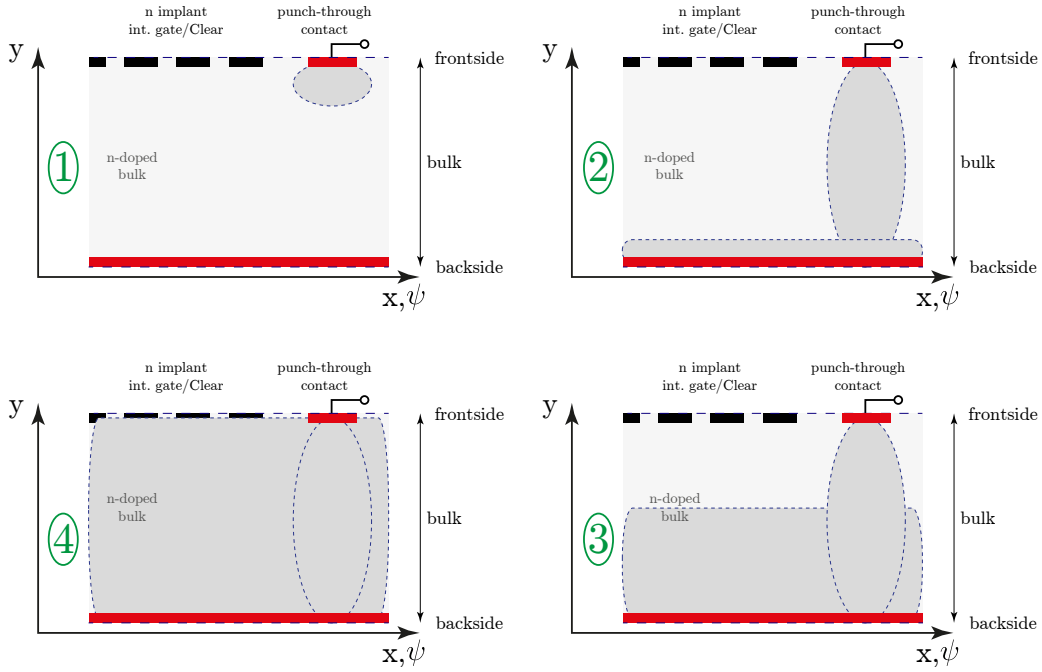


Figure 3.4: Sketch of the sideward depletion process inside DEPFET pixel. 1) At the punch through contact a negative voltage is applied. 2) For hv ≈ -35 Volt the depletion zone spread to the backside. 3) The bulk starts to get depleted. 4) The bulk is fully depleted. [13]

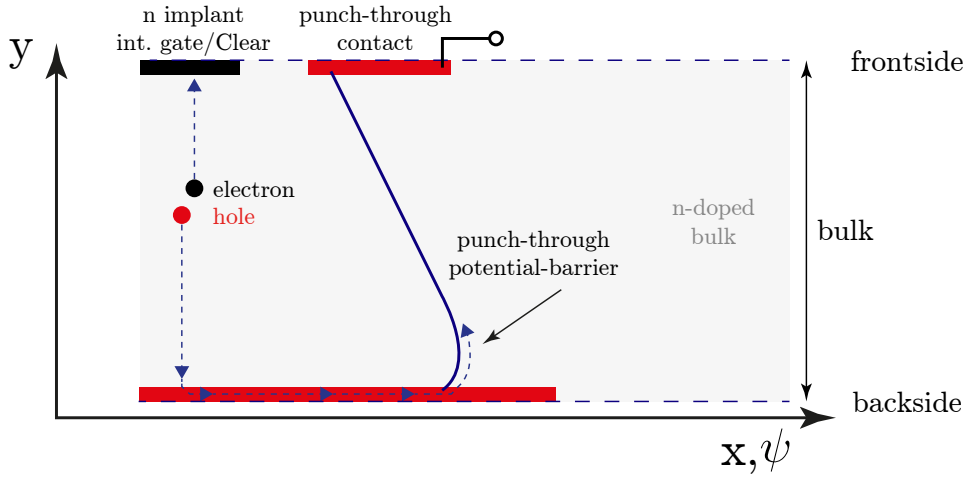
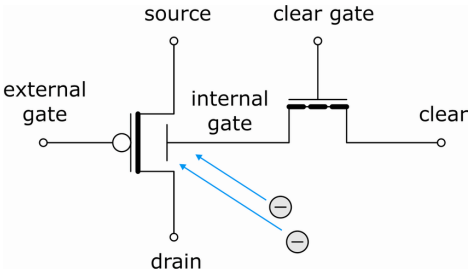
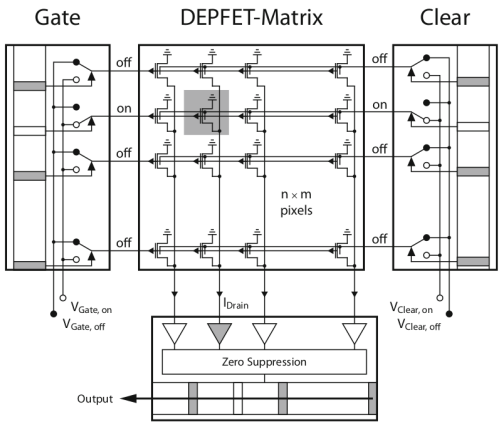


Figure 3.5: Sketch of the punch-through effect. The holes drift to the backside. Afterwards they overcome a potential barrier. They cross the bulk to the punch through contact. [13]



(a) Equivalent circuit symbol to one DEPFET Pixel. [15]



(b) Four-fold readout scheme. Four DEPFET pixel-rows are enabled by the gate-on voltage, and cleared by the clear voltage. [8]

voltage is reset and the transistors of the respective pixel are switched off. The procedure is performed sequentially for each four-row bundle. The readout of the entire matrix requires 20 µs. [5]

3.1.5 Pedestals

The pedestal value of a single DEPFET Pixel is the drain current I_D measured when no signal electrons are collected inside the internal gate. The measured drain current is also called dark current. A conductive channel with holes is created between the source implant and the drain p^+ implant. Each drain current readout therefore has an amount of dark currents. To extract the signal I_{signal}, the pedestals must be subtracted from th drain current I_D

$$I_{\text{signal}} = I_D - I_{\text{pedestals}}. \tag{3.5}$$

Due to process variations, the doping concentration is not homogeneous. Therefore, every pixel has a slightly different pedestal value. [13]

3.2 Front-end Electronics

Outside the sensitive region, the application-specific integrated circuits (ASICs) are located. These are required for controlling the DEPFET pixel, for its readout and data processing. The following section describes the functionality of the Switcher, DCD and DHP chips located directly on the PXD9 module.

3.2.1 Switchers

The so called switchers are responsible for driving the gate, controlling the row access and clearing the internal gates in the rolling shutter mode. For the entire DEPFET pixel matrix 6 switcher are required, which are placed on the long side of the sensitive area. Each switcher has 32 output channels for the

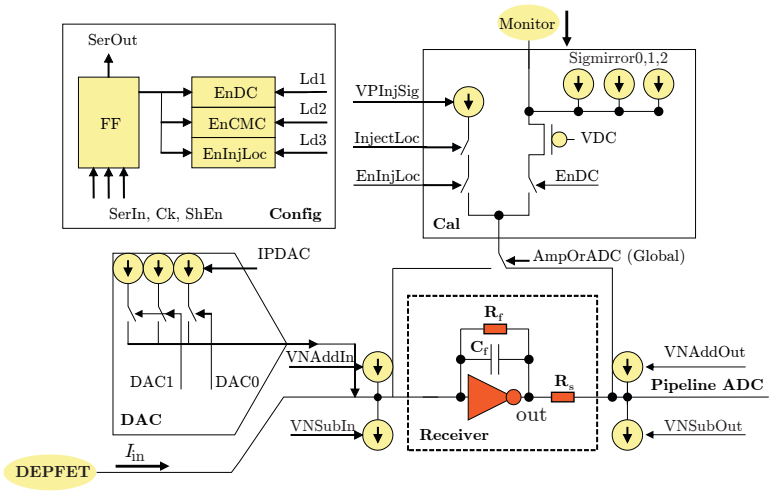


Figure 3.7: Basic circuit of the analogue channel of the DCD. The receiver amplifies the incoming DEPFET current before it is received by the pipeline ADC. [13]

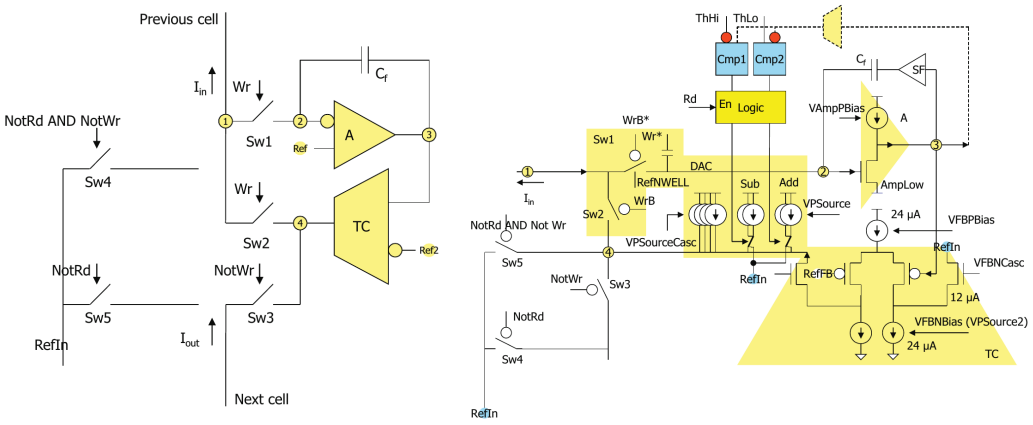
clear and gate lines. The selection of row segments for the readout is controlled by shift registers and strobe signals. They are configurable by uploading a specific switcher sequence. [16]

3.2.2 Drain Current Digitizer

For the readout of the DEPFET pixels a conversion from analog to digital currents is necessary. This digitization is done by the Drain Current Digitizer (DCD). Four of these are needed at the bottom of each module. The basic analog circuit of the DCD is shown in figure 3.7. The DCD receives the DEPFET drain current as an input current I_{in}. For each DEPFET pixel an individual current can be added, the so-called `DAC-IPDAC`. In the following, all current names in DCD are shortened without the abbreviation `DAC-`. The same amount of current for all input channels provided by the DCD can be added with *VNAddIn* and subtracted *VNSubIn*. The subtraction and addition of current can be used to increase the measuring range of the readout current. More details can be found in section 5.3. With the enabled analog common mode correction *ACMC*, the amount of current flowing into the receiver can be controlled. The advantage at this mode is that the common mode noise, which can occur in the power supply lines additionally to the noise from the detector and electronics, can be compensated by the analog feedback. The receiver then amplifies the DEPFET current. After amplification, an additional current source *VNAddOut* and *VNSubOut* allows to add and subtract globally an amount to the DEPFET current.

The DCD provides 256 analog channels, each with an internal pipeline to an Analog-Digitial Converter (ADC). It has a restricted input range of 20 µA to 40 µA. Therefore, the DCD provides the possibility of an offset correction before digitization (2-bit DAC), which is used to subtract the offset transistor currents I_{ped} from the readout current. (see section 3.1.5).

The DCD includes Current-Memory Cells (CMCs), which basic layout is shown in figure 3.8(a) on the left hand side. It is composed of an Amplifier A, a differential Transconductor TC and a Capacitor C_f, which is used as the memory element. These cells are implemented as cyclic Analog to Digital



(a) Basic layout of Current Memory Cell. (b) More detailed layout of Current Memory Cell.

Figure 3.8: Layout of Current Memory Cell (CMC) used in pipeline ADC inside the DCD. [17]

Converters (ADC). The CMC is able to store currents between -8 and 8 μA. For writing a current at node 1, switches 1 and 2 (Sw1 and Sw2) are closed and the hold capacitor C_f is charged. The amplifier A causes a potential at node 3 which is proportional to the input current I_{in}. A feedback current at node 4 is generated by the transconductor TC, which increases until the input current is balanced. Afterwards, Sw1 is opened again and the current is stored in the capacitor C_f. The storing process is finished. For readout switch number 3 (Sw3) is closed and the stored current is flowing out of the cell. Adjusting several DAC settings and supply voltages (figure 3.8(b) right side) modifies the operation of this memory cell. The *PSource* current source is located at node 4. It is configurable by a DAC called *IPSource*. The nominal value of the current source is 8 µA. It is adjustable through *IPSource* by 4 µA . The ground of the Amplifier A is defined as *AmpLow* voltage. The output voltage is taken by the transconductor TC as its input. Its source is called *IFPBias* and its sinks *IPSource2*. The right output of the transconductor is kept at a potential *RefIn*, while the left side is connected via node 4 to the cells output and input. For detailed information on the working principle see [17]. In the section 5.2 the application of these quantities is explained.

3.2.3 Data Handling Processor (DHP)

The main task of the Data Handling Processor (DHP) is to further process the digital data received from the DCD and reduce the data rates. Furthermore, it controls the DCD and the switchers. Data processing (signal procession and data reduction) includes pedestal subtraction (see section 3.1.5), zero-suppression and the common mode correction.

The so-called zero suppression is a method for data reduction. Only signals above a certain threshold are kept.

The common mode (CM) is noise, thus a signal offset, which affects every pixel in one quadruple row segment. This noise is filtered with the help of the so called two parse average method. The first step is to calculate the mean value over the entire measured data. Values larger than the estimation are replaced with the first common mode value. The mean value is taken again to the already processed data set and subtracted from the signal values. Finally, values above a defined threshold are processed further off module. The corrected and reduced data is stored in a buffer and sent further to the data

acquisition system (DAQ) when receiving a trigger signal. Besides the data processing, the DHP also generates and distributes all timing signals (clocks) to the other ASICs. Furthermore, it provides the Joint Test Action Group (JTAG) control interface to be able to configure all ASICs. The DCD and the DHP chips are located at the top or bottom of the sensitive region inside a PXD9 module. More details regarding the module layout are described in section 3.4. [18]

3.3 Biasing of PXD module

Each module to be characterized is powered by a LMU power supply (PS). This provides 23 power nets and two ground nets, which are necessary to operate the modules. In the following, the powering lines are introduced according to their use:

- Two ground nets ensure the **grounding** of the modules, the analog ground *AGND* and the digital ground *DGND*.
- The **DEPFET static voltages**, in total nine analog voltages, are attached to the matrix. These include the *source*, *drift* and the sideward depletion voltage *HV*. Additionally, the three coupled clear-gate voltages *ccg 1,2,3* are connected. To prevent forward biasing of the pn-junction, the *bulk* voltage needs be higher than the source voltage. The *guard* voltage prevents electrons not belonging to the signal from interfering with the pixel.
- The **switcher** is supplied by three voltages, the *sw-dvdd, sw-refin* and *sw-sub*. In addition, other analog voltages, the **DEPFET switcher voltages**, are applied to the switcher. There are three *gate-on* voltages, which are applied to two switchers each. In addition, there are the *gate-off, clear-on* and *clear-off* voltages, which are required for reading out the matrix.
- The digital parts of the **DCD** are supplied by the *dcd-dvdd* voltage. For the analog part three voltages are necessary: The *dcd-acdd* , the *dcd-refin* and the *dcd-amplow* voltage.
- The digital blocks of the **DHP** are powered by the *dhp-io* voltage and *dhp-core* voltage.

In section 6, the relation of the biasing voltages with the pedestal values is detailed. To protect the modules, such in case of connection loss or from over voltage appliance, an emergency shutdown sequence is implemented inside the power supply. [5]

3.4 Module Structure

The following section describes the layout of the so-called PXD9 module. In addition, the setup for the inner detector layer is presented.

The four overall PXD9 module designs are shown in figure 3.10. The four designs are: Inner forward (IF), inner backward (IB) for the inner modules and outer forward (OF), outer backward (OB) for the outer layer of PXD.

In figure 3.9 the cross section of a PXD9 module is shown. In order to reduce the material budget, the active area (the 250×768 pixel area) is thinned to 75 µm. To retain mechanical stability, the connected pixels are surrounded by a 525 µm thick silicon frame, making the module a self supporting structure. The main difference of the four designs is the location of the ASICS, thus the metal routing.

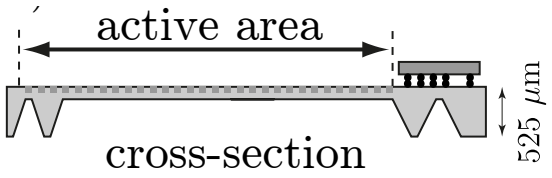


Figure 3.9: Cross section of PXD9 module. Active area is thinned to 75 μm and the supportive area 525 μm. On the supportive area a switcher is depicted. [13]

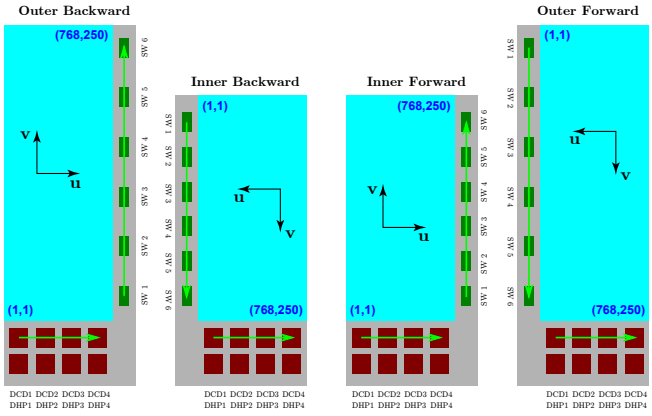


Figure 3.10: Layouts of PXD9 modules. The DCDs and DHPs are placed on the top or bottom, while the six switchers are placed on the balcony. Readout direction is marked with green arrows. The coordinate system (u.v) depict the electrical mapping, while (1,1) is the origin of the geometrical layout. [13]

Four DCDs and DHPs are placed at the top or bottom of the sensitive area based on their final position inside the PXD of the detector in order to have a symmetrical ladder design. 1000 drain lines are connected to the 4 DCDs and DHPs for drain current readout and digitization. They are placed outside the tracking region to minimize the material budget close to the interaction point. Six switchers are placed at the long side of the active area. The active area is separated into two areas with smaller and larger pixel size in order to have smaller pixel pitches closer to the interaction point: This is done to improve the resolution for perpendicular traversing tracks. In the forward region the probability of cluster with two pixels increases. Therefore, the larger pixel size prevents that charge clouds spread over too many pixels, which would decrease the resolution due to charge sharing events. Outer ladders have to be longer to cover the same angle, therefore, they feature larger pixel pitches. The inner layer modules consist of pixels with pixel sizes of $50 \times 55\,\mu m^2$ (central part) and $50 \times 70\,\mu m^2$ (forward and backward part). The outer layer modules are build with pixels with pixels sizes of $50 \times 60\,\mu m^2$ (central part) and $50 \times 85\,\mu m^2$ (forward and backward part). [12, 19]

Two mirrored half modules are glued together and form one so called full latter. To build the Belle II PXD detector (see figure 3.11), eight layers at a radius of 14 mm to the intersection point to fill the inner layer and 12 layers for the outer layer at a radius of 22 mm are needed. The ladders are arranged in a tilted structure to avoid gaps and create overlapping sensitive areas.

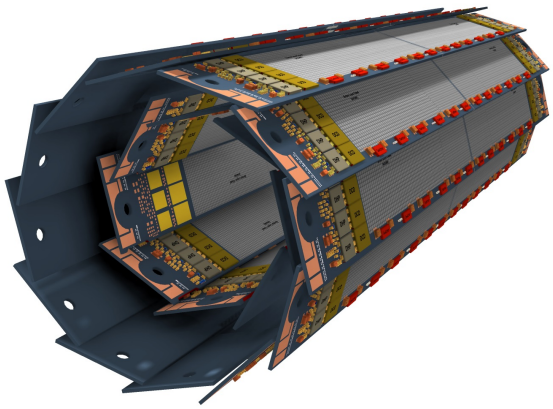


Figure 3.11: PXD for Belle II, with two layers around the beam pipe consisting 40 modules in total. [13]

3.5 Correlation Coefficient

In the following, two correlation parameters are presented, which evaluate the linearity, respectively monotonicity of two data sets. This is especially important when correlations between two measured variables are to be determined to evaluate a possible correlation.

3.5.1 Pearson Correlation Coefficient

The Pearson coefficient measures the strength of a linear association between two variables or two data sets. To calculate the coefficient, a curve is fitted on the data set. The person coefficient r indicates the distance of the two data points x_i and y_i to the best fit. It can be calculated with:

$$r = \frac{\sum_i (x_i - \bar{x})(y_i - \bar{y})}{\sqrt{\sum_i (x_i - \bar{x})^2 \sum_i (y_i - \bar{y})^2}} \tag{3.6}$$

The Pearson coefficient can range from -1 to 1. A perfectly positive linearity receives the value 1. A negative linearity results in -1. A value of 0 indicates that there is no correlation between the two data sets. The strength of the correlation can be categorized as below [42]:

- 0.0 to 0.19 *very weak*
- 0.20 to 0.39 *weak*
- 0.40 to 0.59 *moderate*
- 0.60 to 0.79 *strong*
- 0.80 to 1.0 *very strong*

This method can only determine whether the data are linearly correlated and makes no statement about how monotonic the correlation is. [43]

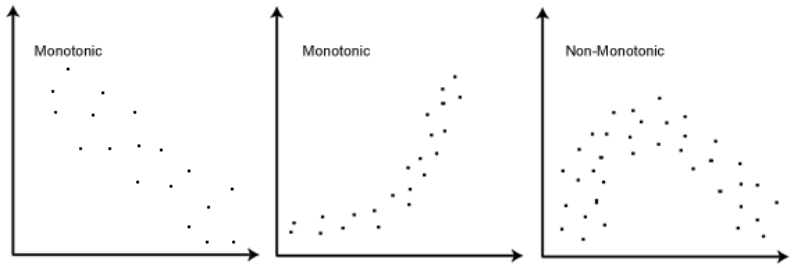


Figure 3.12: Illustration of the meaning of correlation coefficients. The left figure shows a negative monotonic relation and negative linearity ($\rho < 0$ and $r < 0$), the middle figure a positive monotonic but no linear relation ($\rho < 0$ and $r \approx 0$) and the right figure no monotonic and no linear relation($\rho \approx 0$). [44]

3.5.2 Spearman Correlation Coefficient

The Spearman Correlation Coefficient gives the strength and the direction of the monotonic relationship of two data sets. The term monotonic relationship is a statistical definition used to describe a scenario in which the magnitude of one variable increases if the other variables also increase. This scenario would state a positive monotonic relation. A negative monotonic relation is given when the magnitude of one variable increases if the other variable decreases. Examples of monotonic and non-monotonic relationships in comparison to linear relationships are shown in figure 3.12. This method is used when no linear correlation can be assumed of an unknown correlation of two data sets. For determining the coefficient, the two data sets are sorted and ranked respectively to its magnitude. The coefficient ρ is given by:

$$\rho = 1 - \frac{6 \sum d_i^2}{n(n^2 - 1)}, \tag{3.7}$$

where d_i gives the difference in paired ranks and n the number of cases. More details on the definition of the Spearman Correlation Coefficient can be found in [44] and [45]. The correlation coefficient varies between -1 and 1 with 0 implying no correlation. 1 and -1 suggest exact monotonic relationship. [45]

The strength of the correlation can similar be described as the Pearson Coefficient [44].

CHAPTER 4

Experimental Setup for Module Testing

In this chapter, the experimental setup of the module testing lab in Bonn for the calibration of PXD9 modules is described in detail. The PXD9 modules require cooling during the testing procedure. To prevent damage to the modules due to condensation in varying humidity environments, the setup was equipped with temperature and humidity sensors. Consequently, dew point monitoring was installed, including automatic shutdown of the setup to protect it against condensation-related damage. Additionally, the setup is extended by a security interlock system to monitor the associated components.

4.1 Module Testing Setup in Bonn

The module testing setup in Bonn consists of a lead box, a chiller with an integrated temperature controller, the power supply and the measurement PC. A schematic of the setup is shown in 4.1. Via the Data Handling Engine (DHE) the module can be controlled and read out. It is powered by the LMU-power supply via the breakout board. The power supply functionality is described in 3.3. The hardware setup is presented in this section.

4.1.1 Lead Box

The module is placed inside the light-shielded lead box (see figure 4.2). A small hole guides the the kapton cable of the module outside. Above the module, a holder for mounting radioactive sources is located, which is in a fixed position relative to the module. Thus, the lead box is also designed for shielding radiation to the outside. The module is placed on a cooling block to allow to control its temperature during operation. The cooling block is operated with water supplied and tempered by a chiller.

4.1.2 Temperature Control

The chiller regulates the temperature of the cooling block on which the module is placed. Due to a typical power consumption of 9 W [13], the module requires active cooling to prevent damage to heat-sensitive components. The used chiller in the Bonn lab setup is the huber mini chiller olé 300 [20]. It is equipped with a controller that sets the internal temperature at which the water is kept. When the cooling is started, the water circulates through tubes into the cooling block.

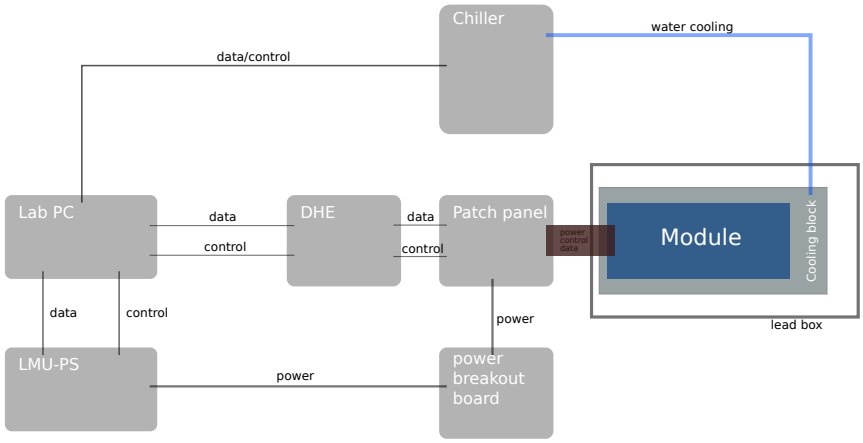


Figure 4.1: Schematics of experimental setup for module testing. The module is placed on the cooling block, which is controlled by the chiller. The kapton cable is connected to the patch panel. Via the DHE the module can be controlled and read out. The module is powered by the LMU PS via the power breakout board. The Lab PC communicates with the chiller.

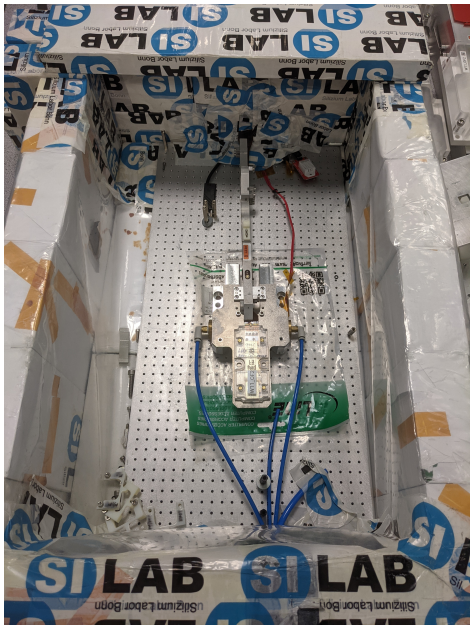
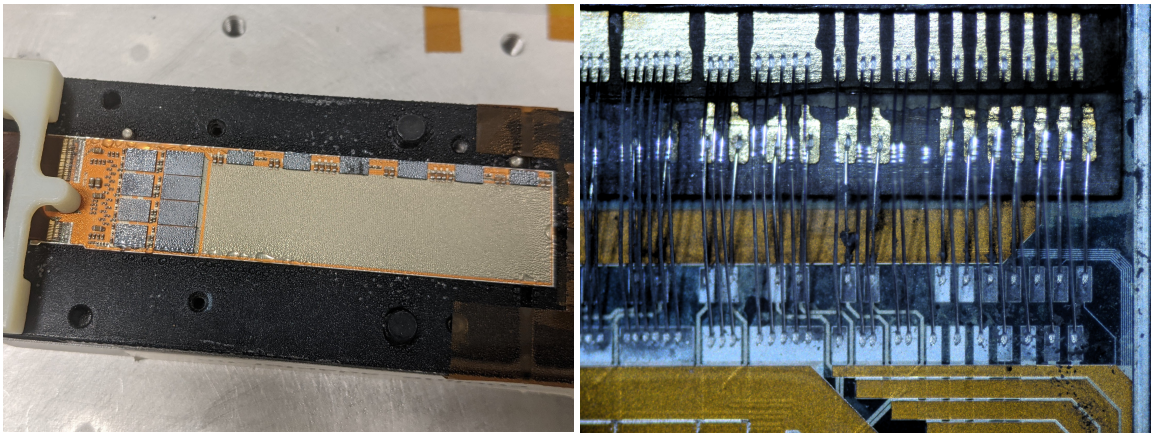


Figure 4.2: Top view of the opened lead box. The module is placed on the cooling block in the center. Lead walls protect the assembly from light and shield from radiation of radioactive sources. Two pass-troughs guide the module cable and the cooling tubes to the outside.



(a) Condensation on surface of module.

(b) Corrupted wire bonds (black spots).

Figure 4.3: Accident on W60_IB. Dew points above target cooling temperature on the 28th of June 2021 [22] lead to condensation on the surface and cause damage which leaves the module inoperable.

Connection between the lab PC and the chiller is established via a built-in serial USB port. The pySoftcheck [21] software provided by the huber company is used to communicate with the integrated temperature control unit. More detailed information for the inter communication can be found in [20].

4.2 Humidity and Temperature Monitoring

During characterization, the module must be operated under different environmental conditions. Due to the required cooling, condensation may occur and result in damage to the module. Previous condensation accidents, as on module W60_IB (see figures 4.3), results in inoperable damage on the modules, as the condensation can lead to corrosion of the wire bonds. Due to the low availability of the modules, a dew point monitoring with an integrated interlocking system is essential to prevent damage.

Two sensors are installed to measure the humidity and temperature. In addition, an automatic interlock has been implemented, which shuts down the module and switches off the chiller before reaching the dew point. In the following sections the procedure is outlined. First, the definition of the dew point is explained. For the measuring procedure, the sensors considered are first compared, suitable ones are selected and the procedure is described. The automatic interlock system and the second interlock system and its functionalities are introduced.

4.2.1 The Dew Point

The dew point, in degrees Celsius, is the temperature above which condensation occurs at a given relative humidity and temperature. When both liquid and air are present in a closed space, there are two continuous flows of molecules. The water molecules vaporize from the surface into the air, while further molecules are captured from the surface of the material. If the air is initially dry and the surface is wet, the process of evaporation begins. During this process, the partial pressure e_v of the vapor begins to increase until the molecular flows are balanced. The balanced state is called saturated

with vapor with the equilibrium vapor pressure $e_s(T)$ [23]. The dependence of the equilibrium vapor pressure on the temperature is based on measurements and formulated in approximate equations. One possibility for the description of the saturation vapor pressure is the Magnus formula which provides a maximum error of 0.1 % and has the following form [24]:

$$e_s(T) = K_1 \exp\left(\frac{K_2 \cdot T}{K_3 + T}\right). \tag{4.1}$$

For a temperature between −45 °C and 60 °C the following parameters are valid

$$K_1 = 6.112\,\text{hPa}; K_2 = 17.62; K_3 = 243.12\,^\circ\text{C}$$

The saturation vapor pressure is exponentially dependent on the temperature. If the surface is cooler than the air, the molecules are more easily trapped by the surface. This leads to so called condensation [23].

The relative humidity RH is defined as [24]

$$\text{RH}(T) = \frac{e_v}{e_s(T)}. \tag{4.2}$$

At the dew point T_D, the relative humidity has a value of 1

$$\text{RH}(T_D) = \frac{e_v}{e_s(T_D)} = 1. \tag{4.3}$$

By dividing RH(T) equation 4.2 with 4.3 it follows

$$\text{RH} = \frac{e_s(T_D)}{e_s(T)}. \tag{4.4}$$

By using the Magnus equation (equation 4.1) and solving for T_D, the dew point can be extracted as

$$T_D(\text{RH}, T) = K_3 \cdot \frac{\frac{K_2 \cdot T}{K_3 + T} + \ln(\text{RH})}{\frac{K_2 \cdot K_3}{K_3 + T} - \ln(\text{RH})} \tag{4.5}$$

The error of the dew point depends on the temperature and humidity error. It can be calculated via Gaussian error propagation

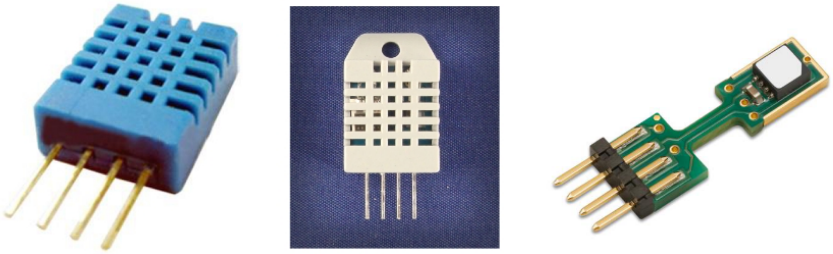
$$\Delta T_D(T, \text{RH}) = \sqrt{\left(\frac{\partial T_D}{\partial T}\Delta T\right)^2 + \left(\frac{\partial T_D}{\partial \text{RH}}\Delta \text{RH}\right)^2}, \tag{4.6}$$

with:

$$\frac{\partial T_D}{\partial T} = K_3^2 K_2^2 \cdot \left[\ln(\text{RH}) \cdot T + K_3 \ln(\text{RH}) - K_3 K_2\right]^{-2} \tag{4.7}$$

and:

$$\frac{\partial T_D}{\partial \text{RH}} = K_2 K_3 \cdot (K_3 + T)^2 \cdot \text{RH}^{-1} \cdot \left[(K_3 + T)\ln(\text{RH}) - K_2 K_3\right]^{-2}. \tag{4.8}$$



(a) DHT11 [25] (b) DHT22 [26] (c) SHT85 [27]

Figure 4.4: The tested sensors measuring the temperature and humidity.

accuracy	DHT11	DHT22	SHT85
temperature	< 2 %	< 0.5 %	< 0.5 %
rel. humidity	< 5 %	< 5 %	< 2 %
resolution			
temperature	1 °C	0.1 °C	0.01 °C
rel. humidity	1 %RH	0.1 %RH	0.01 %RH

Table 4.1: Resolution and accuracy of compared sensors. Given by data sheets: [25], [26], [27]. RH stands for relative humidity units.

4.2.2 Measuring Temperature and Humidity

For this project, different types of sensors and their functionality are tested to measure temperature and the relative humidity. This includes three DHT11 sensors [25], two DHT22 sensors [26] and one SHT85 sensor [27]. All three sensors types are depicted in 4.4. The accuracy of the measurements varies between sensors and measurement quantities. The corresponding data sheet gives parameters regarding the measurement accuracy, which are listed in table 4.1. In addition, the sensitivity of the measurement is compared for all sensors.

In figure 4.5, a sample measurement with all available sensors is shown. The temperature and humidity were measured over night. The temperature measurement shows overlapping measurement data of the sensors until approximately 7 o'clock, which agrees with the accuracy specified in the data sheet. At around 8 o'clock the sensor measurements show discrepancies in the measured values. The sensors were located nearby a window. Since the sun starts shining through the window on the sensors depending on their position at around 8 o'clock, the observed deviations may be related to the measurement conditions. However, the measurement of relative humidity shows differences. An analog Ahlborn measurement device [28] was used as a reference measurement. It is noticeable that the sensors of the DHT11 series deviate from the reference value by up to approximately 30 %. The uncertainties of the SHT85 and DHT22 sensors given in the data sheet agree approximately with the observations and the measurement results. It is noteworthy that the two DHT22 sensors, despite the same design, have a discrepancy of about 10 %. For the following setup the sensor SHT85 and the DHT22 (sensor number 4) are selected, since they show the lowest discrepancies to the reference measurements. If one sensor fails, the second sensor can be used as a reference.

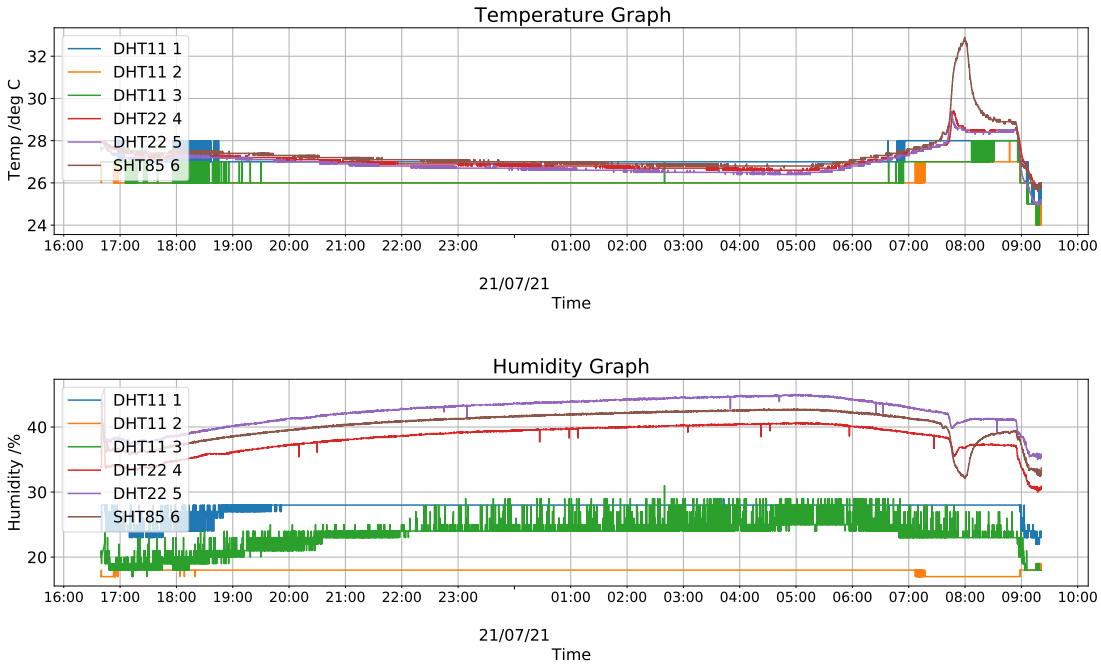


Figure 4.5: Test measurement of the available sensors. Relative humidity and temperature are measured with three DHT11s, two DHT22s and one SHT85.

4.3 Implementation of Protective Interlock Systems

The findings of the previous section is used to implement the dew point monitoring and so-called heartbeat interlock. A closer insight on the complete setup and interconnection is given.

4.3.1 Setup and Intercommunication

The schematic setup is shown in 4.6. The selected sensors are read out by a Raspberry PI. A control system (EPICS) is used to distribute the life measurement data in the network. The Lab PC receives the data and evaluates them. It can communicate with the chiller and the power supply of the modules. A security interlock, using the heartbeat logic, is installed to continuously check the functionality of the components. Technical details are presented in [29].

The sensors DHT22 and SHT85 are mounted in the lab setup. The SHT85 sensor is fixed to the chiller (see figure 4.7(b)) while the DHT22 is placed in the lab box (see figure 4.7(a)). A mini computer, here a Raspberry Pi (see figure 4.8), is responsible for reading out the temperatures and humidity. In the lab setup in Bonn, a Raspberry PI Model B version 1.2 [30] is used. The wiring of the sensors is done via the General Purpose Input/Output pins (GPIO pins). The DHT22 is wired to the GPIO pins of the Raspberry as shown in figure 4.9(a).

The SHT85 is connected via an Inter-Integrated Circuit (I2C bus). In figure 4.9(b) the wiring and the pin outputs of the SHT85 are shown. For the readout, it is necessary to install software packages on the Raspberry. For the DHT22 the Adafruit Circuit packet [31] is used and for the SHT85 a corresponding Python driver [32].

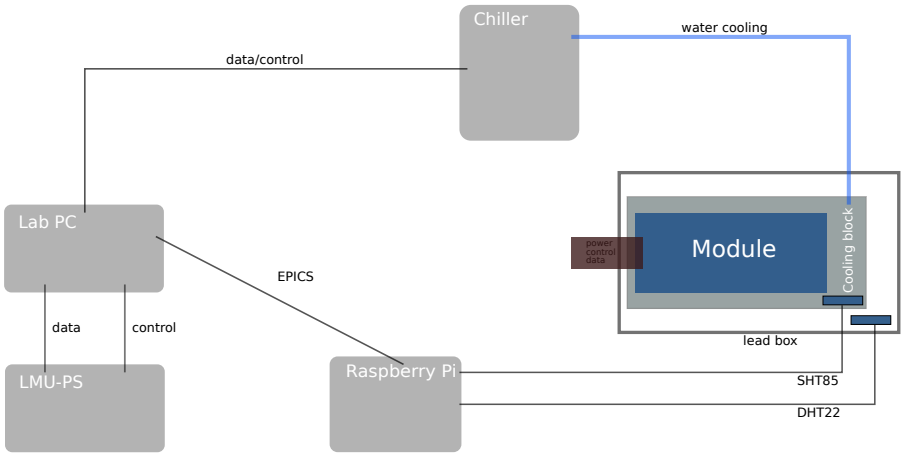
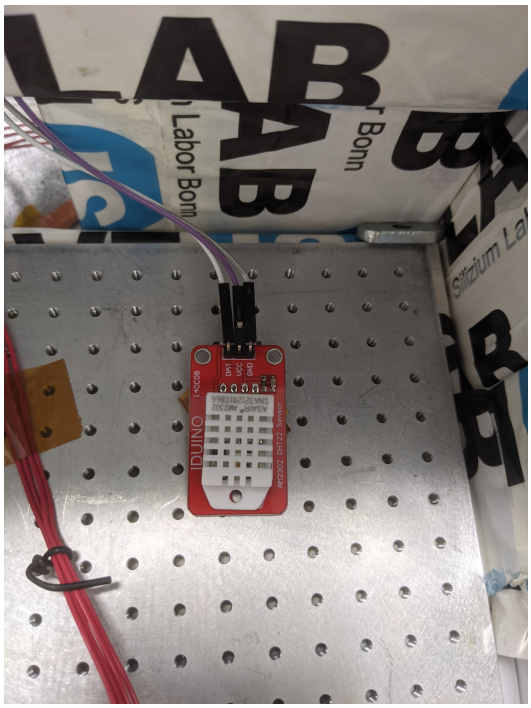
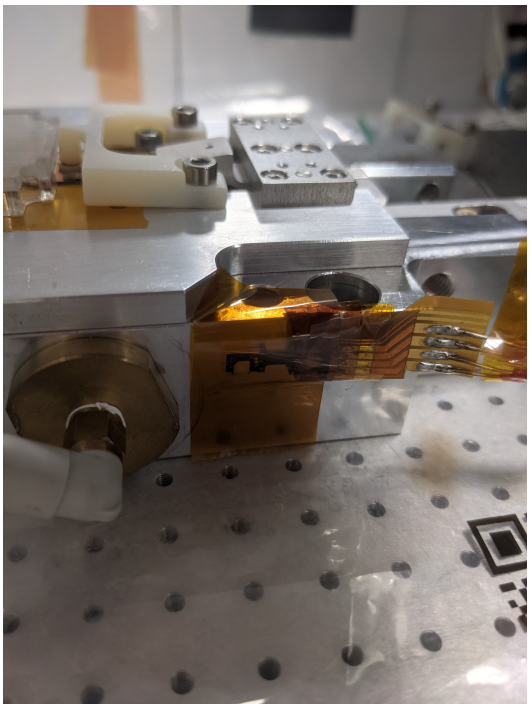


Figure 4.6: Schematics dew point monitoring system. The humidity and temperature data is read out and sent by a Raspberry PI. The Lab PC receives the life measurement data and evaluates them. It can communicate with the chiller and with the power supply of the module.



(a) DHT22 which is placed in the module lab setup box.



(b) SHT85 placed on cooling block controlled by the chiller.

Figure 4.7: Sensor location in lab setup.

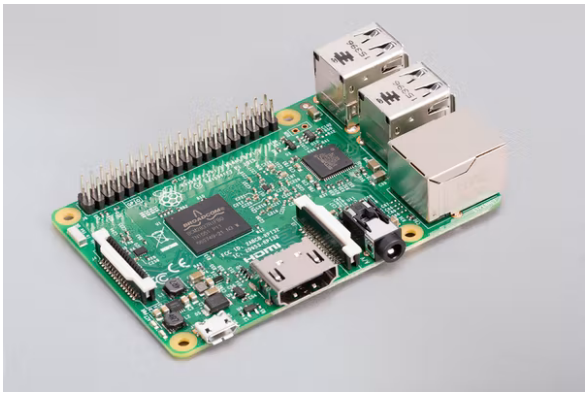
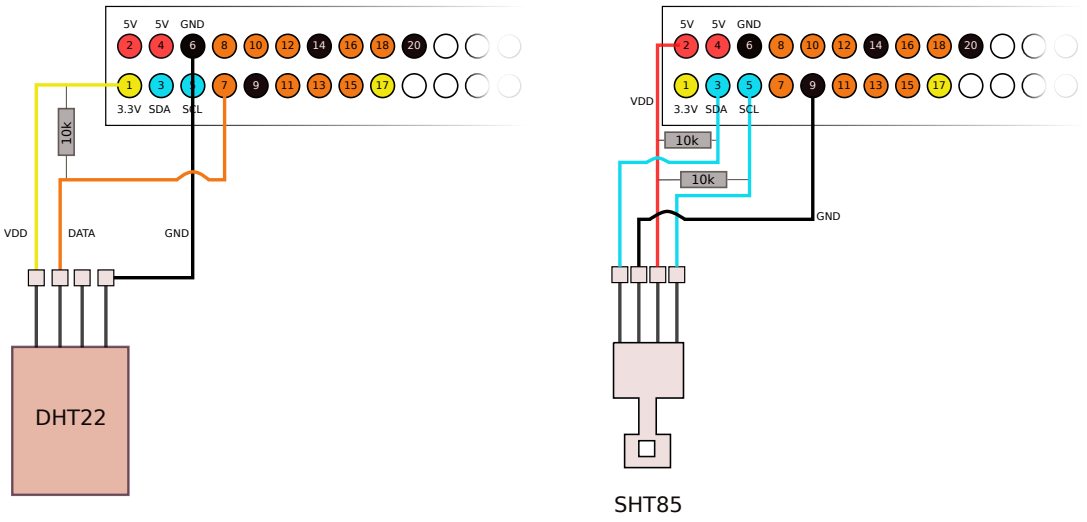


Figure 4.8: The Raspberry Pi Model B is a mini computer with a total of 40 GPIO ports. Only 26 of them are occupied. [30]



(a) DHT22 which is placed in the module lab setup box.

(b) SHT85 placed on cooling block controlled by the chiller.

Figure 4.9: Wiring of sensors to Raspberry Pi.

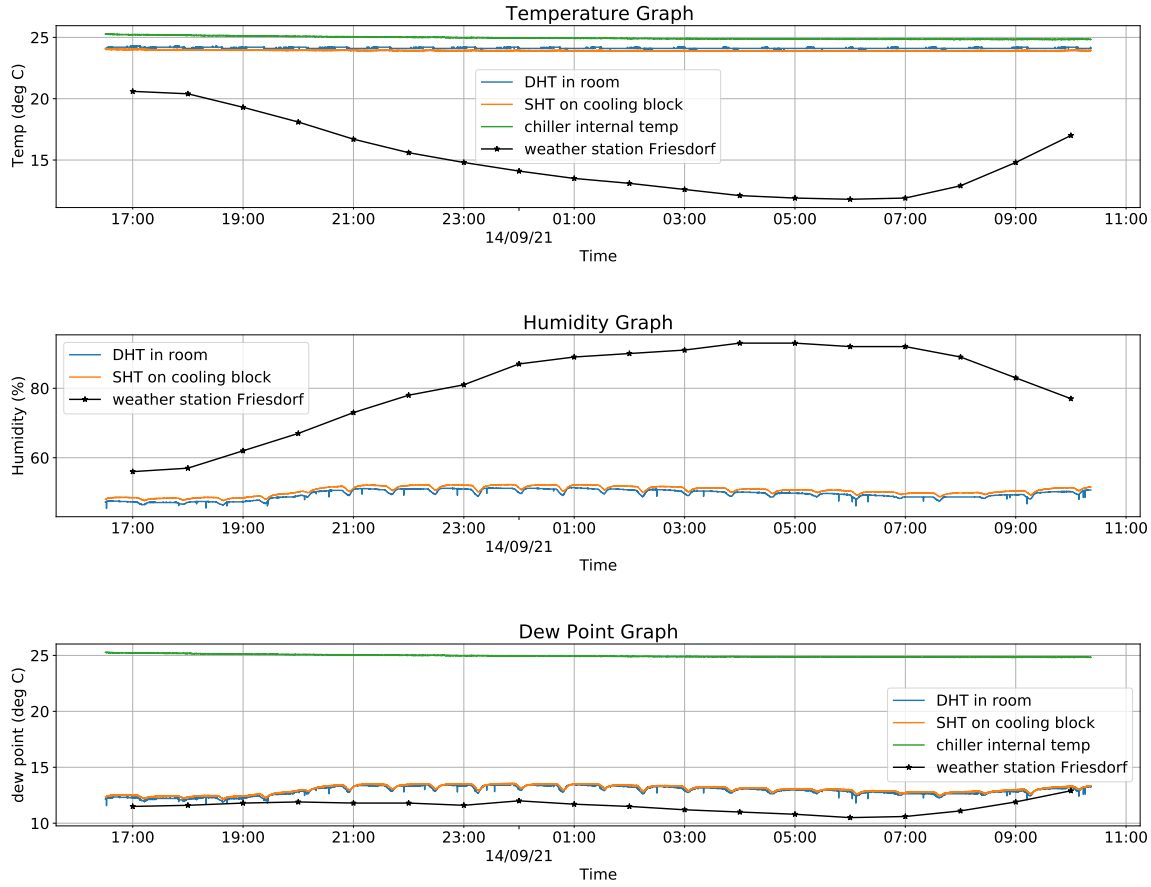


Figure 4.10: Example measurement for temperature and relative humidity. The dew point is calculated and displayed together with the chiller internal temperature for all three measurement types. The data weather station is located in Friesdorf, Bonn [22].

Example Measurement

In figure 4.10 the data of the two sensors for temperature and humidity read out by the Raspberry PI are compared with the weather data for an non-moderated environment. Additionally, the internal temperature of the chiller is plotted. The corresponding dew point is calculated with the formula 4.5. It is noticeable that the temperature and humidity in this measurement in the lab area is relatively constant in comparison to the measurement weather data located outside. The temperature and humidity in the lab in Bonn is controlled by an air conditioner. In the temperature and humidity graphs, recurring periodicities measured by the sensors can be seen. These are also caused by the above mentioned climate control system, which cyclically regulates the humidity and the temperature. The temperature on the cooling block measured by the SHT85 differs from the internal temperature of the chiller. This is a result of the water circulation running through the room via pipes, which can lead to an increase

or decrease in temperature. From the dew point graph it is observed no condensation occurred during this measurement.

Nitrogen Flow

To keep the relative humidity as low as possible, nitrogen gas is injected into the module box with the help of a flow meter. The ambient air consists typically 78 % nitrogen and 20 % oxygen. Adding nitrogen leads to a suppression of the oxygen fraction. The advantage of using nitrogen is that it is chemically inert with any material and it is purified relatively inexpensively.

A test measurement in figure 4.11 shows that even a small amount of oxygen (read-off value of $< 0.5\,\mathrm{L/min}$) has a large influence on the dew point temperature. In less than two hours the dew point could be reduced by $10\,^{\circ}\mathrm{C}$. The temperature remains constant because the module box is not a sealed system.

Control System

To monitor the dew point, the live measurement data must be transmitted in the internal network. The Lab PC can then act accordingly in the event of a damaging danger or sensor failure. For the propagation of the measured variables in the network is the EPICS (Experimental Physics and Industrial Control System) [34] used. EPICS is a program which provides software tools and applications to manage distributed control systems. It uses servers to communicate between computers. The most used server is called Input/Output-Controller (IOC). These can themselves perform local control outputs and at the same time send information in EPICS specific network protocols. Such protocols are called Channel Access. Each IOC provides a Channel Access server, which is communicating with an arbitrary number of clients. The advantage of this methodology is a fast transfer of data between many computers in the network. The IOCs define so-called process variables (PVs). Within PVs measurement data can ideally be send in real time. One PV, for example could always get the current value of the temperature of the SHT85 sensor assigned. The Channel Access Client of a second IOC is able to read out the PV or assign a new value to it. [35] For the intercommunication between the Lab PC and the Raspberry PI the so called pyEPICs is used. This is an interface which is linked to the Python programming language with use of the Channel Access Library.

4.3.2 Dew Point Monitoring

This section describes how to prevent damage on modules due to condensation water. For this purpose, an automatic system has been developed, which monitors the dew point. The conditions resulting in an automatic shutdown, are discussed.

Humidity IOC

To transfer the measured values of temperature, humidity and the calculated dew point to the Lab PC, pyEPICs is installed on the Raspberry PI. An IOC is installed, which reads out the sensors, calculates the dew point and sends the values within PVs in the network. The corresponding IOC is called *Humidity IOC*. The following PVs are created:

- temperature of SHT85,

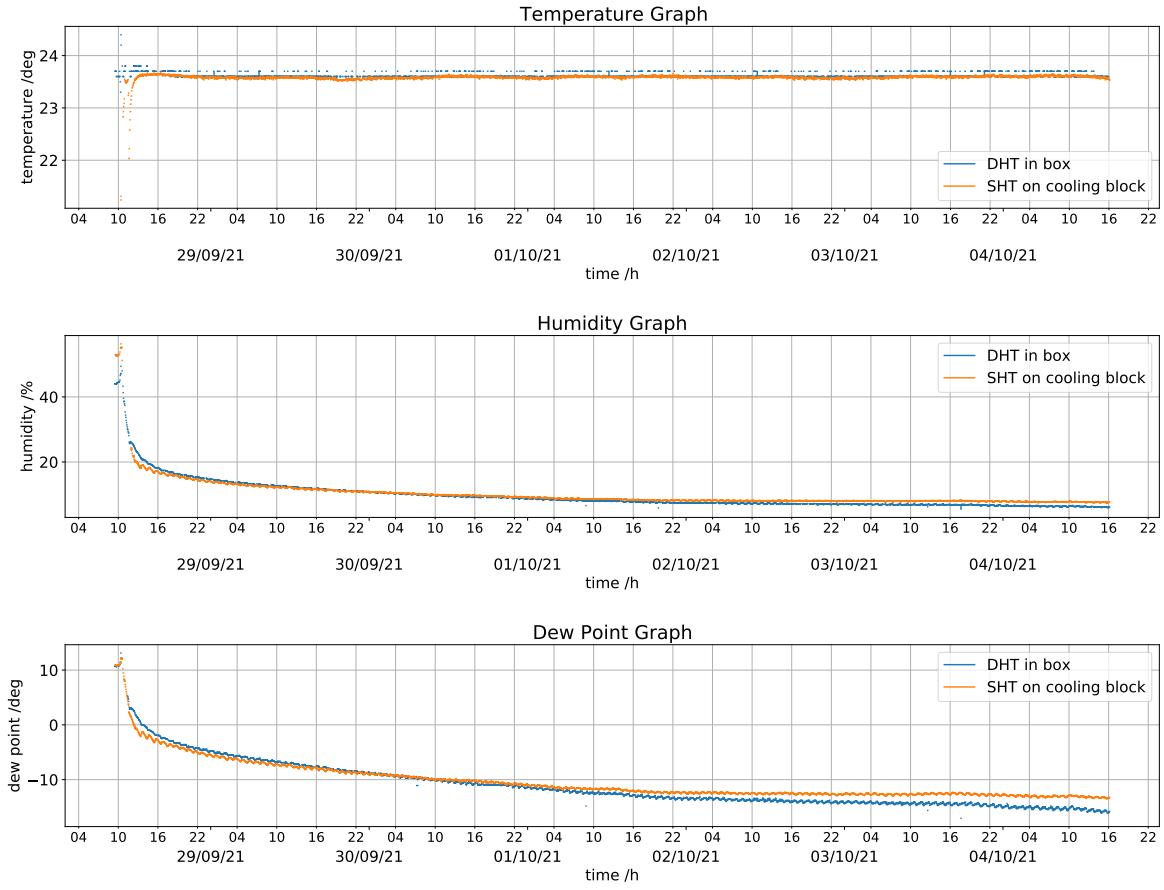


Figure 4.11: Example measurement when adding nitrogen to the module box. Temperature, relative humidity and the resulting dew point are calculated.

$T_{\mathrm{DHT22}}/^{\circ}C$	$\mathrm{RH}_{\mathrm{DHT22}}/\%$	$T_D/^{\circ}C$
23.00 ± 0.12	70 ± 4	17.23 ± 0.80
25.00 ± 0.13	80 ± 4	21.31 ± 0.83
28.00 ± 0.14	80 ± 4	24.22 ± 0.85

Table 4.2: Example temperature and humidity values with associated errors of the DHT22. The dew point is calculated with respective errors.

- temperature of DHT22,
- relative humidity of SHT85,
- relative humidity of DHT22,
- calculated dew point of SHT85 data and
- calculated dew point of DHT22 data.

The PVs are emitted every 0.1 seconds to record any change as fast as possible. However, due to the limited readout rate of the sensors, the value of the PV is only adjusted every 2 seconds for the DHT22 and every second for the SHT85. A widget in CSS (Control System Studio) Studio, which is also used to control the module, displays the measured values.

Interlock IOC

The Lab PC already uses EPICS to control the measured values of the module, such as voltages or currents, with the help of its own IOCs. Another IOC on the Lab PC is needed which processes the measured values sent by the Raspberry PI. In the following, this IOC is called *Interlock IOC*. Besides reading the PVs of the Raspberry PI, it also communicates with the chiller. In the event of an emergency, the Interlock IOC shuts down the chiller. Additionally an emergency shutdown of the module is triggered via the Power Supply. This is done with the help of the already existing emergency shutdown PV (see section 3.3). One of the following conditions must apply for an emergency case:

- The dew point T_D of a sensor exceeds a temperature of 17 °C:

$$T_D > 17\,^{\circ}\mathrm{C}$$

- The difference between the internal chiller temperature T_C and the dew point T_D is less than 3 °C:

$$T_C - T_D < 3\,^{\circ}\mathrm{C}$$

- A component, e.g. sensor or Raspberry PI fails.

The three degrees limit is chosen on the basis of the dew point error calculation (see equation 4.1). Table 4.2 lists possible temperature, humidity scenarios and the resulting dew point along with error for the DHT22. This sensor has a higher measurement uncertainty (as stated in table 4.1) than the SHT85 and therefore dictates the uncertainty. The error of the dew point does not exceed 1 °C. The

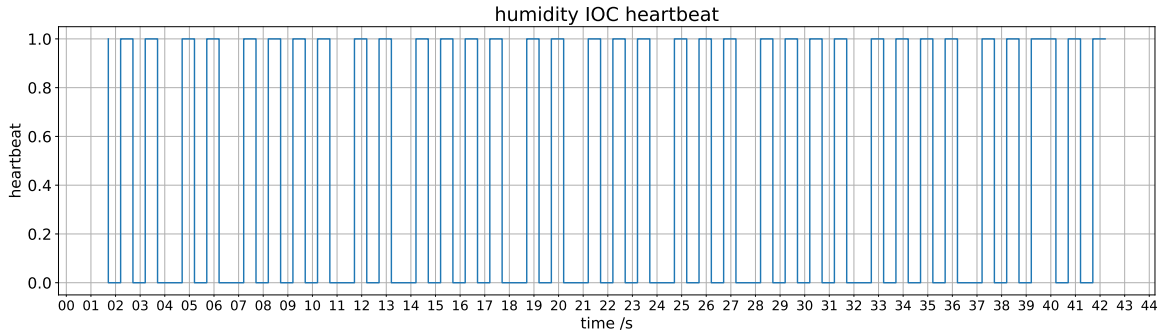


Figure 4.12: Reality how heartbeat arrives at the receiver at the example of the heartbeat of humidity IOC.

additional 2 °C degrees difference is added as a safety range, because of other uncertainties as for example the discrepancies of the temperature of the cooling water which arise due to the pipes that transport it into the cooling block. The 17 °C limit for the dew point was chosen as an additional safety factor, since this limit is so high that room temperature could reach this dew point.

4.3.3 Security Interlock

To guarantee the functionality of the two IOCs described above (humidity IOC and interlock IOC), another protection interlock is implemented. If the two IOCs are not started, stopped, or a connection error occurs, this should result in an automatic shutdown of the module. For this purpose, a link up condition is defined, where the two IOCs send an alive signal periodically. This alive signal is called *heartbeat*. The basics on the heartbeat logic are taken from [36]. In the following the heartbeat functionality is explained in detail. Furthermore, the implementation of the heartbeat receiver is introduced, which checks the alive signal and acts accordingly.

Heartbeat Sender

A heartbeat PV is additionally defined in each IOC which is assigned either a 0 or a 1 with a target frequency of 2 Hz.

In reality, the pattern is not emitted that periodically. For the humidity IOC, for example, the SHT85 is read out every second and the DHT22 every second second. In the humidity IOC the chiller communication takes place every three seconds. This leads to time delays in the process of sending the pattern. In addition, there are time delays and variations in the transmission path through the network. An example how an alive signal for the receiver could look like is shown in figure 4.12.

Heartbeat Receiver

A component is needed, which receives and evaluates this alive signal. Therefore an extension is built into the already existing psApp IOC, which is providing the interface to the LMU-PS. Since the psApp is not a pyEPICs IOC, so-called process databases are needed for the extension of the receiver logic and additional required PVs. Each database defines the functionality of an IOC, which contain so-called records. The records specify how the data is handled. The name of each record defines the name of the new PV. For example, a database can have multiple input records that can receive PVs. It

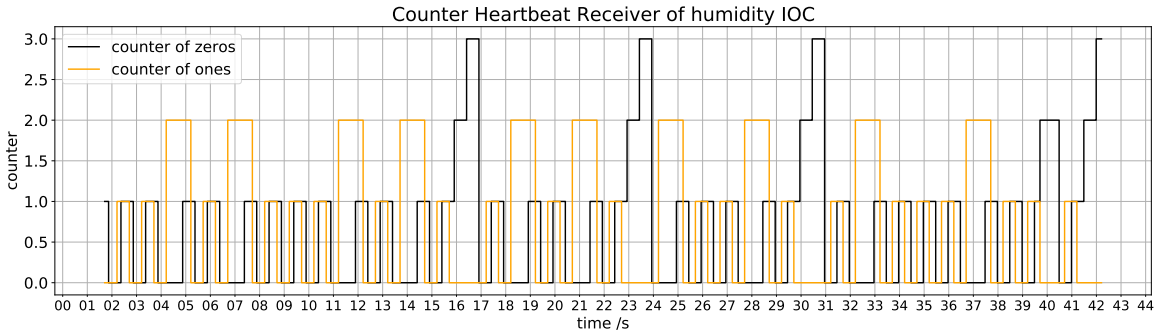


Figure 4.13: The internal counters of security interlock are displayed. In black the zero counter and in orange the one counter. The counters are incremented every 0.5 s. If a 0 heartbeat signal is received, the zero counter is reset and the one counter starts counting up.

could also contain calculations records, which can process data. Furthermore, there are also binary output records that return the response of the processed data.

For the psApp as the heartbeat receiver two new databases are necessary. One analyzes the alive signal of the humidity IOC and the other of the interlock IOC. The databases have the same logical structure:

- They receive the signal of the heartbeat send by the humidity/interlock IOC via an input record.
- Two counter calculation records are used which are reset as soon as a heartbeat 0 or a 1 is detected. I.e. if a heartbeat 0 is received, the zero counter is reset. At the same time the one counter counts up until a heartbeat 1 is received again. Each counter counts every 0.5 s. An example of the two counter values are shown for the database responsible for the alive signal of the humidity IOC in figure 4.13. Here, the counters do not exceed a value of three. In addition, the irregularity of the heartbeat receiving becomes apparent by the different maximum values of the counters before they are reset again.
- The next calculation record is responsible for monitoring the counters every second. It checks if one of the counters reaches a limit of 20. This is the case if no new signal has been received from the heartbeat. The counter limit was chosen this way because a stable operation should be guaranteed. This means that even short network failures cannot lead directly to an emergency case. A counter of 20 corresponds to a duration of 10 s. If there is no alive signal from the heartbeat after 10 s, the IOC is declared dead by another record.
- When the IOC is defined as dead, there is an additional record which then triggers the emergency shutdown PV, which powers down the module.

4.4 Verification Interlock System

The interlock systems have been extensively tested, while example scenarios were triggered. Two examples for emergency scenarios are presented for the dew point monitoring interlock as for the security interlock system.

4.4.1 Dew point monitoring Interlock Testing

The following steps were performed:

1. The chiller temperature control is started.
2. The module mounted on the chiller is powered.
3. One of the sensors is humidified to emulate a dew point, which violates the criteria defined in section 4.3.2.

An example measurement is shown in figure 4.14. The values for the temperature, the relative humidity and the dew point of the sensors are plotted. Additionally, the chiller internal temperature is shown. The status of the chiller, whether it is on (1) or off (0) and also the status of the Emergency Trigger PV is depicted. If the PV shows a value of 1, the emergency shutdown of the module is triggered. A value of zero causes no change.

The SHT85 data shows the chiller cooling down the cooling block, when the internal temperature control is started. A small temperature increase can be seen when the chiller is started. This is due to the start of the temperature regulation. The SHT85 detects an increase in humidity at the cooling block, also after the cooling start. At 10:20 the module starts to power up and the temperature of the SHT85 measurement rises. At 10:25:50 the humidity measurement values of the DHT22 is intentionally increased. Accordingly, the dew point of the DHT22 rises quickly. As soon as this exceeds the minimum 3 °C difference condition, the chiller is automatically switched off. In addition, the emergency shutdown PV triggers and the module is switched off.

4.4.2 Security Interlock Testing

A sample measurement of the internal counters of the heartbeat receiver can be seen in figure 4.15. Here the humidity IOC was stopped on purpose after 30 s. The last signal was the heartbeat 1. Accordingly, the zero counter starts counting up. From a counter of 20 the humidity IOC is declared as dead. The declaration triggered an emergency shutdown of the module and turned off the chiller. Thus, the functionality of both IOCs responsible for monitoring the dew point can be verified.

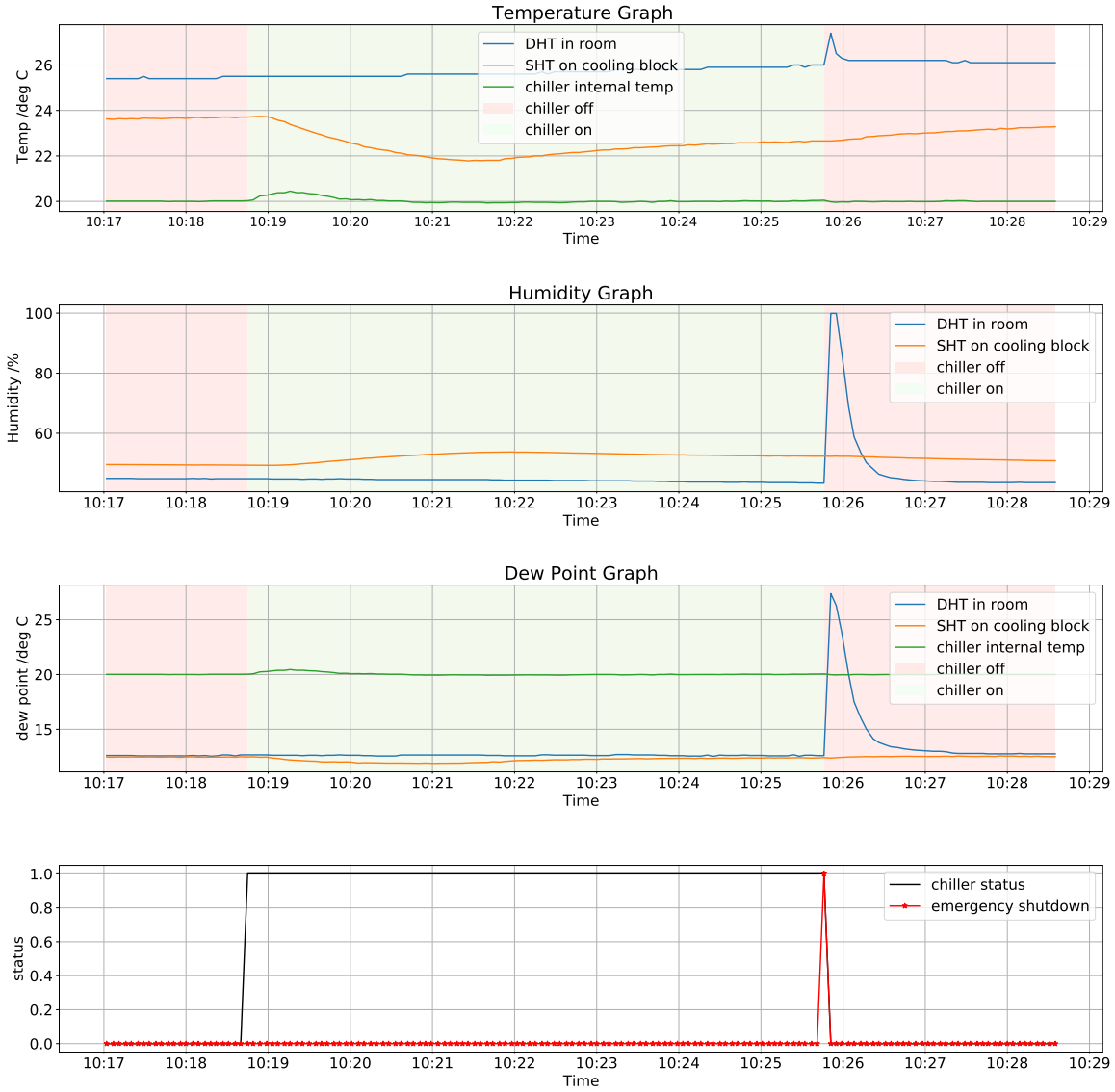


Figure 4.14: A test of the security function is displayed. Temperature, relative humidity, the dew point of both sensors and the internal temperature of the chiller are displayed in the same color code as in figure 4.10. The Emergency Shutdown Trigger PV is shown in the bottom plot. A value of 1 means a shutdown of the module. Additionally the chiller status (ON = 1, OFF = 0) is shown in black. In addition, this information is given in the background color (ON = green, OFF = red).

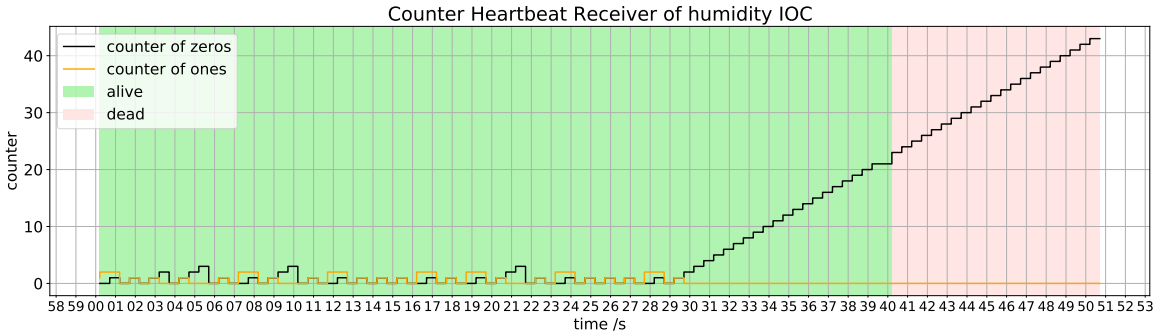


Figure 4.15: Verification of functionality of Security Interlock. The counters are again displayed in black for the zero counter and in orange for the one counter for the humidity IOC. The background color represents whether the IOC is defined as dead or alive.

CHAPTER 5

Calibration Scans of PXD modules

In order to achieve a homogeneous DEPFET pixel response for each module, they undergo a calibration procedure. Certain settings, as matrix biasing or DCD settings, must be tuned on different components of the module. In this chapter, the calibration methods applied to the PXD9 modules are explained. Additionally, results from different modules are compared.

5.1 Pedestal Scan

This section describes how pedestals, the so called dark current, are measured and evaluated. The definition of the pedestals is given in section 3.1.5. The measurement of the pedestals is performed while no signal electrons are collected inside the internal gate. With the help of a number of memory dumps for the current biasing setting, the drain current is read out pixel-wise. The memory dump constitutes the process of taking all information contact in RAM and writing it on a storage drive. Without memory dumps the data would just get lost due to the overwriting property of the RAM. To reach higher statistics the frame number can be specified to define the number of memory dumps.

The mean of the measured pedestal frames are calculated for each pixel. An example is shown in figure 5.1. The histogram on the left shows the pedestal distribution split up for each of the four DCDs. Due to the limitation of 255 ADU given by the ADC range, each pixel has an effective range of 255 ADU minus the pedestal value. In the right plot the mean pedestal values per pixel are displayed within the pixel matrix on its corresponding geometrical position. The distribution of pedestal values is mainly given by previously mentioned deviations (see section 3.1.5) during the production process. The inhomogeneous behavior on pixel level must be taken into account by updating the pedestal map continuously. [37]

5.2 Transfer Curves Analog Digital Conversion (ADC)

The DCDs Analog to Digital Converters (ADCs) convert the measured drain currents of all DEPFET pixels into a digital signal. The description of the DCD can be found in section 3.2.2. In order to ensure optimal operation the ADCs have to be calibrated in the testing procedure. In this section the ADC scan is explained in detail.

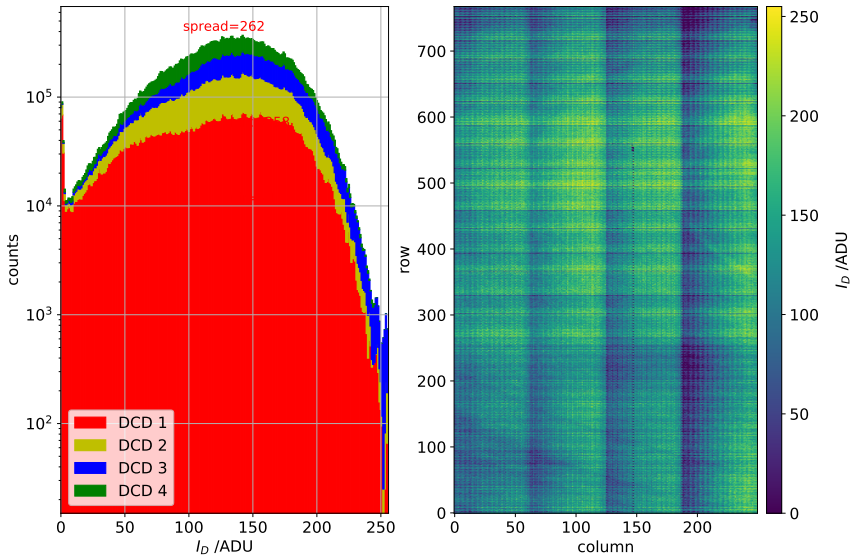


Figure 5.1: Measurement of pedestals of module W60_OF1. No Offsets or ACMC are applied. The mean values for each pixel over 200 frames is taken.

5.2.1 Measurement

By measuring so called ADC transfer curves, while sweeping over a predefined range of supply voltages and DCD settings, the optimal working point can be obtained. The ADC can output 256 digital values. For measuring the transfer curves gradually increasing input is applied to the ADCs. Discrete digital output values of the ADC, that result in a staircase, are measured. The step width is defined as the least significant bit (LSB):

$$1\,\mathrm{LSB} = \frac{\text{dynamic range of transfer curve}}{\text{number of steps}} \tag{5.1}$$

The ideal ADC transfer curve crosses the steps in the center and results in a perfect linear correlation of input and output code as shown in figure 5.2. Thus, a good digital resolution over the full dynamic range of the ADC is ensured.

5.2.2 Characteristics of Transfer Curves

Opposing to the theoretical concept, an ADC transfer curve is never perfectly linear. There are different effects to classify the quality of a transfer curve. A deviation of a step's size to the ideal one is called *Differential non-linearity (DNL)*. The *Integral non-linearity (INL)* is defined by the difference of the measured transfer curve to the ideal one in y direction. In an ideal ADC transfer curve, DNL and INL values are zero. A gap in the ADC curve, caused by a measured step width of zero, would result in a DNL value of -1. This effect is called *Missing Code*. Furthermore, an offset to the ideal transfer curve (*Offset Error*) and deviations to the slope of the transfer curve (*Gain Error*) can be measured.

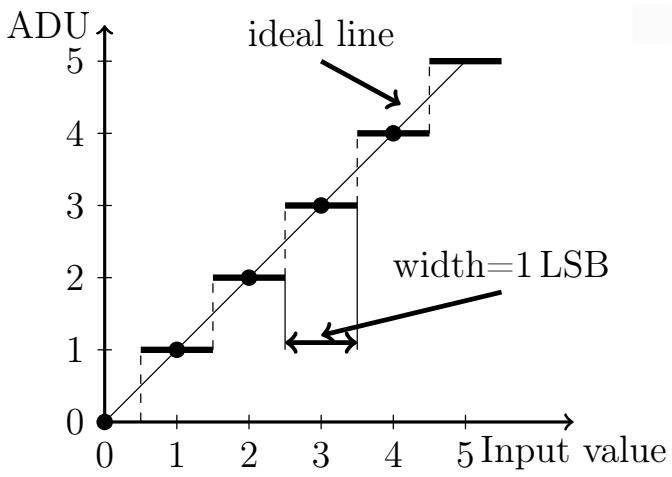


Figure 5.2: The ideal ADC transfer curve characterizes the digitized output code of the ADC as a function of the input current. The step structure arises due to the limit of the discrete digital output values of the ADC. One least significant bit (LSB) corresponds to one step width. The ideal transfer curve crosses the steps in the center.[13]

The quality of transfer curves also depends on the range. Typically the digital output code does not reach the full range of 256 Arbitrary Digital Units (ADU). To determine the noise a minimum of 512 samples is measured for every DAC value. The noise is given by the standard deviation of those samples. [38]

The classification of each ADC transfer curve takes all of the previously mentioned effects into account. An example of an ADC transfer curve measurement is shown in 5.3. Since the whole range is covered, it is approximately linear and consists of a small number of missing codes, this transfer curve was graded good. The color scheme of every step indicates the frequency at which each input-output bin was recorded.

5.2.3 Optimization Parameters

To reach the best performance of the ADC, DAC settings and the supply voltages can be adjusted. The three important DAC settings which influence the performance of the ADC are listed below [17, 38]:

- **IPSource** and **IPSourceMiddle** influence the total dynamic range of the transfer curve. When set too low, the linearity of the value gets lost due to the missing codes. When set too high the range decreases. The registers influence the ADC reference of the upper/lower half of the module.
- **IPSource2** influences the working point of transconductors TC.
- **IFBPBias** is the biasing current of TC. Its value also mainly influences the range of the transfer curve.

Furthermore, there are two supply voltages for the DCD that influence the operation:

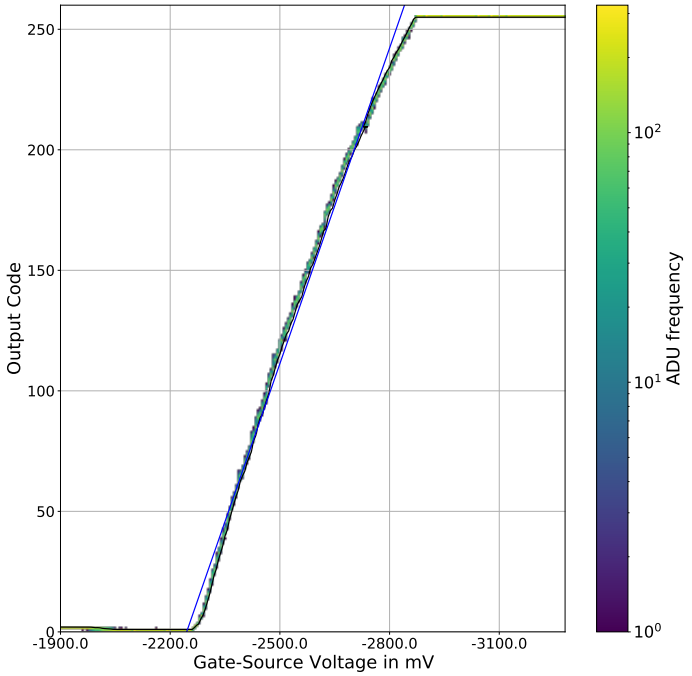


Figure 5.3: Example of ADC transfer Curve using the DEPFET current source. The figure shows the dependency of the output code in arbitrary digital units (ADU) on the gate-on voltage. This ADC curve is recorded in channel 32 of module W60_OF1.

- **RefIn** is a reference voltage at several nodes inside the CMC. Its value has an high impact on the missing code effect.
- **Amplow** is the ground potential for amplifiers, which affects the input range. The range of the curve is not affected by this parameter. An *AmpLow* too low can cause missing codes, while an *AmpLow* too high results in high noise.

The ADC Scan can be used to find the ADC and DAC settings for the best performance. Two- and one-dimensional scans through subsets of the parameter space are performed.

5.2.4 Current Sources for ADC Scan

There are three different possibilities to record the ADC transfer curves using the DHE, the DCD internal current source or the DEPFET current source [13]:

- The *DEPFET current source* is used as the default setting of the ADC scan. It is depending and controlled by the gate-on voltage

$$I_D \propto V_G^2, \tag{5.2}$$

and can therefore be used for recording transfer curves. It is sufficient in terms of current range, current step size and time duration for the scan.

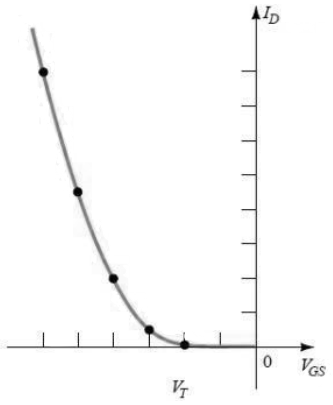


Figure 5.4: Ideal FET Curve. Drain current I_D as a function of gate-on voltage V_G. FET turns on above threshold V_T.

- From previous observations the *DCD internal current source* is not accurate enough to resolve INL and DNL errors. Furthermore, its strength does not cover the full dynamic range of the lowest gain.
- The advantages of using the *DHE current source* are a very fine control and low noise. Due to the design of the module it takes very long to characterize all parameters of the ADC scan. The DHE current source gives a very precise value on the inserted current. Therefore, it is used for further measurements in obtaining precisely the gain and the transconductance of the pixel matrix, which is described in section 8.

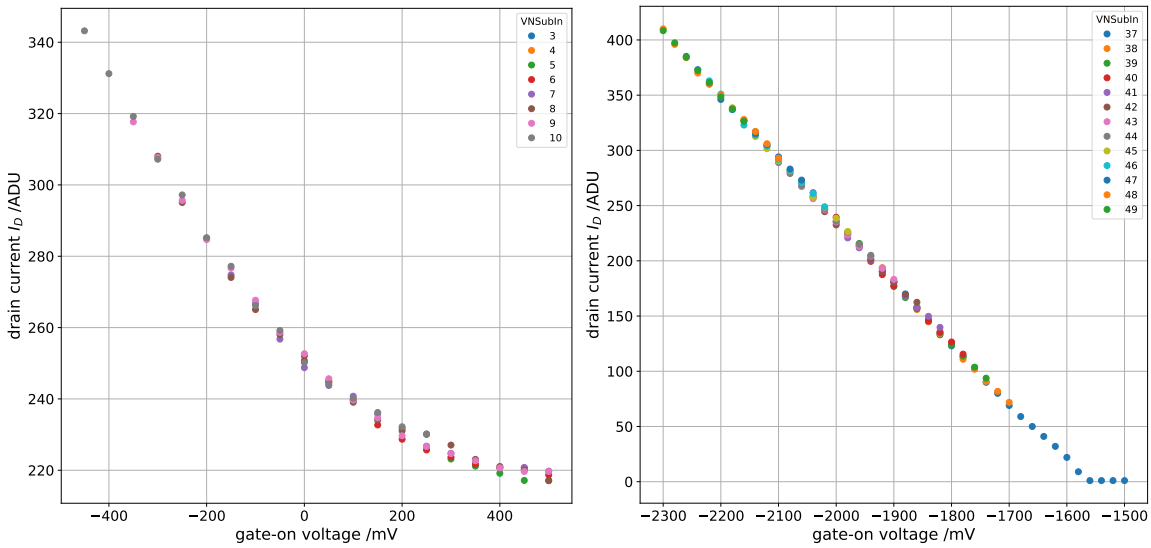
5.3 DEPFET IV Scan

With the help of the DEPFET IV scan the FET threshold and the transconductance for each pixel can be evaluated. Within the DEPFET IV scan, a current voltage scan (IV), the transistor current is measured as a function of the gate-on voltage. The drain current I_D is measured while increasing the gate-on voltage V_G. For this purpose pedestals are taken. Due to the limited dynamic range provided by the DCD as discussed in 5.2 the drain current is recorded with different settings of *VnSubIn*, which can be applied at the internal current sink of the DCD at the input node (see section 3.2.2). The difference of the ADC value can be added to the data of the higher *VnSubIn* value. [37]

5.3.1 FET Threshold and Transconductance

Example measurements of the DEPFET IV scan are shown in figure 5.5, where the different *VnSubin* settings are depicted by the color code.

To understand the functionality of the DEPFET IV scan, the equation of the drain current I_D given in 3.1 needs to be investigated. Under the assumption of an empty internal gate ($Q_{sig} = 0\,e^-$) equation



(a) (b)

Figure 5.5: Examples of DEPFET IV scan to determine a) the FET threshold with *VNSubIn*-settings from 0 to 10 and b) the transconductance with *VNSubIn*-settings from 36 to 49 the in pixel at row 320 and column 124 for module W60_OF1. Swept gate-on voltage is shown on x-axis in mV, while drain current is depicted on y-axis in arbitrary digital units ADU.

3.1 simplifies to [14]

$$I_D = -\frac{W}{2L}\mu_h C_{ox}\left(V_G - V_T\right)^2 . \tag{5.3}$$

Due to the dependency of the drain current I_D on the gate voltage V_G, the DEPFET IV curves give important characteristics on the DEPFET pixels. The threshold voltage V_T of the DEPFET pixels can be extracted. In figure 5.4 the ideal dependency on the gate-on V_G is depicted. The drain current I_D remains zero until the FET-threshold is reached, where the FET is turned on. It is rising quadratic with the gate-on voltage V_G. Figure 5.5(a) shows the measured drain current I_D as a function of the gate-on voltage V_G. The quadratic dependency on the gate-on voltage becomes clearly visible. The extraction of the FET threshold plays an important role for irradiated modules where oxide damages occur and results in a decreased threshold. The slope of the DEPFET IV Curve can also be used to determine the transconductance (see equation 3.4), which with empty internal gate ($Q_{sig} = 0$) is given as [14]

$$g_m = \frac{\delta I_D}{\delta V_G} = \frac{W}{L}\mu_h C_{ox}\left(V_G - V_T\right) . \tag{5.4}$$

The measurement (figure 5.5(b)) takes place in a lower gate-on range, where the quadratic curve behaves approximately linear.

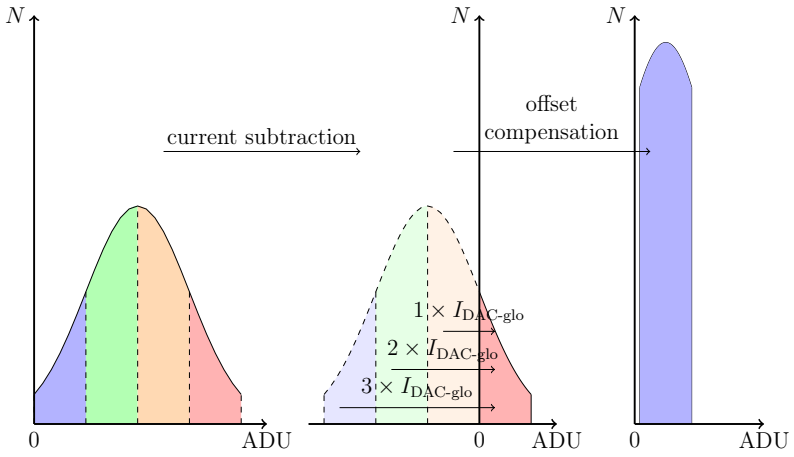


Figure 5.6: The Offset Calibration process is outlined. A pedestal distribution is shown where N is the number of pixels. The pedestal distribution is first divided into four parts. Then it is shifted to the lower dynamic range of the ADCs using the *VNSubIn*-settings. After applying the offset compensation with the help of the offsets k and the global variables $I_{DAC-glo}$, this results in the desired narrow distribution. [13]

5.4 Offset Calibration

The purpose of the offset scan is the equalization of the pedestal response of the modules. Thus, a pedestal distribution as narrow as possible should be achieved in order to homogenize the response of the pixels. Signals, which give a current close to 0 ADU, as for example minimum ionizing particles (MIPs), cannot be resolved by the DCD directly. Therefore such shift enables a higher measurement range.

The pedestals can be minimized with the help of a 2-bit offset compensation. Thereby, a certain amount of current can be added to the drain current of each pixel. This current is set by the DHP and sent to the DCD. Due to limitations in the inter-ASIC communication, only 3 different current values can be added for all pixels. Therefore a global current $I_{\text{DAC-glo}}$ is defined. The systematic process is outlined in figure 5.6. The pedestal distribution is then divided into four parts depending on their pedestal values. Those regions are displayed in different colors. The drain current values I_{ped} of the four pedestal groups are added to the global current weighted with an multiplication factor k. This value can take numbers between 0 and 3. Hence, the individual current I_{ind} is a multiple of the global current:

$$I_{\text{shift}} = I_{\text{ped}} + k \cdot I_{\text{DAC-glo}} = I_{\text{ped}} + I_{\text{ind}}, \quad k \in \{0, 1, 2, 3\} \tag{5.5}$$

The consequence is a shift of the pedestal groups above each other. The measurement is done by recording multiple pedestals within each pixel for different offset values k. Additionally, the *VNSubIn* (see section 3.2.2) settings are considered to further improve the offset results. Thus pedestals of all pixels are measured for all possible combinations of the three different applied offsets and a range of *VNSubIn*. [13]

Within the analysis, the best global current for each ASIC pair (DHE and DCD) and offset value for each individual pixel is found. Additionally, there is the possibility to determine offsets gate-wise. This gate-wise methodology is applied before the ADC scan is performed, because a pixel-wise analysis can lead to pedestal gradients along different gates. This effect can be compensated by the ACMC.

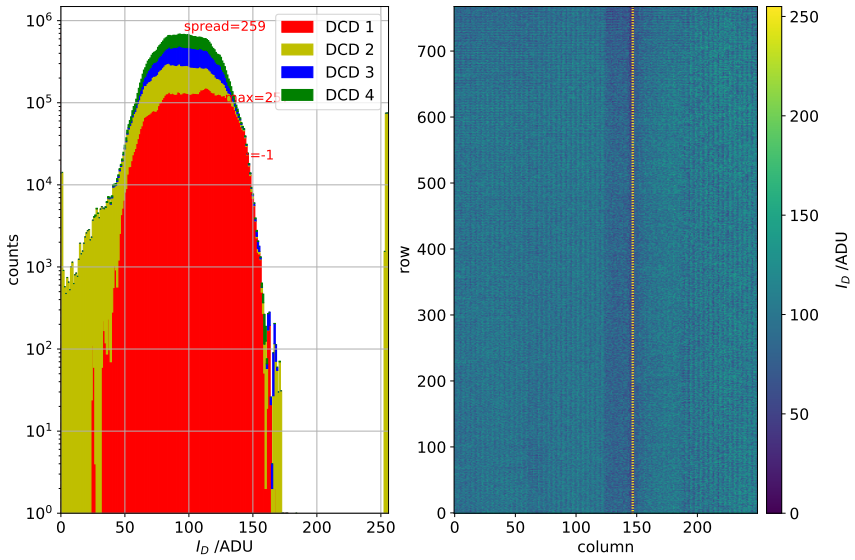


Figure 5.7: Pedestal Distribution with Offset Compensation applied pixel by pixel for module W60_OF1. On the left a 1D histogram is depicting the pedestal value of each pixel. The right shows the pedestal value on the respective geometrical position inside the DEPFET matrix. ACMC is used. The colors stand for the different DCDs. Additionally, the pedestals are depicted on their respective position inside the module matrix.

For the ADC scan no ACMC is applied to avoid influences the ADC scan. The *VNSubIn*-settings are important for pedestals that are far away from the mean value within each gradient. These cannot be compensated for by the ACMC. Therefore, the *VNSubIn*-settings that can be applied gate-wise are combined with the offset results. [37]

An example of a pixel-by-pixel analysis with applied ACMC can be seen in 5.7. Compared to the pedestal distribution without offset and ACMC in figure 5.1, it is clearly narrower. The matrix looks in addition more homogeneous.

5.5 HV IV Scan

For the HV IV scan, the hv is set over a certain range and the hv current is measured. The hv at load, at regulator and the requested hv are recorded. This allows to compare different modules. In addition, the HV IV curves contribute to the characterization of the module. An example measurement of module W60_OF1 is shown in 5.8.

For absolute low hv no depletion is expected yet, accordingly no hv current flows. From about $-50\,\mathrm{V}$ downwards, an hv current can be measured. The maximum current is limited by the power supply hardware. At the limit, the requested voltage thus differs from those applied at load and at regulator. Because of the depletion behavior, an exponential increase of the current is expected and observed. To compare modules with each other, an hv setting as reference point at which half of the maximum current range for the measurement is reached. [37]

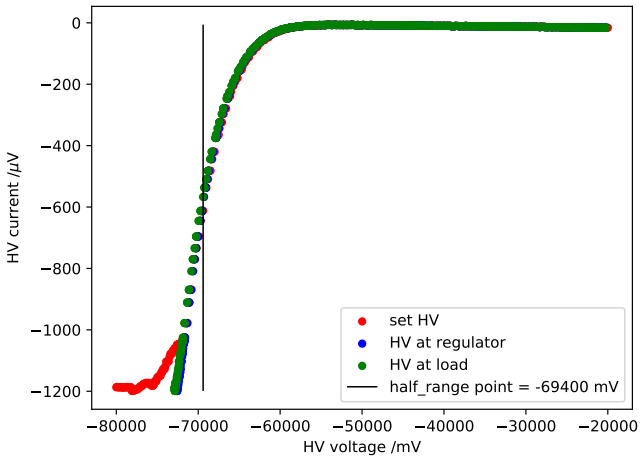


Figure 5.8: Results of the hv current as a function of the hv for module W60_OF1. The hv at load at regulator and the set hv are marked in colors.

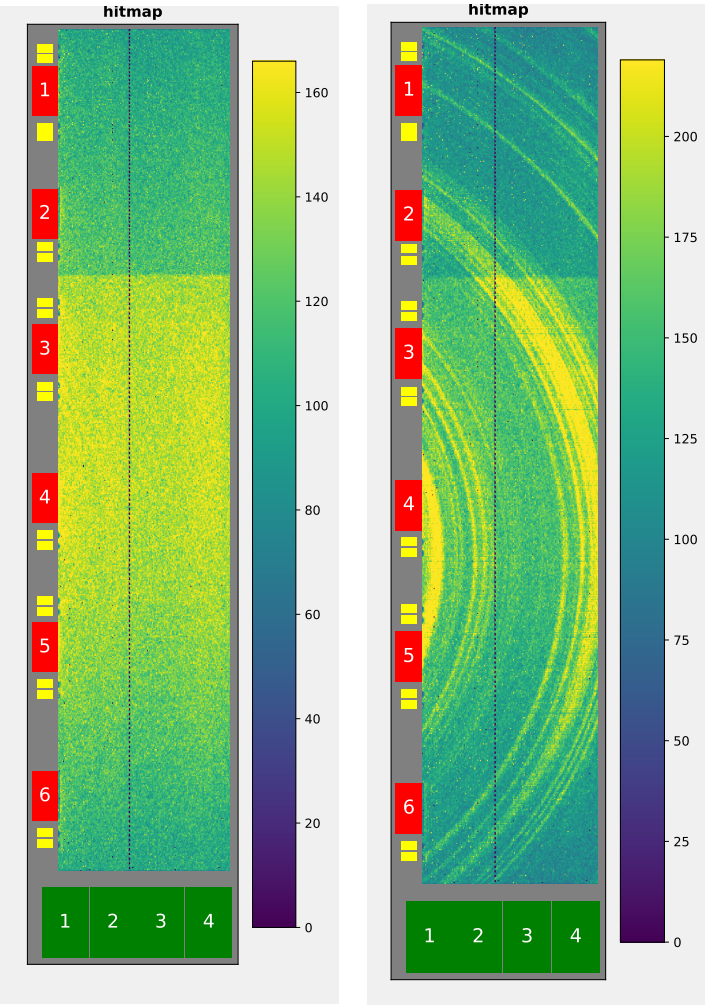
5.6 Source Scan

The aim of the source scan is to find a parameter setting for the biasing voltages drift, clear-off and high voltage (hv), where the pixels response as homogeneous as possible. In the following, the measurement process is discussed followed by an explanation of the data processing and results are explained.

To provide sufficient statistics, a strong radioactive source, which is installed above, is used. This is then installed above the module. During the measurement zero suppressed data for different biasing voltage parameters is recorded. Meaning drift, hv and clear-off will be swept while the drain current is being recorded.

In order to select the optimal biasing parameters, different components can be taken into account. Therefore, the hitmap displaying a 2D histogram, where each bin corresponds to a DEPFET pixel, is considered. For each pixel, the number of hits above a certain threshold is counted. In the third dimension, the counts are displayed. With the settings of bias voltages the hitmap appears homogeneous. An example hitmap for a good parameter setting compared to a bad parameter setting is shown in 5.9. The matrix region with smaller pixel size shows a reduced number of hits, due to lower statistics in those sections. An almost homogeneous distribution of hits can be seen at the center part, where the source was placed exactly on top.

Since the scan measures certain voltage settings over a large parameter space, the decision for the best setting is mainly based on comparing the most probable value of the cluster charge distribution (see figure 5.10) for each parameter settings. This process obtains the largest output with the highest internal amplification (see section 3.1.1) and results in the highest charge collection efficiency. A ^{90}Sr source (with approximately 33 MBq activity), electron emission leads to a Landau like cluster charge distribution. Doping effects during the production of the matrix could cause ring-like patterns on the hit map. These only appear for certain combinations of biasing voltages when the pixel region is partly depleted. Therefore, the best parameter settings ideally show the most homogeneous and least



(a) Hitmap with good parameter settings with hv= −51 V, drift= −5 V and clear-off= 3 V.

(b) Hitmap with bad parameter settings with hv= −46 V, drift= −5 V and clear-off= 2 V.

Figure 5.9: DEPFET pixel hitmaps are shown for biasing voltage settings for module W60_OF1. A ^{90}Sr source (33 MBq activity) was used with a measurement duration time of 400 s. The dotted black line shows 3 dead drain lines next to each other inside the module. The colorbar shows the number of hits.

amount of ring-patterns. [37]

5.7 Comparison of Tested Modules

In the following, correlations of the results of several scans for different modules are compared. The aim is to gain understanding about different behaviors of the modules. First, the optimal biasing settings of the modules determined from the source scan are discussed. These are put into correlation with the half range point of the hv current. Then the hv range in which full depletion occurs is

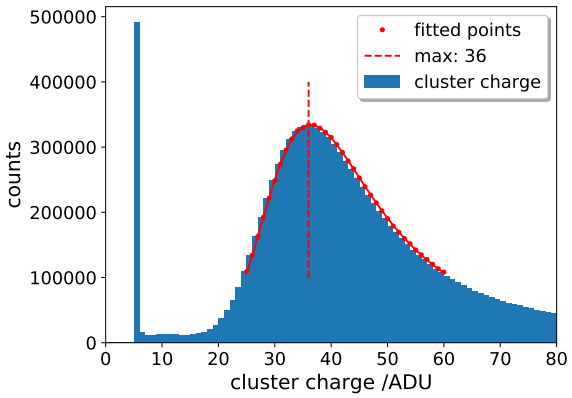


Figure 5.10: Cluster charge distribution for W60_OF1. A ^{90}Sr source (33 MBq activity) was placed with a measurement duration of 400 s.The selected settings are hv = −51 V, drift = −6 V and clear-off at 2 V. A landau distribution is fitted to find the most probable value.

evaluated for several modules. Finally, the optimal DCD settings for different modules are discussed.

5.7.1 Matrix Biasing

The optimal biasing voltage settings, hv, drift and clear-off voltage, which are determined from the source scan, ideally have the same magnitudes due to the same design and production process. In table 5.1 the optimal biasing voltages of the investigated modules are listed and related to the half current range point obtained from the hv iv scan. It is noticeable that the values of the biasing voltages are in the same order of magnitude, but not the exact equivalent. Such differences indicate a different behavior of the modules, which can occur due to the complex production process.

Between the half range point and the optimal hv a correlation is expected. A smaller half range point and a more positive optimal hv setting would indicate an earlier depletion. In figure 5.11 the possible correlation is visible. The influence of the drift and the clear-off voltages on the depletion should not be neglected. Since the clear-off settings are the same for all modules, only the influence of the drift voltage must be taken into account for the comparison. The correlation plot shows that the two values with a drift voltage of −5 V lead to a deviation as expected. The so-called Pearson correlation coefficient (see section 3.5.1) gives an indication of how linear the data sets behave. The value 0.797 indicates a strong linearity. Thus, a correlation between the optimal hv and the half range point can be confirmed approximately. Possible deviations may occur due to the selection process of the optimal hv setting, because several settings are always suitable for the hv for optimal depletion. More details on the depletion range on hv are listed in the next section 5.7.2. The different depletion points of the modules could indicate different resistivities of the modules.

5.7.2 Depletion Zone

In this section, the depletion region as a function of hv is discussed. For this purpose, source scans are performed over a large parameter range in biasing settings. The charge cluster spectrum (see figure 5.10) is examined and the most probable value is extracted. A high most probable value indicates a high charge collection efficiency. It reaches its maximum when the detector bulk is fully depleted.

	W56_OB1	W56_OF1	W57_OB1	W57_OF2	W57_IB	W60_OF1	W67_IB
hv /V	−56	−56	−54	−50	−55	−51	−54
clear-off /V	2	2	2	2	2	2	2
drift /V	−6	−5	−5	−6	−6	−6	−6
half range point hv /V	−70.5	−71.3	−69.0	−68.8	−70.6	−69.4	−69.5

Table 5.1: Comparison of the scan results of the source scan to the hv iv scan. The the biasing settings, hv, clear-off and drift are related to the half current range point.

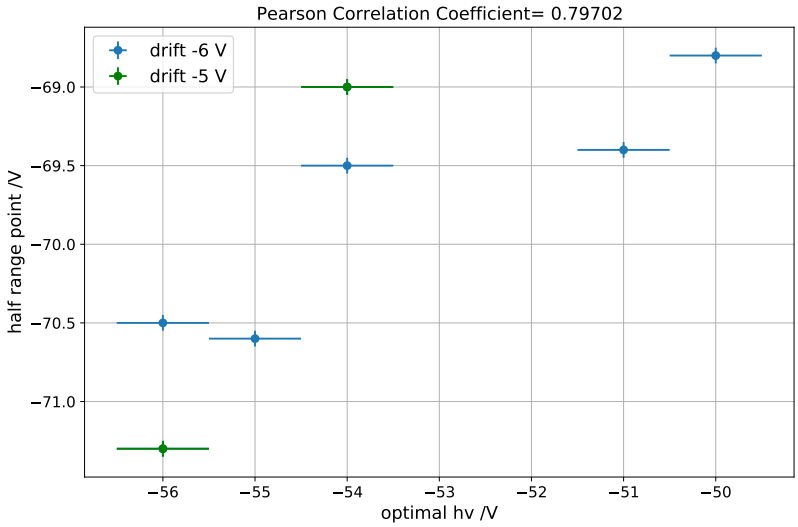


Figure 5.11: The optimal hv settings are plotted against the respective half current range points for different modules. The data of all modules was recorded with a clear-off setting of 2 V. The yellow data points mark the deviating drift settings of −5 V.

The results of the measurements using a ^{90}Sr source (33 MBq activity) are compared with the results of using a ^{109}Cd source (1 850 MBq).

In figure 5.12, hv settings are plotted against the most probable value of the respective cluster charge spectrum for a ^{90}Sr source for module W57_OF2. The different settings for drift and clear-off are indicated by color. A plateau region in which a complete depletion is considered is noticeable. Signals with a value of 25 ADU are overlaid by the noise signal and can therefore no longer be measured.

In this case, the plateau describes a width of approximately 8 to 10 V. Above hv $>$ −49 V an under depletion is observed. In this case parts of the silicon bulk are not depleted, which results in incomplete collection of signal electrons within the internal gate and prohibits the measurement of a fraction of the signal. Hv has the largest influence on the charge collection efficiency, and therefore on the depletion for more positive hv. For an hv more negative than −59 V an over depletion can be identified. Here the deposited charges start to drift to the drift and transistor implant. Thus a fraction of charges are lost in the implants before reaching the internal gate. As observed in figure 5.12 the clear off and the drift potentials have the highest impact on this scenario. Decreasing the clear-off voltage leads to a wider plateau region. A too low clear-off setting could lead to a back injection effect, where charge flows in reverse from the clear implant back into the internal gate. More details of this effect are discussed in [40].

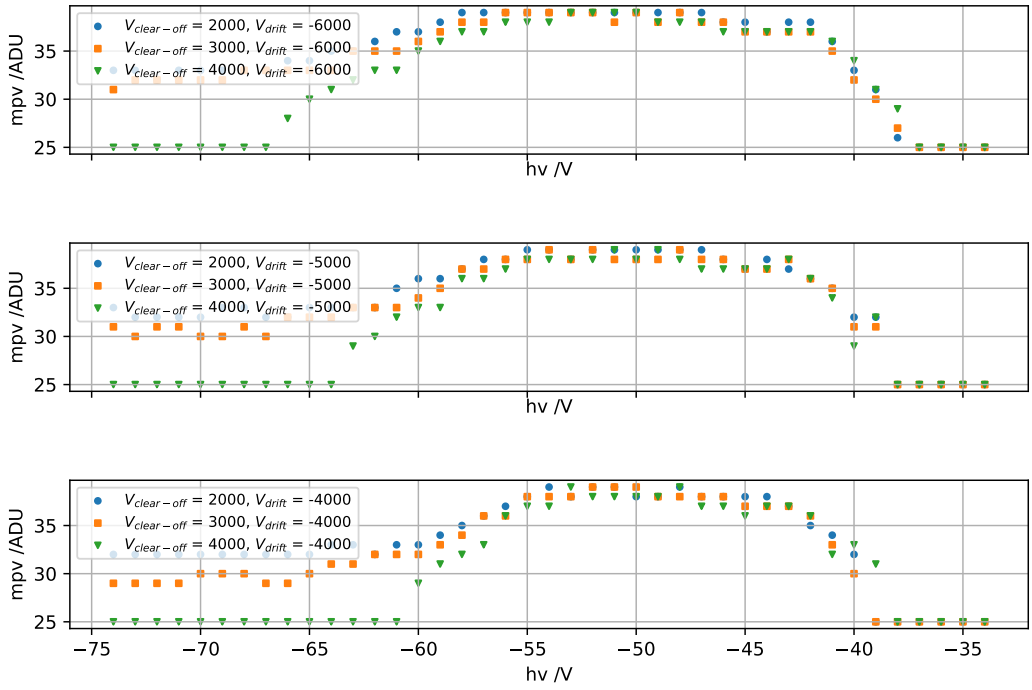


Figure 5.12: Most probable value (mpv) extracted from cluster charge spectrum from parameter source scan with a ^{90}Sr source measured for module W57_OF2.

Comparing the plateau region of the ^{90}Sr scan with the ^{109}Cd scan (see figure 5.13), the results are consistent. From hv < 56 V the over depletion occurs, which depends strongly on the clear-off and the drift potential. The ^{109}Cd source emits x-rays. Therefore a charge spectrum with K_α and K_β peaks is expected. For more positive hv the K_α peak is still overlaid by the noise. With a signal above 20 ADU, the K_β peak is already measurable and misinterpreted as the maximum signal. Therefore, the charge spectrum must be considered in more detail. Thus, from -40 V a K_α signal is observable. The depletion starts at < -46 V. A consistency between the parameter scan for the two sources is expected, since the charge collection efficiency should not depend on the type of incoming radiation.

The approximate plateau regions of the examined modules are listed in table 5.2. A shift with respect to the plateau range is visible. Differences in the optimal biasing settings were already discussed in the previous settings. A correlation of the optimal hv settings to the depletion plateaus is expected. Uncertainties occur due to the approximate estimation of the pixel plateau. In addition, the optimal hv setting can also only be roughly determined, since the most probable value in the plateau is relatively constant. Shifted plateaus within modules indicate different resistivity of the modules.

Compared to previous studies (see [41]) for the depletion zone, the general behavior for over and under depletion can be confirmed. Furthermore, a rough shift of the plateau regions to more positive hv values can be observed.

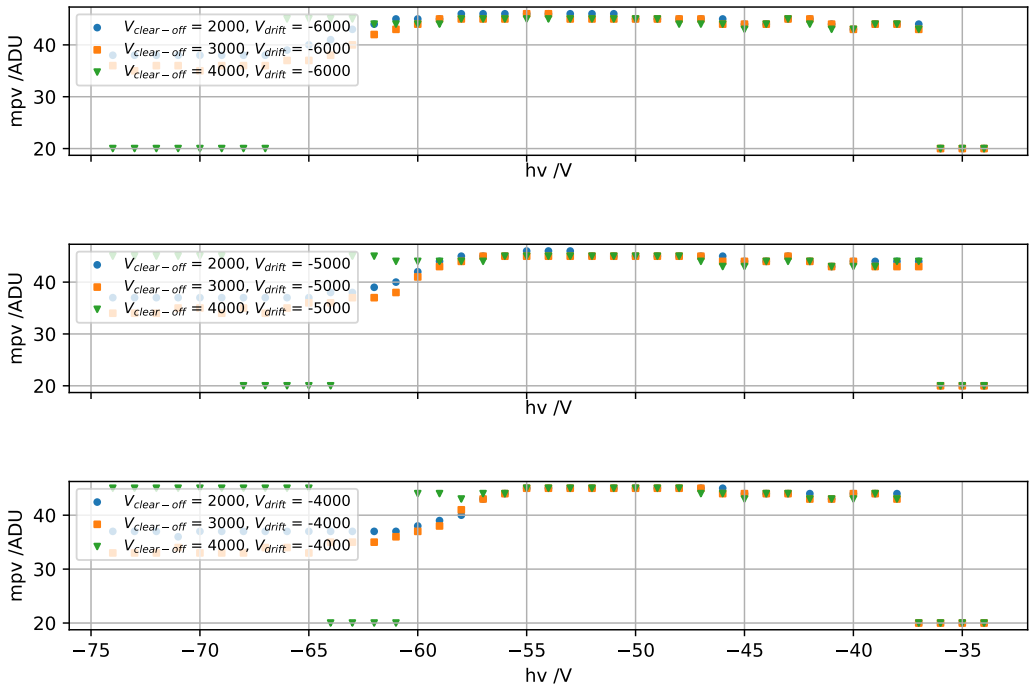


Figure 5.13: Most probable value (mpv) extracted from cluster charge spectrum from parameter source scan with a ^{109}Cd source measured for module W57_OF2.

	W57_OF2	W57_IB	W60_OF1	W67_IB
plateau range /V	−46 to −55	−49 to −59	−48 to −58	−48 to −56
optimal hv /V	−50	−55	−51	−54

Table 5.2: Comparison of plateau depletion range in relation to the optimal hv setting for different modules.

CHAPTER 6

Biasing Voltage Studies

In this chapter, the newly developed scan of the biasing voltages of the PXD module is presented. The scan focuses on the dependence of the voltages, drift, clear-off and high voltage (*hv*) on the pedestals (as well as the noise and dispersion) and the current of the hv. First, the measurement method is introduced. Afterwards, the results of the collected data are analyzed.

6.1 Measurement Biasing Voltage Scan

The methodology for the measurement when applying biasing voltages is based on the pedestal scan, which is explained in detail in section 5.1. In the pedestal scan the drain current is measured gate-wise by the DCD while the DEPFET pixel is on, assuming there is no further charge in the internal gate. Additionally, the hv current is measured continuously. In this study, the two measurements are performed for different bias voltages. More details on the applied biasing voltages are listed in section 3.3. A pedestal measurement and hv current measurement are performed for each individual combination of the three voltages, drift, clear-off and hv. A higher number of frames also gives the possibility to determine the noise of the pedestal distribution. The measurement results of one biasing parameter setting are presented in figure 5.1. Additionally to the display of pedestal value per pixel, the distribution over all pixels is depicted in a histogram, too. The distribution determines the so-called pedestal distribution. The measurements are performed with an offset applied on the whole matrix (see section 5.4). The ACMC Correction is turned off (see section 3.2.2).

The range of the biasing voltages is listed below:

- *drift* voltage: from −2 V to −6 V in steps of 1 V.
- *clear-off* voltage: from 1 V to 5 V in steps of 1 V.
- *hv*: from −65 V to −40 V in steps of 1 V.

The pedestals are recorded for 100 frames per individual setting.

In order to achieve the most accurate result possible, which shows the behavior depending on the biasing voltages, a section can be defined on the pedestal distribution. This excludes pixels that deviate from the typical behavior of the majority. Therefore, the well performing pixels that range between 50 to 200 ADU in the main distribution are used for further studies. An example of a pedestal distribution

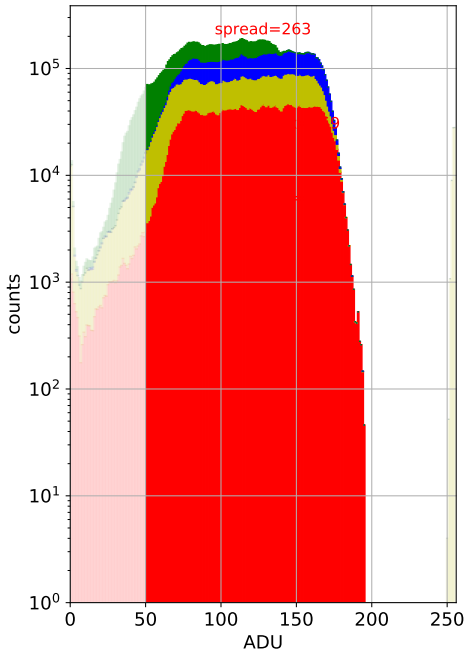


Figure 6.1: Pedestal Measurement on Module W60_OF1 including 100 recorded frames, drift = −6 V, clear-off = 2 V and hv = −51 V, with ACMC turned off and offset applied. The color code separates the four DCDs. A cut on the pedestal distribution is made outside of 50 and 200 ADU.

with using the cut is shown in figure 6.1. In addition to the cut in the pedestal range, a region of interest can be selected within the matrix. This is advantageous for modules with many noisy pixels, broken drain or gate lines.

In order to measure the biasing voltages as a function of the pedestals, the dispersion and the noise, the pedestal data must be further processed. To relate the measurement to the pedestals via the biasing voltages, the median value of the selected distribution over the number of frames N_f inside each pixel $I_{\text{ped per pixel}}$ is taken:

$$I_{\text{med ped per pixel}} = \texttt{median}\left(I_{\text{ped per pixel}}(N_f)\right) = \begin{cases} I_{\text{ped per pixel}}\left[\frac{N_f}{2}\right] & \text{if } N_f \text{ is even} \\ \frac{\left(I_{\text{ped per pixel}}\left[\frac{N_f-1}{2}\right] + I_{\text{ped per pixel}}\left[\frac{N_f+1}{2}\right]\right)}{2} & \text{if } N_f \text{ is odd} \end{cases}. \tag{6.1}$$

The mean value is taken over the sum of the pedestals of every pixel:

$$\texttt{median pedestals} = \texttt{mean}\left[I_{\text{med ped per pixel}}\right] = \frac{\sum^{N_p} I_{\text{med ped per pixel}}}{N_p}, \tag{6.2}$$

with N_p being the number of pixels. The dispersion is a quantity on the spread of the pedestal values of the whole matrix. It is calculated with the median of the pedestal distribution of each pixel. For the

matrix, the standard deviation needs to be applied. The dispersion is defined as:

$$\texttt{dispersion} = \texttt{std}\left(I_{\text{med ped per pixel}}\right) = \sqrt{\frac{\sum^{N_p}(I_{\text{med ped per pixel}} - \mu)}{N_p}}, \tag{6.3}$$

with μ being the population mean. The noise is given by the standard deviation in each pixel. This quantity represents the deviation of the frames within each pixel with respect to the average value:

$$\texttt{noise} = \texttt{mean}\left[\texttt{std}\left(I_{\text{ped per pixel}}(N_f)\right)\right] \tag{6.4}$$

The three quantities that contribute to the evaluation of the measurement are determined for each measurement step.

6.2 Results

The following section deals with the median pedestals, dispersion, noise and hv current in correlation to the biasing voltages, drift, clear-off and hv. In each sub chapter a different quantity is examined.

6.2.1 Pedestals

In figure 6.2, the median pedestals for different biasing voltage settings are related. Systematic gradients for the values of median pedestals as a function of the settings are noticeable. In the following, the influences of the biasing voltages on the median pedestals are investigated. A projection is made on the respective voltages.

High Voltage (hv)

For more negative hv, higher pedestal values are observed. One reason for the increase is the application of the hv on the back side. The more negative it becomes, the larger the depletion zone in the pixel. The effect can be observed in the projection plot in figure 6.3. Since the backside acts like a far gate, linearity is expected between the influence on the FET, i.e. the dark current and the hv. This is confirmed by the Pearson coefficient (see section 3.5.1), which has a value close to -1. This is based on the coupling of the potentials. If the hv potential changes, this influences the electric field of the p-channel between source and drain and thus also the pedestals. Since full depletion is reached at about -50 V to -60 V, a slight different strength is observed from -60 V, because the fully depleted pixel semiconductor area has become a depletion zone. This effect can be observed before with all other examined modules, too (see section A.1.1). For W57_OF2 and W57_OB1, a lower range for hv was selected, hence the saturation is particularly noticeable from approximately hv = -60 V on.

Drift Voltage

Another observation is the gradient of median pedestal values as a function of drift voltage. In figure 6.4 the projections on the drift axis are plotted for two hv settings. A linear relationship becomes visible. A possible explanation is that the potential of drift implant also couples to the FET channel. Consequently, this will result in an increased pedestal current. The occurring behavior might be

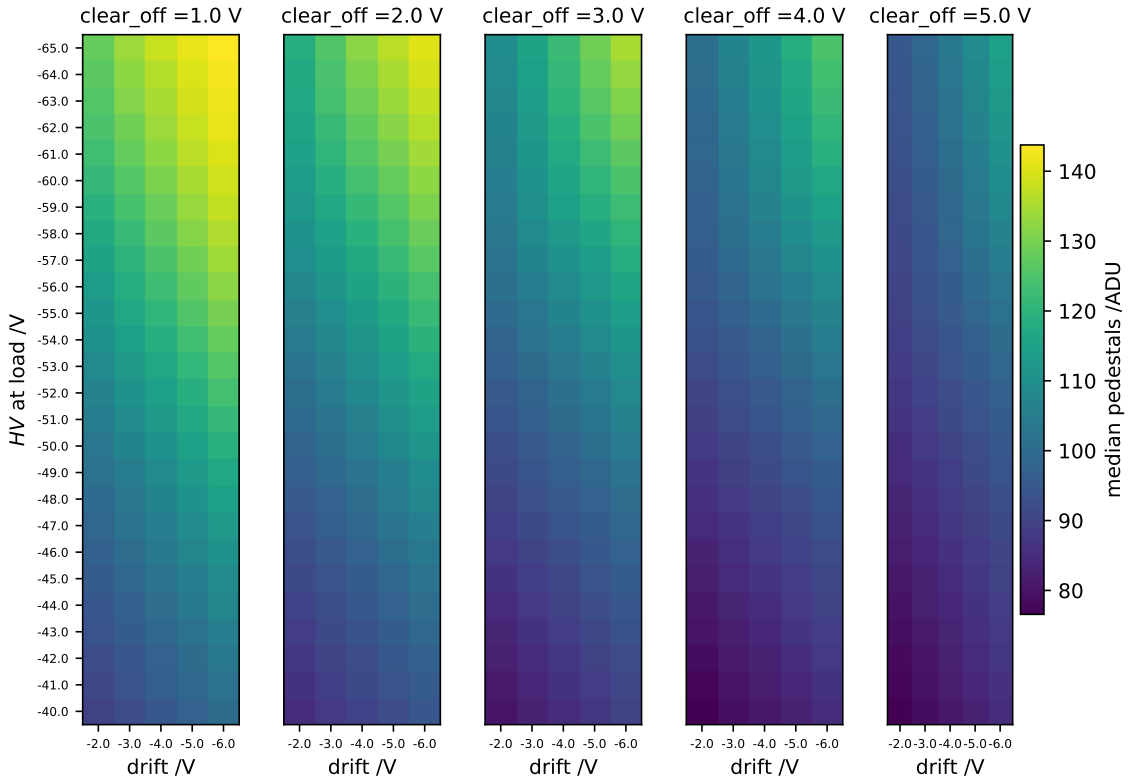


Figure 6.2: The values of the median pedestals are shown for different biasing settings for module W60_OF1. The values for hv are plotted on the y-axis. On the x-axis, the values for the drift voltage are shown. The color code indicates the size of the median pedestals. The different plots were taken for different clear-off settings.

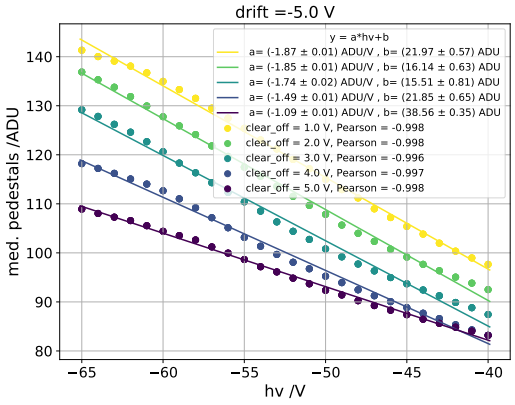
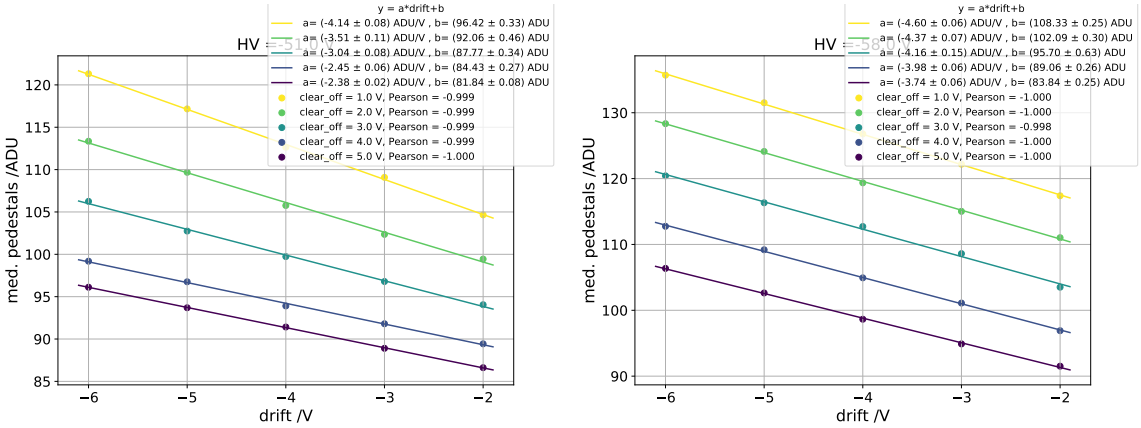
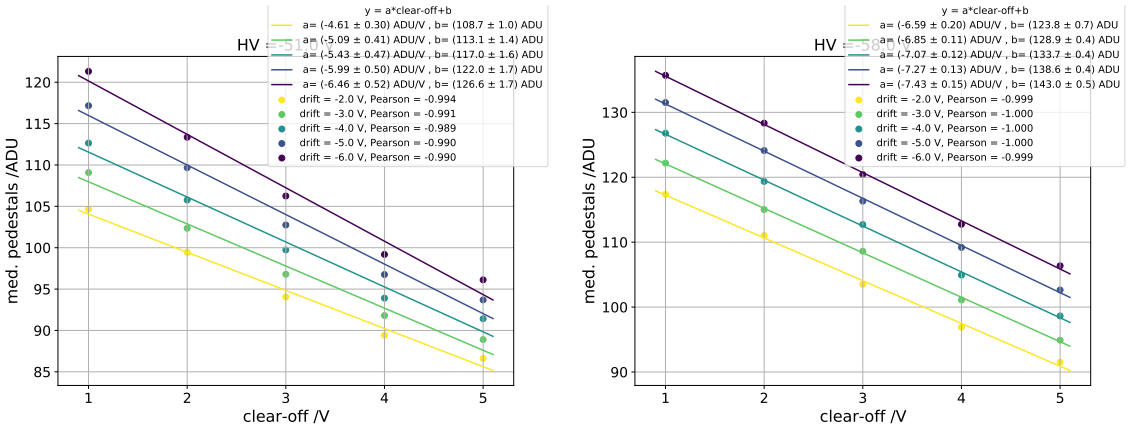


Figure 6.3: Median pedestals plotted against hv voltage at a constant drift voltage of −5 V for module W60_OF1. The different colors represent different clear-off settings .The Pearson coefficient indicates the linearity of the data points.



(a) hv = −51 V (b) hv = −58 V

Figure 6.4: Median pedestals plotted against the drift voltage for two different example settings of hv for module W60_OF1. The different colors represent different clear-off settings. The Pearson coefficient indicates the linearity of the data points.



(a) hv = −51 V (b) hv = −58 V

Figure 6.5: Median pedestals plotted against the clear-off voltage for two different example settings of hv for module W60_OF1. The different colors represent different clear-off settings. The Pearson coefficient indicates the linearity of the data points.

also caused by leakage currents. Accordingly, more thermal excitation are caused for more negative drift voltages, which leads to an electron current flow. These accumulate in the internal gate and thus amplify the measured drain current. However, leakage currents are less strong in non-irradiated modules and probably have only a small contribution here.

Clear-Off Voltage

When looking at the projection of the median pedestals onto the clear-off voltage, a similar effect as for the drift voltage can be observed (see figure 6.5). A higher clear-off voltage leads to a smaller

	W57_OB1	W57_OF2	W65_IF	W57_IB	W60_OF1
clear-off /ADU/V	−7.55	−13.67	−23.25	−8.93	−7.04
drift /ADU/V	−5.91	−7.69	−5.56	−5.72	−4.17
hv /ADU/V	−2.08	−1,91	−2.91	−3.02	−1.61

Table 6.1: Mean influences of biasing voltages on median pedestals for different modules. The mean influences are extracted from the slope of the linear regression. The drift and clear-off voltage influence is compared with an example voltage of hv = −58 V, while the hv influence is calculated with drift = −5 V.

dark drain current (median pedestals). This effect is probably due to the process already explained above. Thus, the clear-off implant potential might couple to the FET channel. Figure 6.5 shows that the connection with the median pedestals and the clear-off voltage deviates from linearity. When the voltage difference between clear contact and common clear gate (CCG) (see section 3.3) is too small, CCG no longer acts as a barrier between clear contact and the internal gate. Thus, electrons can flow from clear back into the internal gate. This phenomenon occurs at a difference of about 3V. The smaller the potential difference between CCG and clear-off, the more likely the effect of so called back injection occurs. The effect is described in detail in [40, 46]. With the performed measurement this can be considered a possible cause.

Furthermore, it is noticeable that a more negative hv leads to a stronger influence of the drift and clear-off voltages on the pedestals. This is to be explained with the depletion process. At a more positive high voltage such as here hv = −51 V the bulk is not fully depleted.

Comparison

All variables hv, clear-off and drift have an influence on the FET as discussed above. When comparing the correlations between drift and clear-off against the median pedestals, a significantly higher influence of the clear-off voltage on the median pedestals can be noticed. With a slope of the linear fit to the correlation of approximately −4 ADU/V to −7 ADU/V, it has the greatest influence on the FET. This effect can be explained by the layout of the DEPFET pixel (see figure 3.2). The clear implant is located much closer to the FET than the drift implant, which is placed beneath the gate viewing on the top of the layout. This means that it can have the strongest coupling to the FET channel. Since the back implant is the furthest away from the source implant, it has the least influence on the FET channel. Thus, the strongest effect for the clear-off voltage correlation is observed. The assumption is confirmed by the observation of the other modules (see section A.1.1), which show the same behavior. A closer comparison, however, shows that the influences occur to different extents. In table 6.1 the mean values of the influences of the three biasing voltages, which are obtained from the slopes of the linear regression, are calculated over the different settings. Initially, one would expect a uniform behavior between the modules in the ideal case. However, it can be seen in table 6.1 that the measurements differ from the assumption. Due to the production process and different pixel sizes of inner and outer modules, deviations in the behavior of the different modules can occur. In addition, a different gate on voltages were set for the respective measurements. Influences of the gate on voltage on the module behavior could be investigated in future studies.

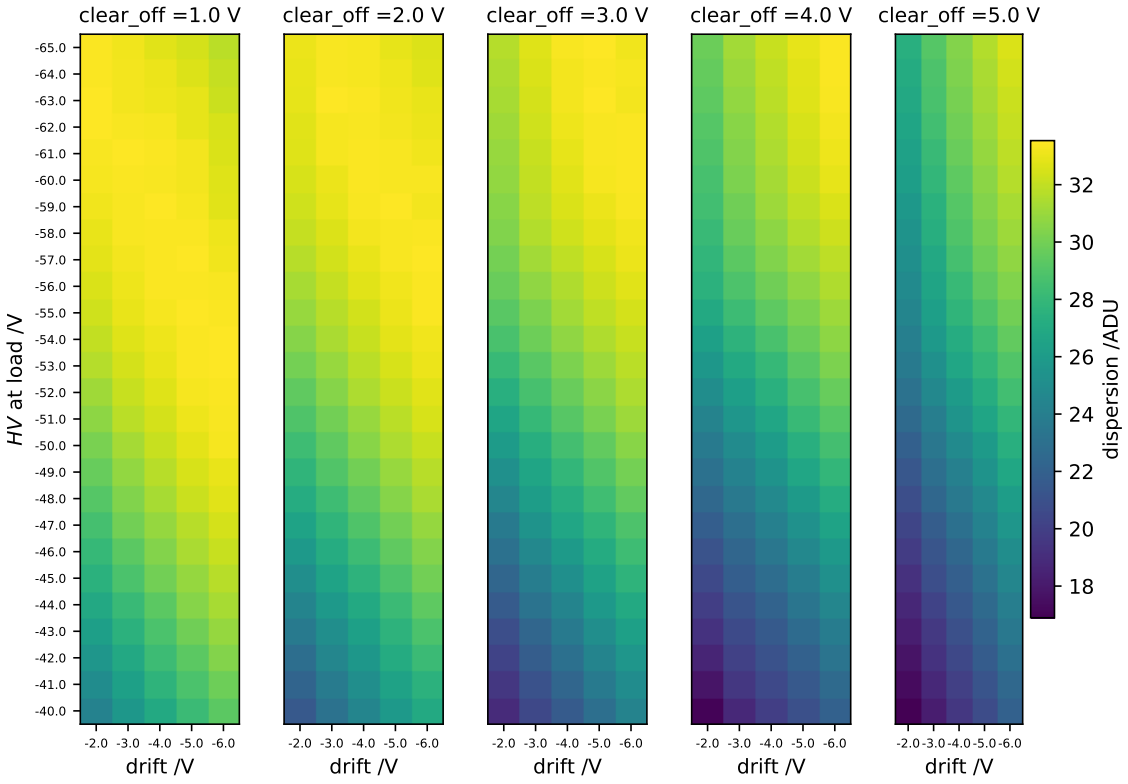


Figure 6.6: Dispersion plotted against the drift voltage for two different example settings of hv for module W60_OF1. The different colors represent different clear-off settings. The Pearson coefficient indicates the linearity of the data points.

6.2.2 Dispersion

In this section the dispersion is examined. The value of dispersion is plotted as a function of the three biasing voltages: drift, clear-off, and hv (see figure 6.6). The color code represents the value of the quantity to be examined. As in the case of the dark FET currents, systematic correlations can be recognized. In the following, the influences of the individual biasing voltages are examined.

Biasing Voltages

When looking at the projection of the drift-axis in figure 6.7, different behaviors stand out. Larger clear-off settings lead to a seemingly linear correlation, which becomes evident by the value of Pearson coefficient, which is close to -1. Smaller clear-off settings seem to saturate for enough negative drift values. For higher drift voltages, i.e. at a smaller difference to the source voltage, narrower pedestal distributions are observed.

The correlation for clear-off shows a similar behavior as the correlation for drift voltage (see figure 6.8). For some settings linearity could be assumed and for others not. When examining the dispersion

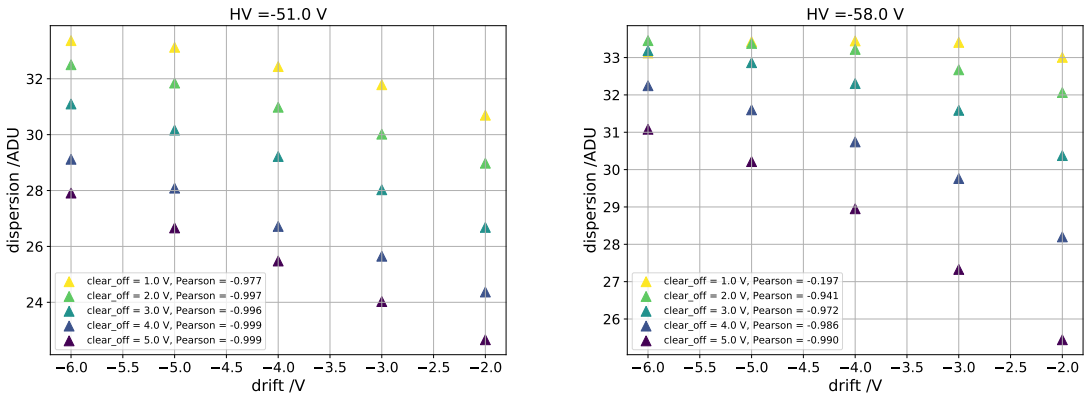


Figure 6.7: Dispersion plotted against the drift voltage for two different example settings of hv for module W60_OF1. The different colors represent different drift settings. The Pearson coefficient indicates the linearity of the data points.

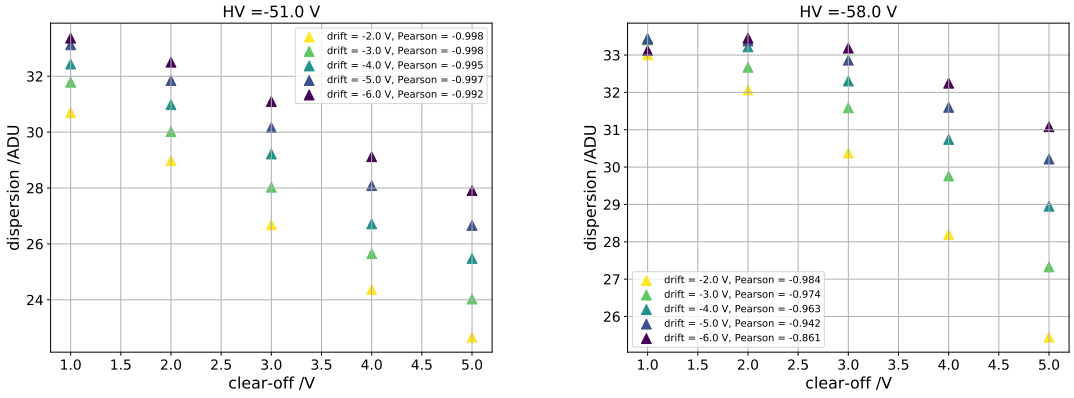


Figure 6.8: Dispersion plotted against the clear-off voltage for two different example settings of hv for module W60_OF1. The different colors represent different clear-off settings. The Pearson coefficient indicates the linearity of the data points.

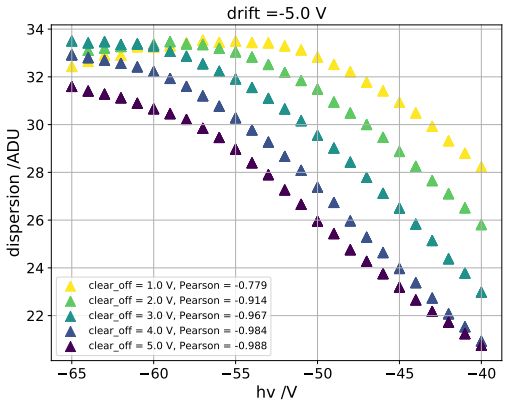


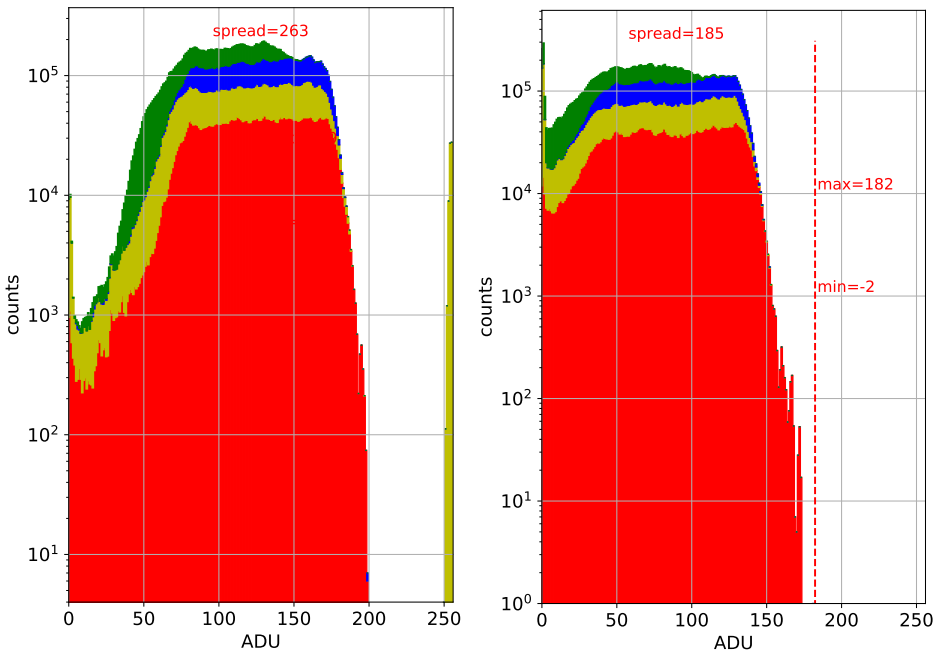
Figure 6.9: Dispersion plotted against hv voltage at a constant drift voltage of −5 V for module W60_OF1. The different colors represent different clear-off settings .The Pearson coefficient indicates the linearity of the data points.

as a function of hv in figure 6.9, saturation is also observed from about 60 V for certain biasing combinations. As for the median pedestals, the effect is strongest visible in combination with the clear-off voltage. Due to the position of the clear implant where the clear-off voltage is applied it has the largest influence on the FET.

From this behavior, the first presumption could be that the closer the drift voltage approaches the source voltage, the more likely relatively high or low currents effects the leakage current. When observing the pedestal distribution for different biasing settings, however, it becomes clear that the observed effect is probably caused by other reasons. Different biasing settings shift the pedestal distribution. For the correlations that do not show any differences in dispersion, they always move only in the selected range between 50 and 200 ADU. For some settings, a change of the biasing voltages leads to a shift where some pedestal values occur outside this range. This in turn leads to a smaller calculated broadening of the pedestal distribution. Two example pedestal distributions with different biasing settings are shown in figure 6.10. The left plot shows the distribution with hv = −58 V, drift = −2 V and clear off = 1 V. The right plot shows the distribution with the same hv and drift settings. The difference arises with the clear off setting which is at 5 V. It is noticeable that the distribution is now shifted to the left, but apparently has not lost its actual width. The smaller calculated dispersion arises due to the truncation of the pedestal distribution.

Comparison

By comparing the effects to the other modules (see section A.1.2) the result is confirmed. Only the measurement as a function of hv seems to show differences. For example, the dispersion increases for more negative hv for module W57_IB. The differences suggest that there are deviations for the appropriate biasing settings for each module to generate the best performance. For the calibration process, a source scan is performed, as described earlier in section 5.6, to obtain the best combination of biasing voltages for the best possible signal.



(a) Clear-off voltage = 1 V.

(b) Clear-off voltage = 5 V.

Figure 6.10: Two pedestal distributions are shown with the settings drift = −2 V and hv = −58 V for module W60_OF1. The color code separates the different DCDs.

6.2.3 Noise

The noise is examined. It is plotted as a function of the biasing voltages in figure 6.11. In contrast to the quantities examined above, no structures can be seen. Rather, the resulting pattern seems to be randomly distributed. In addition, the noise does not change significantly. The highest value is 1.2 ADU and the lowest 1.06 ADU. Consequently, it can be assumed that the biasing voltages have no influence on the noise. Comparing with the other modules, a similar non-significant behavior can be found.

6.2.4 High Voltage Current

Finally, the hv current I_{HV} is investigated as a function of the biasing voltages, which is represented by the color code in figure, 6.12. The current stagnates depending on the high voltage, because the power supply cannot resolve a current smaller than 5 μA. The projection onto the hv axis makes this effect clear (see figure 6.13). In the following the influence of the biasing voltages on the hv current is studied.

High Voltage

For higher high voltages more negative currents are measured. No linear relationship is expected here. The current is expected to flow at around −35 V. After reaching a full depletion from −50 to −60 V a punch through current is observed in addition to the nominal bulk current. This leads to a steep drop

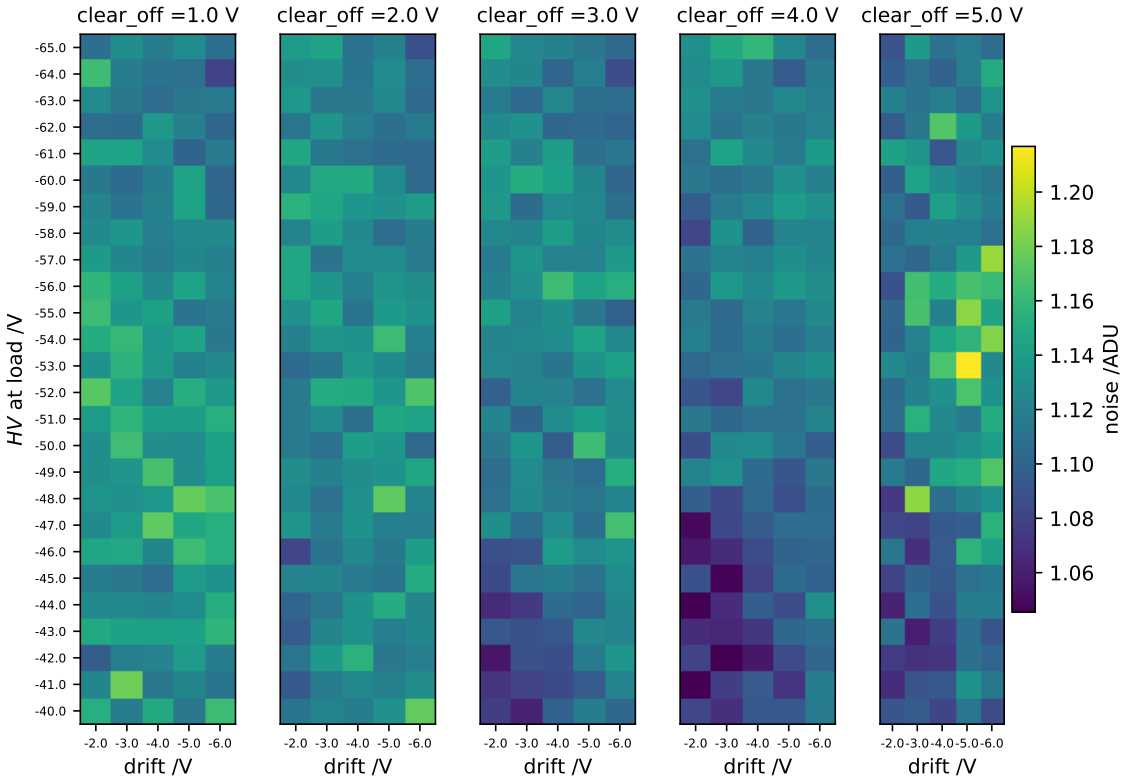


Figure 6.11: Noise values depending on hv (y-axis) and drift voltage (x-axis) for module W60_OF1. The color code indicates the size of the noise. The different plots were taken for different clear-off settings.

of the high voltage current for even more negative hv. The holes of thermal created electron hole pairs drift to the backside. To reach the source contact they have to overcome a small potential barrier. The punch through effect is explained in detail in section 3.1.3.

Drift Voltage

Considering the projection on the drift axis in figure 6.14, different effects are observed. For some combination settings the current rises absolutely for more positive drift voltages. Here the punch through effect between the backside and the drift can be observed, which leads to the strong decrease of the current. The effect is strongest at the largest deviation of drift and hv, because the potential barrier for the hole current can be overcome more easily. For low clear-off values (1 and 2 V) a second effect, that leads to higher currents for more negative drift voltages can be seen. A possible explanation, why this effect can occur is due to the previously discussed back injection effect, where charge flows back into the internal gate instead of being emptied from the clear gate through a punch through.

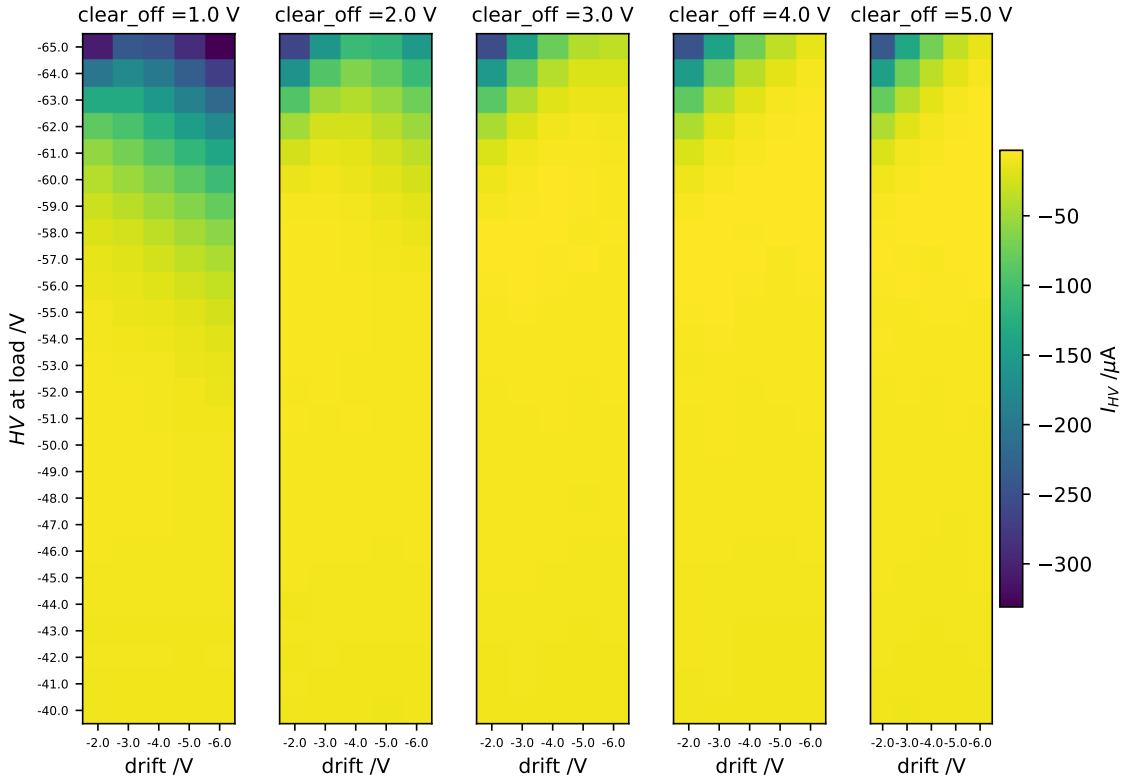


Figure 6.12: The values of the hv current are shown for different biasing settings for module W60_OF1. The values for hv are plotted on the y-axis. On the x-axis the values for the drift voltage are shown. The color code indicates the size of the dark currents, the median pedestals. The different plots were taken for different clear-off settings.

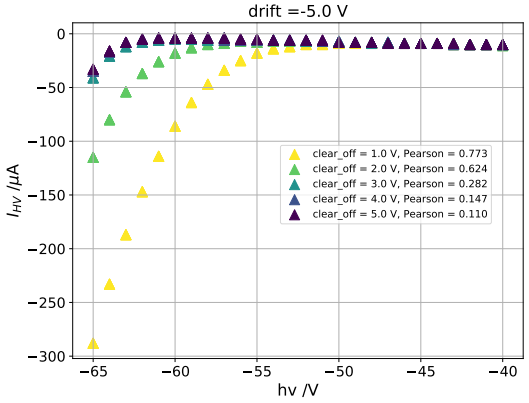


Figure 6.13: Hv current plotted against hv voltage at a constant drift voltage of −5 V for module W60_OF1. The different colors represent different clear-off settings .The Pearson coefficient indicates the linearity of the data points.

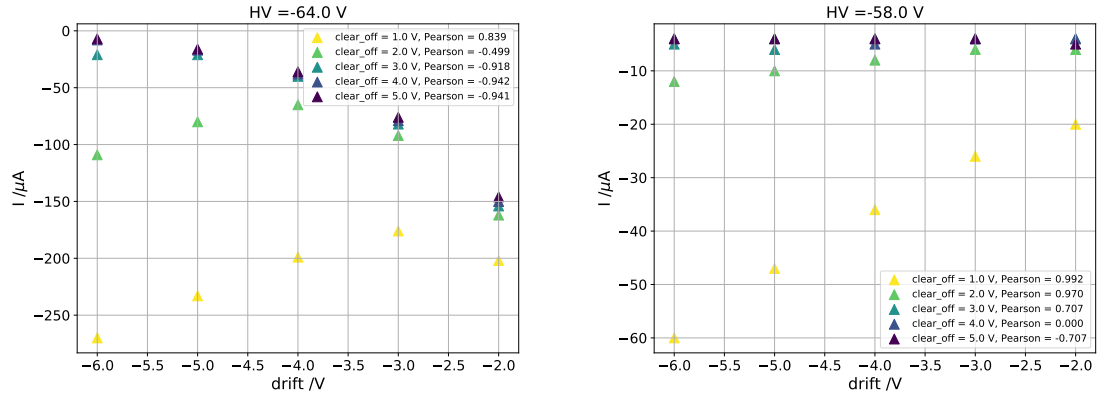


Figure 6.14: Hv current plotted against the drift voltage for two different example settings of hv for module W60_OF1. The different colors represent different drift settings. The Pearson coefficient indicates the linearity of the data points.

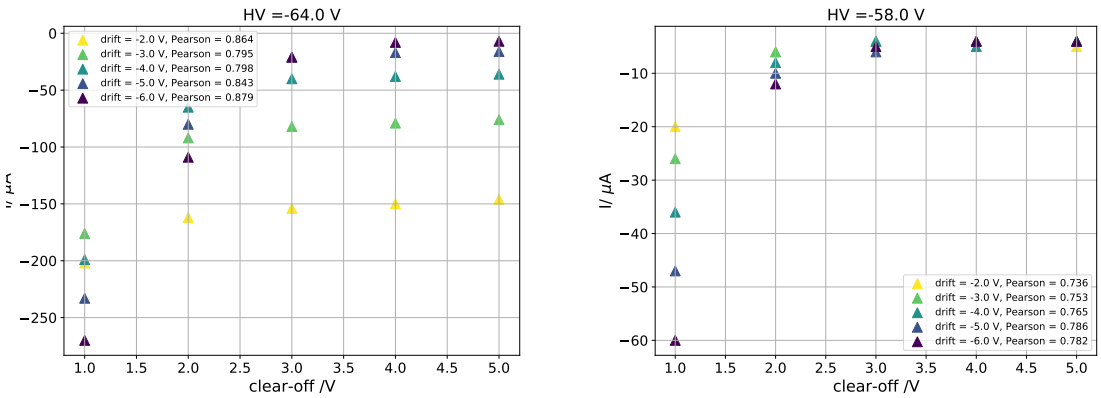


Figure 6.15: Hv current plotted against the clear-off voltage for two different example settings of hv for module W60_OF1. The different colors represent different clear-off settings. The Pearson coefficient indicates the linearity of the data points.

Clear-Off Voltage

Since the clear-off implant is very close to the source implant or punch-through contact in the layout, a similar behavior as for the drift voltage is observed in figure 6.15. Thus, a more negative clear-off voltage leads to a higher bulk current. A voltage drop occurs above a certain threshold, which is caused by the punch-through effect. For hv = −64 V and a constant negative current for more positive clear-off voltages the curve starts saturating. This is the case, because at hv = −64 V a full depletion is present and the bulk current can flow constantly. The additional voltage drop results from the punch through effect. A similar behavior can also be observed when examining the projections for the other modules (listed in section A.1.3), which can be explained by the punch through effect. The similar behavior of the inner modules compared to the outer modules suggests that differences are also caused by the different types of modules.

CHAPTER 7

DCD Gain

Primarily, the DCD is there to amplify and digitize the DEPFET signal (drain currents). Using a calibration of the conversion constants, the so called DCD channel gains, the actual relative drain currents can be determined from the output values (digital values) of each module. Both the dynamic range (input range) and the pedestal spread depend on the DCD gain. The larger the gain, the smaller the dynamic range and the greater is the pedestal spread, because the differences between the individual pixels are amplified more. An exact calibration of the gain is required to evaluate DEPFET parameters like the transconductance and the internal amplification. In addition, the DCD gain affects the energy resolution. At constant noise, the resolution depends linearly on the DCD gain. The measurement and analysis of the DCD transfer characteristics are presented in this chapter. The results of the measurements of six modules are discussed and compared.

7.1 Measurement and Evaluation of ADC transfer curve

The *DCD gain* can be measured for each ADC channel by injecting known currents and recording the corresponding output values. In this case a precision current source built into the DHE is used, which is swept over an adjustable range by the a Field-Programmable Gate Array (FPGA). The current source provided by the DHE is needed to be able to have the most precise resolution on the current as possible (see section 5.2.4). The measurement is executed by the ADC Scan, which is described in detail in section 5.2. The procedure results in a transfer curve for every channel. The DCD channel gain is extracted as the slope of a linear fit to the curve The result of a transfer-curve measurement of an ADC channel is shown in figure 7.1. The transfer curve is measured with a trigger frequency of 1000. The DAC input values of the current source are sampled from 0 to 25 000 DAC. The DCD output is measured in Arbitrary Digital Units (ADU). The fit is performed as a part of the standard ADC scan analysis. A fitting range from 30 to 240 ADU is used. By doing a linear regression of transfer curve data, the slope can be extracted in units of DAC/ADU. To convert the DAC input values into current it has to be converted by a factor f [47].

$$f = 3\,814.33\,\mathrm{pA/DAC}$$

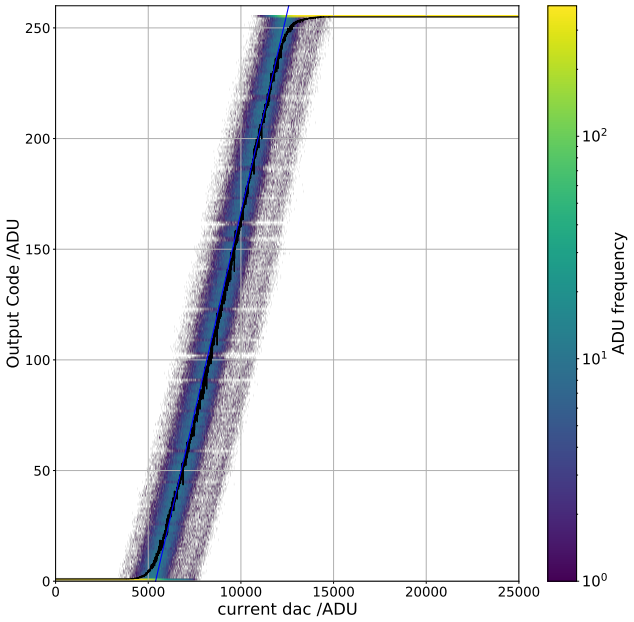


Figure 7.1: Results of an ADC transfer curve measurement with the DHE current source for channel 246 of module W60_OF1. The plot shows a 2D histogram of the DCD output codes on the y-axis as a function of the settings of the DHE current source DAC on the x-axis. The bin size of the x-axis is 5 and corresponds to the step size of the DAC input values. The bin size of the y-axis is 1. The color value corresponds to the number of occurrences.

Thus the DCD channel gain is given by

$$\text{DCD gain} = \text{ADC slope} \cdot \frac{1}{f}. \tag{7.1}$$

In the following the y-axis intercept of the fit is referred to as the DCD channel offset.

7.2 Results of ADC Transfer Curve Measurement

In the following section the parameters extracted from the ADC transfer curve, the ADC gain and the offset are compared and investigated. The distribution of the parameters over the channels of individual DCDs are compared to evaluate the homogeneity. In addition, the parameters are set in relation to the raw pedestals. The aim is to find out which values are mainly dominating the pedestal distribution.

7.2.1 DCD Gains of DCD

The first parameter to be examined is the DCD gain. As explained above, the DCD gain is first compared among the DCD and then set in relation to a pedestal distribution.

percentage deviation ΔADC gain	W56_OB1	W56_OF1	W57_OB1	W57_OF2	W57_IB	W60_OF1	W67_IB
DCD 1	3.07 %	3.98 %	7.70 %	0.98 %	11.74 %	8.45 %	4.38 %
DCD 2	3.53 %	9.45 %	1.41 %	18.22 %	4.23 %	4.70 %	7.09 %
DCD 3	1.30 %	3.30 %	4.31 %	3.19 %	8.32 %	6.11 %	1.35 %
DCD 4	6.42 %	1.08 %	4.83 %	0.19 %	1.37 %	4.83 %	3.71 %
average of DCDs	3.58 %	4.45 %	4.56 %	5.65 %	6.42 %	6.02 %	4.13 %

Table 7.1: The difference of the mean DCD gain to the lower and upper part of the DCDs for different modules are listed. The lower part range is defined from channel (16,0) to (23,7), while the upper part is visible from channel (24,8) to (24,8).

Comparison to all channels

The DCD has 256 channels as already discussed in 3.2.2. Geometrically they are placed on a 16 x 16 matrix. Two 16-channel columns form a double column. For example the DCD column 0 with channel 0 through 15 and column 1 with channel 16 trough 31 form the zeroth double-column. The data of the 32 channels of a double column are sent out to the DHP on a multiplexed 8 bit bus [17]. The gains of all ADC channels of module W60_OF1 are shown in figure 7.2. The plot shows the gain of each channel as a function of its position on its respective DCD. Channel 10 through 15 are not connected to any pixels, because there are only 250 channels per DCD needed to cover all 1000 channels of the PXD9 matrix and appear therefore white. For dead channels no gain can be determined. They also appear white in the plot. The causes are invalid data sets or constant output, which result no transfer curve.

A geometric pattern can be observed in the variation of the gain values. The pixels of the top and bottom halves of the DCDs appear to respond systematically different from each other. Table 7.1 lists the relative difference of the mean DCD gain between the upper and lower half of the respective DCDs of the tested modules. The relative difference is calculated by

$$\text{relative difference} = \frac{\text{mean gain upper region} - \text{mean gain lower region}}{\text{mean gain full DCD}}. \tag{7.2}$$

The DCD Gain deviations of the half DCDs of W60_OF1 are maximal around 8 % in DCD 1. The average deviation of the halves is 6 %. In figure 7.3 the histograms of the upper and lower pixel parts are depicted. Two distribution functions with shifted centers can be seen. The standard deviations for the two distributions for example of DCD 1 give a value of 0.28 ADC/µA for the lower part and 0.21 ADC/µA for the upper part of the gain in the DCD. Further, the standard deviation for all other distributions in the upper and lower parts of the other DCDs show a similar value. The mean value of the standard deviation for all distributions of the DCDs in the upper and lower part is 0.26 ADC/µA. Thus, the ratio of the individual regions are relatively uniform. The relative average deviation of each halves is 0.55 ADC/µA. Therefore a smaller dispersion than the distance to the mean value can be noticed for all distributions. This proves the systematic deviation of the values of all channels from the region of the mean. When comparing the relative difference between the halves of the DCDs with other modules (see table 7.1), it is noticeable that this behavior does not occur within every DCD. For example DCD 4 of module W57_OF2 does not show any visible deviation. Nevertheless, this module also includes a DCD, DCD 2, which has the highest deviation of any investigated module with a value of 18.22 %. All DCD footprints showing the DCD Gain for each module are figured in the appendix A.2.1. The deviations of the DCD halves denote that half of the pixels have a different gain than the

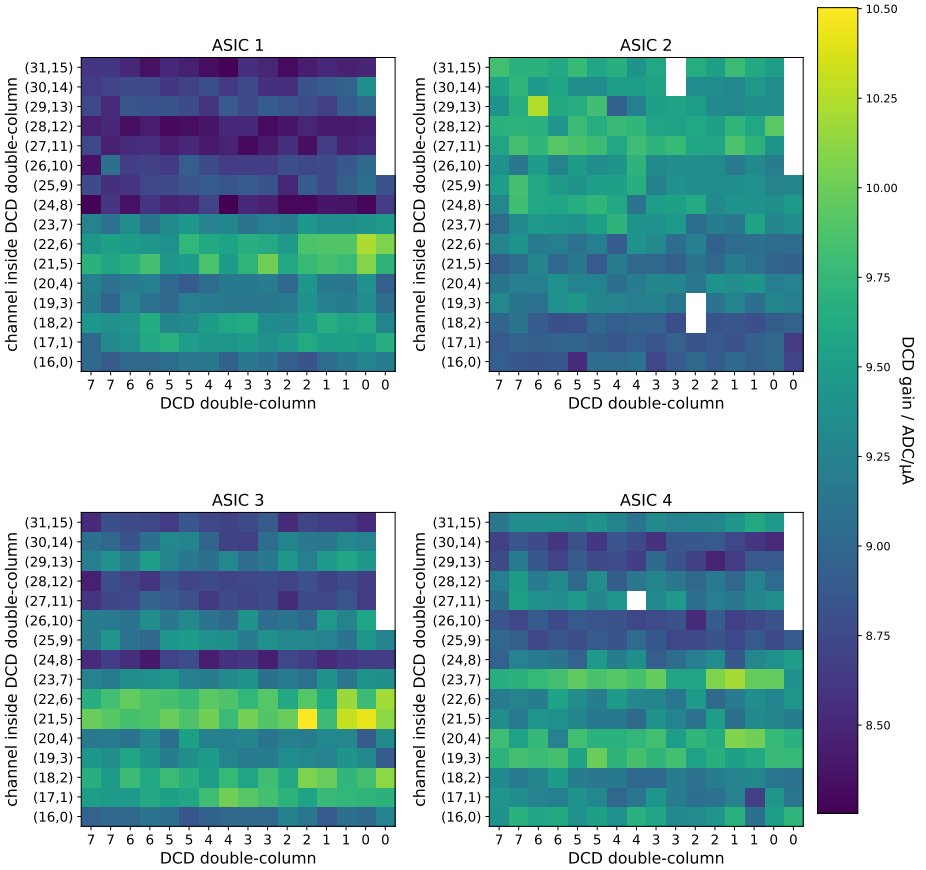


Figure 7.2: Results of the ADC gain measurement of module W60_OF1. The gain of each ADC channel is shown as a function of its position on the DCD footprint. Channel 10 to 15 in double-column 0 are disconnected and therefore marked in white.

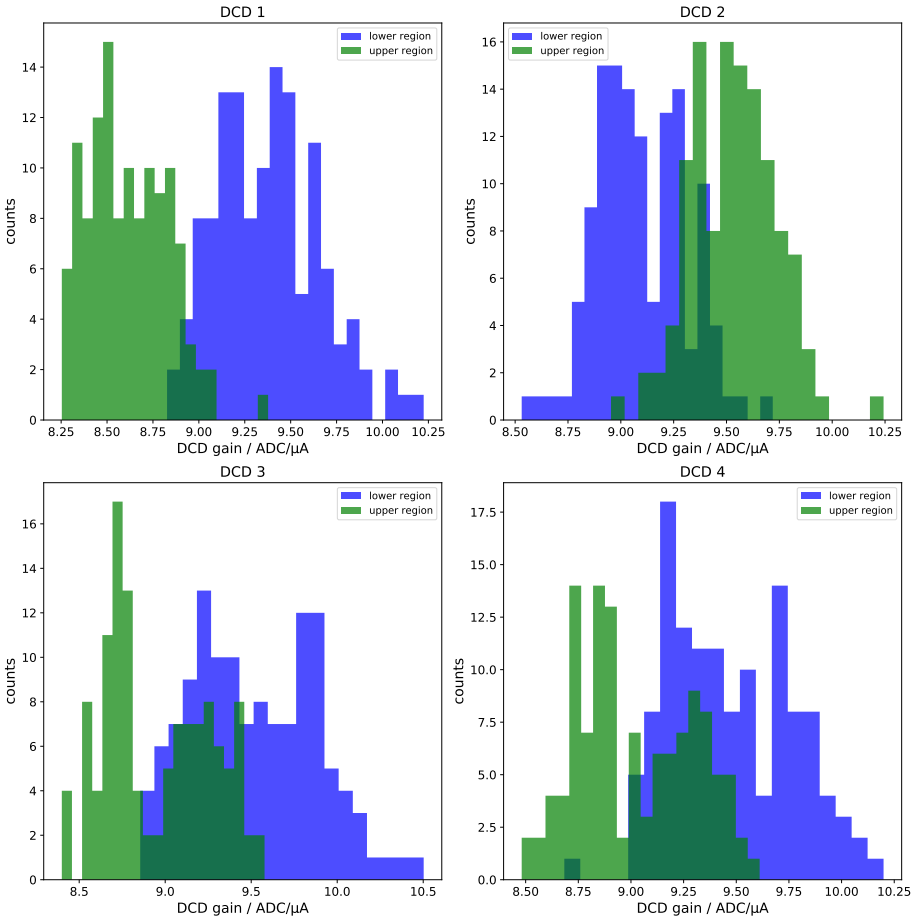


Figure 7.3: Results of the DCD gain measurement of module W60_OF1. The gain of each ADC channel is shown in a histogram in units of ADC/µA. The number of DCD channels is plotted on the y-axis. The green distribution shows the gain of the channels of the upper part of the DCD, while the blue are give the lower part.

other half of the pixels in each DCD. The corresponding pixels are located directly next to each other in the module.

In addition, a four-row pattern occurs. Two rows belong to systematically lower gains and two to systematically higher ones. These structure is four times visible inside the DCD footprint. This pattern appears 4 times within one DCD. The deviation between between lower gain and higher gain inside this four-row pattern deviates less significant in module W60_OF1 than the half DCD effect. The mean average deviation of the mean ADC gain and the lower gain part and and higher gain part gives approximately 4 % (see table A.1 in appendix). Comparing to the other module this effect occurs to varying strengths for different DCDs as already observed in the half DCD pattern. For the module W57_IB, the four row pattern effect with a deviation of 7.61 % is even more concisely visible on average than the half pattern effect with a deviation of 6.42 %. On the whole module W57_OB1 the effect does not occur.

A possible explanation for these visible structures is the way of biasing the chip, where internal voltage drops could arise inside the DCD.

	W56_OB1	W56_OF1	W57_OB1	W57_OF2	W57_IB	W60_OF1	W67_IB
mean DCD gain per Module in ADU/µA	9.51	9.74	9.40	9.66	9.93	9.20	11.17
mean DCD gain per DCD in ADU/µA	9.25/9.76/ 9.89/9.29	9.56/10.76/ 9.41/9.25	9.50/9.19/ 9.71/9.56	9.45/9.99/ 9.69/9.50	10.48/9.30/ 10.33/10.33	9.01/9.31/ 9.25/9.25	11.28/11.17/ 10.88/11.34
IPSource	75/75 85/80	85/85 85/85	85/85 80/85	80/75 80/80	80/90 80/85	95/85 95/90	85/85 85/85
IPSource2	75/80/ 75/85	85/85/ 75/85	85/85/ 85/85	75/85/ 70/75	95/85/ 80/80	95/85/ 95/95	80/80/ 80/80
IFPBias	70/75/ 85/80	80/80/ 80/85	75/75/ 70/75	90/75/ 85/80	90/90/ 80/90	80/90/ 85/90	90/80/ 80/85
IPSourceMiddle	84/80/ 82/82	74/70/ 84/84	76/84/ 76/82	74/82/ 76/82	78/84/ 74/84	84/84/ 82/84	84/82/ 82/82
dcd-refin	725	750	725	750	700	775	700
dcd-amplow	325	375	350	350	200	200	375

Table 7.2: Mean DCD gain with respect to the DCD settings per DCD. The different values for the four DCDs are separated with a slash.

Comparison to DCD Settings

In this section the mean DCD gain for each module is compared with the DCD settings. It is investigated whether the expectation of a high correlation of the DCD settings with the ADC gain is correct. This claim is supported by the expected high dependence of the DCD settings to the total dynamic range of the ADC transfer curve. The optimal DCD settings are determined by the ADC scan for optimal performance (see section 5.2). The mean over all DCD gain values per DCD of one module is taken to observe the mean DCD gain. The results of each module is shown in table 7.2 with respective to the *IPSource*, *IPSource2* and the *IFBPBias* DCD settings and respective voltages. It is noticeable that the DCD gains per DCD but also per module do not differ significantly from each other. By comparing the optimal DCD settings, an influence to the DCD gain cannot be excluded, as these also do not vary significantly. Modules W57_IB and W60_OF1 have slight higher DCD-settings in comparison to the rest. However, a correlation cannot be confirmed, since even more statistics with deviating DCD settings would be needed .

DCD Gain vs. Pedestals

The purpose of setting the DCD gain in relation to pedestals is to find out which parameter dominates the pedestal distribution. To investigate the correlation of the DCD gains and the raw pedestals, a pedestal measurement needs to be performed. When taking a pedestal frame a pedestal distribution for each pixel is taken depending on the frame number. The pedestal frame number used for this measurement is equal to 1000. A the pedestal distribution is called raw when no ACMC and no offsets are applied. More details on the measurement procedure, pedestal scan, can be found in section 5.1. The measurement for all pixels are shown in 7.4. Here the distribution of each DCDs are plotted in a histogram. Furthermore the pedestal values of each pixels are depicted inside the geometrical matrix of the module.

Since several frames have been taken, we get several pedestal data per pixel. To correlate the pedestals to the ADC gain the pedestals per channel need to be calculated. Therefore we first take the median of the pedestal distribution of each pixel. Then the median over the pixels per a channel has to be taken. The correlation plots for each DCD are shown in 7.5. The Spearman correlation coefficient, stated above each plot, gives a quantity on the monotonicity of the data sets as described in section 3.5.2. In this case the Spearman correlation and not Pearson correlation is used because it is

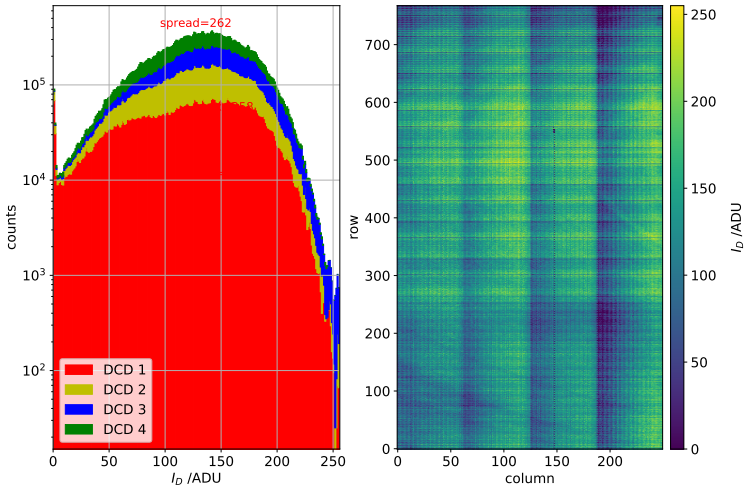


Figure 7.4: Pedestals distribution used for correlation in module W60_OF1. This distribution is called raw, because no Offset and no ACMC is applied. The Measurement was done with frame number 1000.

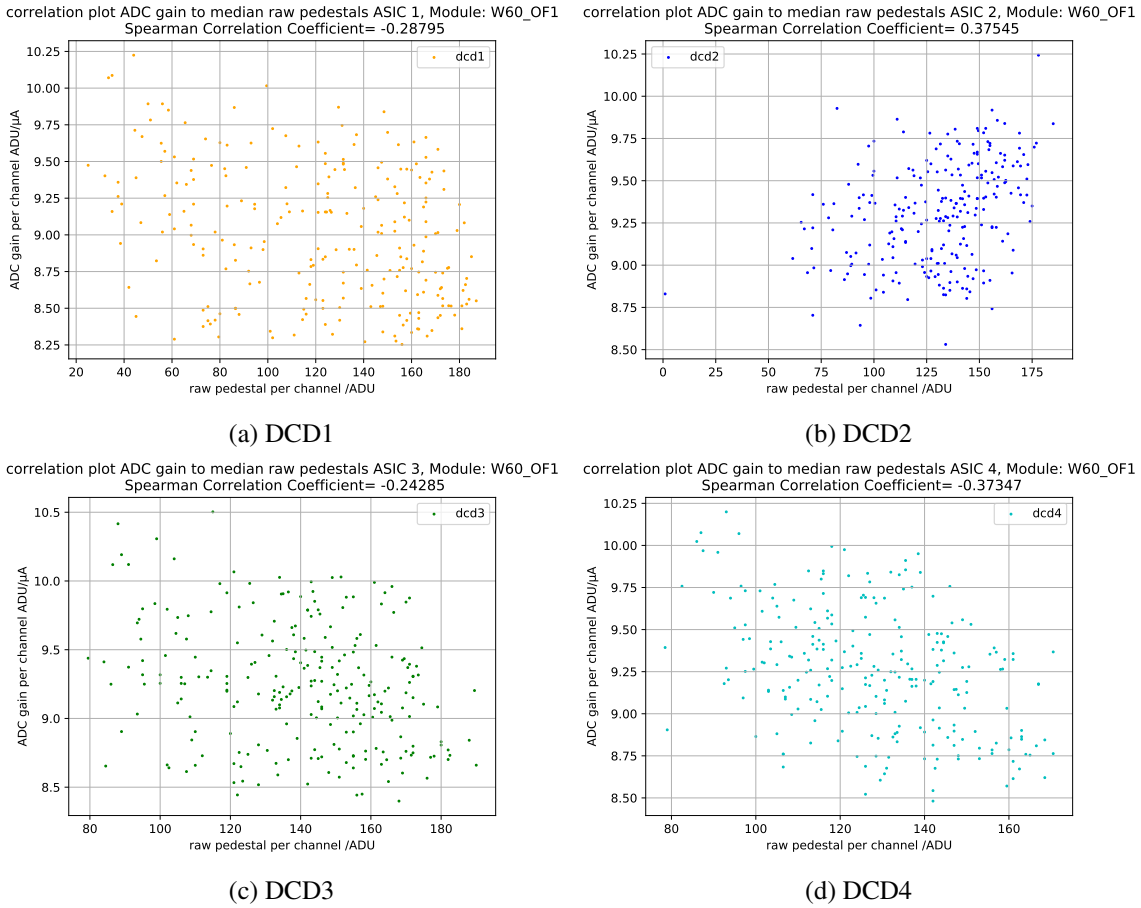
not known whether it is a linear relationship. By checking the Spearman correlation coefficient for all DCDs a monotonic correlation can't be determined. DCD 1, 3 and 4 seem to have a slight tendency into negative correlation with value from −0.24 to −0.37. Anyhow due to the different behavior of DCD 2 with a value of 0.37 and due to the very low values of the correlation coefficient with a mean coefficient of -0.13 for all DCDs there is no correlation between the ADC gain and the median raw pedestals assumed. This observation is also made on all other examined modules (see appendix A.2.1). Only in module W57_IB a stronger correlation for negative monotonicity for each DCD can be found. Since all DCDs behave differently and overall no large coefficients are observed, it can be assumed that the pedestal distribution is only partly dominated by the DCD gain.

7.2.2 Offsets of DCD

Now the second parameter extracted from the ADC transfer curve above will be examined in more detail. The offsets within the geometric structure of the DCD are compared first and the correlation to the pedestals is investigated.

Comparison to all channels

When plotting the DCD channel offsets as a function of their respective geometrical positions on the DCD footprint no significant row pattern is visible (shown in figure 7.6). Indeed the two parts of the DCD are again apparent. In addition to that, a gradient from absolute lower to higher offsets from left to right is noticeable in all DCDs. The offsets correlate linearly to the pedestals (discussed below). Due to variations in the production, as for example in homogeneous doping it is assumed that each pixel behaves differently. The left-to-right gradients across individual DCDs visible inside the channels are appearing most likely due voltage drops across the module. Another possibility are



(a) DCD1

(b) DCD2

(c) DCD3

(d) DCD4

Figure 7.5: Correlation plot of median raw pedestals against ADC gain. The Spearman Correlation gives Coefficient gives a quantity of how monotonic the data set behaves. The measurements are done for module W60_OF1.

cooling issues of the DCDs. A temperature measurement of each DHP can rough estimated at the mass testing setup in Bonn. When comparing the temperature with the mean offset of the DCD there is no dependency for all modules is apparent. On the other hand a gradient in temperature already was investigated before [13]. Therefore the determined proportionality of each DCD offset to the temperature could be possible. Obviously this does not directly explain the gradient in each DCD. Thus it would be interesting to measure the temperature more precisely along one DCD in future observations.

Offsets vs. Pedestals

Next, the correlation of the offsets to the pedestals is studied. For this purpose, the same raw pedestal distribution is used as for the comparison to the DCD gain (see figure 7.4). The median pedestals are calculated for each channel.

In figure 7.7 the Pearson Correlation Coefficient is sated above each plot. More information on both correlation coefficients are described in section 3.5.1. When checking the Pearson Correlation

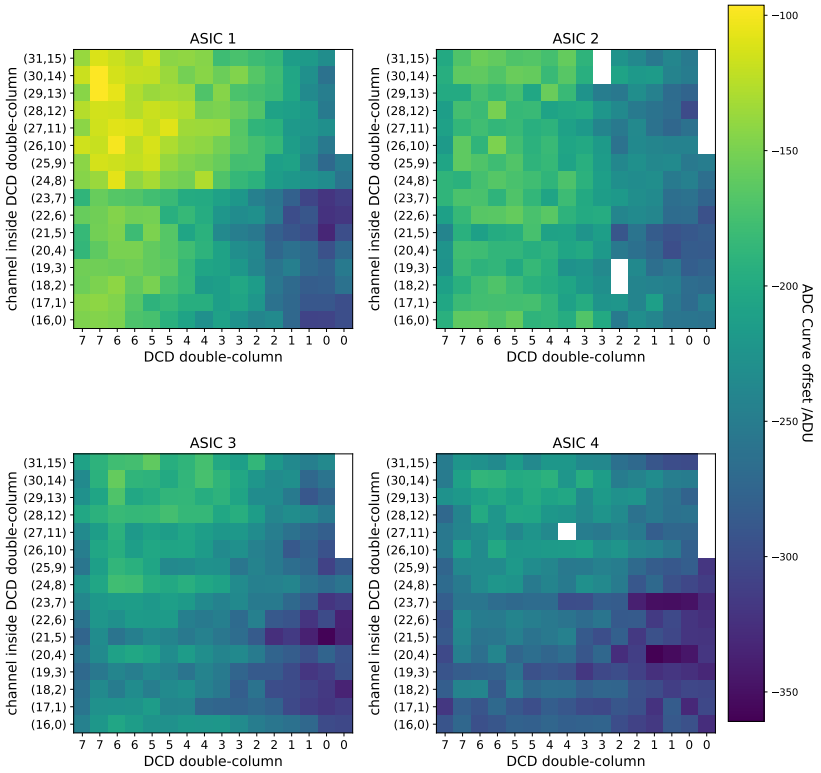
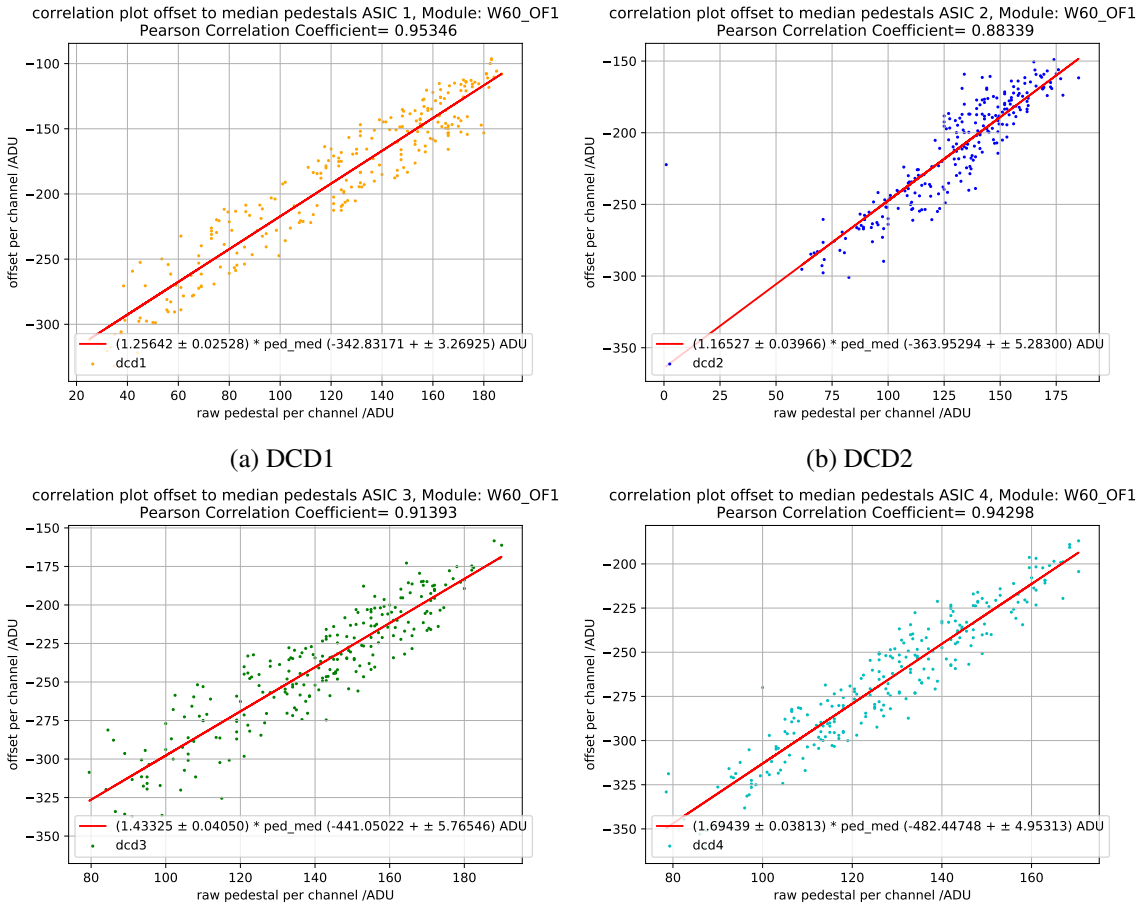


Figure 7.6: The Offset of the transfer curve is defined as the y interception of the fit of the ADC transfer curve. It is again plotted inside the geometrical footprint of the DCD for module W60_OF1. Channel 10 to 15 in double-column 0 are disconnected and therefore marked in white.

Coefficient a strong linearity can be determined. As 0 gives no correlation a value of around 0.9 for all DCDs state a strong positive linear relation. The deviations from the linearity are most likely arising due to the median calculations to be able to correlate. One channel encloses 192 pixels, which all behave differently with different pedestals as stated already in the last section. The correlation coefficients of the other modules confirm the observation of a linear relationship, demonstrated in section A.2.2. The pedestals are defined than the sum of he current evoked by the external gate, without the internal gate is filled. When applying the DHE source current to each channel, the signal current is rising on top, while the pedestal current stays the same in the ideal case. The same behavior is apparent for the offsets. Consequently, the expectations of a proportionality between the offset and the raw pedestals can be confirmed.



(a) DCD1

(b) DCD2

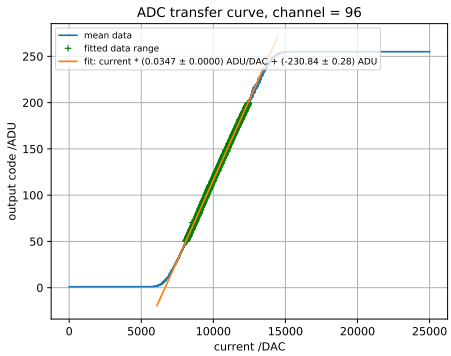
(c) DCD3

(d) DCD4

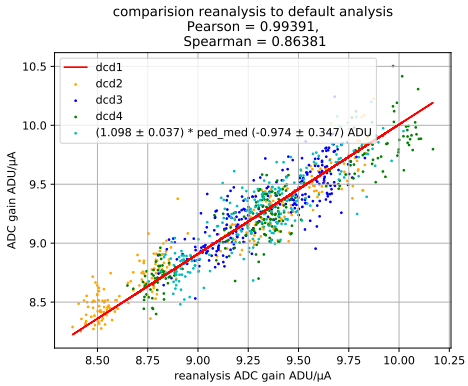
Figure 7.7: Correlation plots of median raw pedestals against offsets of ADC transfer curve are shown. The Pearson Correlation Coefficient gives a quantity of how linear the data set behaves. The measurements are done for module W60_OF1.

7.3 Reanalysis of ADC Gain

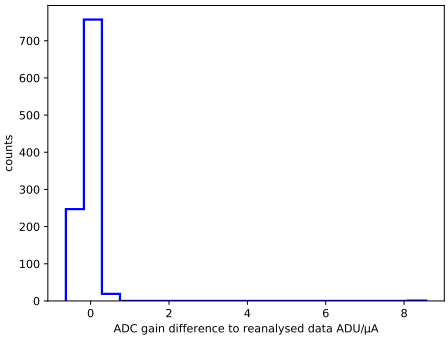
For reasons of quality checking for the ADC Gain extraction, the raw data set of the ADC Scan (section 5.2) was taken and the linear regression of the ADC transfer slope was reanalyzed. To receive a high quality linear fit a cut on the data was applied. Thus the range from 50 to 200 ADU of the output code was used for the linear regression. The analysis generated by the default PXD analysis uses a fitting range from 30 to 240 ADU. Both methods were executed executed with the polynomial function provided by python numpy. An example of the ADC curve of one channel is shown in figure 7.8(a). Comparing the mean chi square value for all channels of both methods, it is deviating. The reduced mean chi squared for example of module W60_OF1 for the default method implemented inside the PXD lab framework sates approximately a 50 % higher value than the reanalysis yield. Anyhow the reanalysis does not take the noise into account. As shown in figure 7.8(b) both methods give very similar results for the ADC gain. The Pearson Correlation Coefficient with 0.99 accentuates this assumption. In additionally, the absolute difference of the two DCD gains from both methods can be calculated. The results are shown in a histogram in figure 7.8(c). The majority of the data do not differ. Therefore the reanalysis of the ADC scan data gives an approval of the so far done default analysis provided by the PXD9 default analysis.



(a) Reanalysis of ADC transfer slope of channel 96, module W60_OF1, in blue. In orange the data is marked, which is used for the linear regression. The range is set from 50 ADU to 200 ADU.



(b) Comparison of default analysis and reanalysis of ADC gain for all DCDs. The Spearman Coefficient gives a quantity of 0.864. In addition a linear regression was made depicted in red.



(c) Absolute difference of default analysis and reanalysis of ADC gain for all DCDs.

Figure 7.8: Reanalysis of ADC Gain. Left plot shows example on how reanalysis was made. Right plot shows Comparison to default analysis.

CHAPTER 8

Transconductance and Internal Amplification

In this chapter, the transconductance of the DEPFET Pixels are determined, which can be calculated from the ratio of the drain current to the applied voltage. In addition, the internal amplification of the DEPFET Pixels are extracted. It is defined as the signal current per electron. Both values are compared per pixel to determine the homogeneity of the DEPFET matrix. A systematic alteration of the transconductance or the internal amplification over the matrix could lead to different signal currents between the pixels within the same event and therefore to a misinterpretation of the charge spectra of all pixels. Both parameters are correlated and the oxide capacity is determined.

8.1 Transconductance

First, the transconductance is discussed in this section. The measurement and extraction of transconductance, the results and conclusions are presented.

8.1.1 Measurement and Analysis of Transconductance

The measurement for extracting the transconductance is performed by measuring the drain current I_D of each pixel by sweeping the gate-on voltage V_G. To achieve a higher dynamic range, the drain current is recorded with different *VNSubIn*-settings. Thus the median of the data with different *VNSubIn*-settings (shown in figure 5.5(b)) is taken. The measurement procedure is presented in detail in section 5.3.

As stated before in equation 3.4, the transconductance is defined as the ratio between the change in drain current and the gate-on voltage:

$$g_m = \frac{\partial I_D}{\partial V_G}. \tag{8.1}$$

Therefore a linear regression is performed on the data set. It is applied on the output code exceeding 60 ADU for each pixel inside the DEPFET Matrix to receive the most precise result. Due to the definition of drain current, a quadratic relationship is observed at more positive gate-on voltages. The lower the gate-on voltage, the more likely it is to observe experimentally a linear relationship. Therefore the limit is set to process linear correlated data points. At the same time it should not be set too high to have enough statistics for a linear regression.

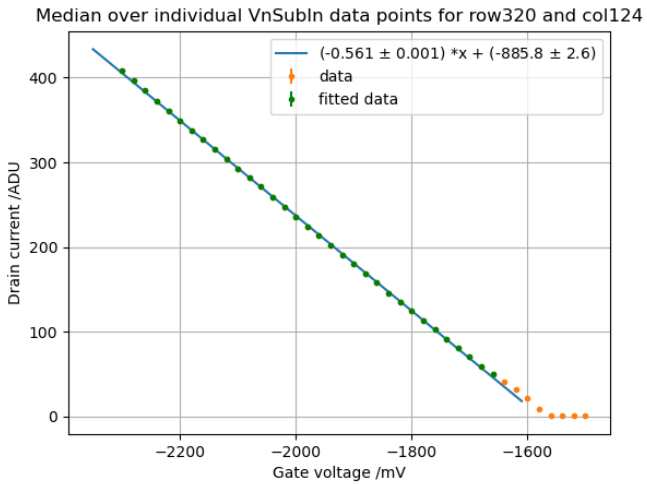


Figure 8.1: Example DEPFET IV curve for median VNSubIn settings for pixel in row 320 and column 124 for module W60_OF1. The drain current is plotted against the gate on voltage. The linear regression plot (blue) is applied on a particular data set, which is marked in green. The data marked in orange does not have any impact on the linear regression curve.

The transconductance is obtained from the slope of the linear regression curve. An example curve of one pixel is shown in figure 8.1. In figure 8.2 the transconductance g_m is depicted for each pixel in units of ADU/mV inside the PXD9 matrix. The white dotted line is associated with the four dead drain lines of module W60_OF1. The values of the transconductance in each pixels are displayed in a 1D histogram. They are evenly distributed and form a Gaussian distribution with a standard deviation of 43.5 ADU/V. The median value of the transconductance for the module W60_OF1 equals $g_m = -592.26\,\mathrm{ADU/V}$. As the output of each transconductance still depends on the output code measured in arbitrary digital units ADU, the transconductance is called correlated here. A correction of the transconductance is necessary here, because the transconductance spread in the histogram is smaller than the spread of the DCD gain as discussed in chapter 7. In the pixel representation of the transconductance, a certain recurring pattern is noticeable. In an interval of 2x2 pixels, the values of the transconductance alternates systematically between high and low values. Nevertheless, no statement can be made about the origin of this structure, because it could also be affected by the characteristic properties of the ADC, the DCD gain.

Therefore, the uncorrelated transconductance $g_m^{\text{non-corr}}$ needs to be calculated. This can be computed by taking the varying influence of the DCD gain, into account:

$$g_m^{\text{non-corr}} = \frac{g_m^{\text{corr}}}{\text{DCD gain}} \tag{8.2}$$

The calculation is done for each pixel.

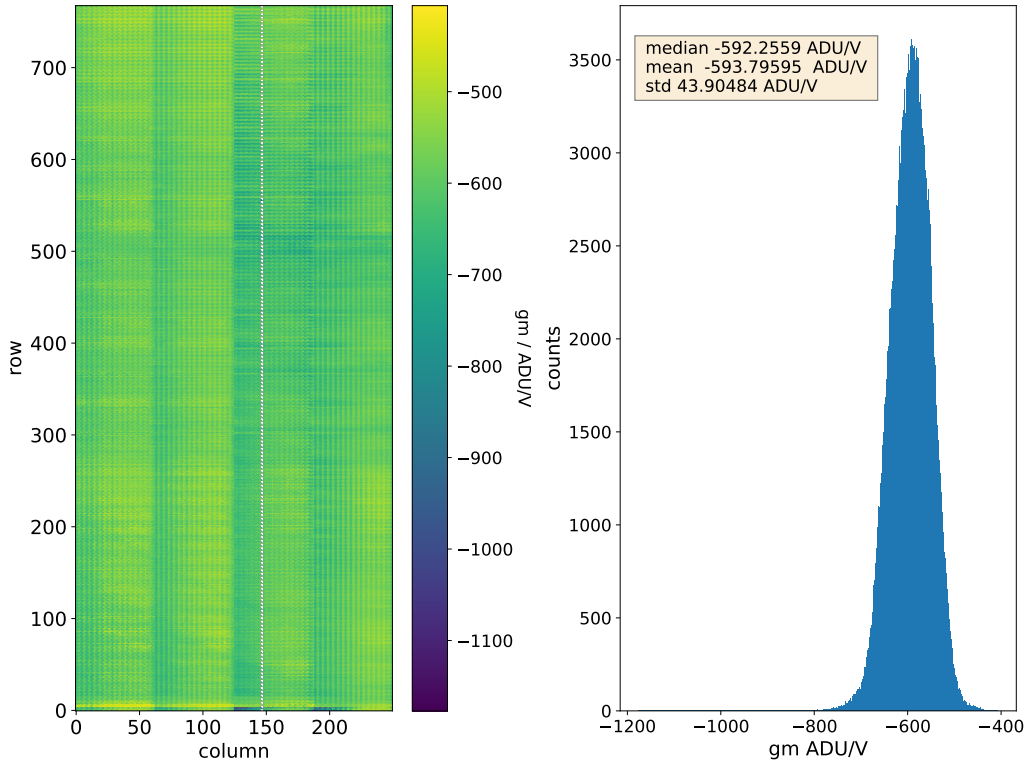
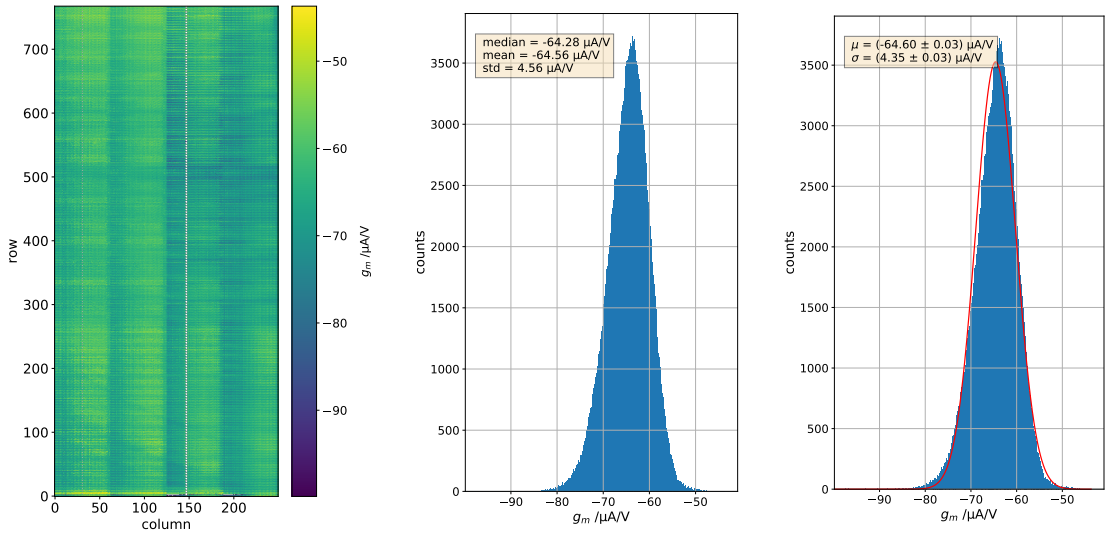


Figure 8.2: The values of the correlated transconductance for each pixels are shown for module W60_OF1. In the left plot the values are distributed in the PXD9 matrix of the module. The transconductance is depicted for each channel via the color code on its geometrical position inside the DEPFET matrix. On the right a histogram with the values for each pixel is filled. The median value gives $-592.26\,\mathrm{ADU/V}$.

8.1.2 Results

In the following, the results of the transconductance are discussed. The transconductance is considered in relation to all pixels to check the homogeneity of the matrix. A comparison of the uncorrelated transconductance among the pixels will be made. The results for each pixel are shown in figure 8.3. As before, the value of the transconductance is shown in dependence on its geometrical position on the pixel matrix. In addition, the 1D histogram shows the distribution of the values for the transconductance.

In an ideal case, the matrix would depict the same transconductance for every pixel. In reality every pixel behaves differently even taking the different characteristics of each ADC into account. Inside the matrix, several structures are noticeable (see figure 8.4.) In the following, the occurrence of the visible patterns are investigated on several modules. The dependence on the DCD gain is examined. This is necessary to exclude possible further influence. The impact of the transconductance on the pedestals is investigated. Finally, different pixel types are studied according to the charge spectrum of a radioactive ^{109}Cd source.



(a) The transconductance is depicted for each channel via the color code on its geometrical position.

(b) The incidence of the values for each pixel is plotted. The median value gives $-64.3\,\mu A/V$.

(c) The incidence of the values for each pixel is plotted. A Gaussian distribution is fitted.

Figure 8.3: The values of the uncorrelated transconductance for each pixels are shown for module W60_OF1. The values are distributed in the PXD9 matrix of the module.

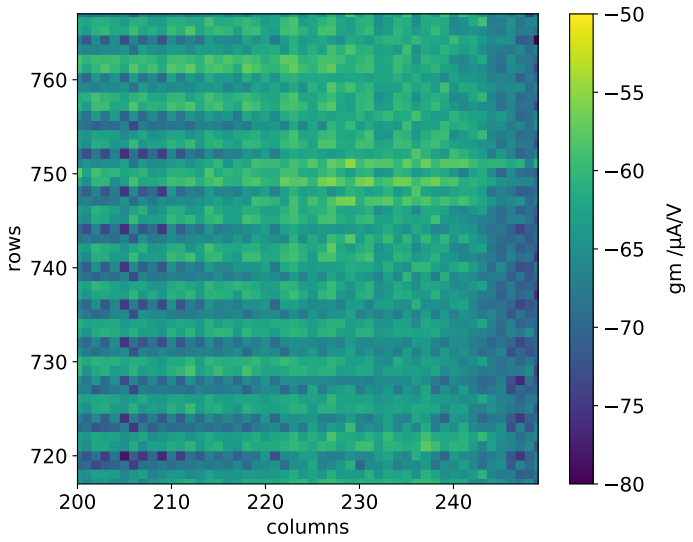


Figure 8.4: Zoom of the values of the uncorrelated transconductance for each pixels for module W60_OF1. The transconductance is depicted for each channel via the color code on its geometrical position inside the DEPFET matrix.

	W56_OB1	W56_OF1	W57_OB1	W57_OF2	W57_IB	W60_OF1	W67_IB
g_m/µA/V	−72.8	−73.4	−61.7	−65.9	−65.6	−64.3	−46.0
std (g_m)/µA/V	11.8	11.1	22.1	4.8	6.2	4.6	6.6

Table 8.1: The calculated uncorrelated transconductance for each module, extracted out of the measurement of the drain current in dependence on the gate-on voltage. The characteristic of each ADC, the DCD gain, is taken into account.

Comparison to other Modules

To compare the values of the transconductance the median values are taken. No Gaussian mean is used, as the distribution is not fully Gaussian as depicted in 8.3(c). The median value takes the shift of the distribution into account (arising due to recurring structures described below). The median value for the transconductance for the whole matrix of module W60_OF1 gives −64.3 µA/V. The remaining transconductance per pixel plots for the other modules are listed in the appendix in section A.3.1. In all modules recurring structures inside the pixel matrix are occurring. When comparing the median transconductance of every module (see table 8.1) there is no clear correlation to the module type and therefore the layout of the module visible.

In the production process each module is manufactured on a special SOI silicon wafer [48]. The module number corresponds to the wafer it is produced on. Due to the roughly similar values of modules produced from the same wafers, a correlation to the production process on each wafer could be assumed. If the thickness of the oxide layer differs minimally between the wafers, this could lead to different oxide capacities. The transconductance depends directly on the oxide capacitance. Different capacities could be a possible reason why the values differ between the wafers. Another possibility are effectively different resistivity of the bulk or the implants, which can also lead to differing values. For reliable conclusion more statistics and investigations are needed.

The deviating transconductance of the W67_IB module is particularly notable. So far, there is no certain explanation why this module behaves significantly different (31.6 % with respect to the other modules). One possibility is that the FET voltage threshold on this module is much lower. In future studies it would be very interesting to compare the FET voltage threshold with the transconductance value.

Validation Measurement

For validation of the measurement methodology and calculation of the transconductance, another measurement is performed. The transconductance is determined by sweeping the gate-on voltage and measuring the drain current. This time, however, the current is read directly from the power supply at the source line. The slope then gives the transconductance over all drain lines. The result of the validation measurement for module W67_IB is shown in figure 8.5. A linear relation between the gate on voltage and the drain current is observed. Compared to the previous measurement in figure 8.1, the current measurement is not limited by the ADC dynamic range and can be measured throughout the full range. Due to the low resolution of the power supply the transconductance can only be roughly estimated. Applying this methodology, yields a transconductance of −50 mA/V. Since a measurement over the whole module is made, the value must be divided by the number of connected drain lines (1000) to compare the value to the results of the first methodology, where the transconductance is

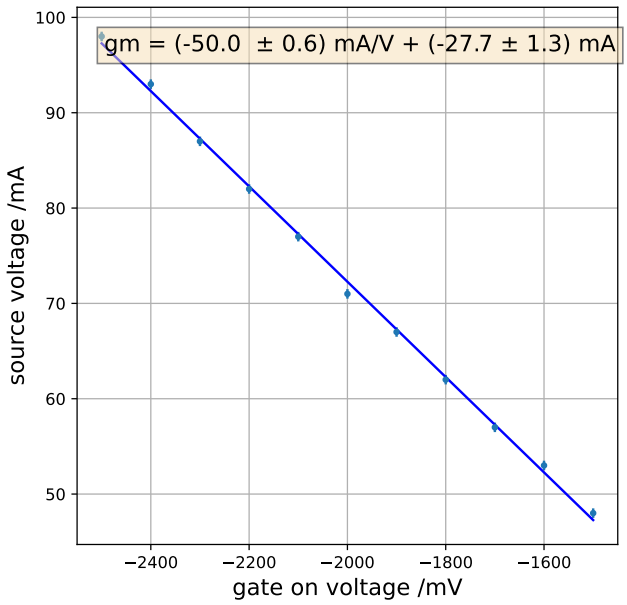


Figure 8.5: Validation measurement of transconductance for module W67_IB. The current was measured directly at the power supply. The resulting transconductance for all drain lines is $-50.0\,\mathrm{mA/V} \pm 0.6\,\mathrm{mA/V}$.

derived per pixel. Four pixels share one drain line as discussed in section 3.1.2. Thus, the pixels of one drain line all share approximately the same value of transconductance. Using the previous evaluation a mean value of $-46.75\,\mu\mathrm{A/V}$ with a standard deviation of $6.6\,\mu\mathrm{A/V}$ was obtained for the module W67_IB. Comparing that value with the result of the validation with $-50.0\,\mu\mathrm{A/V} \pm 0.6\,\mu\mathrm{A/V}$ shows, that the error range does not cover the value of the two variables in each case. Nevertheless the values are in same order of magnitude with a deviation of 6.5 % and are only a rough estimation for every pixel measurement. Thus, the measurement methodology is roughly validated.

DCD Impact

In this section, the influence of DCD gain despite the weighting calculations on transconductance value is investigated. A gradient of the transconductance of each DCD from left to right is observed, which is visible in the projection of the transconductance values onto the column axis which shows a “saw-tooth” pattern (see figure 8.7). This characteristic pattern is also visible in other modules (see section A.3.2). Despite consideration of the DCD gain, the remaining influence of the ADC characteristics on the transconductance is examined. The DCD gain is plotted against the uncorrelated transconductance. Since the DCD gain is extracted channel-wise, the value of the transconductance must be applied per channel. The median value is calculated over the pixels of each channel. The results are depicted in figure 8.6. The Spearman Correlation Coefficient (see section 3.5.2) is stated above each plot, which indicates the strength of the correlation between two data sets. The closer the value is to one it states a higher monotony. A value of 0 states no correlation. In this case, the Spearman Correlation Coefficient and not the Pearson Correlation Coefficient is used, since a

	W56_OB1	W56_OF1	W57_OB1	W57_OF2	W57_IB	W67_IB	W60_OF1
DCD1	0.45	0.83	0.12	0.82	0.48	0.41	0.36
DCD2	0.39	0.59	-0.01	0.59	0.82	0.09	0.40
DCD3	0.69	0.67	-0.12	0.52	0.73	0.60	0.26
DCD4	0.59	0.59	0.56	0.66	0.91	0.27	0.21

Table 8.2: Spearman Correlation Coefficients on Correlation of transconductance and DCD gain.

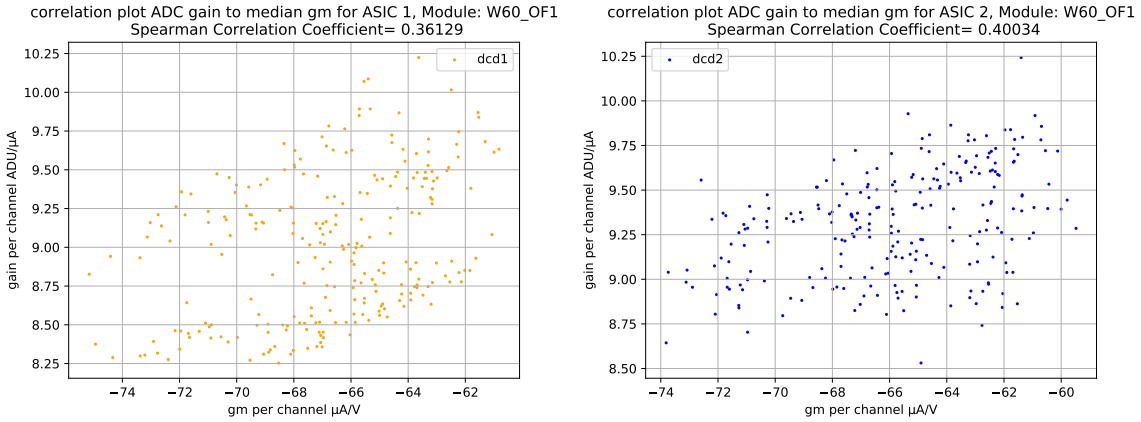
	W56_OB1	W56_OF1	W57_OB1	W57_OF2	W57_IB	W67_IB	W60_OF1
DCD1	−0.08	0.33	−0.51	0.12	−0.29	0.13	0.72
DCD2	−0.45	0.09	−0.66	0.33	−0.48	0.37	0.39
DCD3	−0.05	−0.11	−0.67	0.21	−0.63	0.15	0.24
DCD4	0.17	−0.42	−0.68	0.05	−0.73	0.15	0.01

Table 8.3: Spearman Correlation Coefficients on Correlation of transconductance and raw pedestal values.

linear correlation is presumably not expected due to the weighting process of the transconductance. The Correlation Coefficients state a weak to moderate monotonic relation between the two data sets. Comparing to the other modules (see tabular 8.2), it is noticeable that all of them show a similar or even stronger monotony except of module W57_OB1. This means that, despite the weighting calculation, the characteristics of the DCD still have an influence on the transconductance. Therefore, the visible gradients in the projection plot on the column (figure 8.7) are characteristics for each DCD. They cannot be explained with a matrix effect. Depending on where the voltage supply is applied to the DCD, there are presumably voltage drops of the applied drain current arising. This has a direct influence on the transconductance, as shown in equation 3.4.

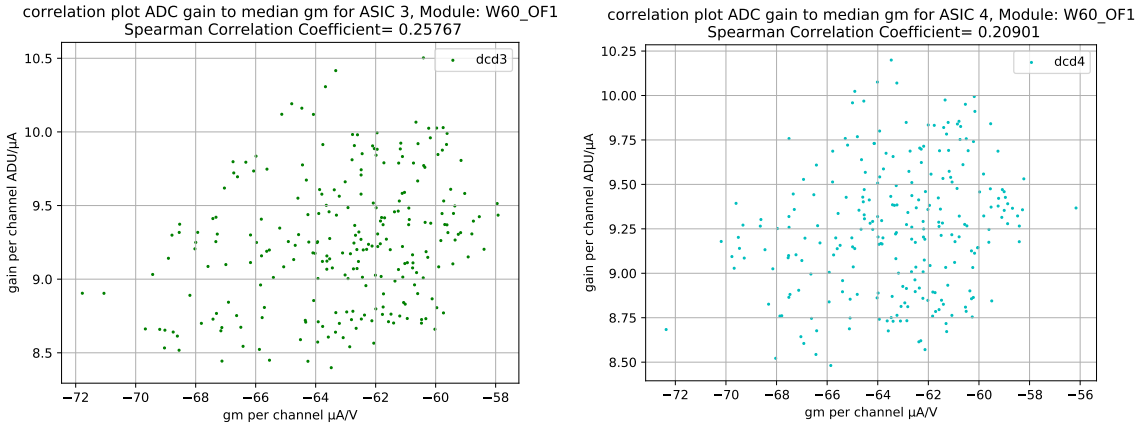
Pedestal Impact

Looking at the projection on the row-axis (see figure 8.7 right), a systematic structure is observed, in which a drop of the transconductance values between row 256 and 512 in the middle of the matrix is visible. It is noticeable that the smaller pixels, i.e. those in the rows from 0 to 256, behave differently than the larger pixels. The negative gradient follows up to row 512, followed by a positive gradient up to the end of the module row 768. This behavior could occur due to a gate-on voltage drop across the matrix. To support this assumption, a pedestal measurement (see section 5.1) is taken. To ensure that the pedestals are not influenced by anything else, a raw pedestal measurement is performed. This means that no ACMC and no offset is applied (see section 5). The number of the frames taken is 1000, which leads to 1000 data points taken per pixel. The measurement results where already used in chapter 7.2 and can be seen in figure 7.4. When observing the distribution of pedestal values along the matrix approximately the same behavior, as visible in the transconductance, can be seen. Thus, lower pedestal values are visible for smaller pixels up to row 256, followed by a rise to higher values up to row 512 and resulting in a negative gradient up to row 768. The theory of a voltage drop along the matrix is therefore supported, since a similar behavior can be seen in the pedestal matrix. However, in order to make a reliable statement about the origin of the gradients, a test measurement would have to be carried out. This particular gradient behavior on the row axes is not always equivalent for other modules. For almost all modules, a difference between the small and large pixel area can be seen.



(a) DCD1

(b) DCD2



(c) DCD3

(d) DCD4

Figure 8.6: The transconductance extracted out of the DEPFET IV Scan vs. the ADC Gain out of the ADC Transfer curves for module W60_OF1. The Spearman Correlation Coefficient gives a quantity on how monotonic the two data sets are.

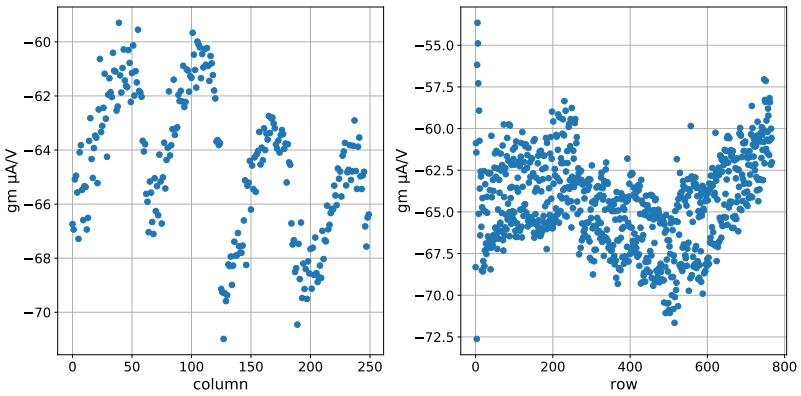
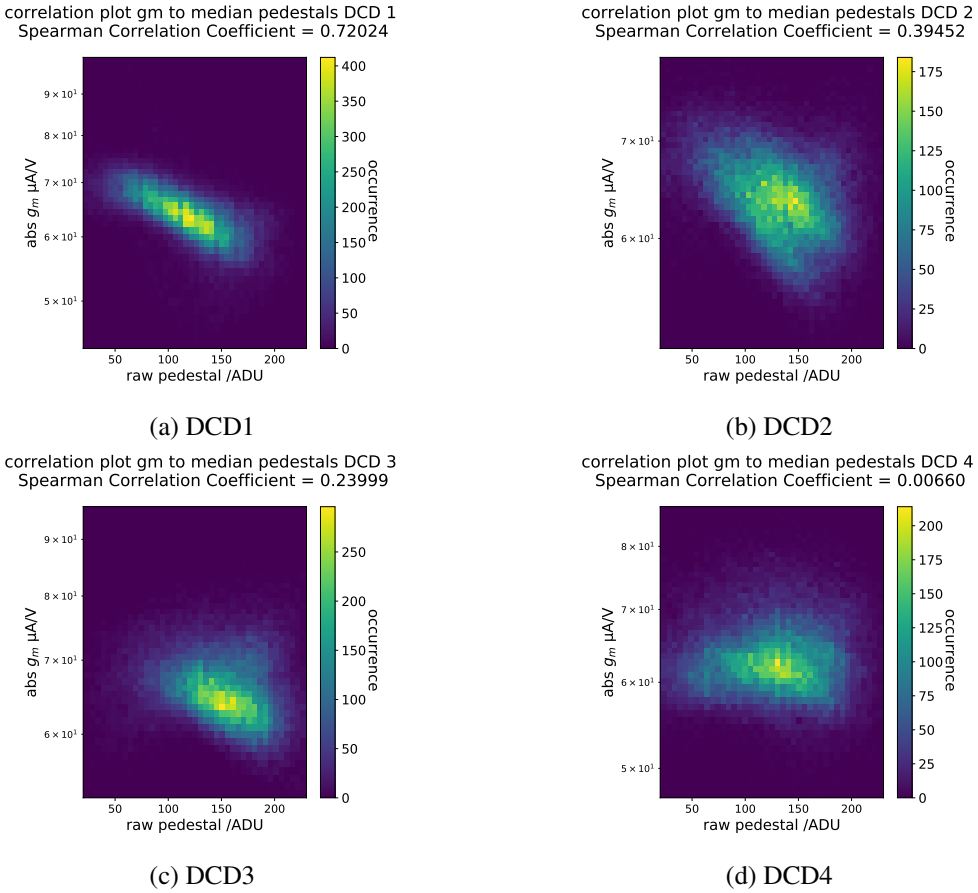


Figure 8.7: Projection of values of the transconductance along the column and the row axes for module W60_OF1.



(a) DCD1

(b) DCD2

(c) DCD3

(d) DCD4

Figure 8.8: The transconductance extracted out of the DEPFET IV Scan vs. the raw Pedestal values per pixel for module W60_OF1. The right plot shows the occurrence of the correlation values. The pedestal distribution is measured without applied ACMC and Offsets. The Spearman Correlation Coefficient gives a quantity on how monotonic the two data sets are.

To correlate the pedestals pixel by pixel with the transconductance, the median is taken over each frame per pixel. The results are shown in figure 8.8 per DCD, where number of occurrence of the distribution of the data points can be examined. As explained before, the Spearman Correlation Coefficient indicates the monotonicity of two data sets.

For the module W60_OF1 with values of a weak positive monotonicity for DCD 1, 2 and 3 can be found with a Spearman Coefficient range of 0.24 for DCD 3 to values indicating strong monotonicity of 0.72 for DCD 1. Nevertheless, DCD 4, does not show any correlation. However, if one compares the results of module W60_OF1 with the other modules (see tabular 8.3 and appendix A.3.4), it becomes apparent that there is no uniform behavior between the transconductance and the pedestals visible. For example, a moderate negative correlation is evident for module W57_OB1 with a Spearman correlation coefficient of -0.51 to -0.68. Module W57_OF2 shows almost no correlation between the two data sets being compared. Accordingly, the pedestal distribution is dominating the transconductance for some modules. Due to the proportionality to the drain current of the transconductance (see equation 3.4), the transconductance is expected to dominate the pedestal distribution. Anyhow, the pedestals

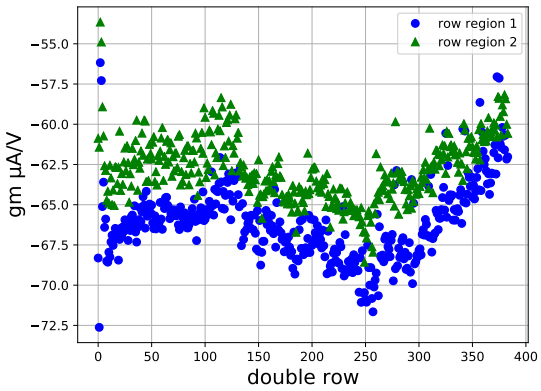


Figure 8.9: Projection of values of the transconductance along double row axes where the two different double rows are marked for module W60_OF1.

can be effected also by other effects. Besides the transconductance effect, the pedestals can also be influenced by the FET threshold. The FET threshold is the limit at which the DEPFET pixel bulk is depleted so that current can flow. In addition, the DCD gain can still have an influence.

Double Row Effect

In addition, another row by row pattern can be recognized. Here the transconductance changes systematically every two rows from higher to lower values. This occurs as follows: Row no. 1 has a low value. Row 2 and 3 show higher values. Row 4 again displays a lower value just like row no. 1. This pattern repeats itself over the whole module. The rows with lower values are defined as region 1, the rows with higher values as region 2. The two different row regions can be observed in the projection of the double row axis (see figure 8.9), in which a shift in the value of the transconductance is visible. This observation is consistent in all other modules examined (see section in appendix A.3.2).

To investigate further, how the two regions are shifted, a source scan (see section 5.6) was performed in which the charge spectrum was recorded. A radioactive ^{109}Cd source (1 850 MBq activity) was used and placed on top of the module in the setup. The measurement time was 400 seconds.

Figure 8.10 shows the charge spectrum of all pixels. The different pixel regions of the lower and higher values of the transconductance g_m are depicted by the color code in green and blue. On the left hand side the raw signal distribution of the module is shown, thus the data is not processed further. The X-ray spectrum with the respective K_α and K_β peak would be assumed. Anyhow, each pixel of the DEPFET pixel matrix is behaving differently. Since we observe the overall distribution of each pixel, the two peaks are overlapping. On the right hand side of the figure, a cluster algorithm is applied with cluster charge one. The cluster algorithm groups pixel charge information, meaning charge sharing events. The total cluster charge is defined as the sum of all partial charges within the found region [48]. For the cluster charge spectrum cluster size 1 was chosen to filter out charge from neighboring pixel events, which are distributed over several pixels.

In both distributions a high noise peak is arising at around 8 ADU. In addition a small peak at around 13 ADU is visible, which is arising due to photon emission. By using the rough energy

possible material	energy K_α/keV	energy K_β/keV
Cu	8.04	8.91
Zn	8.67	9.61
Ge	9.81	11.0

Table 8.4: Possible material list of photon emission peak at around 13 ADU. [49, 50]

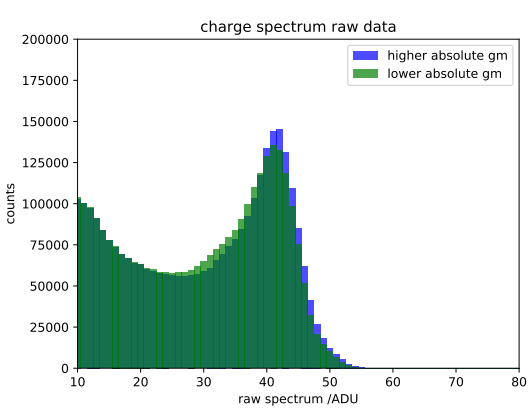
calibration factor of the respective module of 1.91 ADU/keV (calculated in section 8.2.1), different material could come into account. The materials in question are listed in table 8.4 with their respective energy of the photon peaks. None of these materials are used in the surrounding setup. Copper, on the other hand, is more frequently integrated in the module. For example, a copper layer is added to the two aluminum layers for signal routing and power. Additionally, copper serves for the bump pads used inside the aluminum layers [48]. Therefore the peak at 13 ADU most likely arise due to photon emission on copper.

Within the distributions of the signal a slight shift in the entries for the two pixel types can be seen in both the raw charge spectrum and the cluster charge spectrum. A greater absolute transconductance, i.e., a more negative transconductance, leads to higher entries in the charge spectrum. This behavior applies for all other modules (see section A.3.5). Not for all modules a ^{109}Cd source was used. Some utilized a ^{90}Sr. However, these modules show the same behavior. Concluding, this double row effect has a slight impact on the charge spectrum. A possible explanation for this effect are the electrical connections in the PXD layout. This is shown in figure 3.3. The depicted layout structure is repeated for all pixels. It is noticeable that the drift stitch between aluminum layer 1 and the silicon is closer to the inner pixels than to the outer pixels. The two inner pixel rows therefore could behave differently than the outer ones, which could result in the double row pattern. Another reason could be the shared source implant. The stitch of the source line to the silicon layer is located at one pixel, which provides the other with voltage. A voltage drop could occur here. The stitch here is located at the inner pixel, which could lead to the observed pattern. Even if the exact reason for the pattern cannot be specified, it is consistent with the observed pattern due to the layout repeating every four rows.

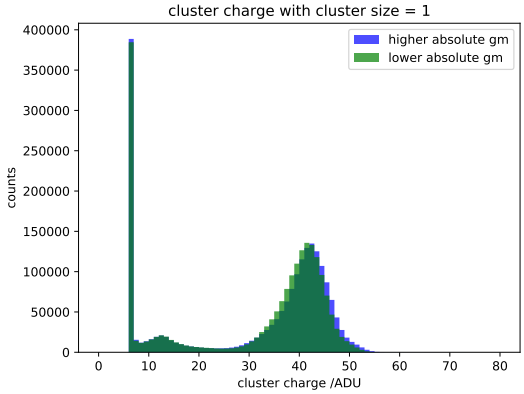
Row Structures

If the structure within the transconductance matrix (see figure 8.3) is considered in more detail, further periodicities occur within the row sequences. In order to find out how these occur in detail, a different representation method is used. In figure 8.11 the projection of each row, i.e. the median value of each row is displayed in color. The median value and not the mean value is used to obtain the most accurate result possible, since the pixels do not behave evenly. The values are plotted from top left to bottom right. The value of position $[0, 0]$ therefore equals to the median value of row 0. At the location $[1, 0]$ appears row 1, to the right lies row 2, etc. After 16 rows, the next row values are plotted beneath. Accordingly, the value of row 16 is located in $[0, 1]$. So the projection of the rows is stacked by 16 rows. For the outer forward module, the small pixels are accordingly placed from $[0, 0]$ to $[15, 15)$.

The already discussed structures are visible inside the representation. On the one hand the gradient with a value drop in the middle of the module is visible. The significant drop in transconductance from line 15 onwards, where the large pixels are located, can be seen. In addition the double row structure with lower-higher-higher-lower transconductance values is clearly visible, which leads to the



(a) Raw Spectrum of ^{109}Cd.



(b) Cluster Charge Spectrum of ^{109}Cd. Cluster Algorithm is applied here.

Figure 8.10: Charge spectrum of a radioactive ^{109}Cd source on module W60_OF1. The measurement duration was 400 seconds. The blue region marks the higher absolute Transconductance (more negative values), while the light green region marks the lower absolute transconductance (more positive values). The dark green region marks the overlap of both regions.

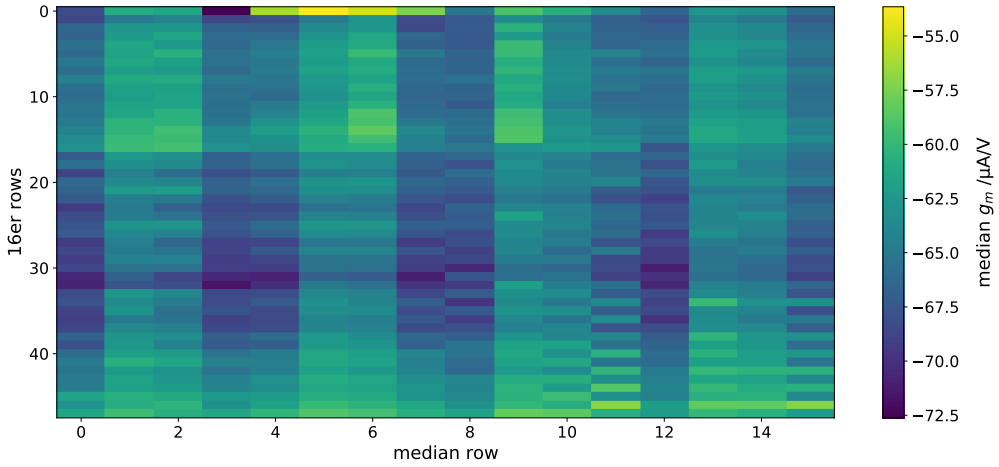


Figure 8.11: Projection of the rows for module W60_OF1 stacked on each other in 16 steps. For the module, the small pixels are located from $[0, 9]$ to $[16, 16)$.

double row effect.

In addition to the already discussed structures, an internal pattern is repeated roughly every 16 rows, especially for the large pixels. Comparing this 16 row periodicity with the pattern of other modules, it is evident that this periodicity occurs consistently (see appendix section A.3.2). For the process of creating the implantations and the poly-silicon lines for the module, the sensitive part of the module is produced with help of a laser beam. The DEPFET pixel technology includes 25 photo-lithographic mask steps and 9 implantations. [48] For the preliminary adjustment, different sized write heads are used for the mobile laser, which processes different sized windows step by step. For the implants, for example, much larger write heads (10 mm for large pixels) are needed than for the poly-silicon lines (4 MM for large pixels). Fine adjustment is performed with the poly gate via self-alignment. One theory that would explain the recurring pattern is that the photo-lithographic masks are misaligned with respect to the poly-gate, so that the implantation edge deviates from the poly-gate, causing the self-alignment to fail. This phenomenon would explain the different behavior between large and small pixels, since different sized write heads are used here. However, it is unlikely that this effect occurs with modules on different wafers, since lithography controls are performed. The 16 row effect is still under discussion and will be analyzed further.

Moreover, it is visible that every fourth row, the transconductance is similar in size. This is to be expected since every fourth pixel row shares the same drain line (see section 3.1.2).

8.2 Internal Amplification

In this section, the internal amplification is discussed, which is another quantity to characterize each pixel. First, the measurement methodology will be explained. Then, the calculation of the internal amplification will be detailed. After that, the observations and results are presented.

8.2.1 Measurement Method and Analysis of Internal Amplification

The Internal Amplification g_q is given by the current response to a single electron in the internal gate (see section 3.1.1). Therefore a source is needed, which is placed above the respective module in the module setup. Here, a radioactive ^{109}Cd source (1 850 MBq activity) is used, which emits X-rays. The emitted photon creates a signal inside the DEPFET pixel via the photoeffect. (6300 electron-hole pairs in silicon per photon [13]). For a duration of minimum 8 hours, measurements where collected for enough statistics in each pixel using the source scan (see section 5.6). Eight hours measurement are used for inner modules and ten hours for outer, because the inner modules are located closer to the source than the outer modules due to their setup. Here the drain current is measured for each DEPFET pixel. With the help of the default source scan analysis the cluster charge can be calculated by using a cluster charge algorithm. Two peaks are expected in the X-ray spectrum due to electron transmission, K_α and K_β. When observing the charge distribution in each pixel (example in figure 8.12), the K_α peak is noticeable. To investigate if the K_β peak is resolved as well, a rough energy calibration is done. For module W60_OF1, a reference measurement was made with ^{55}Fe. Here, the maximum was observed at $x^{\mathrm{Fe55}}_{K-L_3,K-M_3} = 11$ ADU. The iron source is an X-ray emitter. The $K - L_3$ and $K - M_3$ transitions are very close to each other and result in a peak at $E^{\mathrm{Fe55}}_{K-L_3,K-M_3} = 5.9$ keV. For the cadmium source, an overall maximum $x^{\mathrm{Cd109}}_{K_\alpha}$ is observed at 42 ADU, which corresponds to the

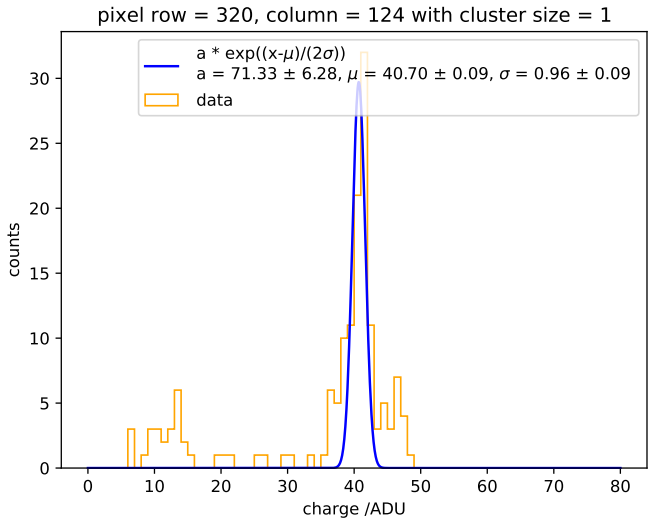


Figure 8.12: Cluster Charge Spectrum in pixel row 320 column 124 with clustersize 1 in module W60_OF1. In blue a Gaussian is fit to the data.

K_α line of $E_{K_\alpha}^{\mathrm{Cd109}} = 22.1\,\mathrm{keV}$ [50]. This results in a calibration factor f_c of:

$$f_c = \frac{x_{K_\alpha}^{\mathrm{Cd109}} - x_{K-L_3,K-M_3}^{\mathrm{Fe55}}}{E_{K_\alpha}^{\mathrm{Cd109}} - E_{K-L_3,K-M_3}^{\mathrm{Fe55}}} = \frac{42\,\mathrm{ADU} - 11\,\mathrm{ADU}}{22.1\,\mathrm{keV} - 5.9\,\mathrm{keV}} = 1.91\,\mathrm{ADU/keV} \tag{8.3}$$

Multiplying the conversion factor by the K_β energy of 25.0 keV gives the following position:

$$x_{K_\beta}^{\mathrm{Cd109}} = f_c \cdot E_{K_\beta}^{\mathrm{Cd109}} = 47.8\,\mathrm{ADU} \tag{8.4}$$

The calculated intensity ratio of the K_α and K_β peak corresponds to 0.22. The expected intensity ratio is 0.21 [50]. Thus, the small peak next to the K_α emission line is associated with the K_β line in figure 8.12. However, since the peak is not particularly visible (in some pixels not visible at all), the energy of the K_α line is used to calculate the internal amplification. The K_β energy is disregarded. Therefore, a single Gaussian fit is applied to model the K_α peak. The mean value of the Gaussian fit of the signal distribution μ_{fit} corresponds to the emission line $E_{K_\alpha}^{\mathrm{Cd109}} = 22.1\,\mathrm{keV}$. This, can be used to calculate the internal amplification:

$$\begin{aligned} g_q &= \frac{\mu_{\mathrm{fit}}}{E_{K_\alpha}^{\mathrm{Cd109}}} \cdot \frac{1}{\text{DCD gain}} \cdot \left\langle E_{eh} \right\rangle \\ [g_q] &= \frac{\mathrm{ADU}}{\mathrm{eV}} \cdot \frac{\mathrm{nA}}{\mathrm{ADU}} \cdot \frac{\mathrm{eV}}{e^-} = \frac{\mathrm{nA}}{e^-} \end{aligned} \tag{8.5}$$

where $\left\langle E_{eh} \right\rangle = 3.64\,\mathrm{eV}$ is the average energy to create an electron-hole pair in silicon [51]. The results for the DCD gain are taken from chapter 7. All measurements were performed with a gate-on voltage of $-2.1\,\mathrm{V}$.

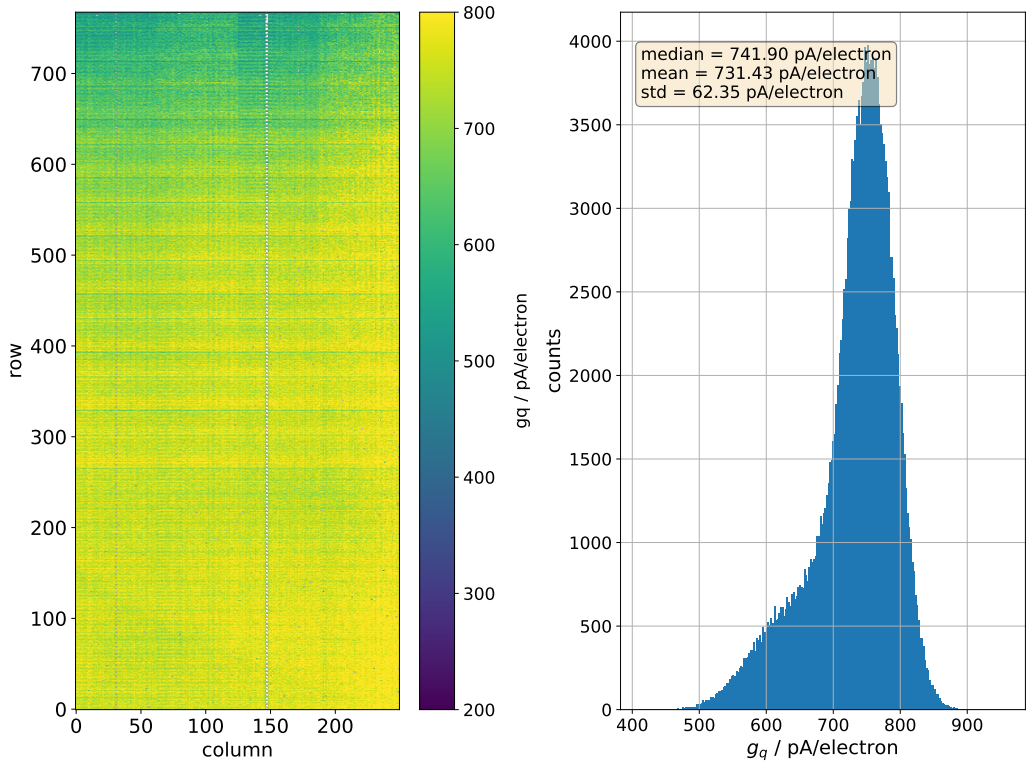


Figure 8.13: The values of the internal amplification for each pixel are shown for module W60_OF1. In the left plot the values are distributed in the PXD9 matrix of the module. The internal amplification is depicted for each channel via the color code on its geometrical position inside the DEPFET matrix. On the right the incidence of the values for each pixel is plotted. The median value gives 743.91 pA/electron.

8.2.2 Results

The Internal Amplification values are displayed within their geometrical position on the DEPFET matrix. The result for each pixel for module W60_OF1 is shown in figure 8.13. In a distribution of a 1D histogram the occurrence of the values are shown. This shows a homogeneous distribution with a median value of 743.91 pA/electron. A zoom to a part of the pixel matrix is shown in 8.14. The results for other tested modules are listed in section A.4.1.

In this section the homogeneity of the values inside the matrix is investigated. In addition, the values are averaged over the pixels, which are then compared among the modules.

Comparison to modules

For better comparison of the internal amplification between modules, the median value is taken over each pixel. This method gives a much more accurate result than using the mean of the overall distribution, because, as shown above, the resulting distribution of the internal amplification is not Gaussian or symmetric. In the table 8.5 the median values of the tested modules are presented. The values are in the same order of magnitude. Nevertheless, they differ significantly from each other (maximal approximately 30.45 %). Even with weighting of the standard distribution, the distributions

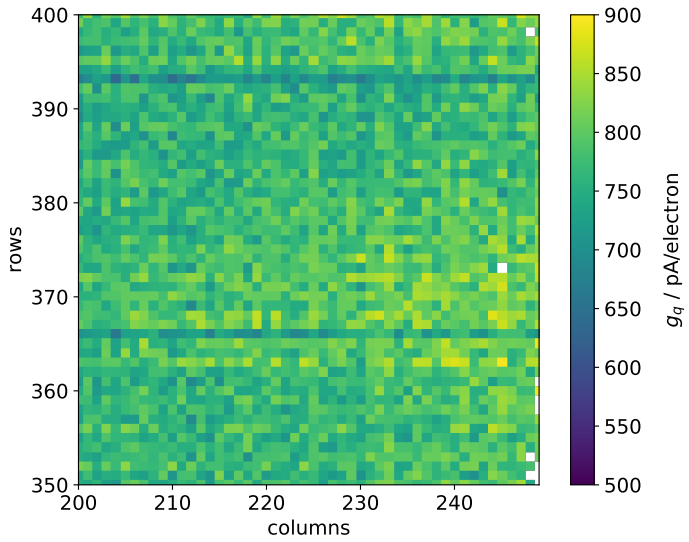


Figure 8.14: Zoom of values of the internal amplification for each pixel are shown for module W60_OF1. In the left plot the values are distributed in the PXD9 matrix of the module. The internal amplification is depicted for each channel via the color code on its geometrical position inside the DEPFET matrix. On the right the incidence of the values for each pixel is plotted. The median value gives 743.91 pA/electron.

	W67_IB	W57_IB	W60_OF1
median g_q / µA/electron	517.40	648.55	743.91
std(g_q)/ µA/electron	49.96	59.52	62.35

Table 8.5: Median internal amplification g_q for different modules.

do not overlap. In particular, the W67_IB module has a significantly smaller internal amplification than the other two modules examined. All values were measured with the same gate-on voltage of −2.1 V. Since the internal amplification depends on both the gate-on voltage and the source current, it is important to also consider the source current. It is noticeable that the source current differs despite the same gate-on voltage for the different measurements. For example, module W67_IB with a source current of 78 mA differs significantly from the source current of module W60_OF1 with 97 mA. This could explain the significantly lower value for W67_IB. However, the module W57_IB has a source current of 81 mA, which fits to the slightly higher internal amplification of this module. To further investigate this effect, a second measurement was performed with a higher gate-on voltage of −2.5 V and a resulting source current of 100 mA for the W67_IB module. A median value of g_q = 558.05 µA/electron with a standard deviation of 56.10 µA/electron is measured. The results show that the expectation of a higher source current to a higher internal amplification is confirmed. Nevertheless, the value still differs significantly from the other modules. Due to the already differently measured transconductance, one could assume that this module corresponds to an outlier. To confirm this assumption more statistics have to be measured. The deviating source currents could be explained by the fact that a higher current in the gate lines could lead to voltage drops in the modules. This

	threshold 4	threshold 5	threshold 8
median g_q / µA/electron	518.72	517.40	518.63
std(g_q)/ µA/electron	50.04	49.96	50.34

Table 8.6: Median internal amplification g_q for different thresholds of module W67_IB.

would lead to the effective gate voltage not being the same. In fact, it is not clear what the voltage drops depend on. One possibility is that they depend on the module structure arrangement. Different kapton lengths thus provide the bias on the module. This results in different kapton resistance. To confirm this theory, more modules would have to be examined. Comparing the internal gain of each module with the previously assumed of about g_q = 400 to 600 pA/electron [5] it is noticeable that the in in detail determined values are roughly higher. The module W60_OF1 differs around 20 %. However, the values were measured before only really roughly and did not take the DCD gain and different pixel response into account.

Influence of Zero Suppressed Threshold

For the measurement of the charge spectra a threshold can be set to avoid possible noise. This saves a large amount of disc space, since less data has to be stored. However, this could also lead to neglecting charges that are below this threshold, which could have an influence on the internal amplification. This is because high thresholds could lead to a lot of charge being contained in neighboring pixels that are not detected by the cluster selection. Thus, a higher threshold could lead to lower amplification. Since the results of the internal amplification appear relatively high, an investigation is made into how large the influence of the set so-called zero suppressed threshold (see section 3.2.3) is.

The results shown above were all measured with a zero suppressed threshold of 5 ADU. The results for the internal amplification for the module W67_IB are summarized in table 8.6, where different zero suppressed thresholds have been set. It is noticeable that the zero suppressed threshold change does not lead to a significant change of the internal amplification of the module. The standard deviation values cover the median values. The highest deviation of the median values is 0.25 %. The deviations seem to be fluctuations in the measurement. Therefore, the statement made above cannot be confirmed here. If a photon deposits the energy in for example four pixels evenly, the cut made with the zero suppressed threshold would cut out the whole event. Therefore the zero suppressed threshold can't have any influence unless the threshold is very close to the K_α peak.

Internal Amplification in pixel matrix

In the pixel matrix clear differences between the magnitude order of internal amplification in the different DCDs can be observed. When the projection of the row and column axes are examined (see figure 8.15 left), a gradient from lower to higher values along the row axis is visible for both modules. The projection of the row axes for module W60_OF1 (see figure 8.15 right) show a gradient effect along the row axis. A lower internal amplification closer to the ASICS is observed here. This observation is consistent with previous measurements of the internal amplification depending on each switcher position [52]. A possible explanation of this gradient could be related to the sampling point at all ADCs. Despite constant ADC sampling time during digitization of the pixel signals during the rolling shutter, some pixels lie further away from the readout chips. Therefore their signals have to

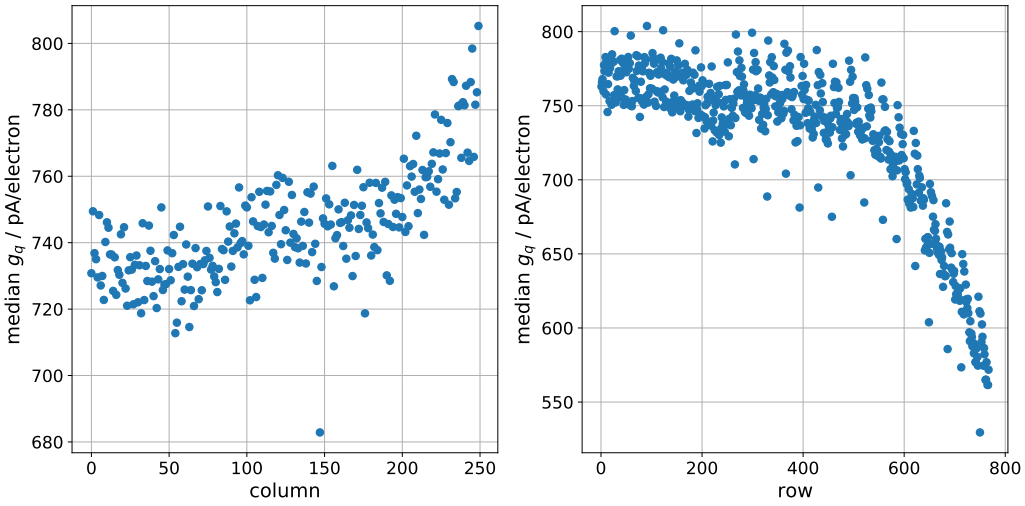


Figure 8.15: Projection of values of internal amplification along column and row axes for module W60_OF1.

travel further distances. The sampling point of the ADCs must be selected in such way that a steady state is created, so that the temporary state disappears in the DEPFET pixel after enabling the external gate. If the sampling point is too high, it is possible that still a part of the temporary state is measured. A too high overshoot followed by an undershoot could explain the effect that the internal amplification of more distant pixels is higher. This observation is consistent with all other investigated modules (see section A.4.2), which have the same sampling point time. In addition to the gradient, a difference between small and large pixel sizes can be seen in the projection onto the row axis. For outer forward and inner forward modules, the pixels with the smaller size are located from row 0 to 256. For the backward module, they range from 512 to 768 (see section 3.4). With respect to the gradient, a smaller transconductance for smaller pixels is observed in the projection. Initially, this is not expected. A larger pixel shows a larger drift region. Thus, in addition to the zero suppressed threshold, the size of the drift region also could have an effect on the charge loss. Therefore, smaller pixels have more favorable drift conditions and thus exhibit a smaller charge loss. However, a second component could play a further role here. For the small pixels there is a higher probability that neighboring pixels are also hit. The clustering algorithm, which is applied to the charge spectrum and the selection of the cluster size 1, presumably sorts out more charges of the smaller pixels, since the probability is higher to be fully hit within one pixel with a larger pixel. Due to the observation that there is a relatively smaller amplification for smaller pixels, the conclusion can be made that the effect of clustering is far outweighs the effect of the smaller drift region.

For the projection on the column axis no large differences in the column axes between the different DCDs are visible in comparison to the projection of the transconductance. Instead a gradient from lower to higher value is visible. Due to the matrix layout the switcher lies on the right hand side. Therefore we observe higher internal amplification values closer to the switchers. This would be expected according to previous understanding, that smaller amplification values are observed in the pixel closer to the DCDs. When comparing the values to the other modules, it is noticeable that the gradient is not constant (see section A.4.2). For module W57_IB a lower amplification is observed at the switchers. For module W67_IB the opposite is observed. However, uncertainties can also

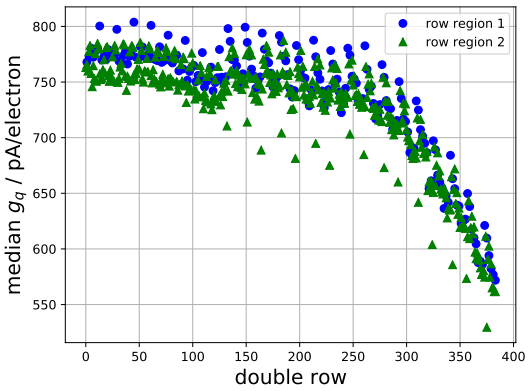


Figure 8.16: Projection of values of internal amplification along double row axes for module W60_OF1. The two different pixel size are marked in different colors.

occur here due to the significant missing statistics of the masked pixels in DCD 4 (approximately 40 %), which shows the highest gradient. These were caused by truncated dynamic ranges of the ADC transfer curve measurement in the DCD gain analysis. Other than that, the internal amplification projection on the column axis is relatively homogeneous in this module. So different behaviors are observed from module to module. This phenomenon is not yet understood. However, the gradients in the projection on the column axis are much less significant than those on the row axis.

Double Rows

In addition to the gradient, a recurring structure of double rows can be recognized as well. This effect was already observed within the transconductance (see figure 8.3). The recurring row wise pattern of higher-lower-lower-higher values of the internal amplification can be seen. This effect is approximately visible, if the projection of the pixel rows are divided into the two double rows (see figure 8.16) as already explained above. The two pixel types that are shifted towards each other do not show a clearly separated area. Compared to the other modules examined, it is noticeable that this effect occurs to varying degrees. It can possibly be explained by the electrical layout of the matrix. The drift stitch is located closer to two pixel rows. The fact that the double row pattern arises in differentiating strength for different modules is still under investigation. This has already been discussed in detail in chapter 8.1.2.

Row Structure

The median values of the projection rows are displayed where 16 row values are stacked. The small pixels are located in this case from $[0, 0]$ to $[15, 15)$. For the module W60_OF1 the result is shown in figure 8.17.

In this case, there are, similar to the transconductance pattern, clear differences between small and large pixels. In addition, a 27-37 row pattern is visible in this case, which is repeated eight times over the pixel area with large sizes. These structures are probably again based on the lithography effect that was already observed in the transconductance structure. During the writing process of the implants

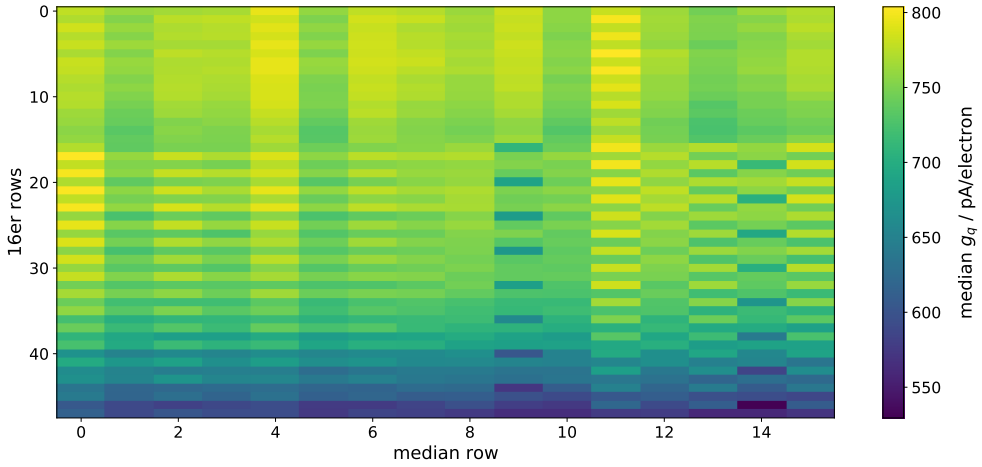


Figure 8.17: Projection of the rows for module W60_OF1 stacked on each other in 16 steps. For the module, the small pixels are located from $[0, 0]$ to $[15, 15)$.

using a laser different writing window sizes are overlapped. Thus, this explains the visibility of the 27-37 row pattern with for example lower entries for the internal amplification. This can be as well observed inside the zoomed matrix part in figure 8.14. Additionally, these are also recognizable in the pedestal scan (see figure 7.4), which supports the theory of the pattern caused by the lithography. Furthermore, a periodicity over all 16 rows is recognizable for large and small pixels. Since the same module is examined as already in the transconductance structure (see in comparison figure 8.11), similar internal structures are assumed. By the definition of the transconductance and the internal amplification, it is expected that these behave proportional to each other. Accordingly, higher internal amplification should be equivalent to higher transconductance. If we compare both patterns, we see approximately the same structure.

When comparing the results, it is noticeable that for both inner backward modules (see section A.4.2) 16 row patterns also occur. These are compatible with the patterns already observed in the transconductance plots.

In addition to the 16 row periodicity of module W60_OF1, the already discussed systematic gradation along the row axis can be observed. Furthermore, the double row effect is faintly noticeable. This seems to be partially overlaid by another effect in some regions of the module. Here, all systematically in each row first a higher amplification and in the next a lower amplification is observed. The two pixel effect can also be explained by the design. Considering the layout (see figure 3.2), it can be noticed that two pixels share one source contact. However, the source contact is not exactly centered, since the clear line also passes through this position. This results in a higher source resistance in one of the two pixels, since the implanted layer is slightly longer in that pixel. Comparing these results with those of the other modules, it is noticeable that the inner structures are of different strength. In module W57_IB and in module W67_IB the double row effect is much more evident than the two row effect.

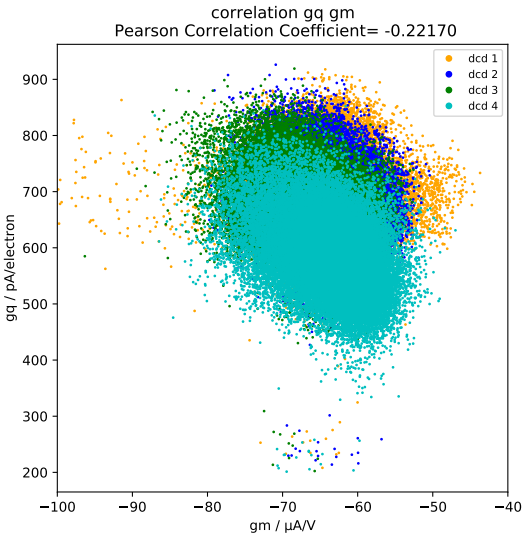


Figure 8.18: Correlation between transconductance g_m and internal amplification g_q of module W60_OF1. The color code indicates the different DCDs. The Pearson Correlation coefficient, gives a value on how correlated the both quantities are.

8.3 Relation of Transconductance and Internal Amplification

In this chapter, the results of transconductance and internal amplification are compared. The expected proportionality of the two quantities is to be confirmed. Furthermore, the absolute oxide capacity of each pixel is calculated.

8.3.1 Correlation Transconductance and Internal Amplification

Now the correlation of the previously determined transconductance and internal amplification is investigated. By the definitions in section 3.1.1 of these a proportionality is expected:

$$\frac{g_q}{g_m} = \frac{1}{LWC_{ox}} \cdot f \tag{8.6}$$

with the width and the length of the transistor L and W, the coupling factor f, which is describing how much the charge in the internal gate will be induced into the channel and the sheet oxide capacitance C_{ox}. When comparing the two quantities for each pixel in figure 8.18, no certain correlation can be recognized on the first view. The individual DCDs are marked in different colors. Only DCD 4 shows a visible linearity. The Pearson correlation coefficient confirms the observations. It has a value of -0.22 which indicates only a weak negative linear correlation.

If we compare this with the results of the other modules, we do not see consistency. For example, the correlation of module W57_IB shows a much more moderate linearity with a correlation coefficient of -0.63. Module W67_IB, on the other hand, has a correlation value of -0.35.

The different measurement methods can lead to uncertainties. These depend, for example, on how accurately linear straight line fits were performed or how strongly the charge spectrum could be

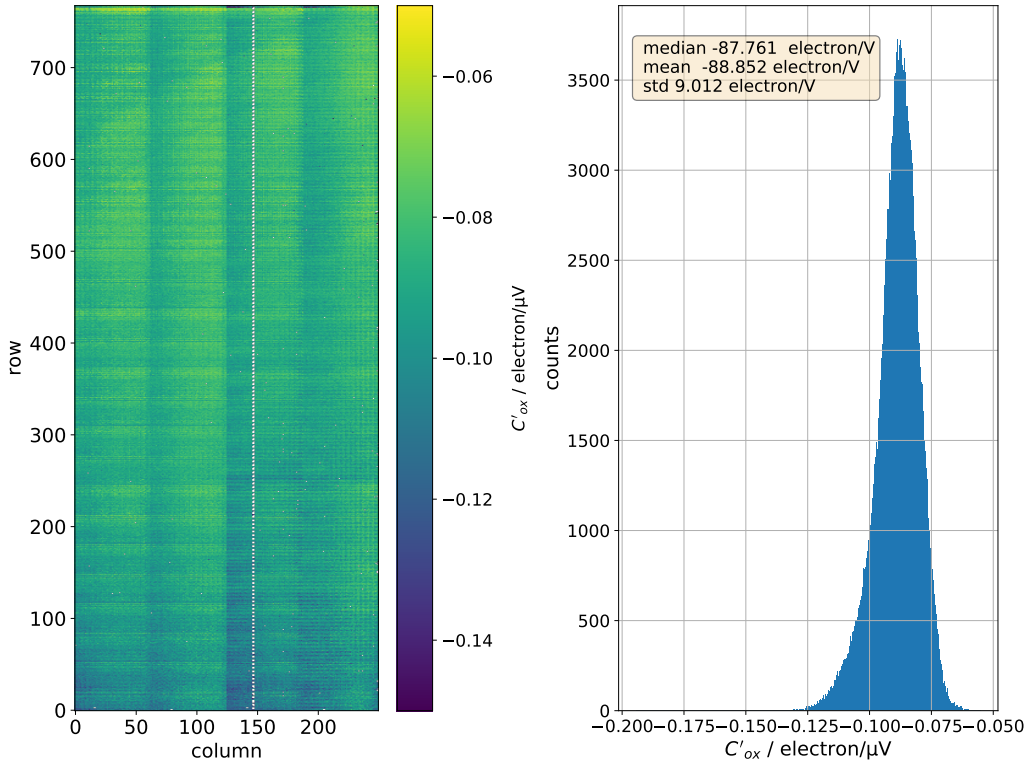


Figure 8.19: The values of the absolute Capacitance for each pixels are shown for module W60_OF1. In the left plot the values are distributed in the PXD9 matrix of the module. The absolute oxide capacitance is depicted for each channel via the color code on its geometrical position inside the DEPFET matrix. On the right the incidence of the values for each pixel is plotted.

extracted in each individual pixel. The inconsistent results could arise to either a systematic error during the measurement. Since the values of all modules were calculated with the same methodology, it could be possible that module W60_OF1 is just an outlier. However, there are not enough statistic to support this theory.

8.3.2 Oxide Capacitance

With the results of the transconductance and the internal amplification, an accurate result for the absolute oxide capacitance C'_{ox} per pixel can examined. This is done by calculating the relation of the two quantities, with equation 8.6. The definition of sheet oxide capacitance C_{ox} has already been introduced in equation 3.2. The sheet oxide capacitance can be also calculated by

$$C_{ox} = \frac{g_m}{g_q} \cdot \frac{1}{LW} f. \tag{8.7}$$

	W67_IB	W57_IB	W60_OF1
median C'_{ox} / electron/V	−88.06	−82.12	−87.76
std(g_q)/ electron/V	14.60	12.99	9.02

Table 8.7: Median oxide capacitance C'_{ox} for different thresholds of module W67_IB.

The absolute oxide capacity is defined as:

$$C'_{ox} = \frac{g_m}{g_q}. \tag{8.8}$$

Since the coupling factor cannot be easily determined, the absolute oxide capacitance is used for the following investigations. The result for each pixel is shown within the DEPFET matrix for module W60_OF1 in figure 8.19. In addition, the distribution of the oxide capacitance over the entire pixels is summarized in a 1D histogram. The median value for the absolute capacitance for module W60_OF1 gives −88 electron/V. The values of the investigated modules are listed in 8.7. The resulting plots for the other modules are given in the appendix A.5.1. Despite the different transconductance and internal amplification values for different modules, the oxide capacitance values are in the same order of magnitude and do not deviate significantly from each other. As expected from the previous calculations of transconductance and internal amplification, DCD differences are again observed. Despite efforts to weight the DCD characteristics, it is evident that they have not been completely canceled out. With the projection to the column axis in figure 8.20 on the left, this observation becomes very clear. In addition to the different values of each DCD, a gradient is also visible within the DCD, which leads to a saw-tooth pattern. The saw-tooth pattern has already been observed within the transconductance projection and has been discussed earlier in this chapter. Due to the connection of the capacitance with the transconductance, the same assumptions about the origins can be presumed. Comparing the result with other modules, deviations can be noticed. For example, for module W57_IB the differences between the individual DCDs are not significant. It is noticeable that the gradients in the DCDs of module W60_OF1 drop exactly in the opposite direction, i.e. from smaller to larger capacitance. This effect cannot be explained by the layout of the two modules, because the switcher for outer forward and inner backward module are on the same side. Only the DCDs are placed on the opposite side (see section 3.4). When looking at the projection in the row axis for module W60_OF1 (see figure 8.20 right side), a gradient is clearly visible. A lower capacity is observed here at the readout electronics, e.g. at the DCDs. Compared to other modules, this behavior is consistent. Also, with modules W57_IB, for example, a higher capacitance occurs with more far readout electronics. The effect occurred already in the internal amplification extraction (see section 8.2.2). Due to the long distances the signals of the more distant pixels have to travel, the required capacitance is higher. If the double row effect is examined again, where different values for the transconductance and the internal amplification occur, it can be seen that this effect is balanced for the capacitance. No double row structure can be recognized further. This also becomes evident in the projection of the double rows in figure 8.21. For module W57_IB the double row effect is still evident. The different behaviors of both modules have already been noticed when comparing the transconductance and the internal amplification.

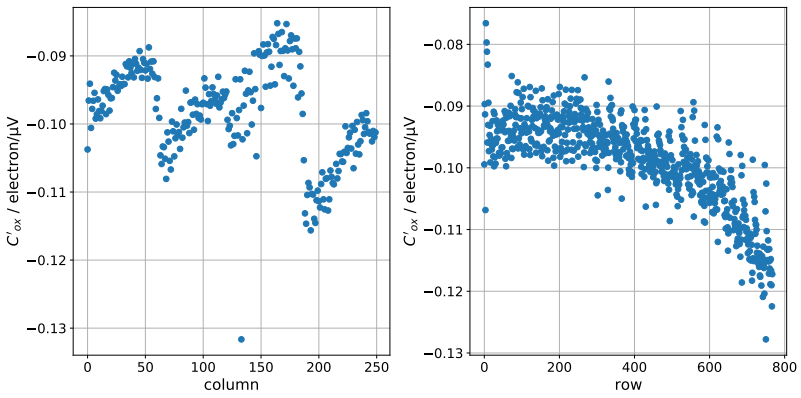


Figure 8.20: Projection of values of the absolute capacitance along the column and the row axes for module W60_OF1.

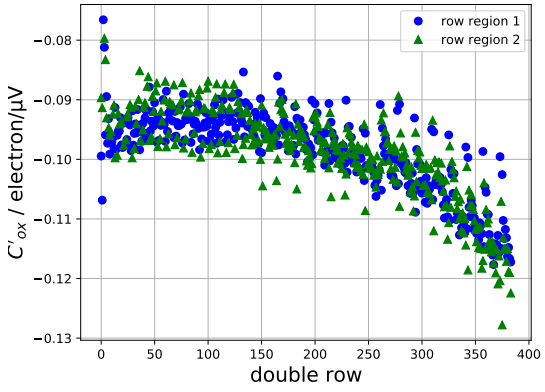


Figure 8.21: Projection of values of the absolute capacitance along double row axes where the two different double rows are marked for module W60_OF1.

CHAPTER 9

Conclusion

With a dew point monitoring system, the experimental lab setup in Bonn was upgraded for safer operation. Sensors were installed in the setup, where live humidity and temperature data is read out with a mini computer. With the help of a control system, the readout data is passed on to the lab computer and is processed. An interlock mechanism was successfully installed to shut down the module and turn off the cooling system if there is a risk of damaging the module due to condensation. The reliability of the dew point interlock was further hardened with a software interlock implemented by a heart-beat exchange between the components. The functionality of the system has been extensively tested.

To better understand the behavior of the PXD module, the influence of the biasing voltages on the pedestals was investigated. Potential couplings between the clear-off, drift and backside to the FET are observed. This results higher measured pedestal values at more negative voltages. Out of the investigated voltages, clear-off has the largest impact on the pedestal values, since the implant is located closest to the FET. In addition, the back injection effect could be observed at too low clear-off voltages. The noise, i.e. the fluctuation of the pedestals had no significant influence on the pedestal values. When investigating the influence of the biasing voltages on the hv current, the punch through effect from the backside to the p implants on the front side could be observed at negative hv settings, which lead to over depletion. In general, it is important for the operation of the PXD detector to understand the DEPFET pixel and its characteristics. The biasing voltage studies show how important it is to have the best possible setting for biasing the matrix, otherwise undesirable effects such as the punch through effect or the back injection effect may occur.

For calculating the transconductance and internal amplification pixel by pixel, the influence of the digitization process of the signal current by the DCD was determined. The determination of the DCD channel gains showed significant variations between DCDs and between channels within each DCD. Therefore the exact evaluation is a necessary prerequisite for the measurement of the DEPFET characteristics. About the origin of this effect so far only assumptions can be made and investigations are still ongoing.

The values of the transconductance g_m and the internal amplification g_q were measured and calculated successfully for the first time pixel by pixel. Deviation in magnitudes between the investigated modules were noticed. For the transconductance, a possible connection to the production on different wafers could be determined. The significant differences that occurred for the internal amplification could possibly be explained by effectively different source currents occurring in the

modules. Periodic structures were observed within each pixel matrix. A double row pattern is visible in g_m and g_q and is most likely caused by specifics of the pixel layout. Another recurring pattern with a 16 row periodicity was observed and could possibly be explained by specifics of the lithography processed used in the module production. For the internal amplification g_q, a clear gradient along the readout direction of the matrix is visible. The reason is not yet fully understood. Shifts in the readout timings of the different parts of the matrix might be the cause. The transconductance and the internal amplification were compared with each other. In contrast to the expectation, a strict correlation was not observed in all cases. Finally, the absolute oxide capacity was calculated, in which the effects described above merge.

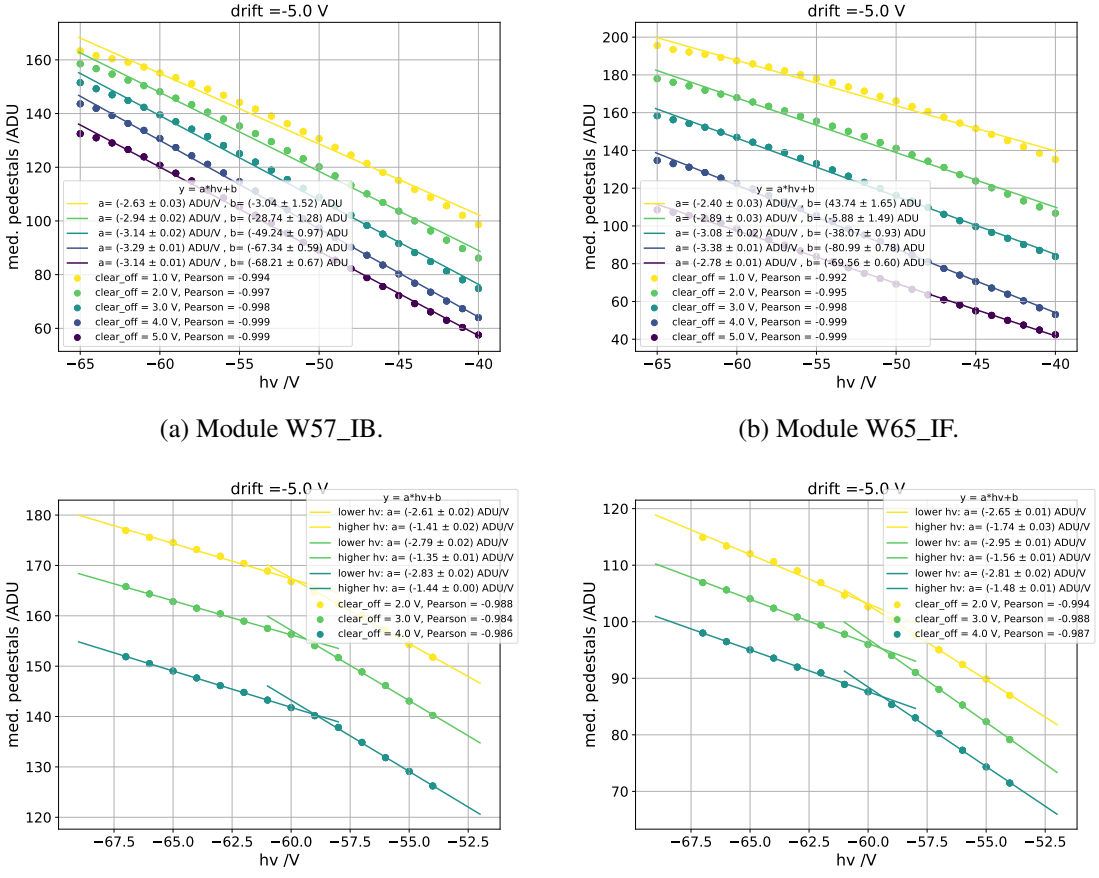
Results from more modules would improve the evaluation of correlations between g_m,g_q and individual wafer properties. Investigation to the irregularities of the gate on voltage dependence to the source current could be done for further modules.A further study of interest would be to investigate the strength or change of the recurring structures in the matrix as well as for the DCD gain, when the modules are irradiated as a function of dose. A large pixel to pixel change can theoretically degrade the charge resolution. Since charge measurement is not the main task of the PXD and the observed discrepancies are limited, the result for the operation have no significant influence on data quality. However, if the visible structures and thus different magnitudes of transconductance, internal amplification on a pixel basis, or DCD gain deviations are amplified by irradiation, this could lead to increased uncertainty in efficiency or reconstruction.

APPENDIX A

Appendix

A.1 Biasing Scans

A.1.1 Pedestals



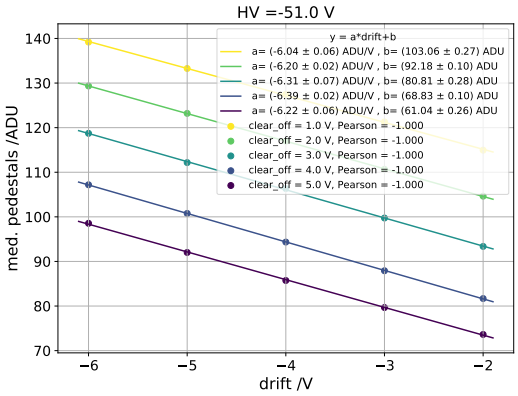
(a) Module W57_IB.

(b) Module W65_IF.

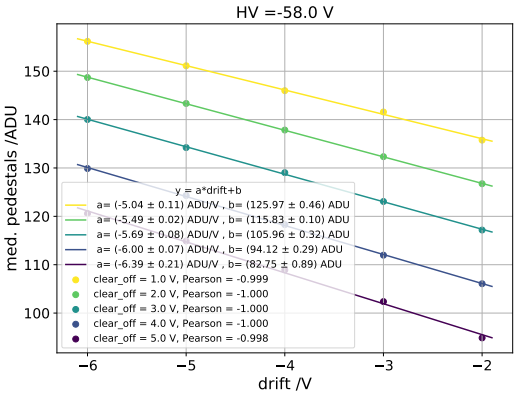
(c) Module W57_OF2.

(d) Module W57_OB1.

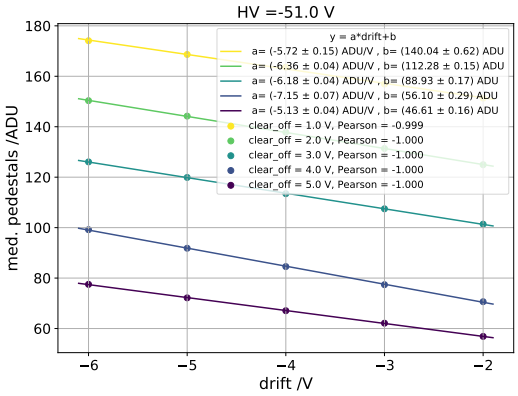
Figure A.1: The projection of the median pedestal values onto the hv axis for drift = −5 V is shown. The different colors represent different clear-off settings. The Pearson coefficient indicates how linearly the data points are related.



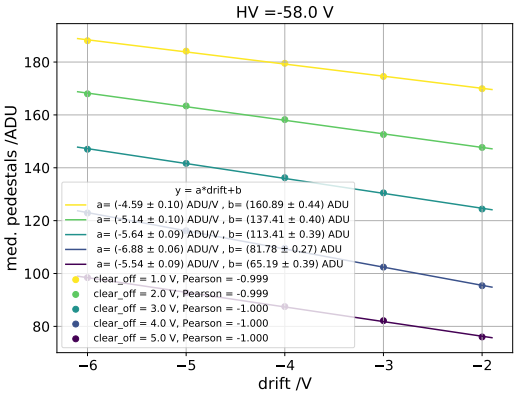
(a) W57_IB.



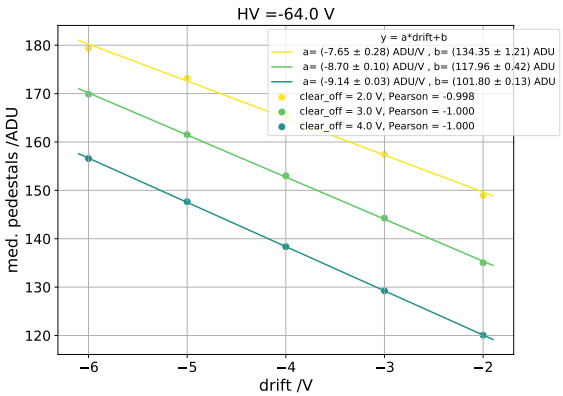
(b) W57_IB.



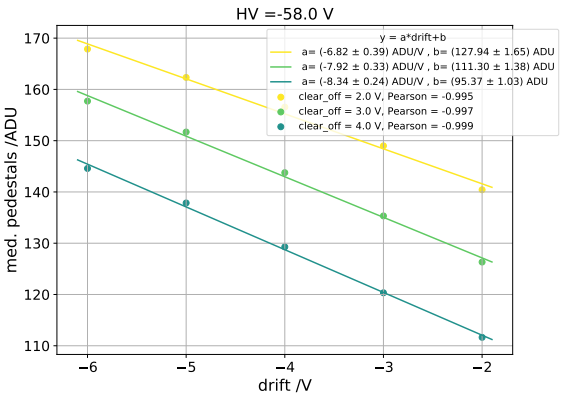
(c) W65_IF.



(d) W65_IF.



(e) W57_OF2.



(f) W57_OF2.

Figure A.2: The projection of the median pedestal values onto the drift axis for two different example settings for hv is shown. The different colors represent different clear-off settings. The Pearson coefficient indicates how linearly the data points are related.

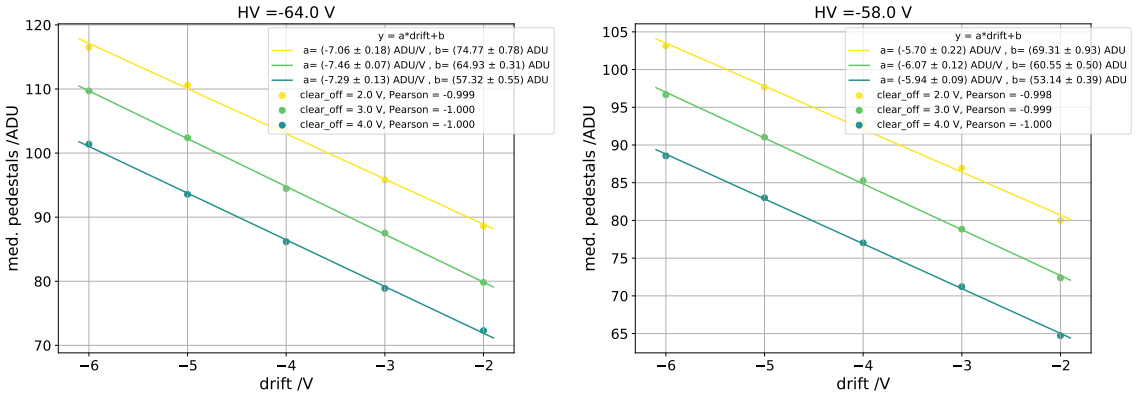
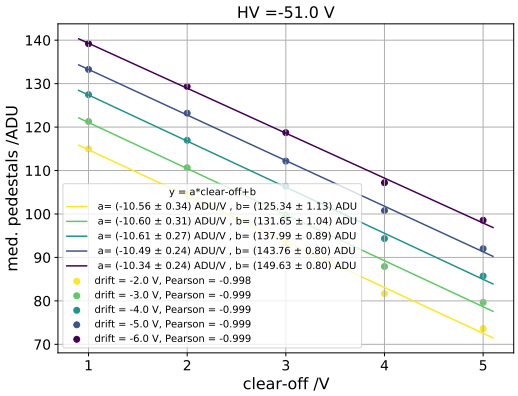
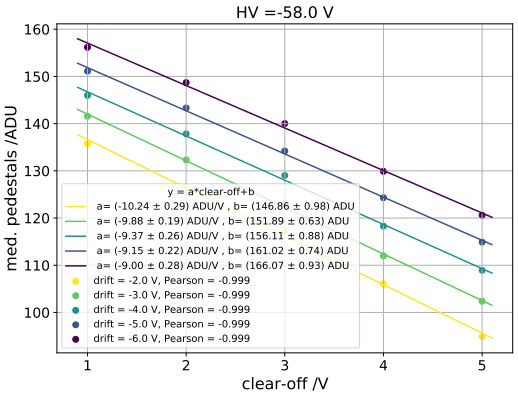


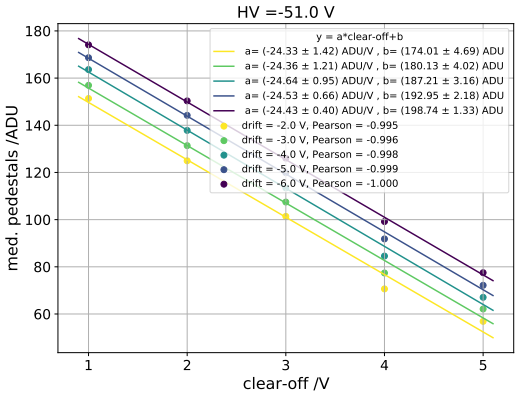
Figure A.3: The projection of the median pedestal values onto the drift axis for two different example settings for hv for module W57_OB1 is shown. The different colors represent different clear-off settings. The Pearson coefficient indicates how linearly the data points are related.



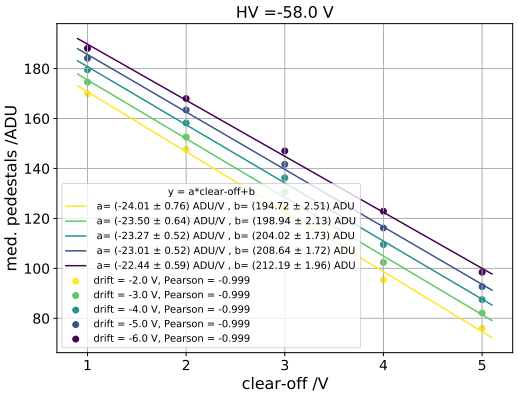
(a) W57_IB.



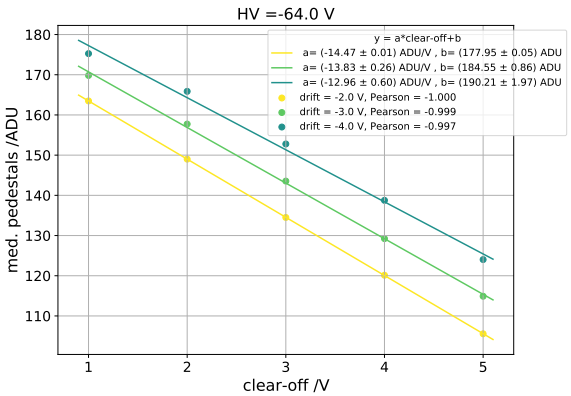
(b) W57_IB.



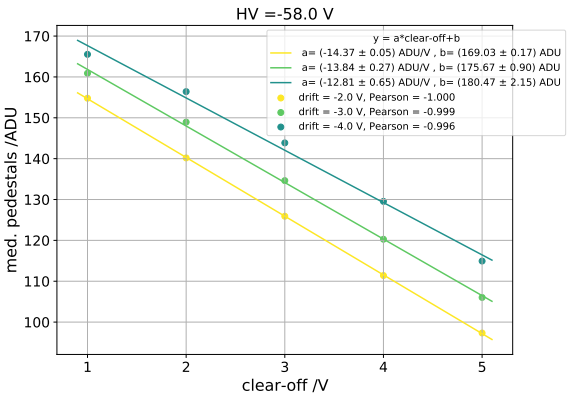
(c) W65_IF.



(d) W65_IF.



(e) W57_OF2.



(f) W57_OF2.

Figure A.4: The projection of the median pedestal values onto the clear-off axis for two different example settings for hv is shown. The different colors represent different drift settings. The Pearson coefficient indicates how linearly the data points are related.

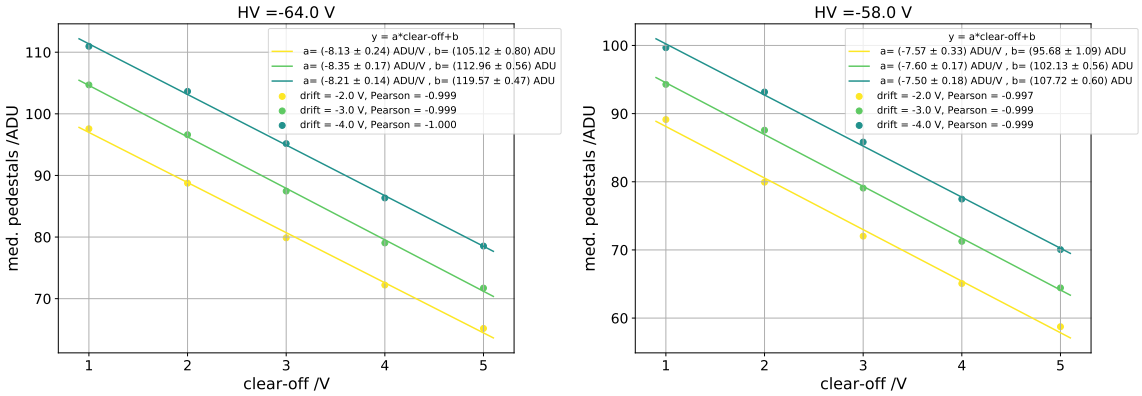
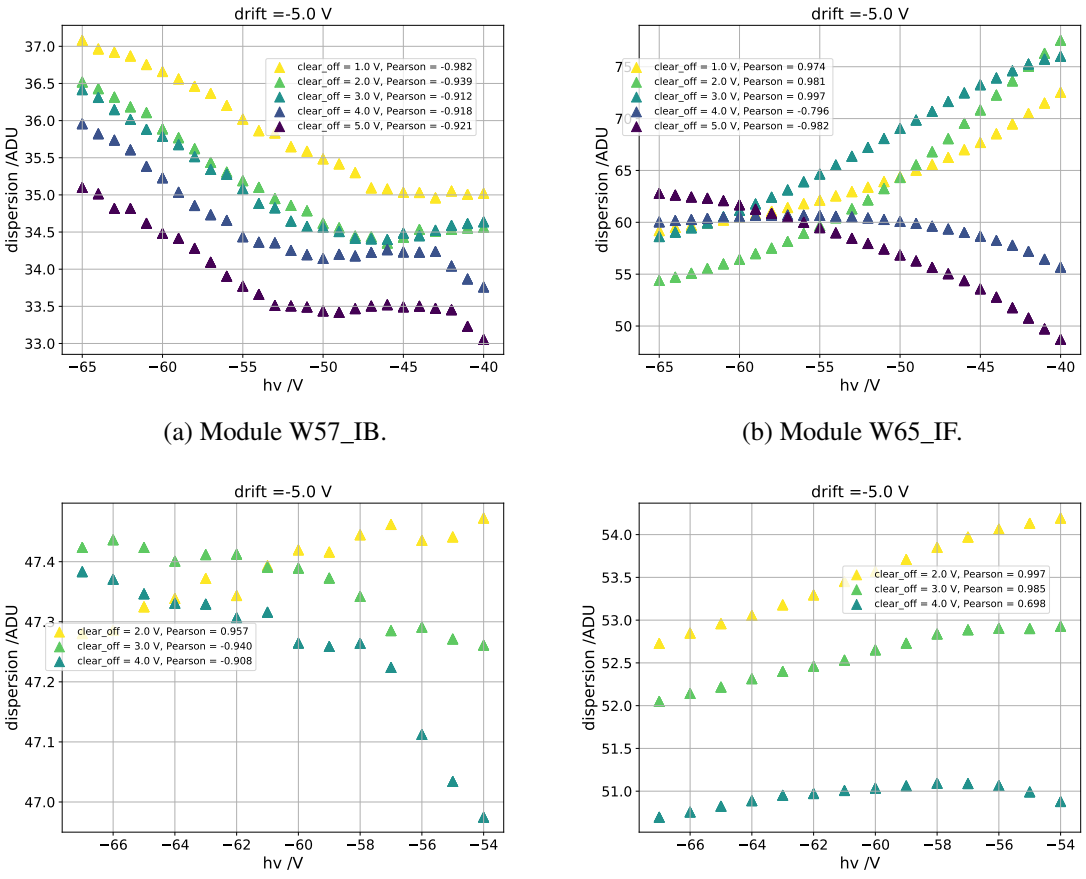


Figure A.5: The projection of the median pedestal values onto the clear-off axis for two different example settings for hv for module W57_OB1 is shown. The different colors represent different drift settings. The Pearson coefficient indicates how linearly the data points are related.

A.1.2 Dispersion



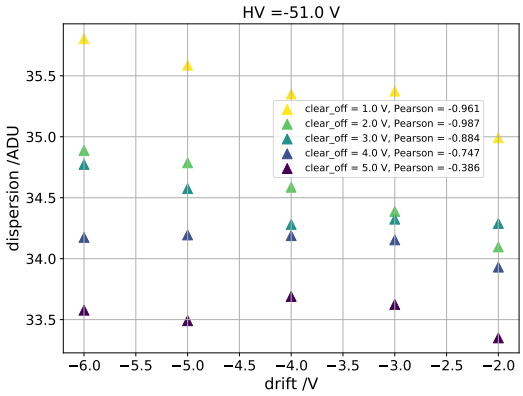
(a) Module W57_IB.

(b) Module W65_IF.

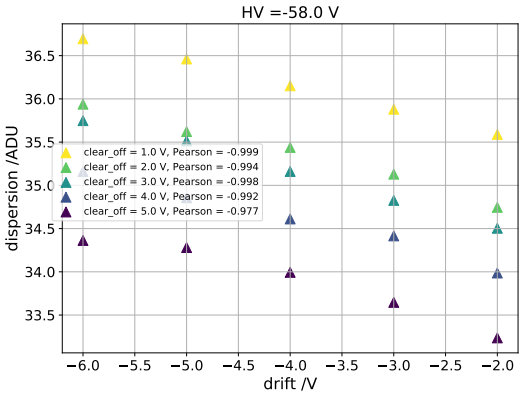
(c) Module W57_OF2.

(d) Module W57_OB1.

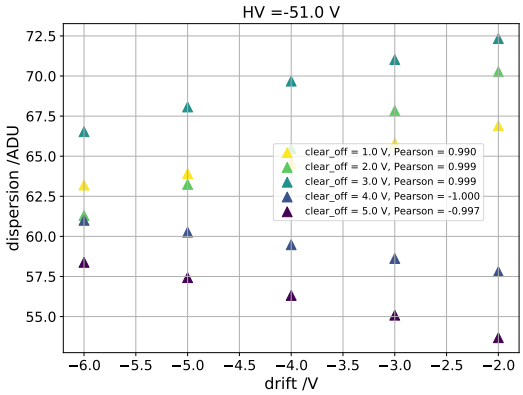
Figure A.6: The projection of the dispersion values onto the clear-off axis for drift = −5 V is shown. The different colors represent different clear-off settings.The Pearson coefficient indicates how linearly the data points are related.



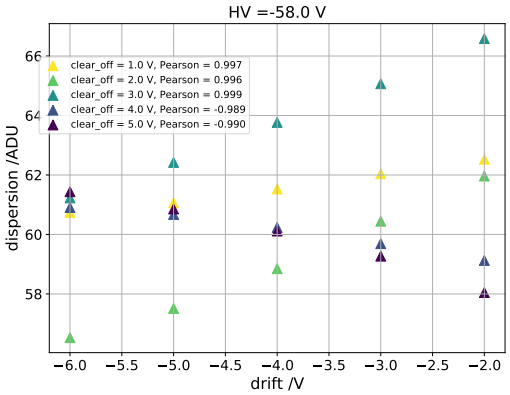
(a) Module W57_IB.



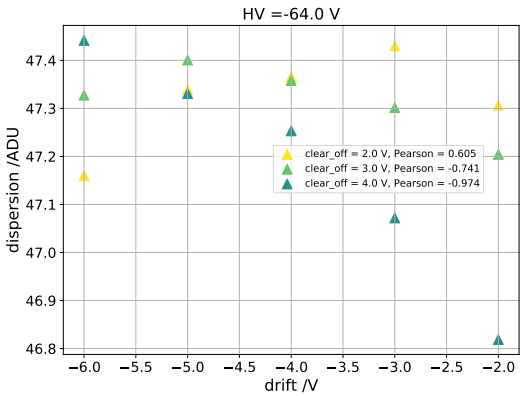
(b) Module W57_IB.



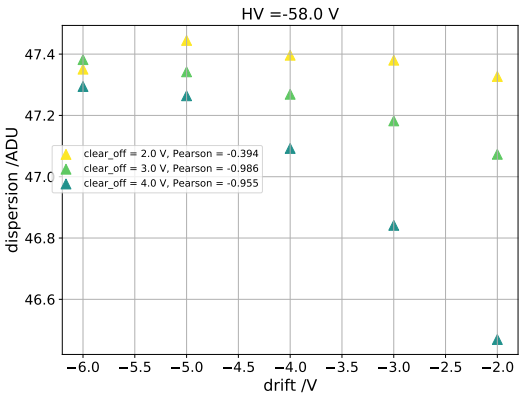
(c) Module W65_IF.



(d) Module W65_IF.



(e) Module W57_OF2.



(f) Module W57_OF2.

Figure A.7: The projection of the dispersion values onto the drift axis for two different example settings for hv is shown. The different colors represent different clear-off settings. The Pearson coefficient indicates how linearly the data points are related.

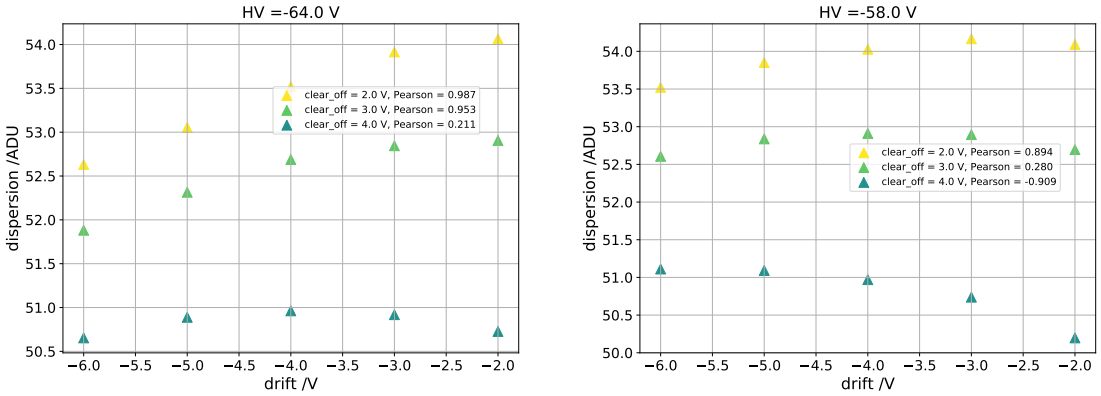
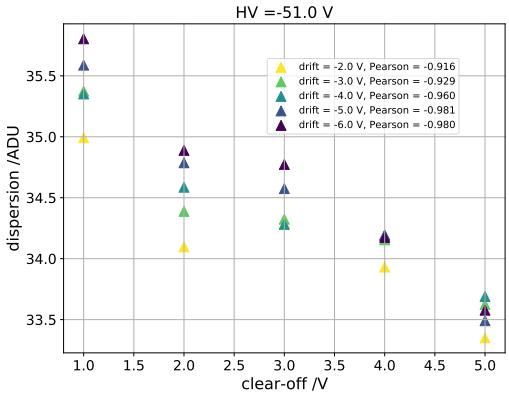
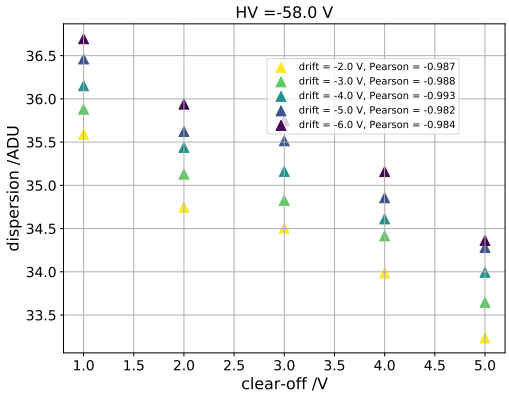


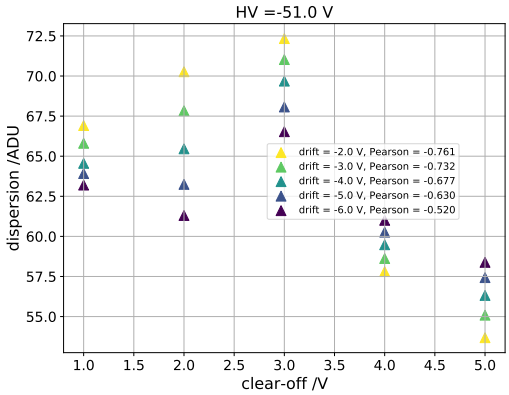
Figure A.8: The projection of the dispersion values onto the drift axis for two different example settings for hv for module W57_OB1 is shown. The different colors represent different clear-off settings. The Pearson coefficient indicates how linearly the data points are related.



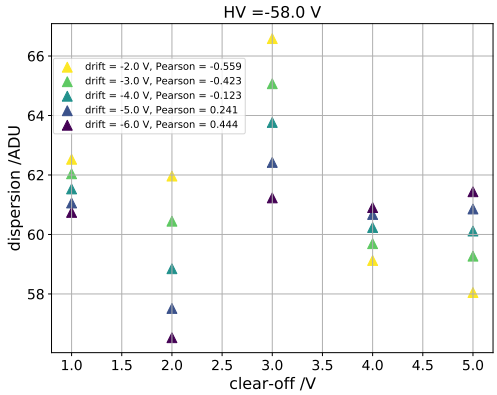
(a) Module W57_IB.



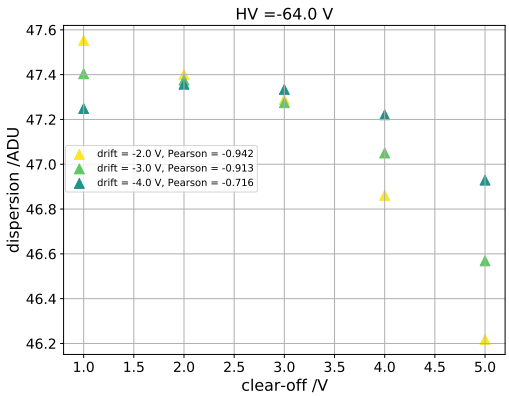
(b) Module W57_IB.



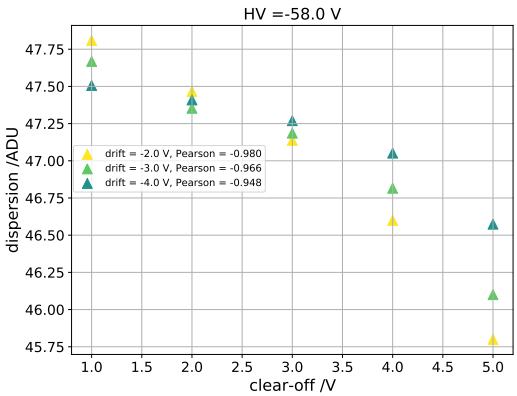
(c) Module W65_IF.



(d) Module W65_IF.



(e) Module W57_OF2.



(f) Module W57_OF2.

Figure A.9: The projection of the median pedestal values onto the clear-off axis for two different example settings for hv is shown. The different colors represent different drift settings. The Pearson coefficient indicates how linearly the data points are related.

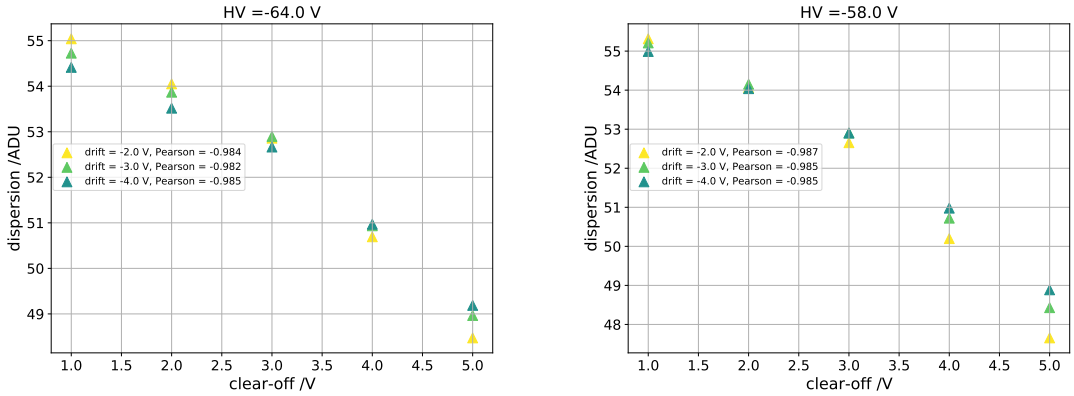
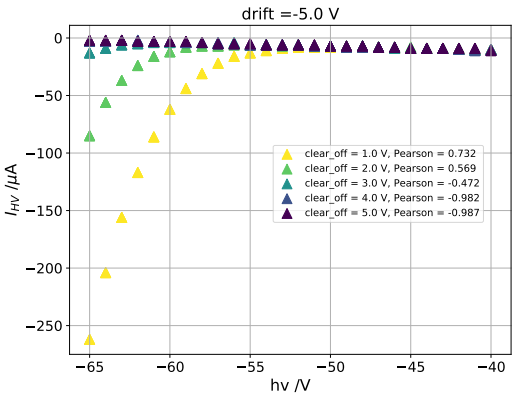
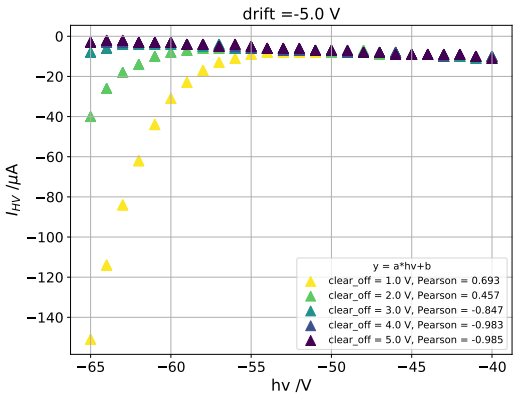


Figure A.10: The projection of the median pedestal values onto the clear-off axis for two different example settings for hv for module W57_OB1 is shown. The different colors represent different drift settings. The Pearson coefficient indicates how linearly the data points are related.

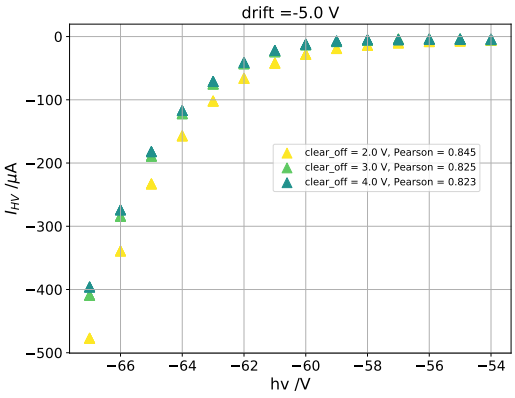
A.1.3 HV current



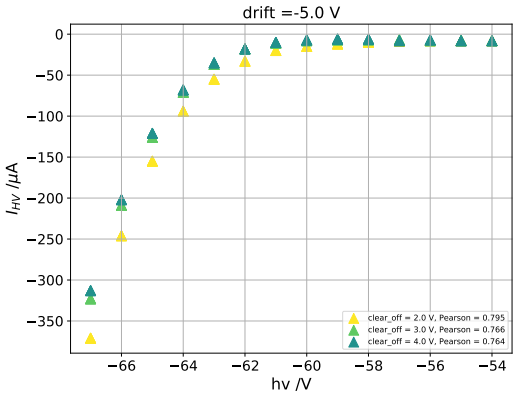
(a) Module W57_IB.



(b) Module W65_IF.

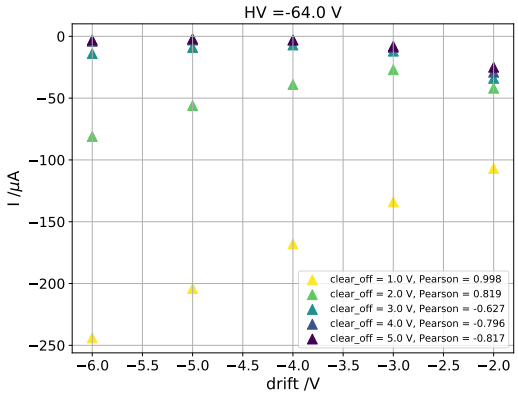


(c) Module W57_OF2.

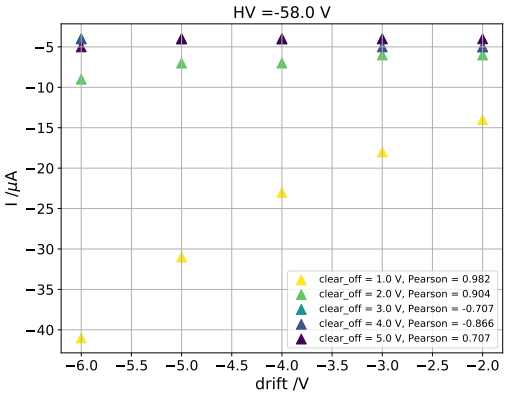


(d) Module W57_OB1.

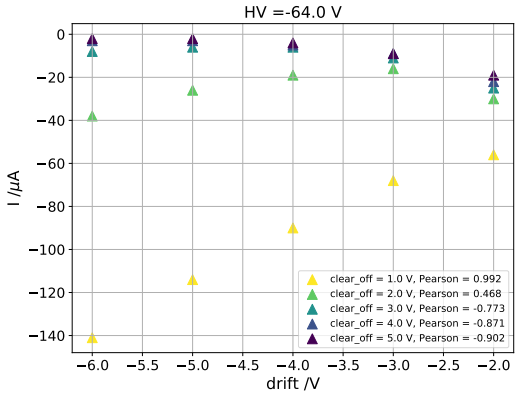
Figure A.11: The projection of the hv current values onto the hv axis for drift = −5 V is shown. The different colors represent different clear-off settings. The Pearson coefficient indicates how linearly the data points are related.



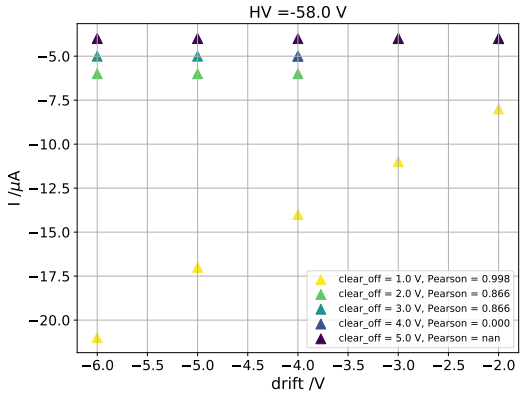
(a) Module W57_IB.



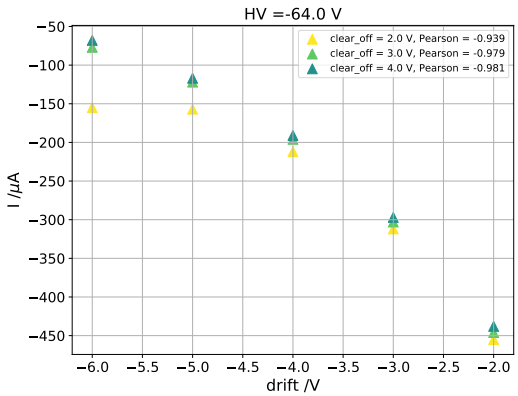
(b) Module W57_IB.



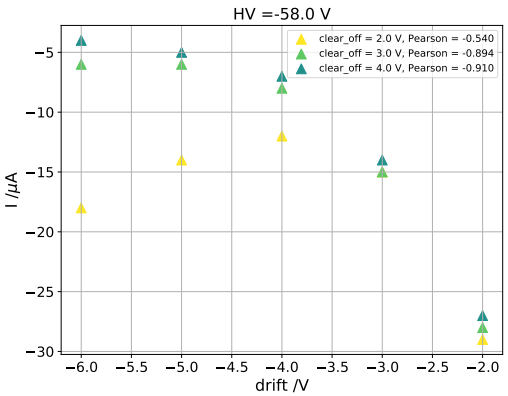
(c) Module W65_IF.



(d) Module W65_IF.



(e) Module W57_OF2.



(f) Module W57_OF2.

Figure A.12: The projection of the hv current values onto the drift axis for two different example settings for hv is shown. The different colors represent different drift settings. The Pearson coefficient indicates how linearly the data points are related.

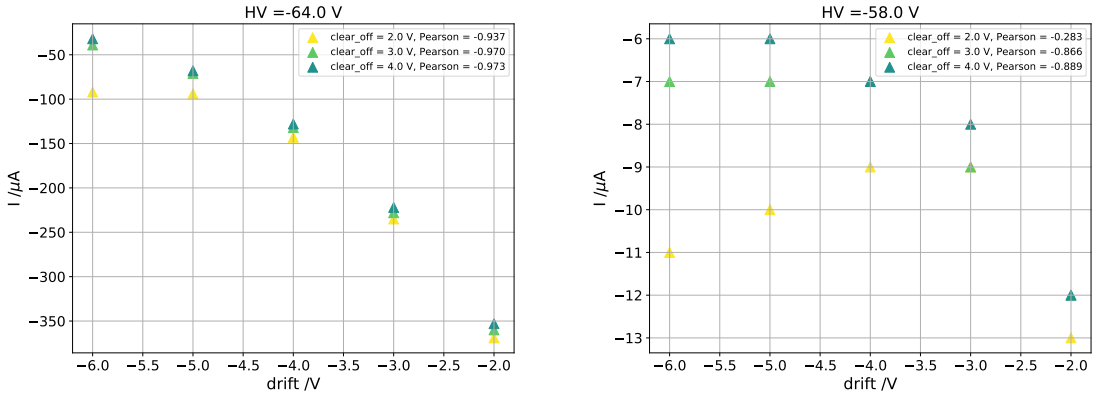
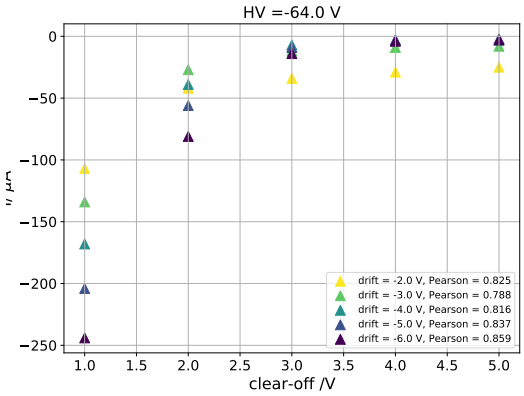
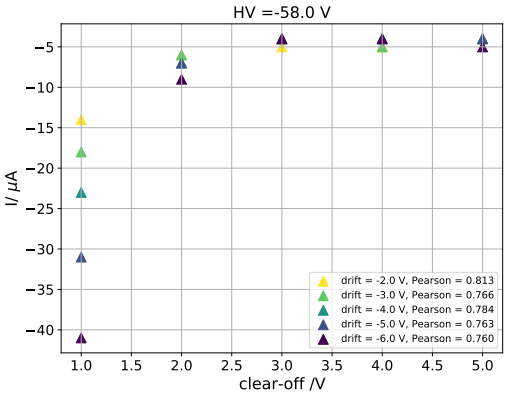


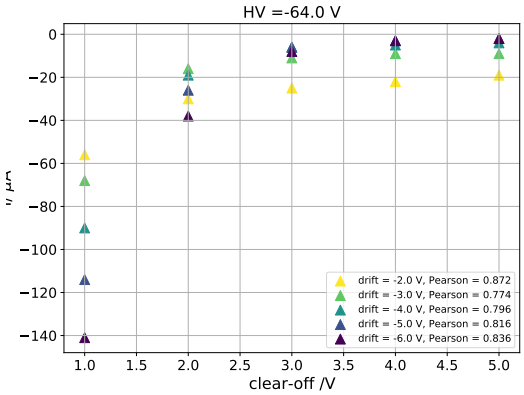
Figure A.13: The projection of the hv current values onto the drift axis for two different example settings for hv for module W57_OB1 is shown. The different colors represent different drift settings. The Pearson coefficient indicates how linearly the data points are related.



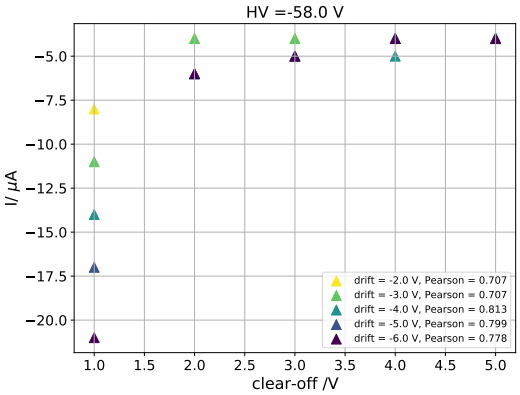
(a) Module W57_IB.



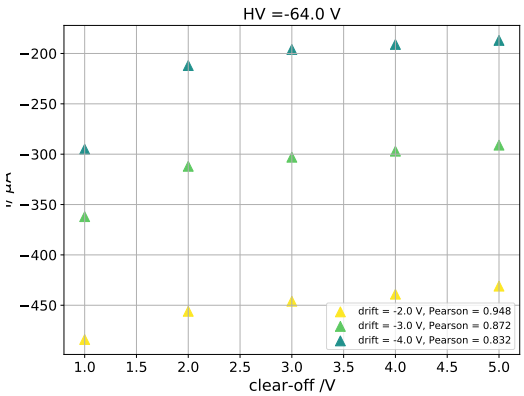
(b) Module W57_IB.



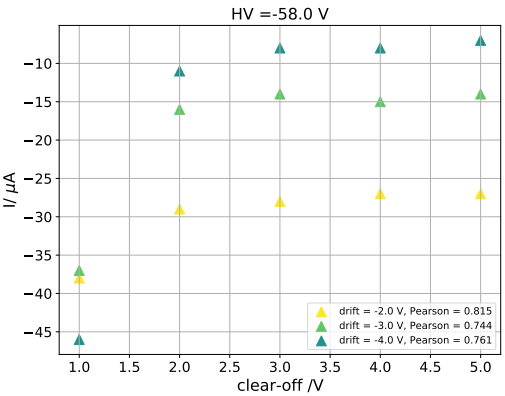
(c) Module W65_IF.



(d) Module W65_IF.



(e) Module W57_OF2.



(f) Module W57_OF2.

Figure A.14: The projection of the high voltage current onto the clear-off axis for two different example settings for hv is shown. The different colors represent different drift settings. The Pearson coefficient indicates how linearly the data points are related.

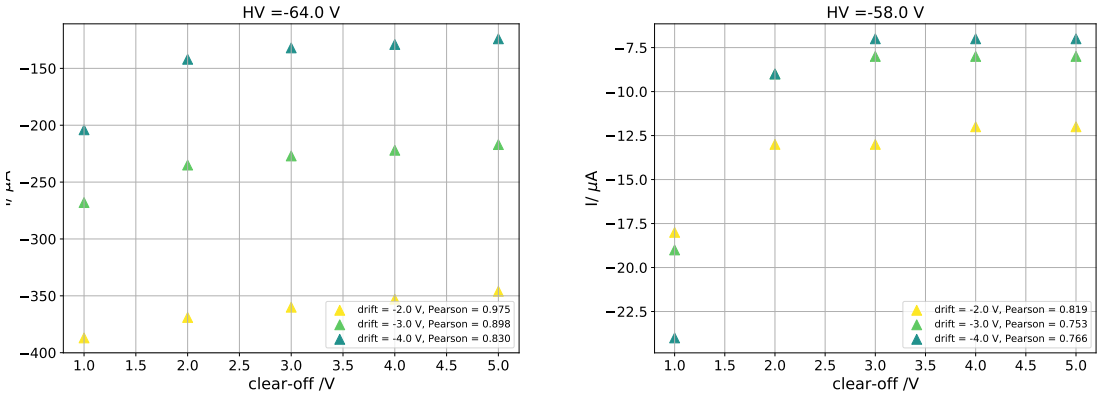
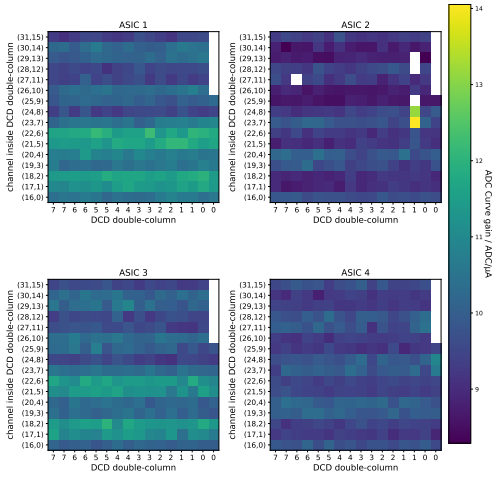


Figure A.15: The projection of the high voltage current onto the clear-off axis for two different example settings for hv for module W57_OB1 is shown. The different colors represent different drift settings. The Pearson coefficient indicates how linearly the data points are related.

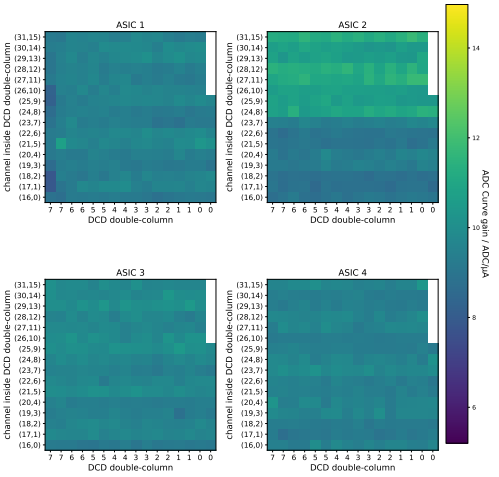
A.2 ADC Transfer Curves using DHE Current

A.2.1 Results ADC Gain

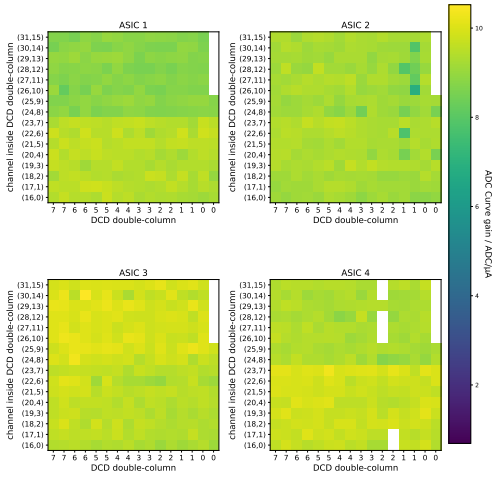
Comparision to Channels



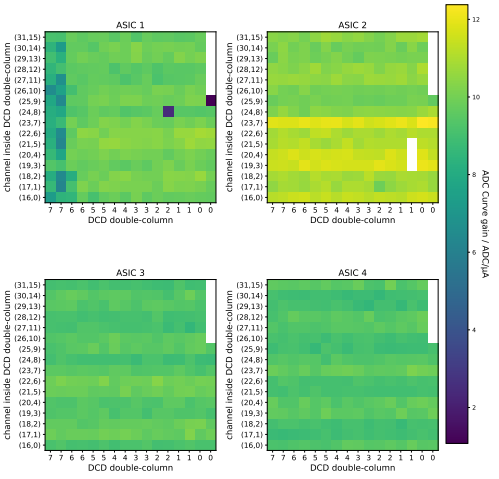
(a) Module W57_IB.



(b) Module W57_OF2.

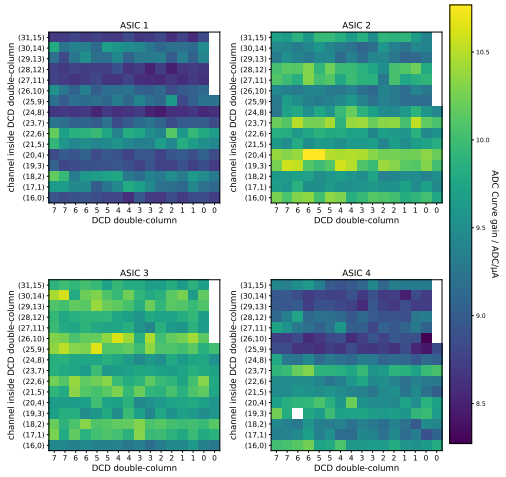


(c) Module W57_OB1.

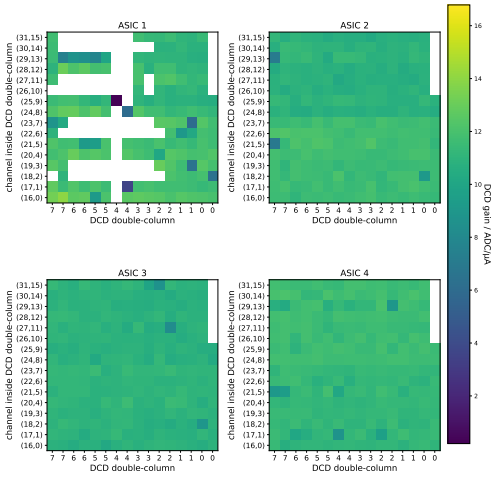


(d) Module W56_OF1.

Figure A.16: The gain of each ADC channel is shown as a function of its position on the DCD footprint. Channel 10 to 15 in double-column 0 is disconnected and therefore marked in white.



(a) Module W56_OB1.



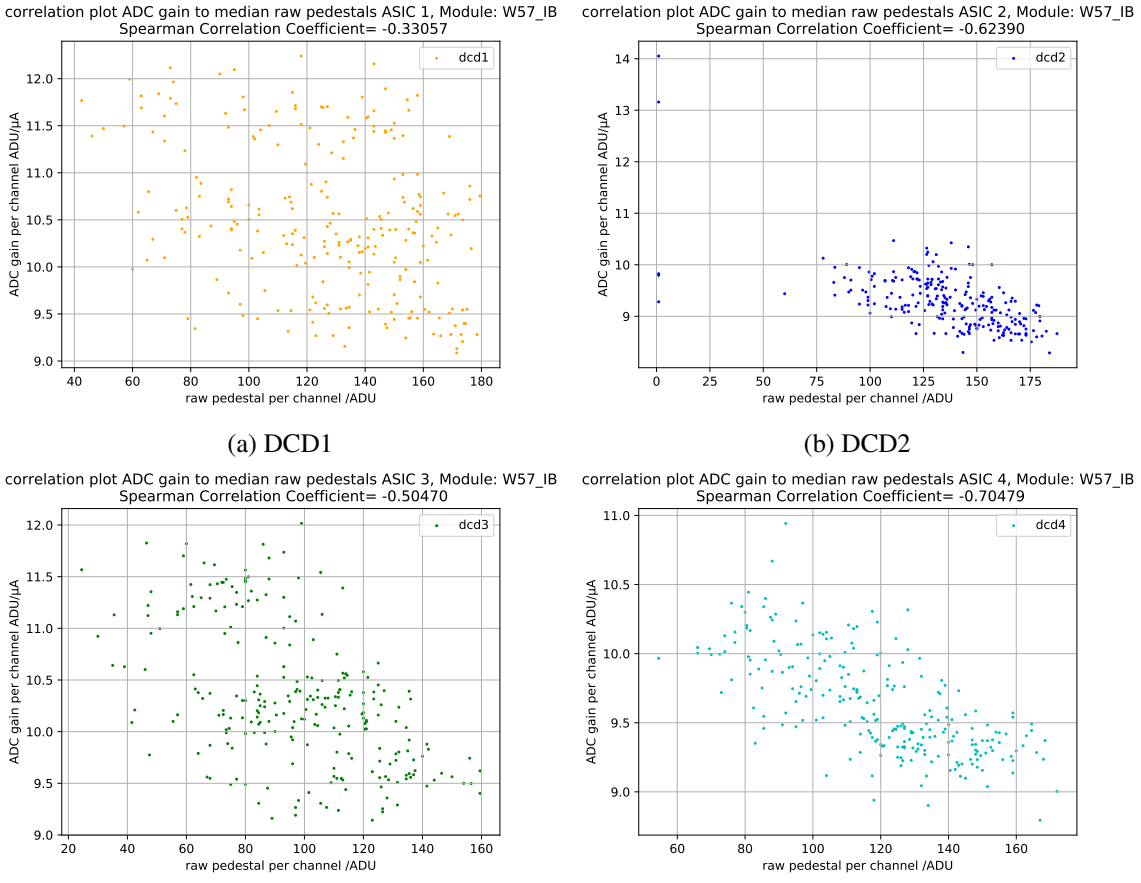
(b) Module W67_IB.

Figure A.17: The gain of each ADC channel is shown as a function of its position on the DCD footprint. Channel 10 to 15 in double-column 0 is disconnected and therefore marked in white.

percentage deviation ΔADC gain	W56_OF1	W56_OB1	W57_OB1	W57_OF2	W57_IB	W60_OF1
DCD 1	6.56 %	1.79 %	0.61 %	2.88 %	8.38 %	4.14 %
DCD 2	5.75 %	5.49 %	0.24 %	4.61 %	7.65 %	1.98 %
DCD 3	4.10 %	5.07 %	0.53 %	3.27 %	8.60 %	6.23 %
DCD 4	4.67 %	1.08 %	0.13 %	3.39 %	5.81 %	4.90 %
average of all DCDs	5.27 %	3.36 %	0.38 %	3.54 %	7.61 %	4.31 %

Table A.1: ADC gain deviation ΔADC gain for all DCDs double row pattern.

Raw Pedestals vs. ADC Gain



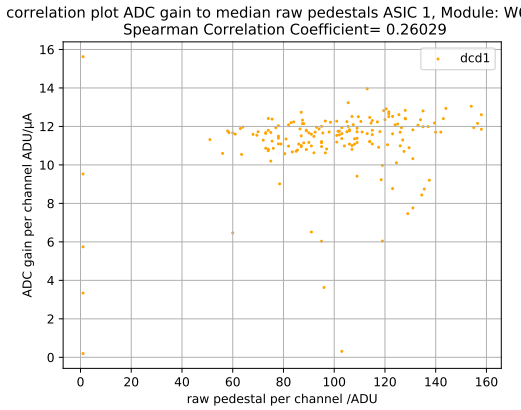
(a) DCD1

(b) DCD2

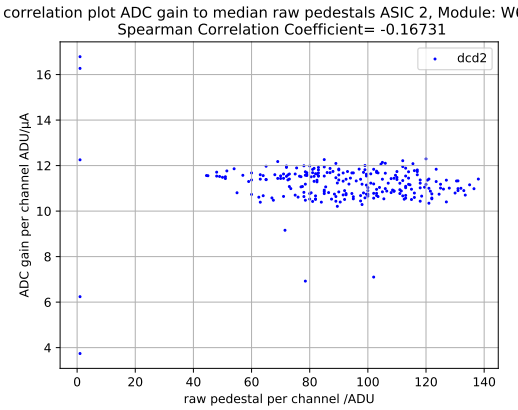
(c) DCD3

(d) DCD4

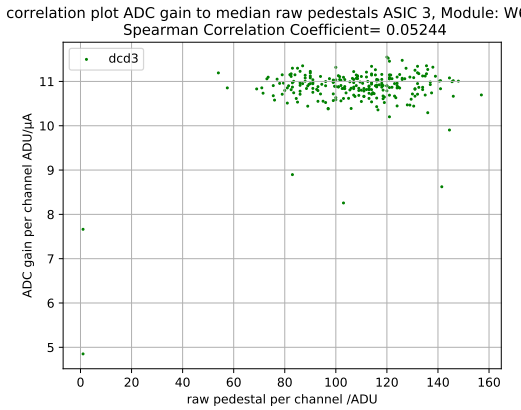
Figure A.18: Correlation plot of median raw pedestals against ADC gain. The Spearman Correlation gives Coefficient gives a quantity of how monotonic the data set behaves. The measurements are done for module W57_IB.



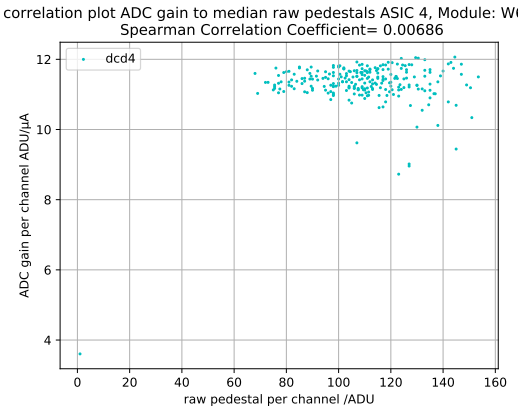
(a) DCD1



(b) DCD2

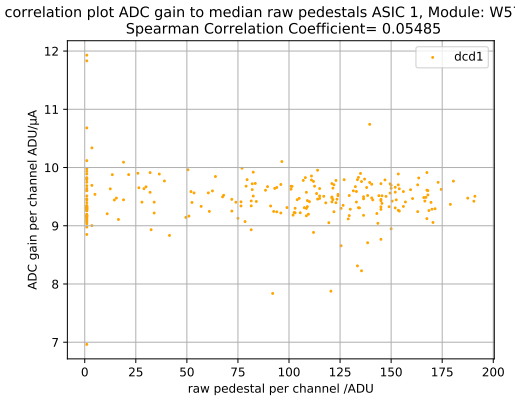


(c) DCD3

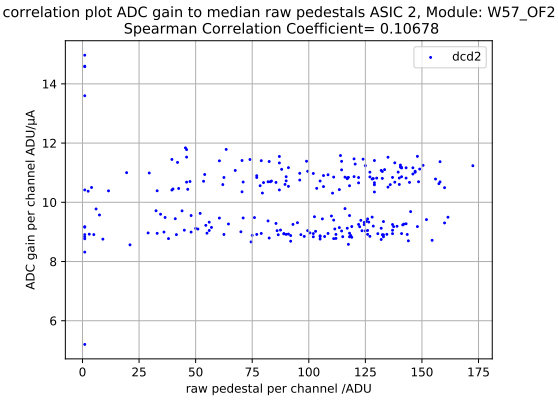


(d) DCD4

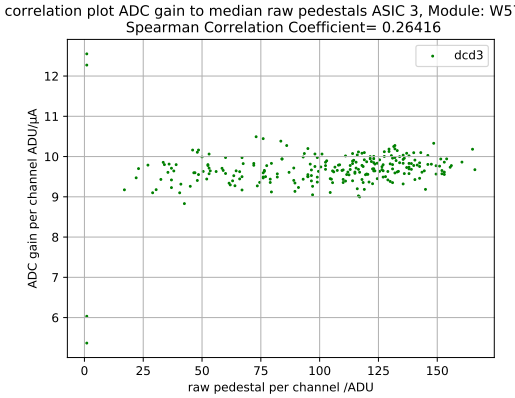
Figure A.19: Correlation plot of median raw pedestals against ADC gain. The Spearman Correlation gives Coefficient gives a quantity of how monotonic the data set behaves. The measurements are done for module W67_IB.



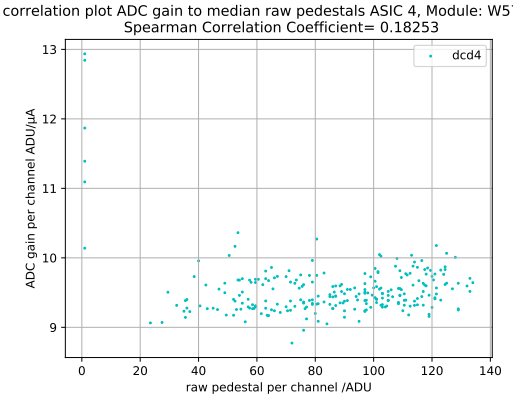
(a) DCD1



(b) DCD2

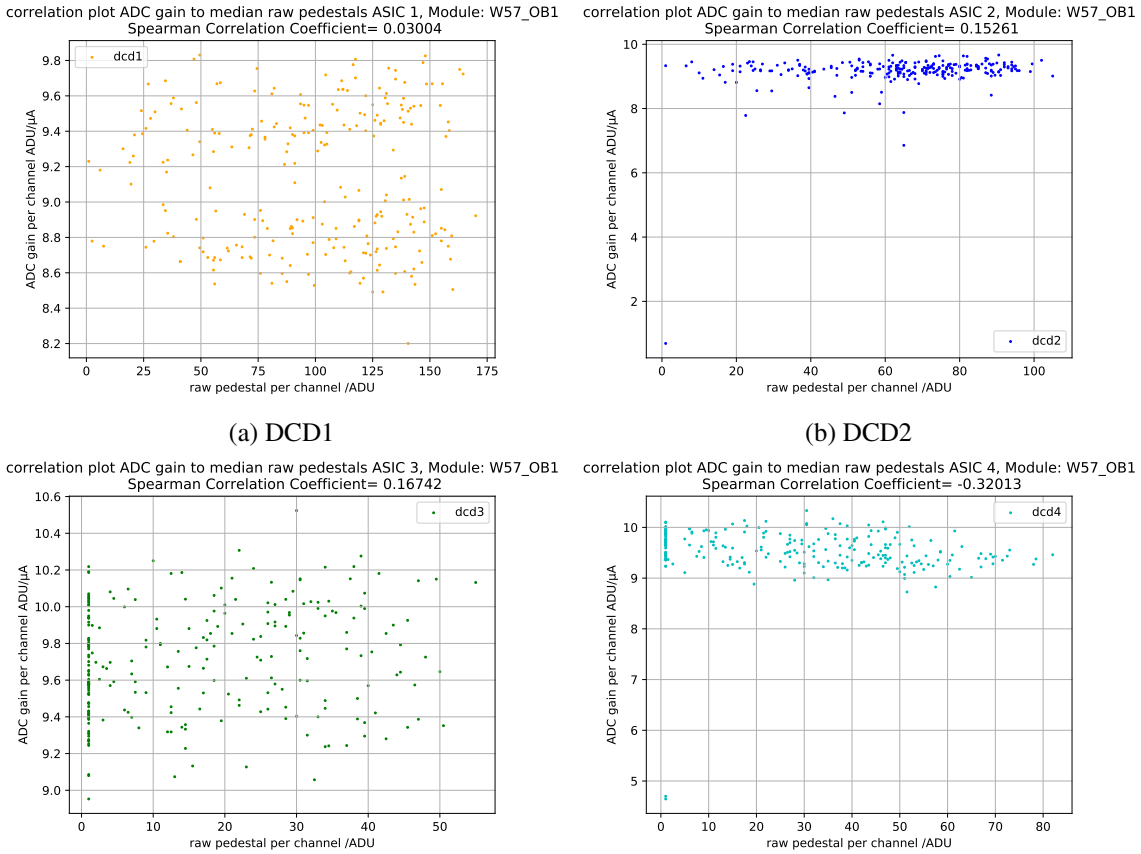


(c) DCD3



(d) DCD4

Figure A.20: Correlation plot of median raw pedestals against ADC gain. The Spearman Correlation gives Coefficient gives a quantity of how monotonic the data set behaves. The measurements are done for module W57_OF2.



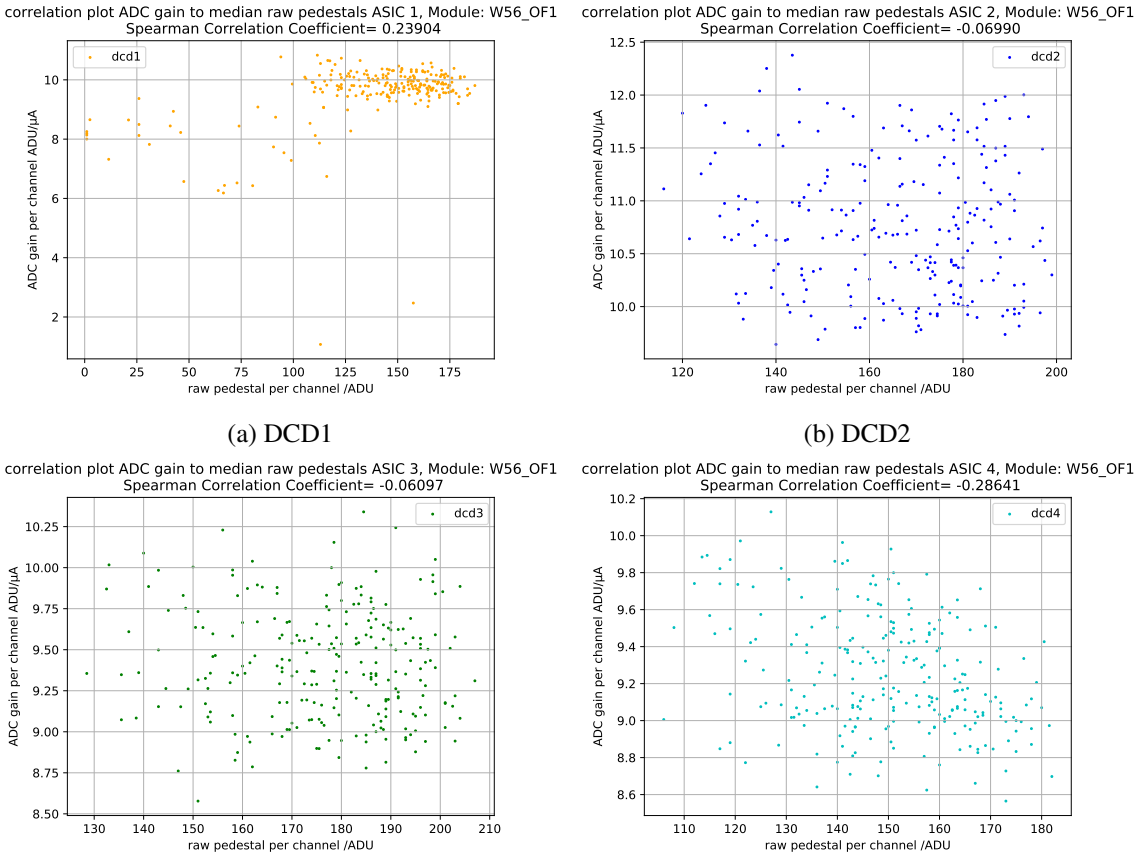
(a) DCD1

(b) DCD2

(c) DCD3

(d) DCD4

Figure A.21: Correlation plot of median raw pedestals against ADC gain. The Spearman Correlation gives Coefficient gives a quantity of how monotonic the data set behaves. The measurements are done for module W57_OB1.



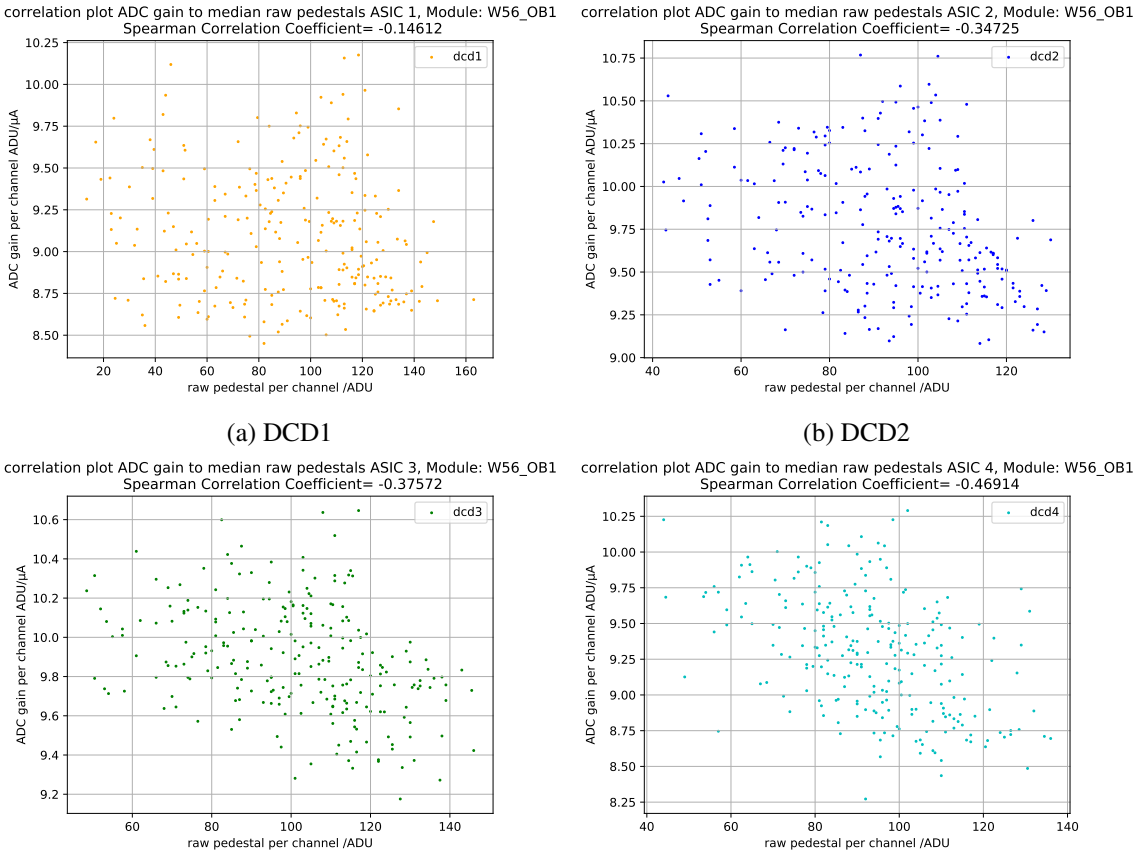
(a) DCD1

(b) DCD2

(c) DCD3

(d) DCD4

Figure A.22: Correlation plot of median raw pedestals against ADC gain. The Spearman Correlation gives Coefficient gives a quantity of how monotonic the data set behaves. The measurements are done for module W56_OF1.



(a) DCD1

(b) DCD2

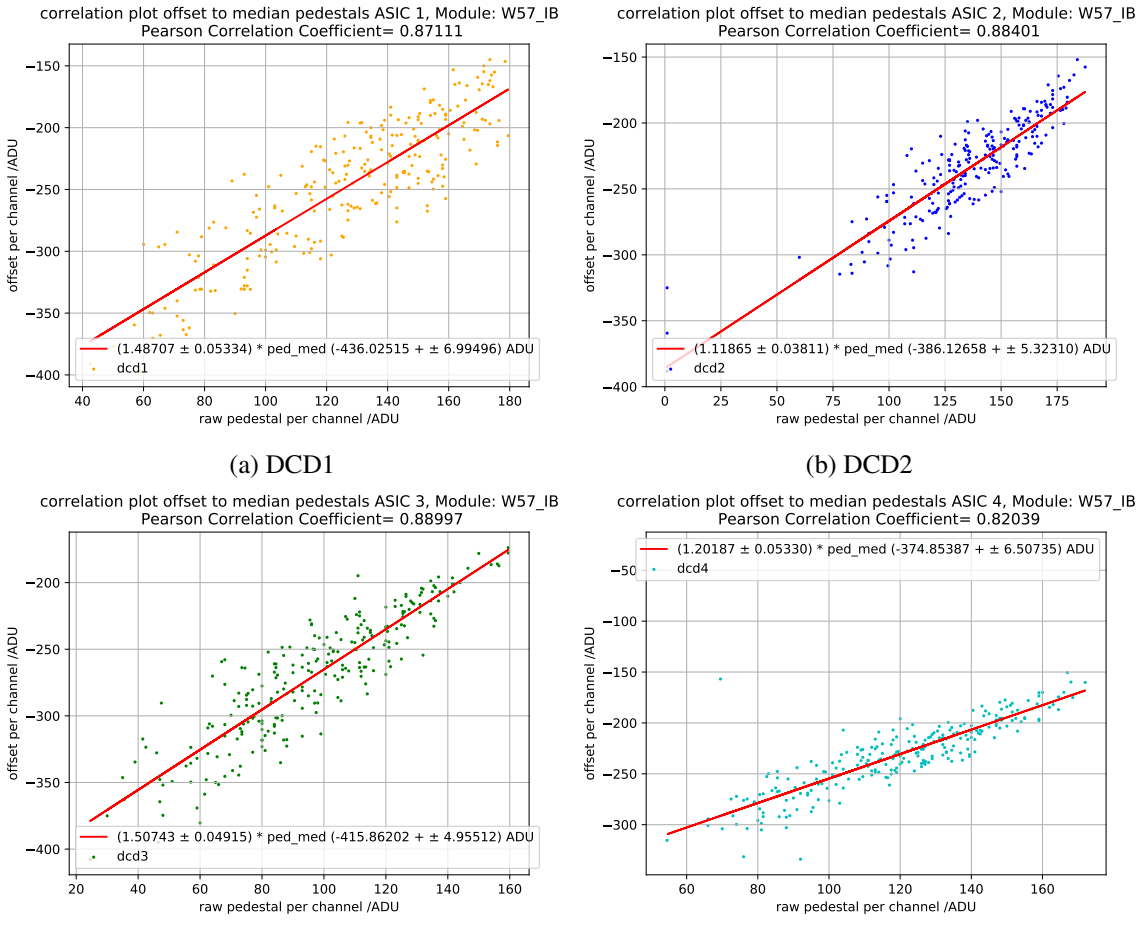
(c) DCD3

(d) DCD4

Figure A.23: Correlation plot of median raw pedestals against ADC gain. The Spearman Correlation gives Coefficient gives a quantity of how monotonic the data set behaves. The measurements are done for module W56_OB1.

A.2.2 Results of Offsets

Comparision to Channels



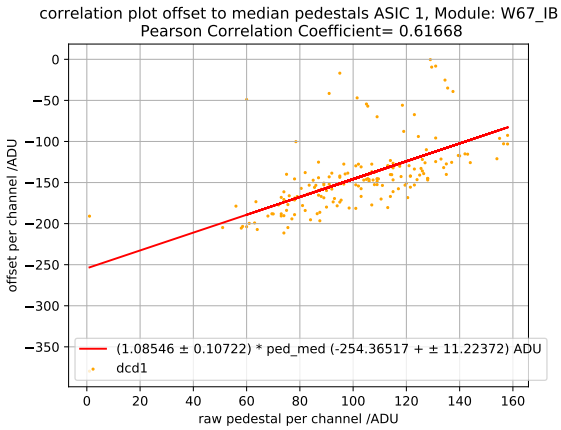
(a) DCD1

(b) DCD2

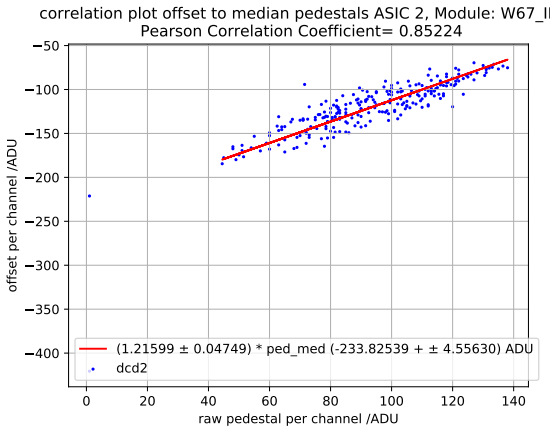
(c) DCD3

(d) DCD4

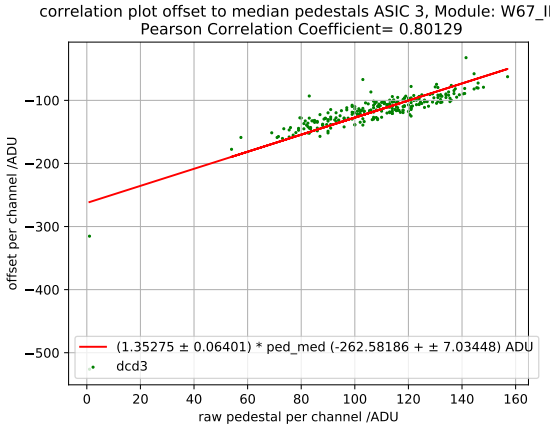
Figure A.24: Correlation plots of median raw pedestals against offsets of ADC transfer curve are shown. The Pearson Correlation Coefficient gives a quantity of how linear the data set behaves. The measurements are done for module W57_IB.



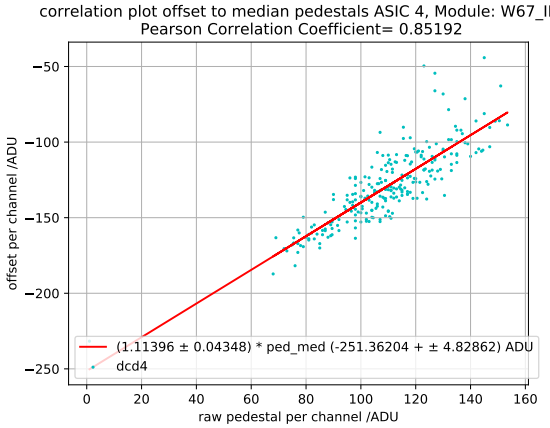
(a) DCD1



(b) DCD2

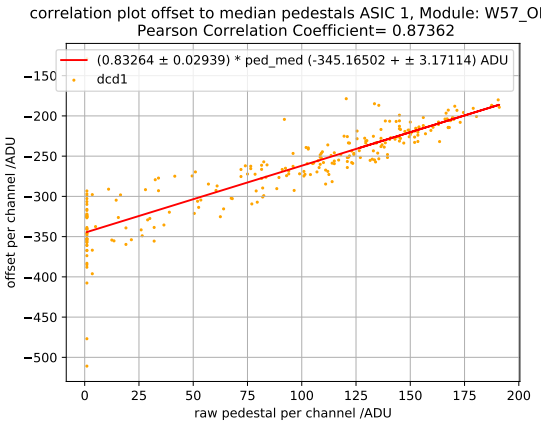


(c) DCD3

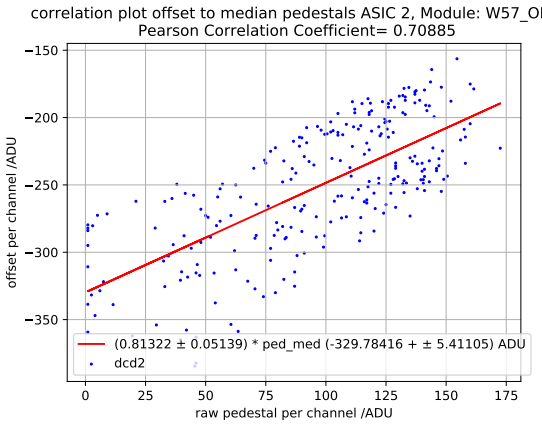


(d) DCD4

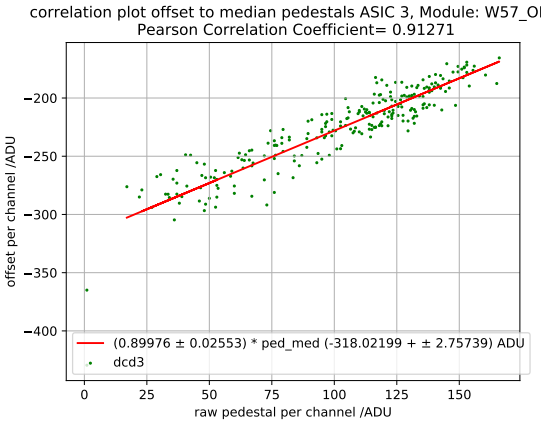
Figure A.25: Correlation plots of median raw pedestals against offsets of ADC transfer curve are shown. The Pearson Correlation Coefficient gives a quantity of how linear the data set behaves. The measurements are done for module W67_IB.



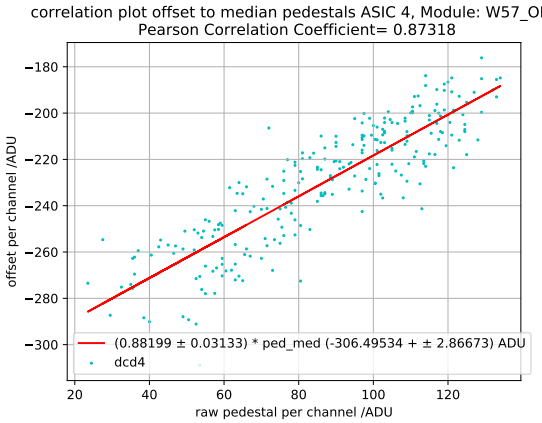
(a) DCD1



(b) DCD2

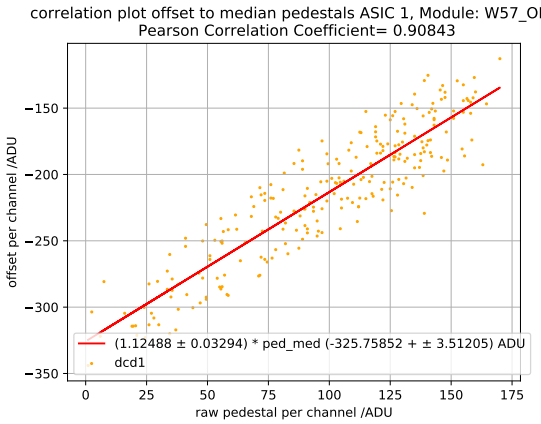


(c) DCD3

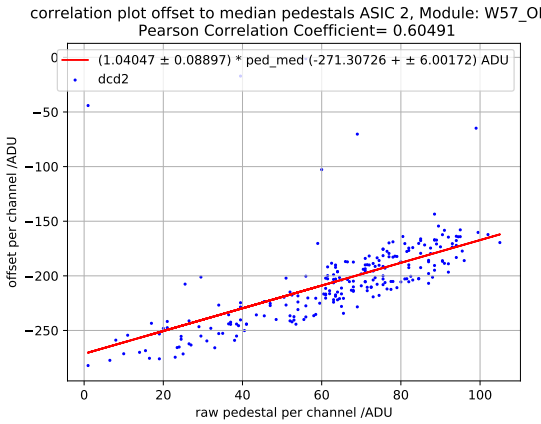


(d) DCD4

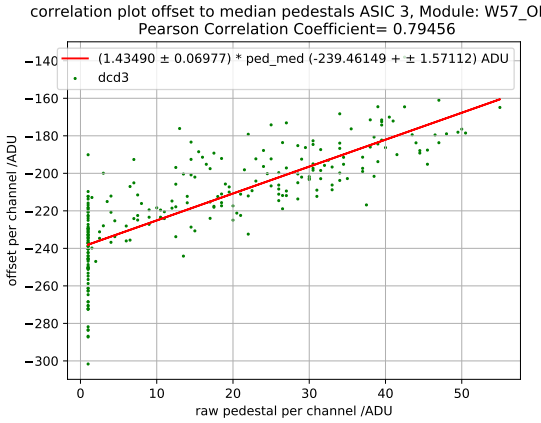
Figure A.26: Correlation plots of median raw pedestals against offsets of ADC transfer curve are shown. The Pearson Correlation Coefficient gives a quantity of how linear the data set behaves. The measurements are done for module W57_OF2.



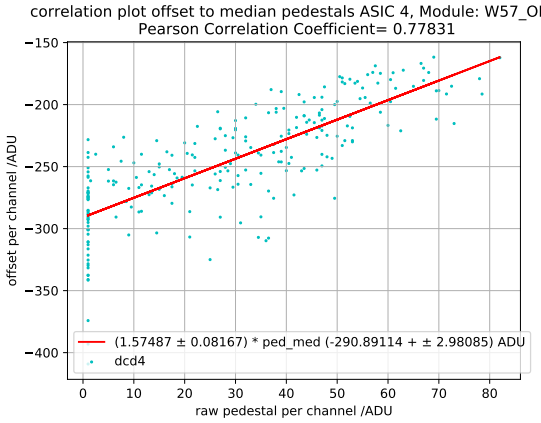
(a) DCD1



(b) DCD2

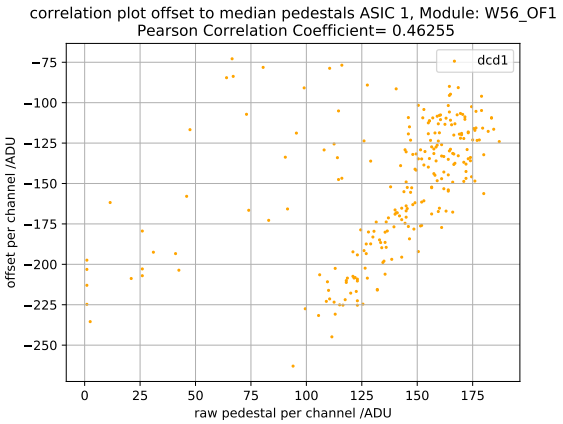


(c) DCD3

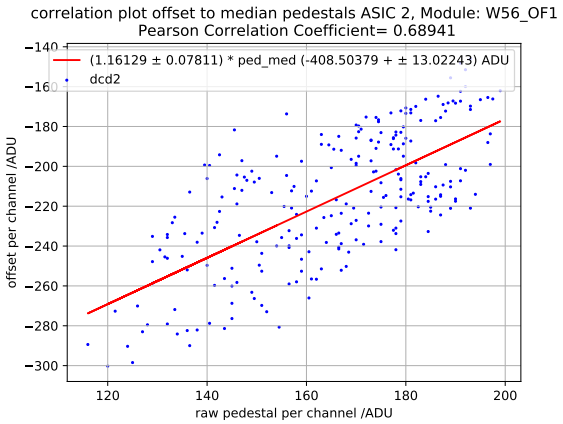


(d) DCD4

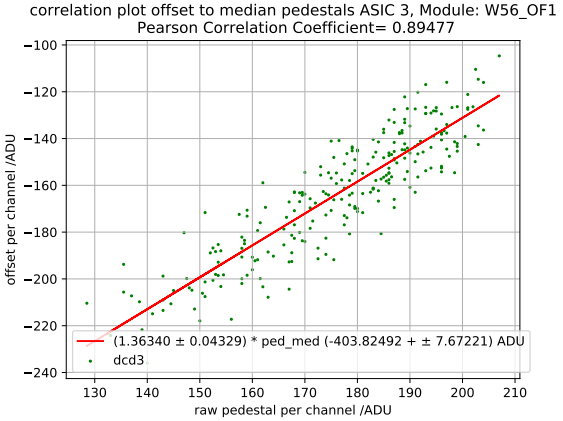
Figure A.27: Correlation plots of median raw pedestals against offsets of ADC transfer curve are shown. The Pearson Correlation Coefficient gives a quantity of how linear the data set behaves. The measurements are done for module W57_OB1.



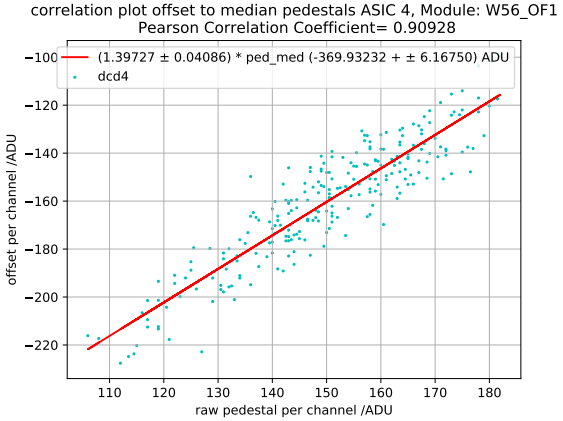
(a) DCD1



(b) DCD2

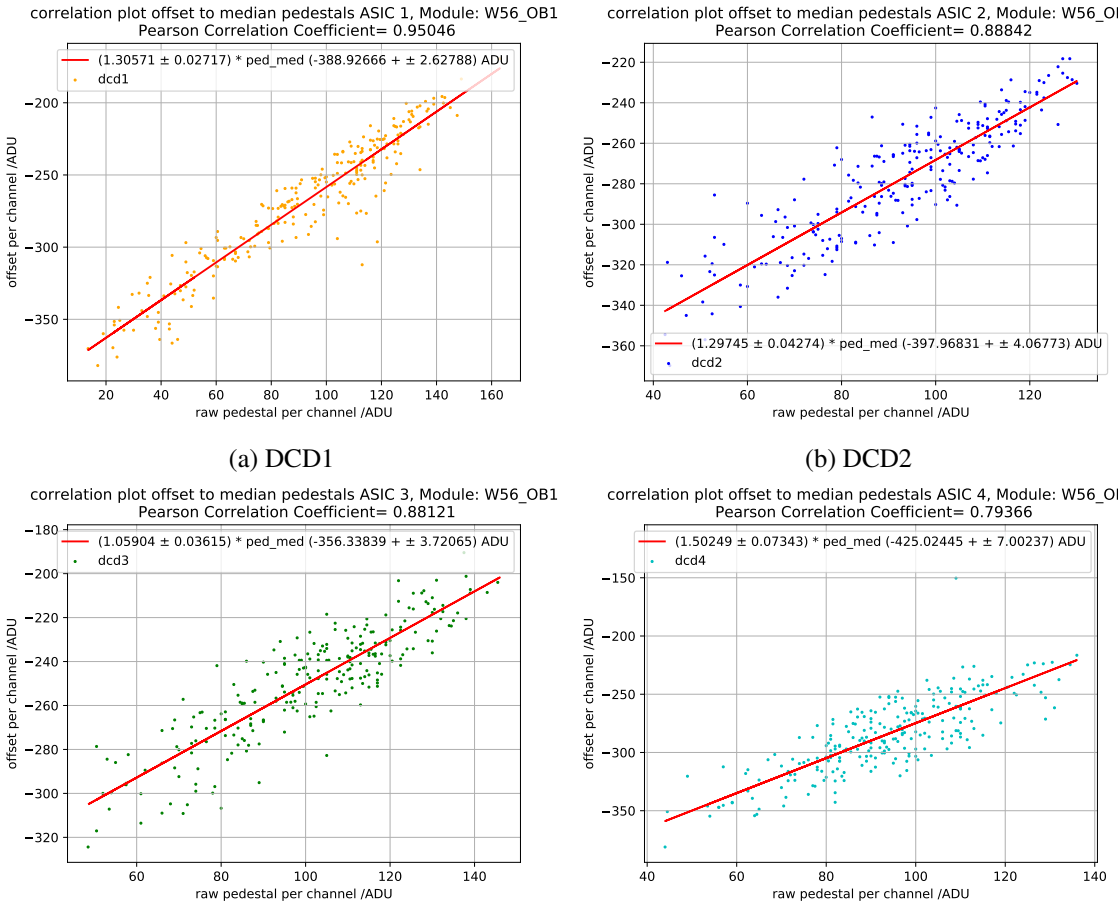


(c) DCD3



(d) DCD4

Figure A.28: Correlation plots of median raw pedestals against offsets of ADC transfer curve are shown. The Pearson Correlation Coefficient gives a quantity of how linear the data set behaves. The measurements are done for module W56_OF1.



(a) DCD1

(b) DCD2

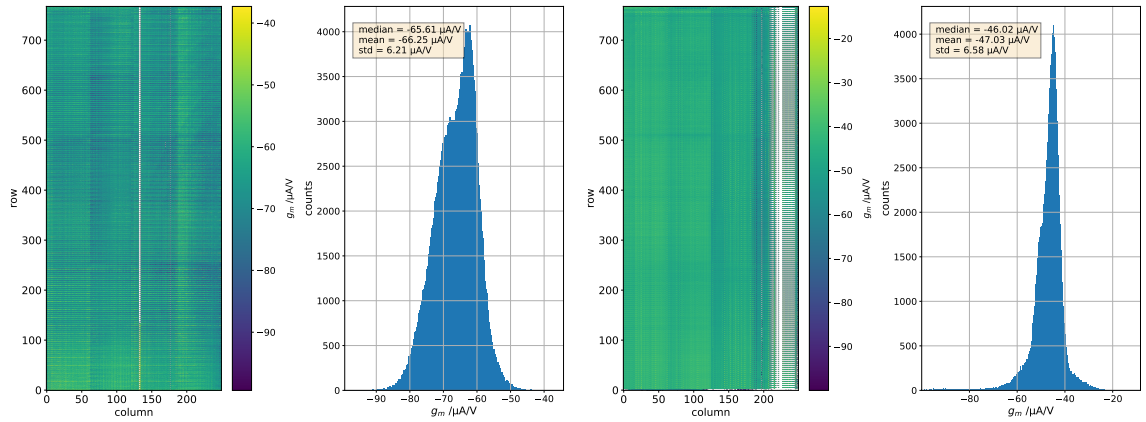
(c) DCD3

(d) DCD4

Figure A.29: Correlation plots of median raw pedestals against offsets of ADC transfer curve are shown. The Pearson Correlation Coefficient gives a quantity of how linear the data set behaves. The measurements are done for module W56_OB1.

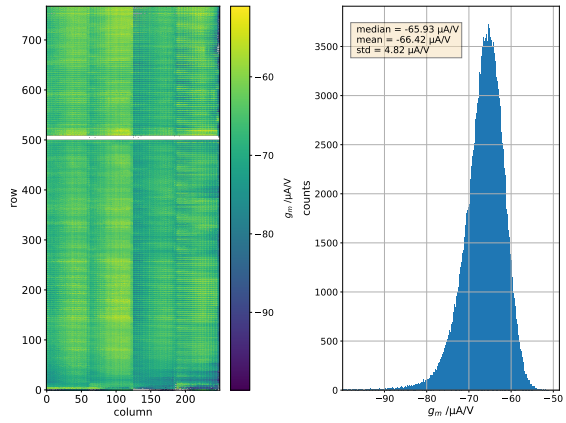
A.3 Transconductance

A.3.1 Comparison to all pixels

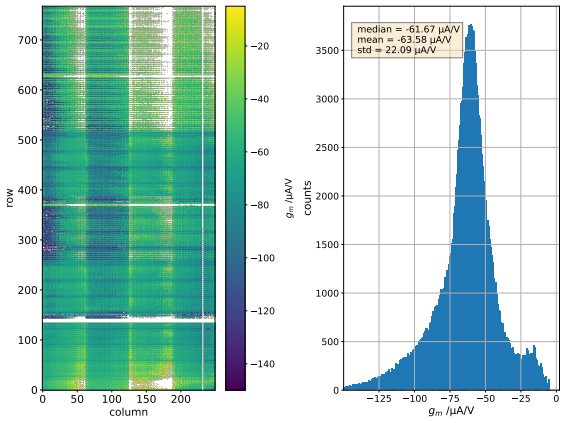


(a) Module W57_IB.

(b) Module W67_IB.

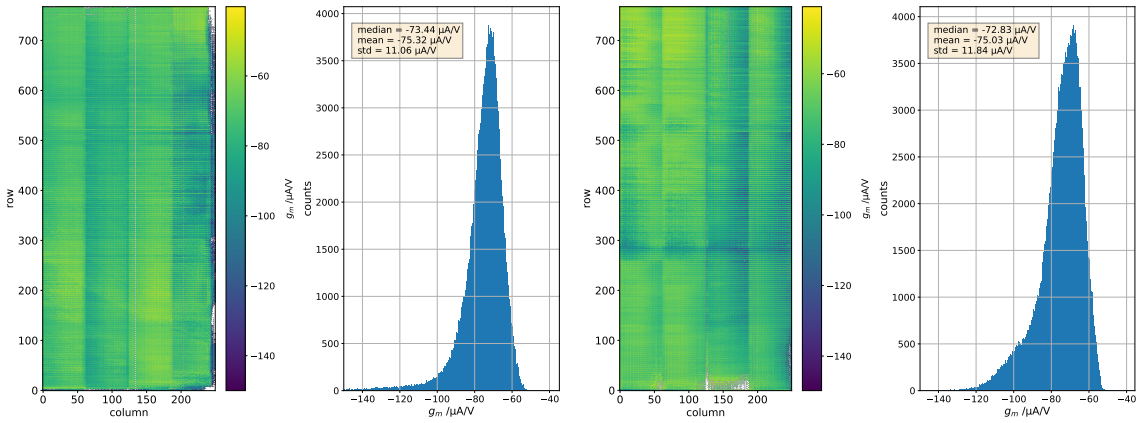


(c) Module W57_OF2.



(d) Module W57_OB1.

Figure A.30: The values of the uncorrelated transconductance for each pixels are shown. In the left plot the values are distributed in the pxd9 matrix of the module. The transconductance is depicted for each channel via the color code on its geometrical position inside the DEPFET matrix. On the right the incidence of the values for each pixel is plotted. On measurements in pixels marked in white no drain current was measured. Thus not the entire dynmaic range for every pixel was measured.

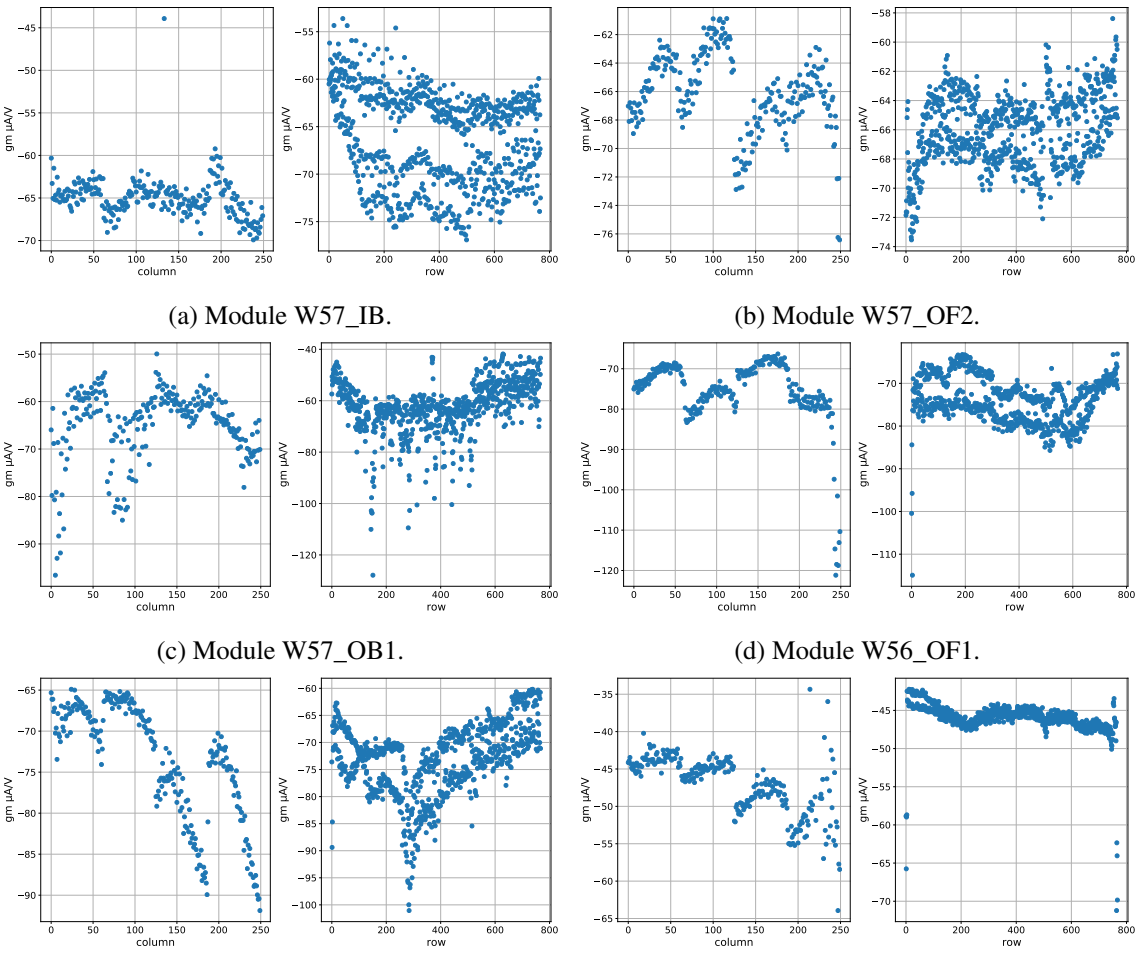


(a) Module W56_OF1.

(b) Module W56_OB1.

Figure A.31: The values of the uncorrelated transconductance for each pixels are shown. In the left plot the values are distributed in the pxd9 matrix of the module. The transconductance is depicted for each channel via the color code on its geometrical position inside the DEPFET matrix. On the right the incidence of the values for each pixel is plotted. On measurements in pixels marked in white no drain current was measured. Thus not the entire dynmaic range for every pixel was measured.

A.3.2 Projection Transconductance



(a) Module W57_IB.

(b) Module W57_OF2.

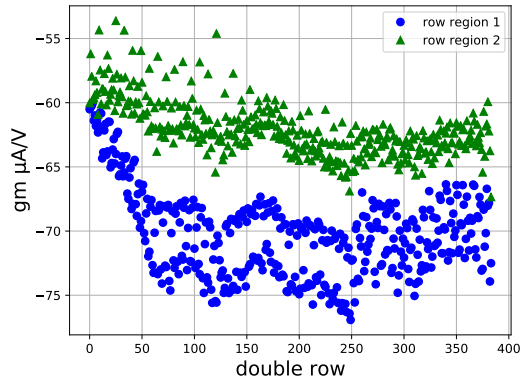
(c) Module W57_OB1.

(d) Module W56_OF1.

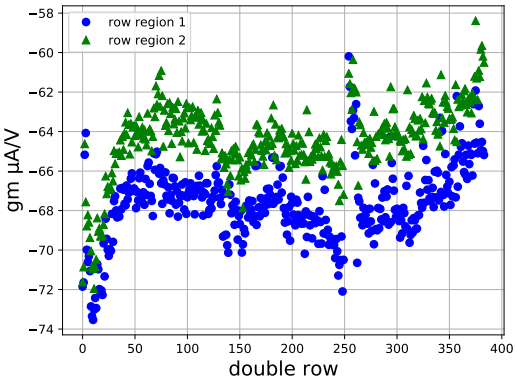
(e) Module W56_OB1.

(f) Module W67_IB.

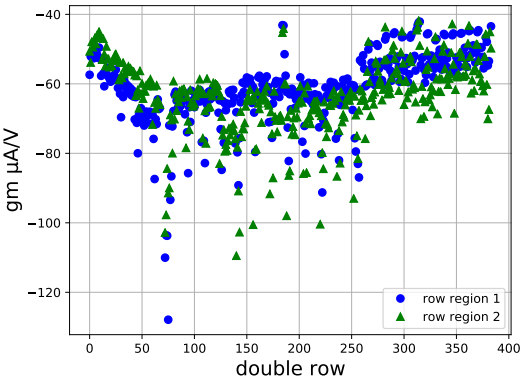
Figure A.32: Projection of values of the transconductance along the column and the row axes



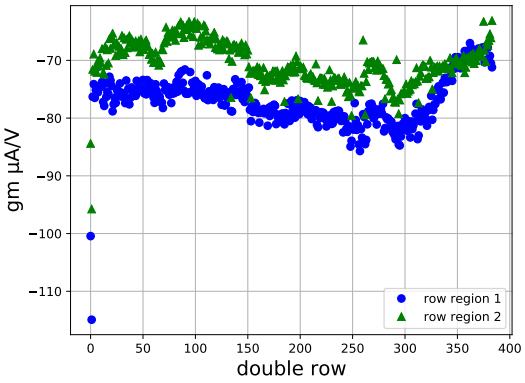
(a) Module W57_IB.



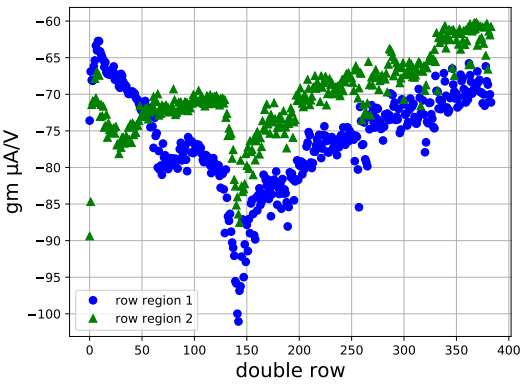
(b) Module W57_OF2.



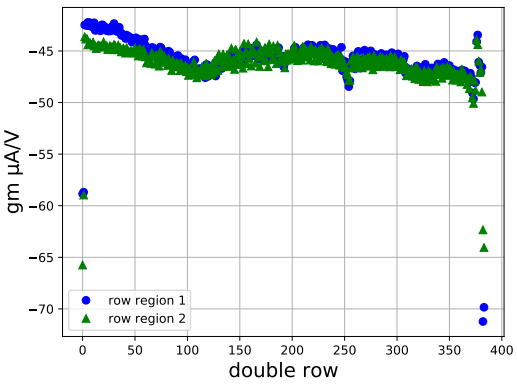
(c) Module W57_OB1.



(d) Module W56_OF1.



(e) Module W56_OB1.



(f) Module W67_IB.

Figure A.33: Projection of values of the transconductance along double row axes where the two different double rows are marked.

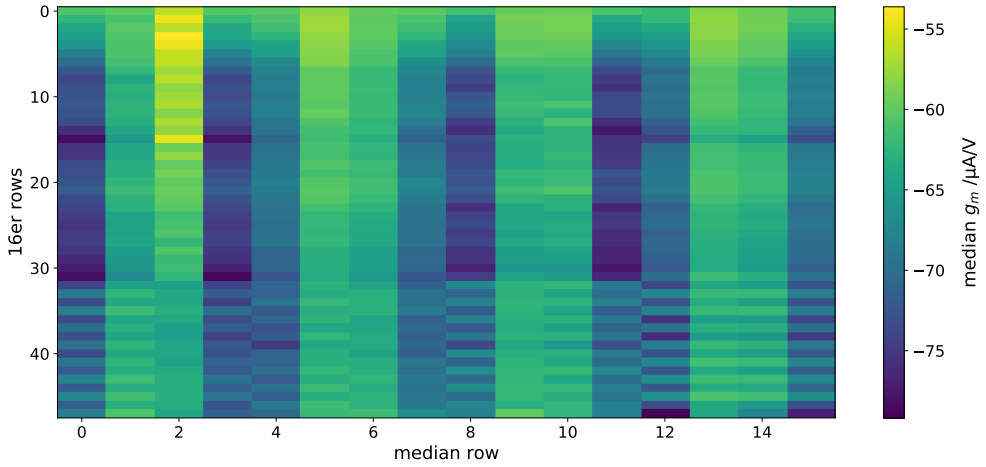


Figure A.34: Projection of the rows for module W57_IB stacked on each other in 16 steps. For the module, the small pixels are located from [0, 32] to [15, 47).

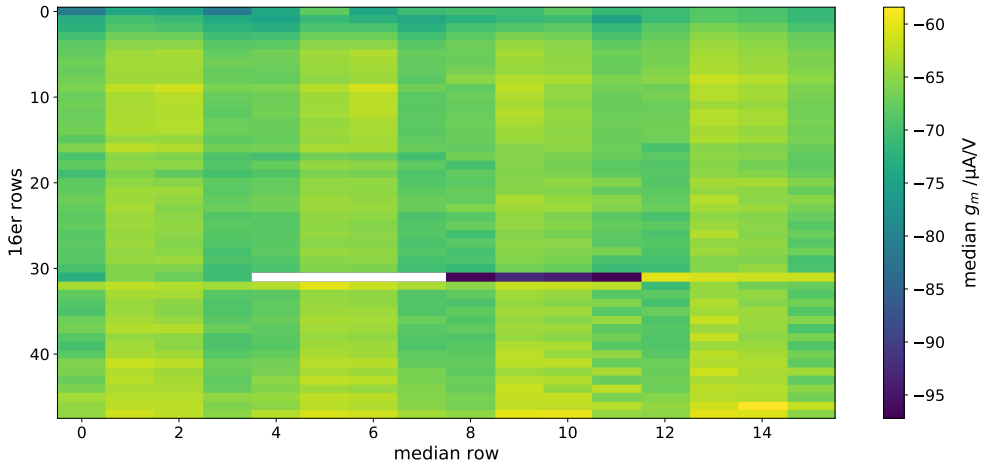


Figure A.35: Projection of the rows for module W57_OF2 stacked on each other in 16 steps. For the module, the small pixels are located from [0, 0] to [15, 15).

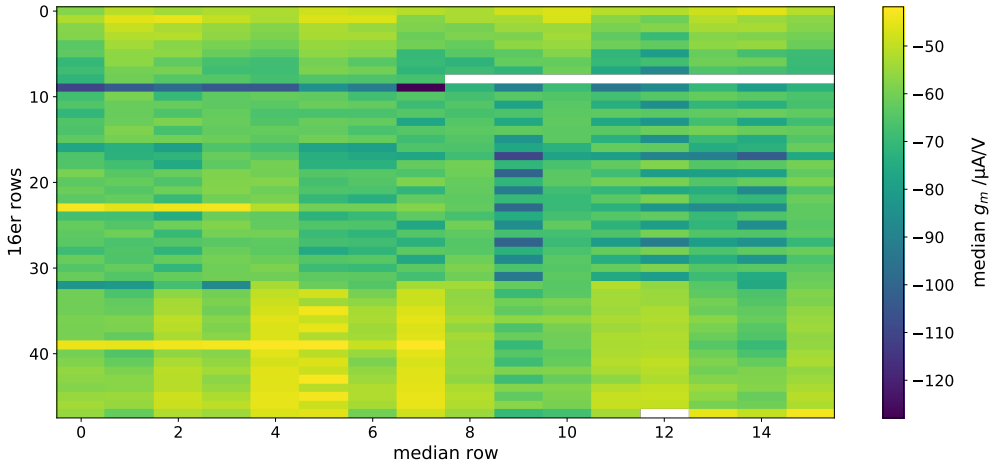


Figure A.36: Projection of the rows for module W57_OB1 stacked on each other in 64 steps. For the module, the small pixels are located from $[0, 32]$ to $[15, 47)$.

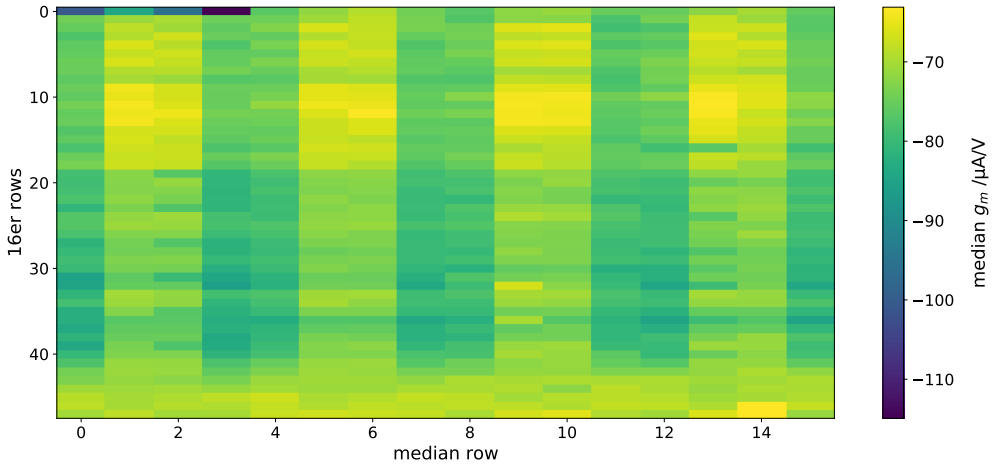


Figure A.37: Projection of the rows for module W56_OF1 stacked on each other in 12 steps. For the module, the small pixels are located from $[0, 0]$ to $[15, 15)$.

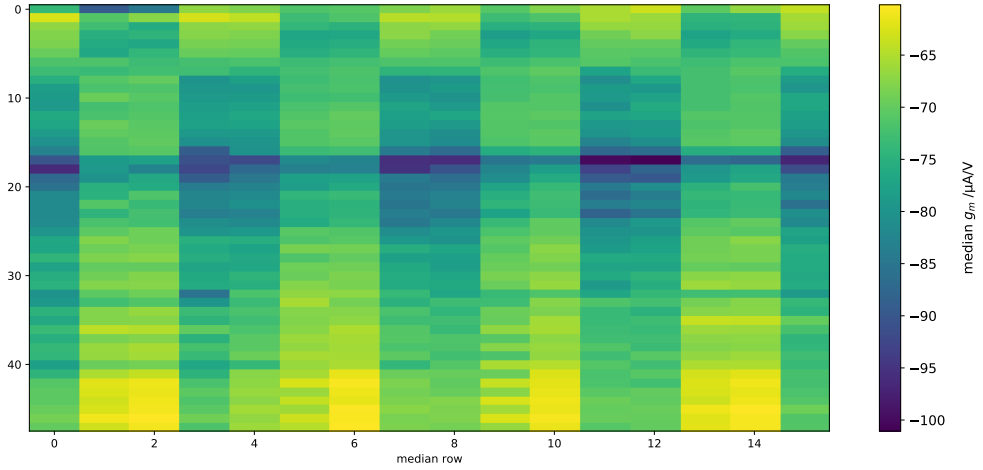


Figure A.38: Projection of the rows for module W56_OB1 stacked on each other in 16 steps. For the module, the small pixels are located from $[0, 8]$ to $[63, 11)$.

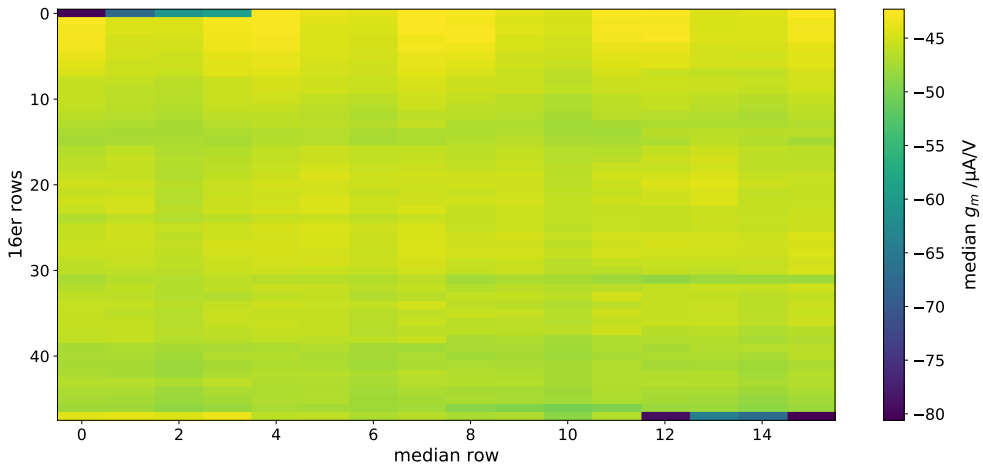
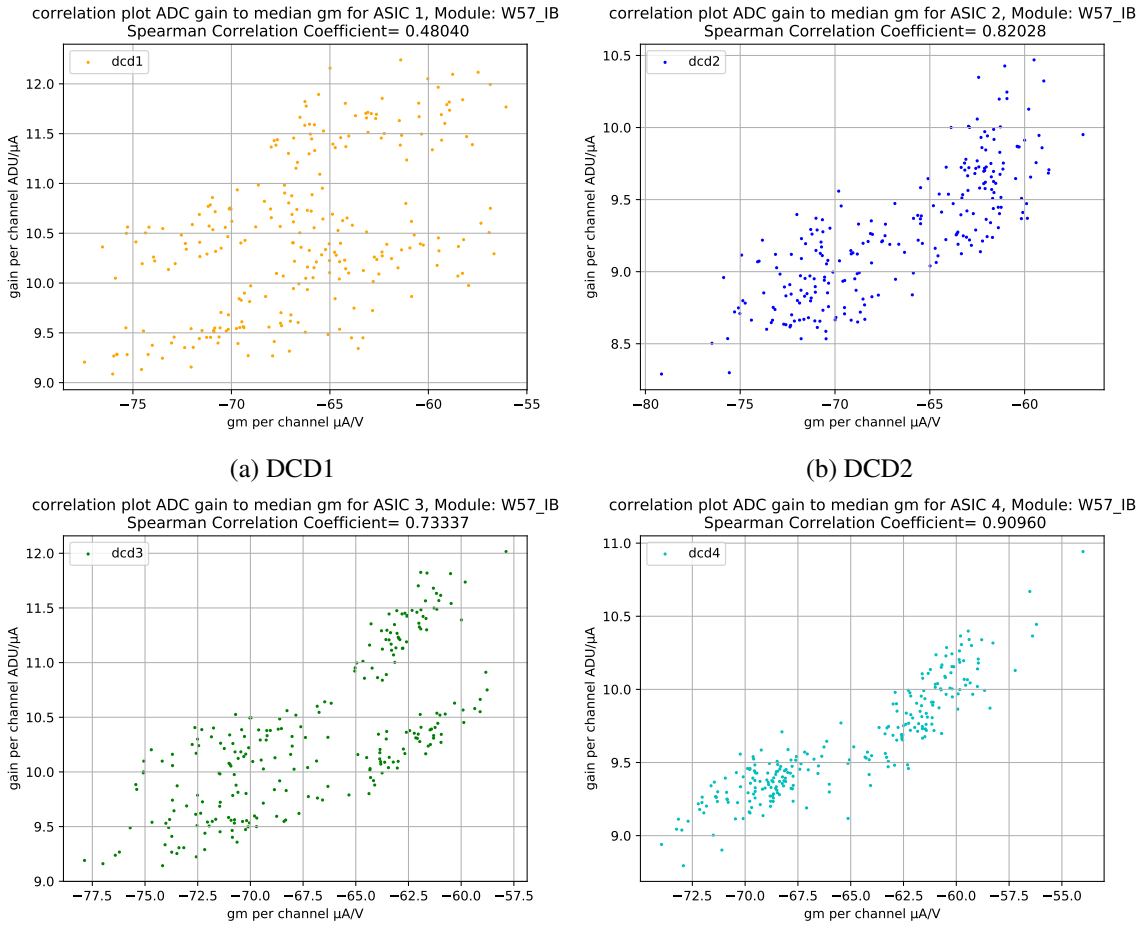


Figure A.39: Projection of the rows for module W67_IB stacked on each other in 16 steps. For the module, the small pixels are located from $[0, 32]$ to $[15, 47)$.

A.3.3 Transconductance vs. ADC Gain



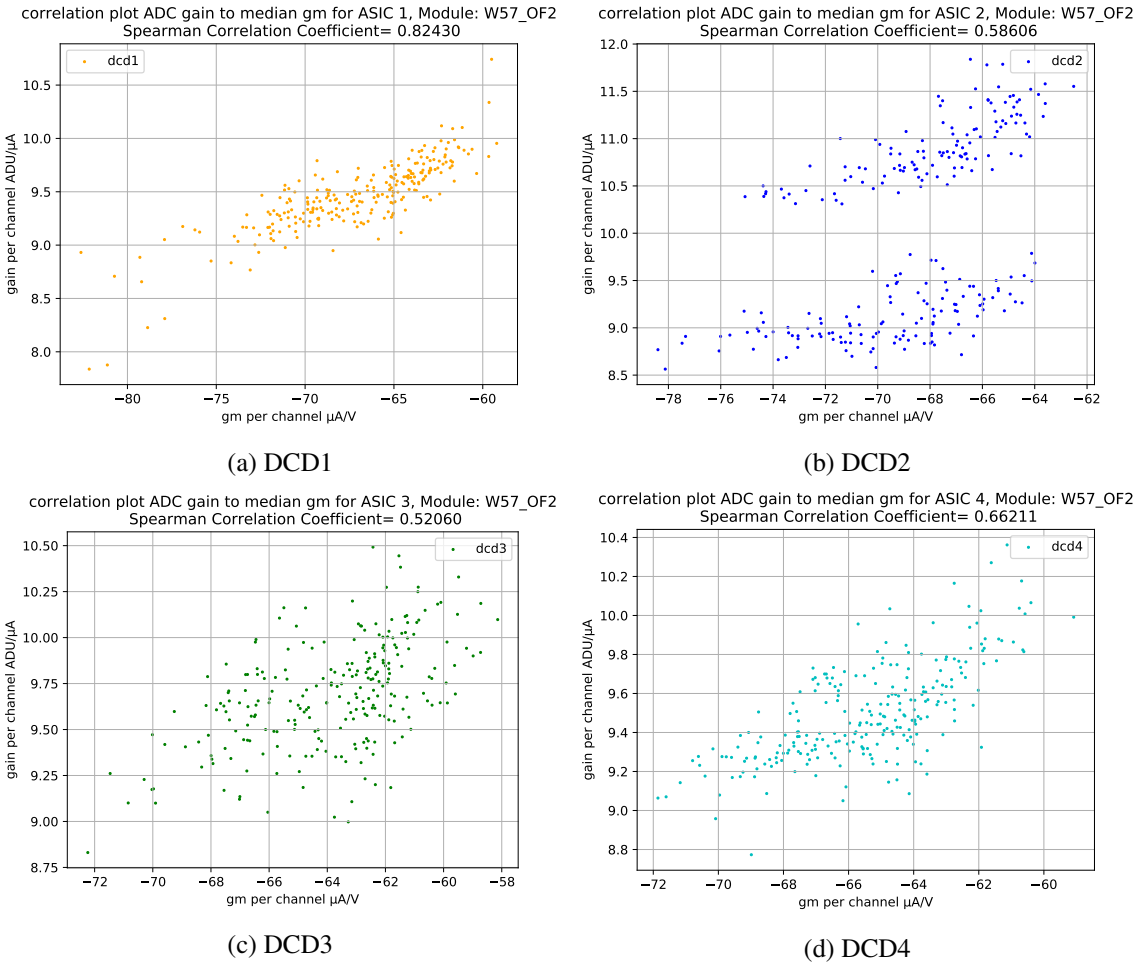
(a) DCD1

(b) DCD2

(c) DCD3

(d) DCD4

Figure A.40: The transconductance extracted out of the DEPFET IV Scan vs. the ADC Gain out of the ADC Transfer curves for module W57_IB. The Spearman Correlation Coefficient gives a quantity on how monotonic the two data sets are.



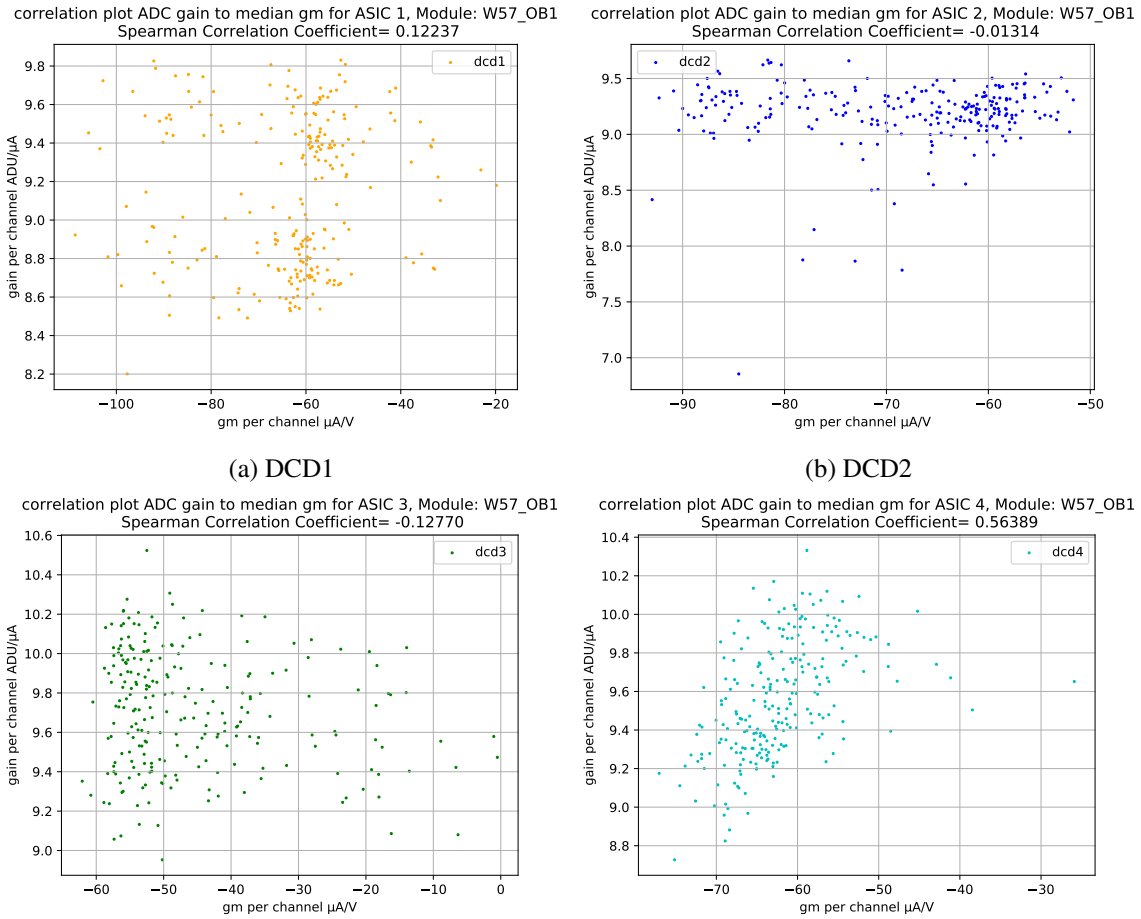
(a) DCD1

(b) DCD2

(c) DCD3

(d) DCD4

Figure A.41: The transconductance extracted out of the DEPFET IV Scan vs. the ADC Gain out of the ADC Transfer curves for module W57_OF2. The Spearman Correlation Coefficient gives a quantity on how monotonic the two data sets are.



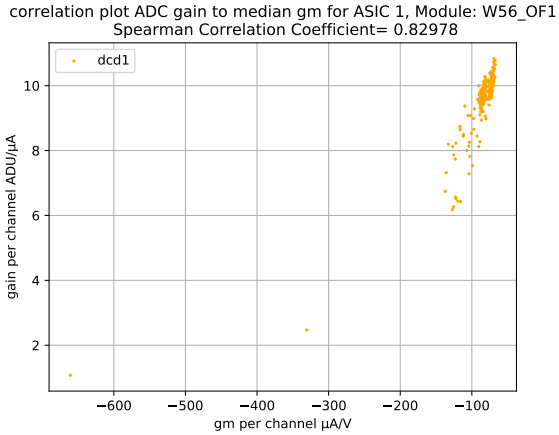
(a) DCD1

(b) DCD2

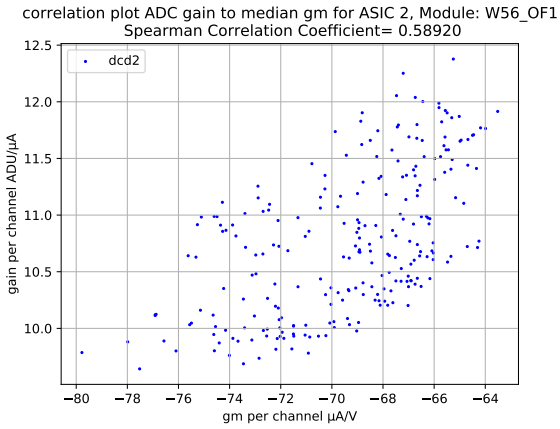
(c) DCD3

(d) DCD4

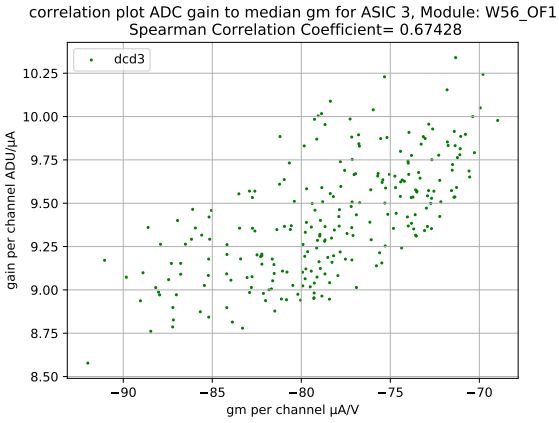
Figure A.42: The transconductance extracted out of the DEPFET IV Scan vs. the ADC Gain out of the ADC Transfer curves for module W57_OB1. The Spearman Correlation Coefficient gives a quantity on how monotonic the two data sets are.



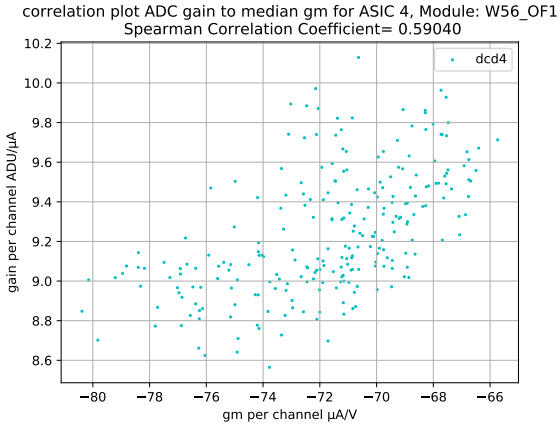
(a) DCD1



(b) DCD2

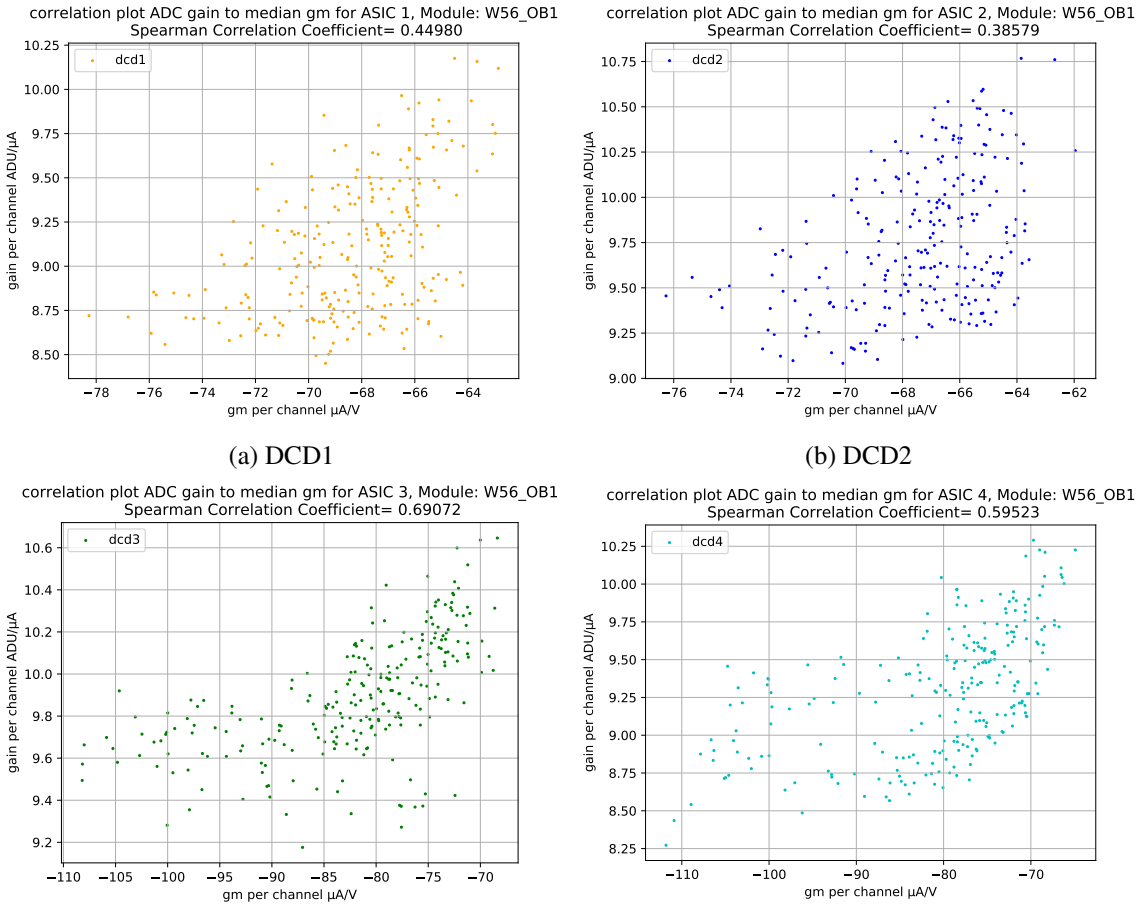


(c) DCD3



(d) DCD4

Figure A.43: The transconductance extracted out of the DEPFET IV Scan vs. the ADC Gain out of the ADC Transfer curves for module W56_OF1. The Spearman Correlation Coefficient gives a quantity on how monotonic the two data sets are.



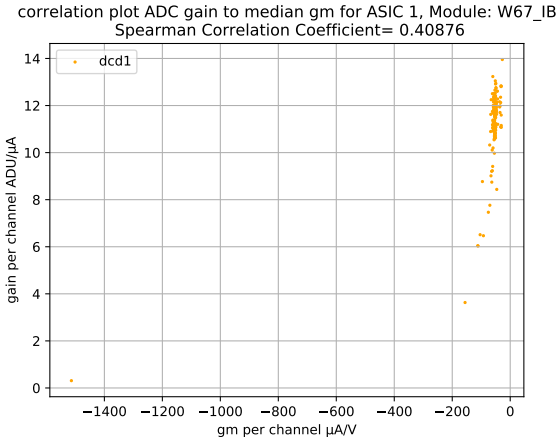
(a) DCD1

(b) DCD2

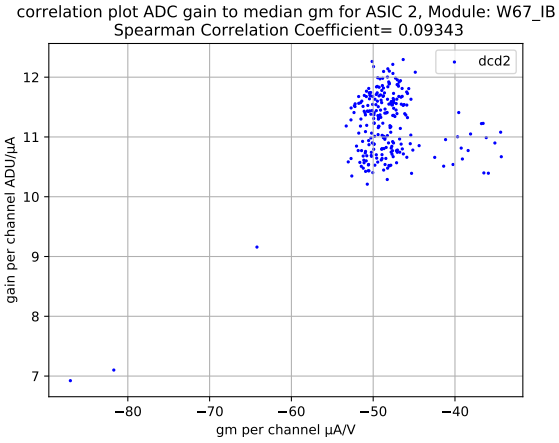
(c) DCD3

(d) DCD4

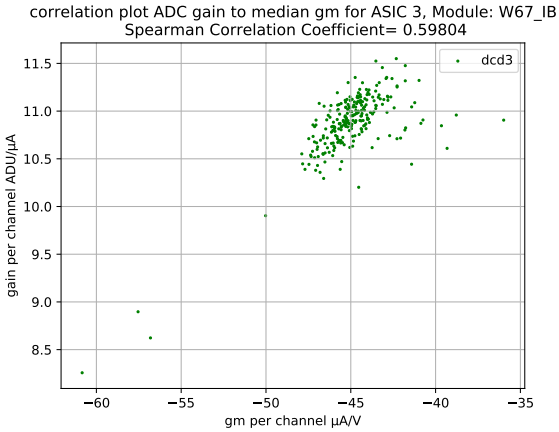
Figure A.44: The transconductance extracted out of the DEPFET IV Scan vs. the ADC Gain out of the ADC Transfer curves for module W56_OB1. The Spearman Correlation Coefficient gives a quantity on how monotonic the two data sets are.



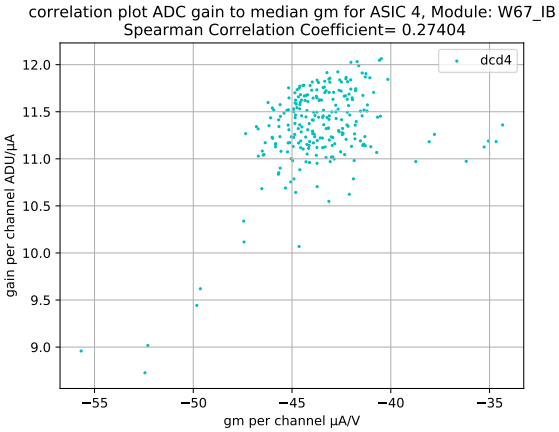
(a) DCD1



(b) DCD2



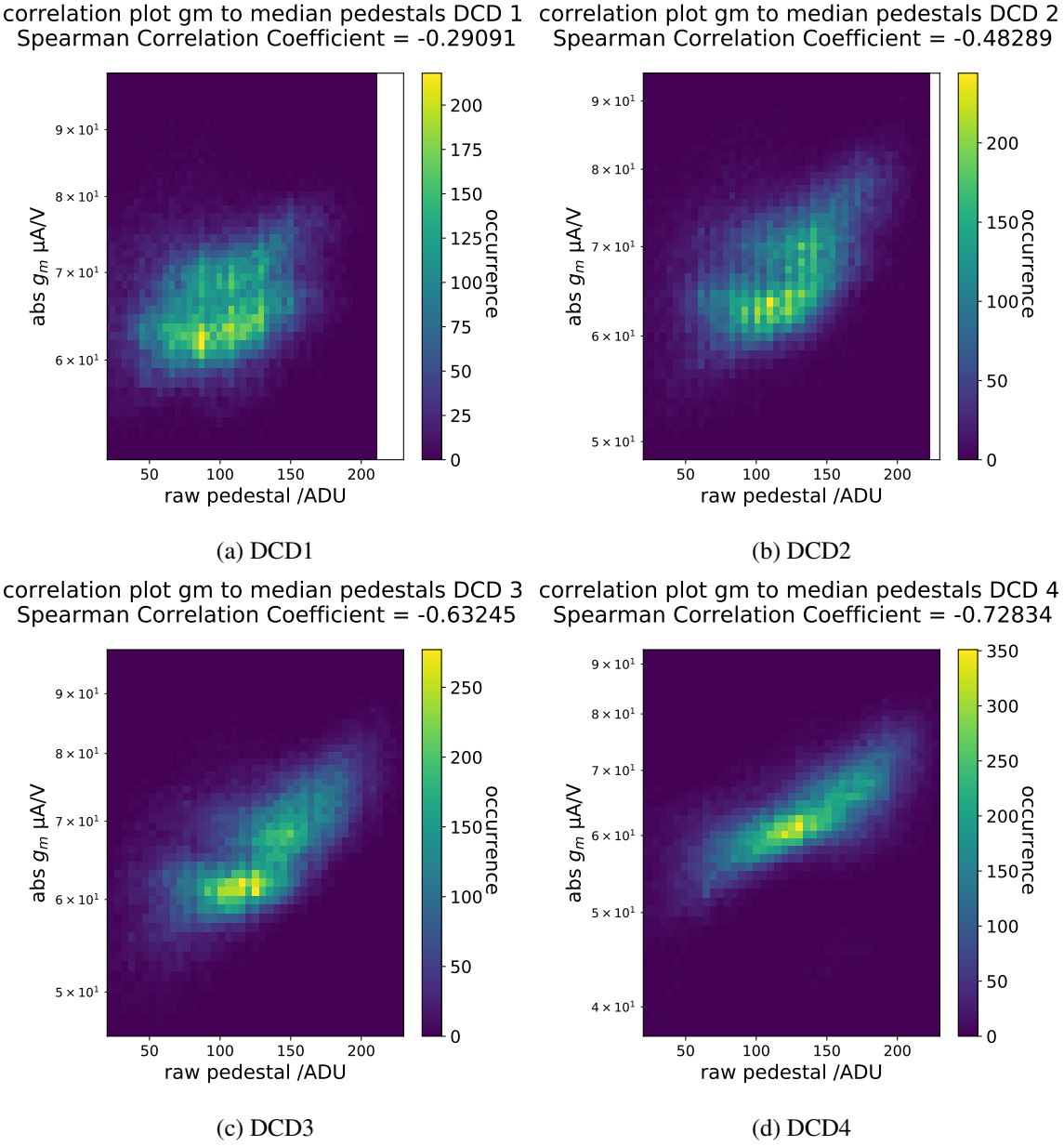
(c) DCD3



(d) DCD4

Figure A.45: The transconductance extracted out of the DEPFET IV Scan vs. the ADC Gain out of the ADC Transfer curves for module W67_IB. The Spearman Correlation Coefficient gives a quantity on how monotonic the two data sets are.

A.3.4 Transconductance vs. raw Pedestals



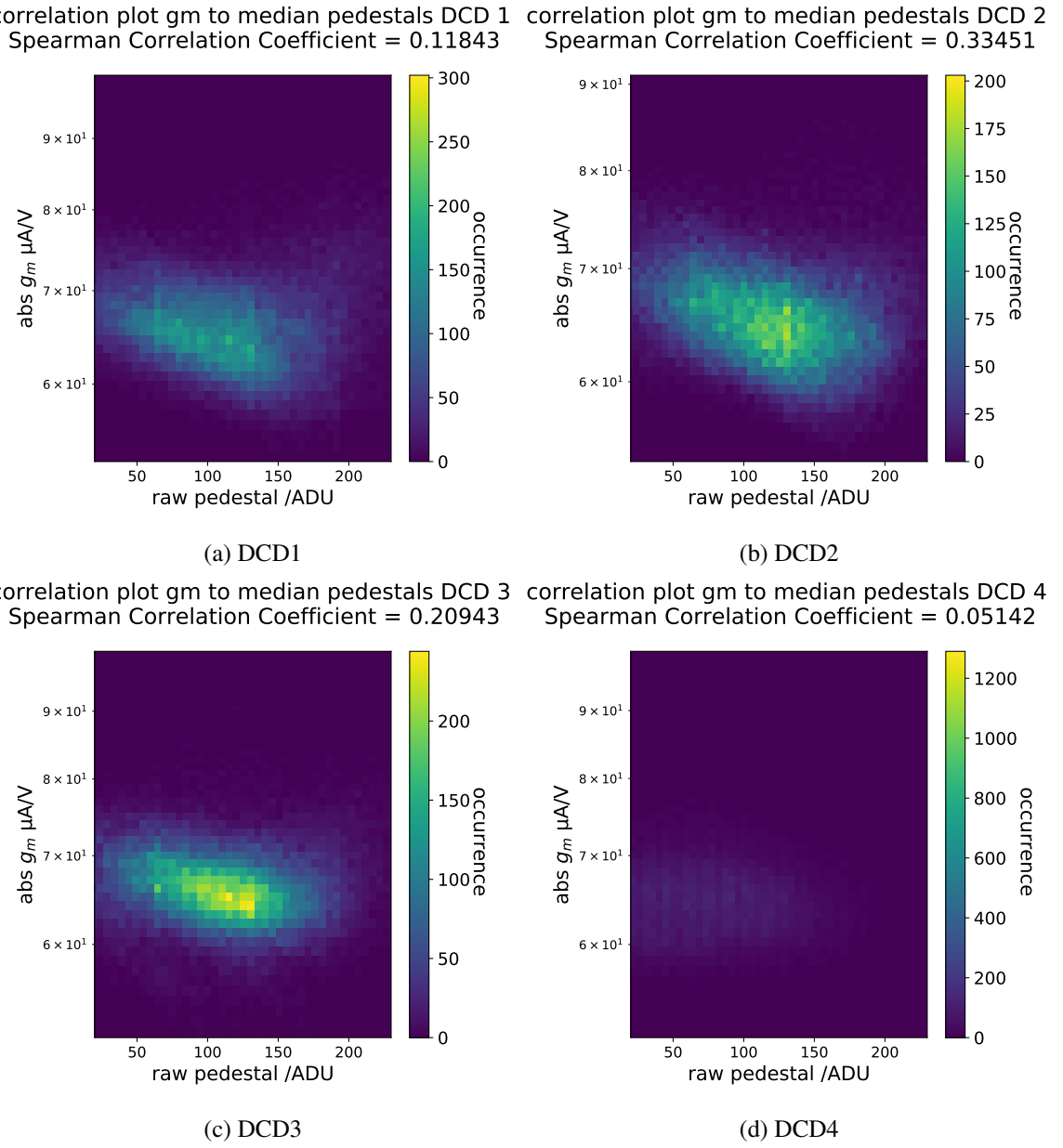
(a) DCD1

(b) DCD2

(c) DCD3

(d) DCD4

Figure A.46: The transconductance extracted out of the DEPFET IV Scan vs. the raw Pedestal values per pixel for module W57_IB. The right plot shows the occurrence of the correlation values. The pedestal distribution is measured without applied ACMC and Offsets. The Spearman Correlation Coefficient gives a quantity on how monotonic the two data sets are.



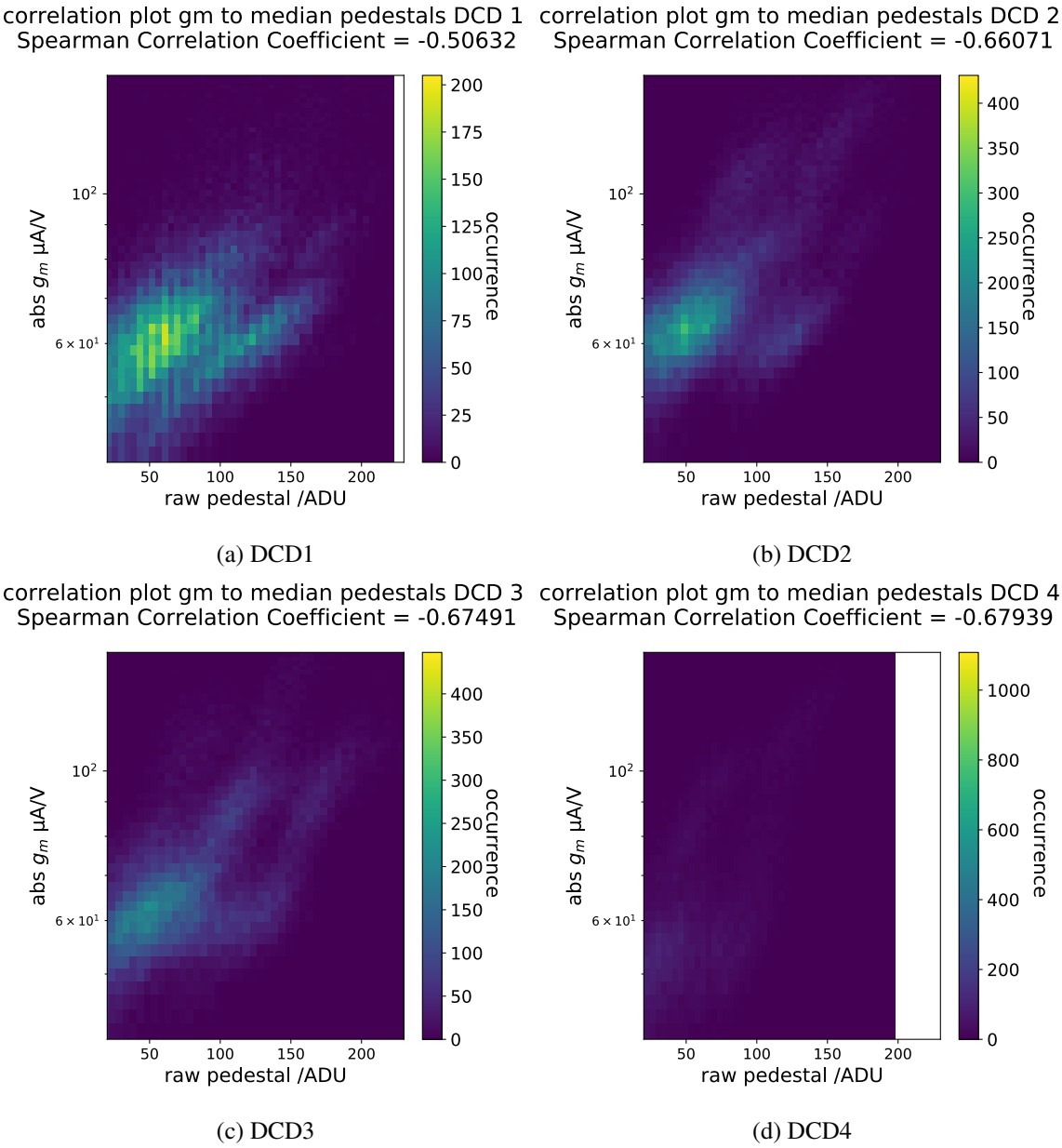
(a) DCD1

(b) DCD2

(c) DCD3

(d) DCD4

Figure A.47: The transconductance extracted out of the DEPFET IV Scan vs. the raw Pedestal values per pixel for module W57_OF2. The right plot shows the occurrence of the correlation values. The pedestal distribution is measured without applied ACMC and Offsets. The Spearman Correlation Coefficient gives a quantity on how monotonic the two data sets are.



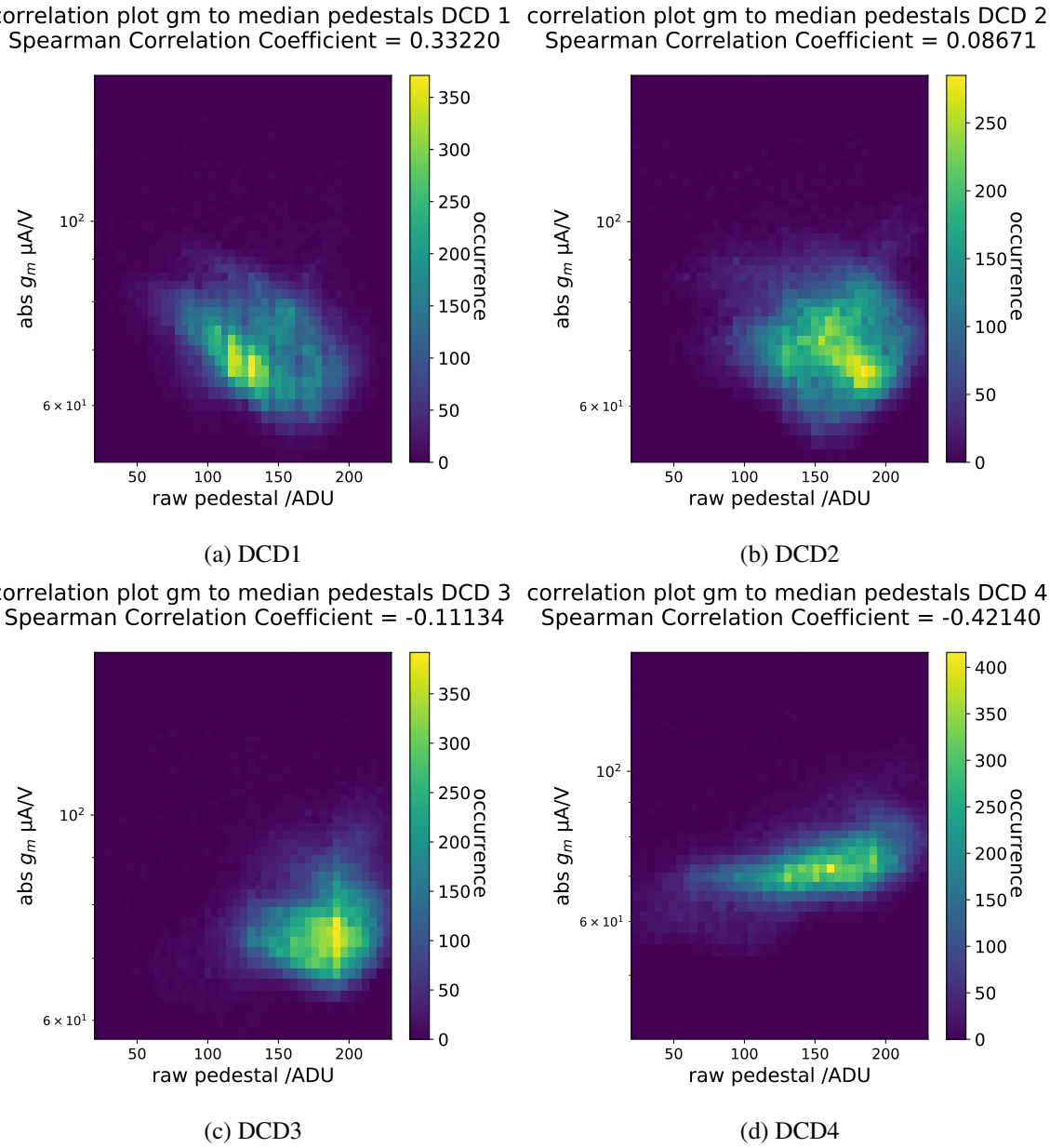
(a) DCD1

(b) DCD2

(c) DCD3

(d) DCD4

Figure A.48: The transconductance extracted out of the DEPFET IV Scan vs. the raw Pedestal values per pixel for module W57_OB1. The right plot shows the occurrence of the correlation values. The pedestal distribution is measured without applied ACMC and Offsets. The Spearman Correlation Coefficient gives a quantity on how monotonic the two data sets are.



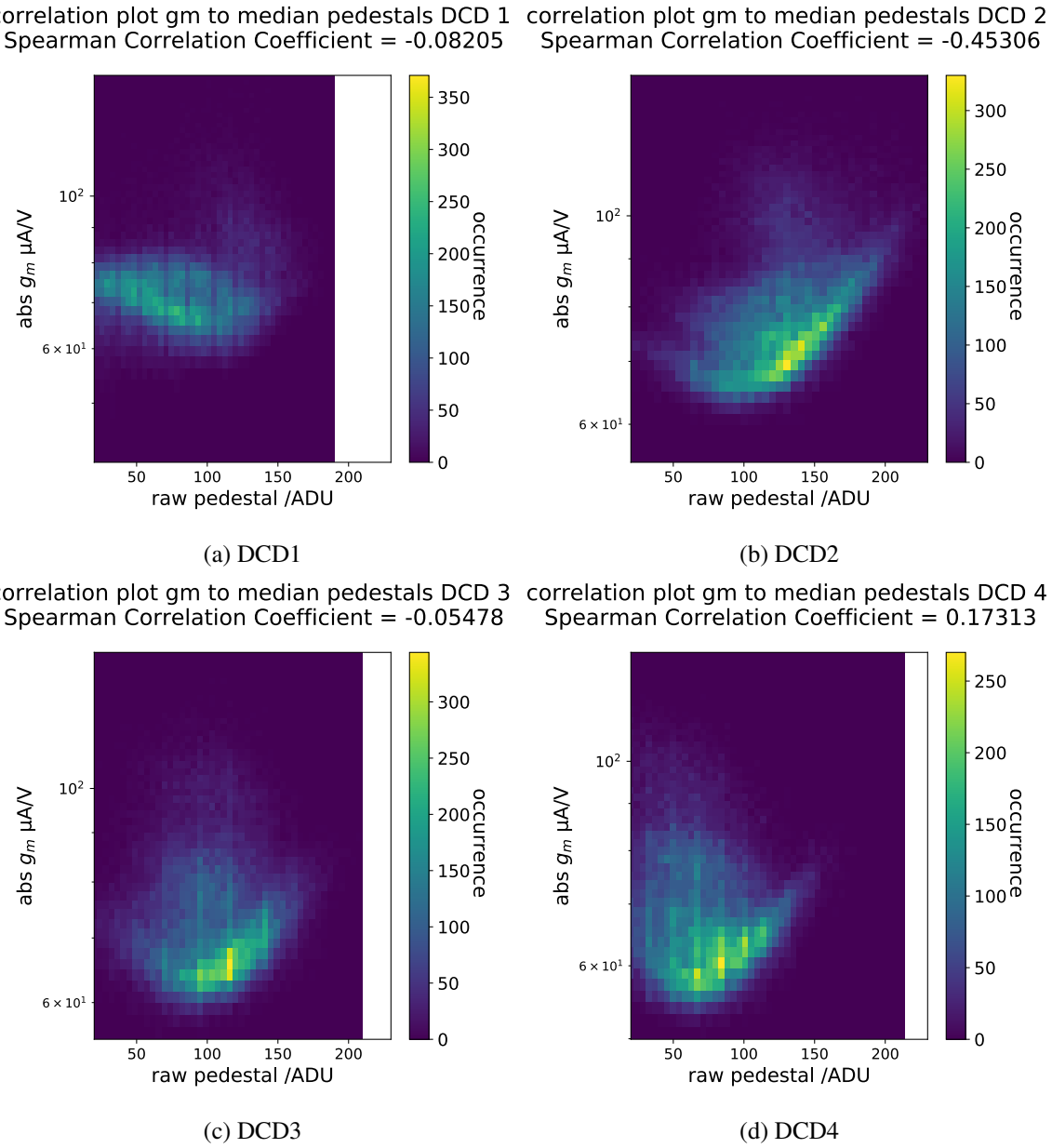
(a) DCD1

(b) DCD2

(c) DCD3

(d) DCD4

Figure A.49: The transconductance extracted out of the DEPFET IV Scan vs. the raw Pedestal values per pixel for module W56_OF1. The right plot shows the occurrence of the correlation values. The pedestal distribution is measured without applied ACMC and Offsets. The Spearman Correlation Coefficient gives a quantity on how monotonic the two data sets are.



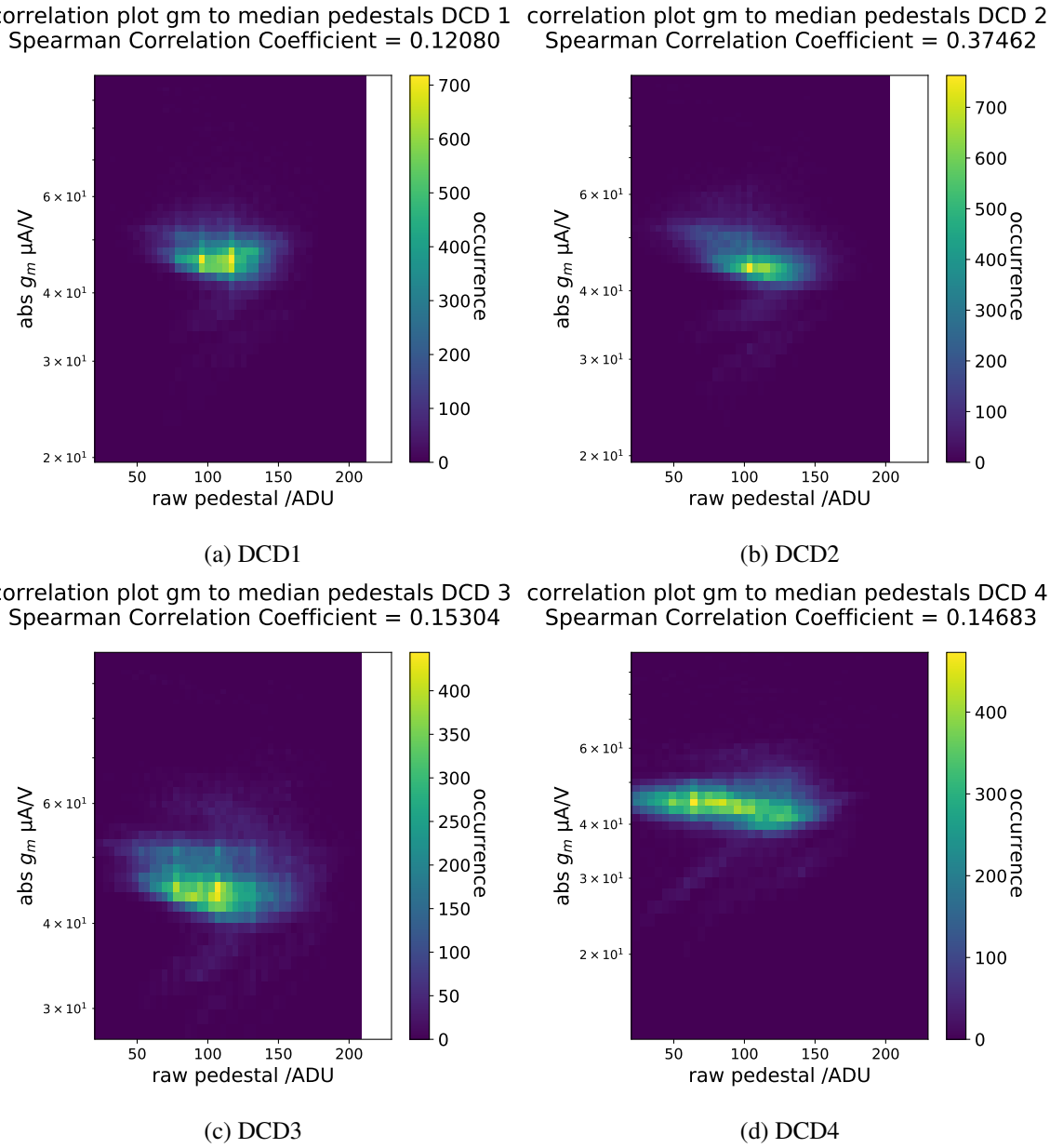
(a) DCD1

(b) DCD2

(c) DCD3

(d) DCD4

Figure A.50: The transconductance extracted out of the DEPFET IV Scan vs. the raw Pedestal values per pixel for module W56_OB1. The right plot shows the occurrence of the correlation values. The pedestal distribution is measured without applied ACMC and Offsets. The Spearman Correlation Coefficient gives a quantity on how monotonic the two data sets are.



(a) DCD1

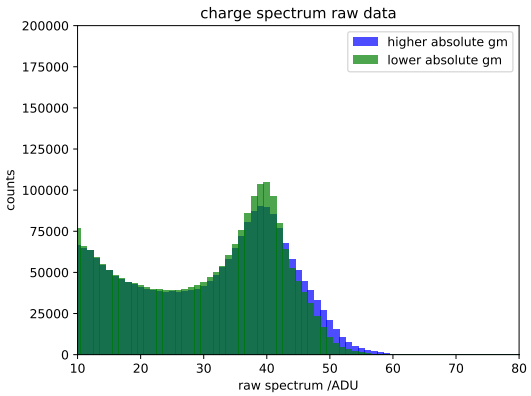
(b) DCD2

(c) DCD3

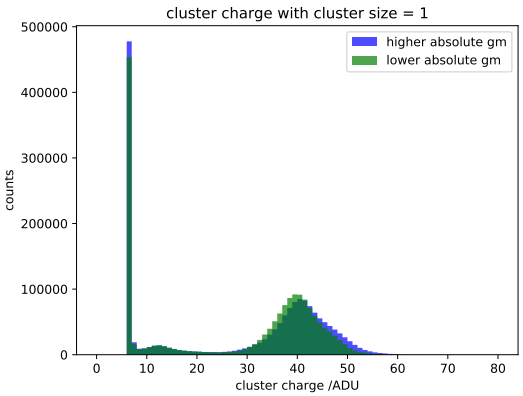
(d) DCD4

Figure A.51: The transconductance extracted out of the DEPFET IV Scan vs. the raw Pedestal values per pixel for module W67_IB. The right plot shows the occurrence of the correlation values. The pedestal distribution is measured without applied ACMC and Offsets. The Spearman Correlation Coefficient gives a quantity on how monotonic the two data sets are.

A.3.5 Double row effect

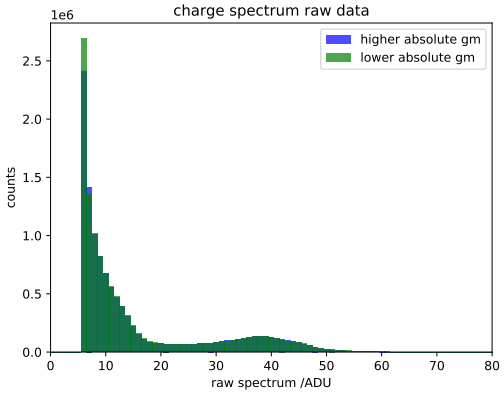


(a) Raw Spectrum of ^{109}Cd.

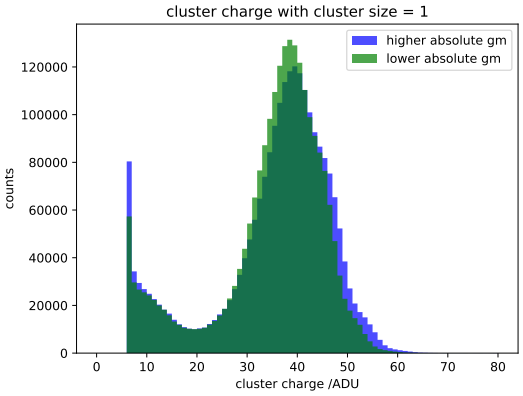


(b) Cluster Charge Spectrum of ^{109}Cd. Cluster Algorithm is applied here.

Figure A.52: Charge Spectrum of ^{109}Cd Source on Module W57_IB. The measurement duration was 400 seconds. The blue region marks the higher absolute Transconductance (more negative values), while the light green region marks the lower absolute transconductance (more positive values). The dark green region marks the overlap of both regions.



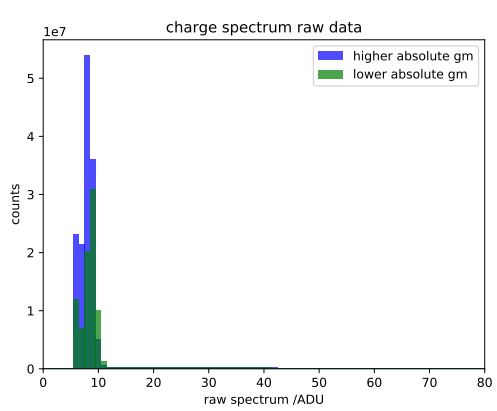
(a) Raw Spectrum of ^{90}Sr.



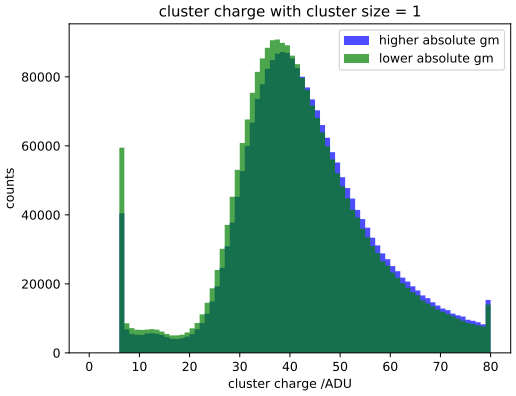
(b)

Cluster Charge Spectrum of ^{90}Sr. Cluster Algorithm is applied here.

Figure A.53: Charge Spectrum of ^{90}Sr source on Module W57_OF2. The measurement duration was 300 seconds. The blue region marks the higher absolute Transconductance (more negative values), while the light green region marks the lower absolute transconductance (more positive values). The dark green region marks the overlap of both regions.

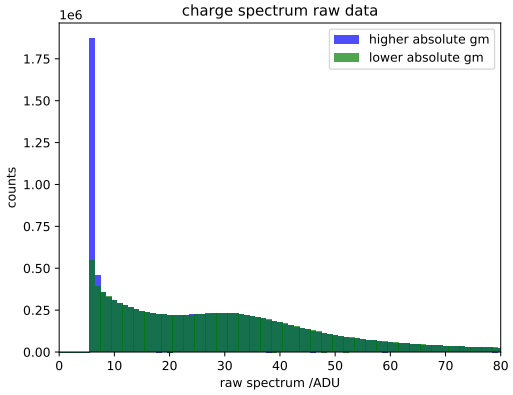


(a) Raw Spectrum of ^{90}Sr.

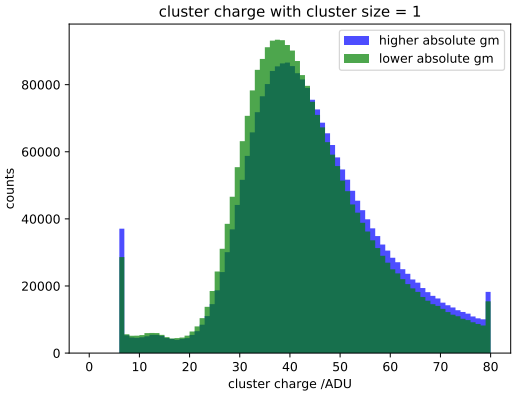


(b) Cluster Charge Spectrum of ^{90}Sr. Cluster Algorithm is applied here.

Figure A.54: Charge Spectrum of ^{90}Sr source on Module W57_OB1. The measurement duration was 400 seconds. The blue region marks the higher absolute Transconductance (more negative values), while the light green region marks the lower absolute transconductance (more positive values). The dark green region marks the overlap of both regions.

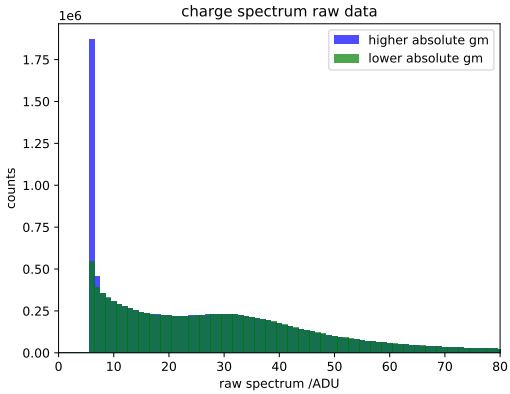


(a) Raw Spectrum of ^{90}Sr.

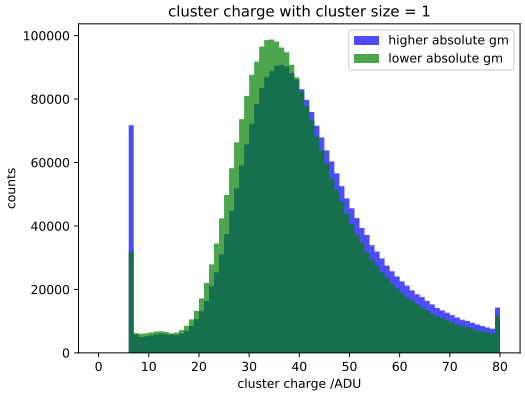


(b) Cluster Charge Spectrum of ^{90}Sr. Cluster Algorithm is applied here.

Figure A.55: Charge Spectrum of ^{90}Sr source on Module W56_OF1. The measurement duration was 300 seconds. The blue region marks the higher absolute Transconductance (more negative values), while the light green region marks the lower absolute transconductance (more positive values). The dark green region marks the overlap of both regions.

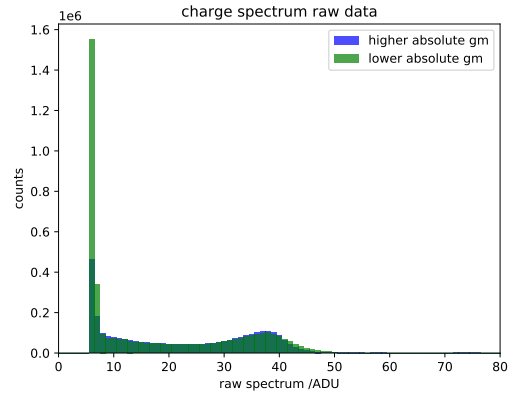


(a) Raw Spectrum of ^{90}Sr.

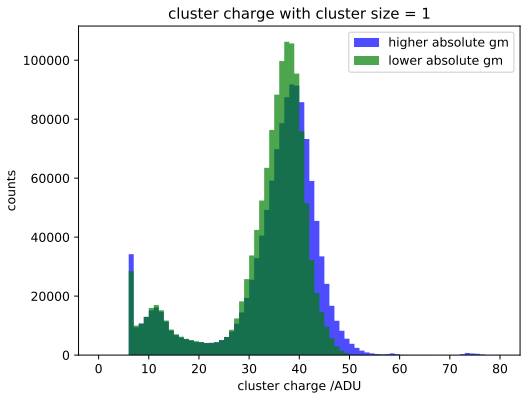


(b) Cluster Charge Spectrum of ^{90}Sr. Cluster Algorithm is applied here.

Figure A.56: Charge Spectrum of ^{90}Sr source on Module W56_OB1. The measurement duration was 300 seconds. The blue region marks the higher absolute Transconductance (more negative values), while the light green region marks the lower absolute transconductance (more positive values). The dark green region marks the overlap of both regions.



(a) Raw Spectrum of ^{109}Cd.

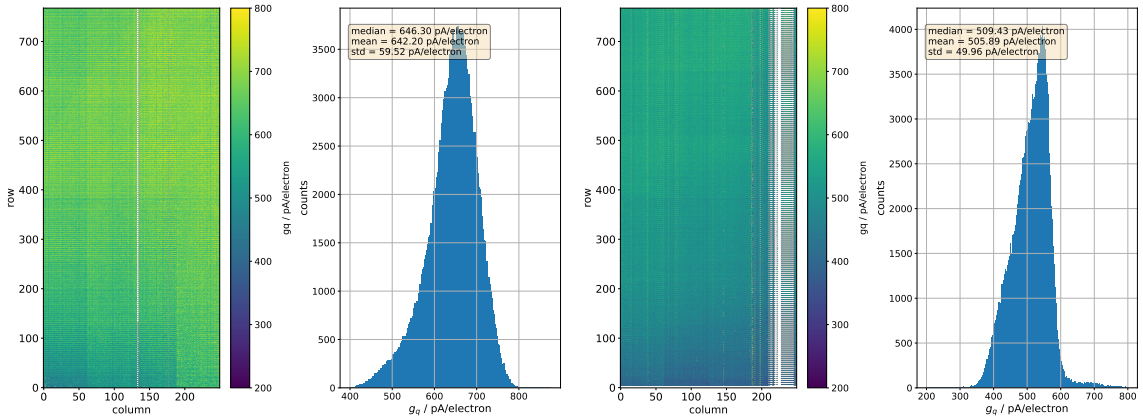


(b) Cluster Charge Spectrum of ^{109}Cd. Cluster Algorithm is applied here.

Figure A.57: Charge Spectrum of ^{109}Cd source on Module W67_IB. The measurement duration was 300 seconds. The blue region marks the higher absolute Transconductance (more negative values), while the light green region marks the lower absolute transconductance (more positive values). The dark green region marks the overlap of both regions.

A.4 Internal Amplification

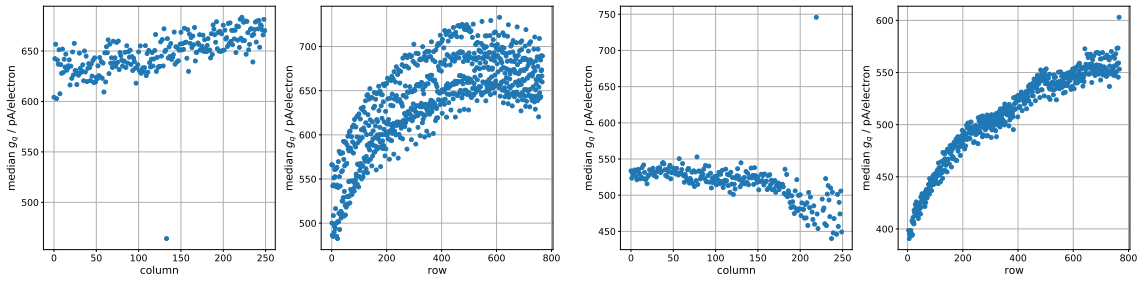
A.4.1 Comparison to all pixels



(a) Module W57_IB. (b) Module W67_IB.

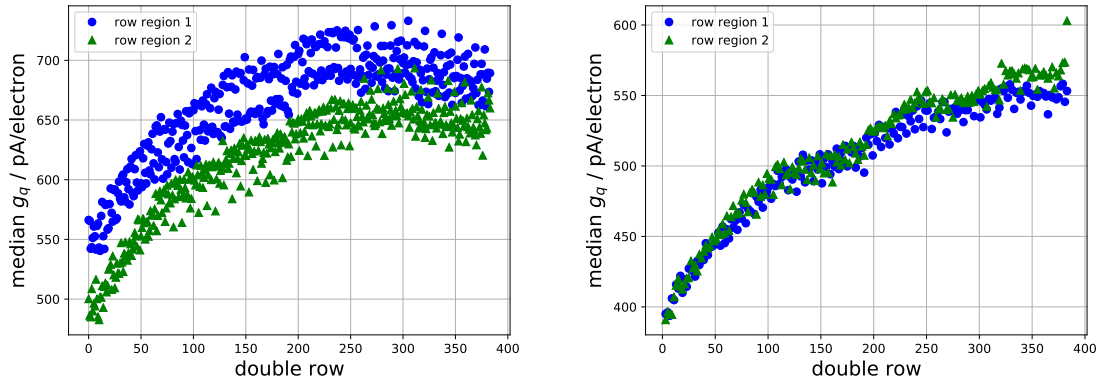
Figure A.58: The values of the internal amplification for each pixels are shown. In the left plot the values are distributed in the PXD9 matrix of the module. The internal amplification is depicted for each channel via the color code on its geometrical position inside the DEPFET matrix. On the right the incidence of the values for each pixel is plotted.

A.4.2 Projection Plots



(a) Module W57_IB. (b) Module W67_IB.

Figure A.59: Projection of values of internal amplification along column and row axes.



(a) Module W57_IB.

(b) Module W67_IB.

Figure A.60: Projection of values of internal amplification along double row axes. The two different pixel size are marked in different colors.

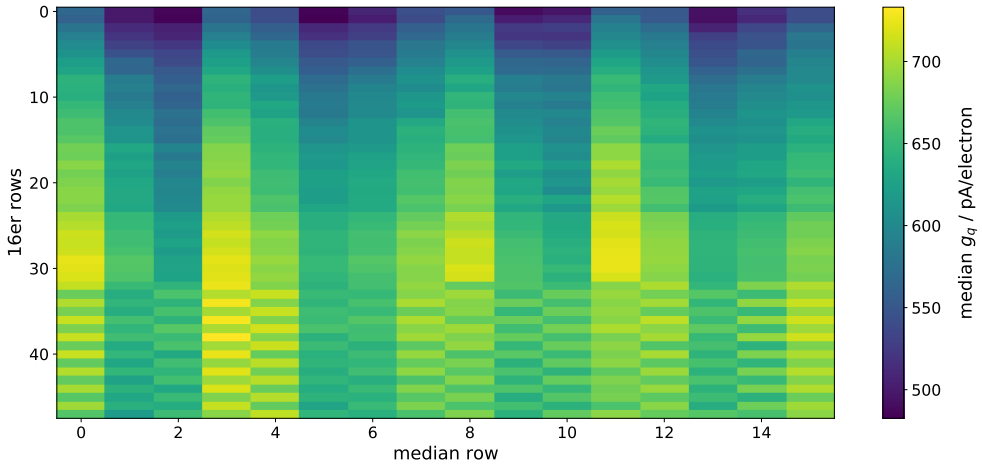


Figure A.61: Projection of the rows for module W57_IB stacked on each other in 16 steps. For the module, the small pixels are located from $[0, 32]$ to $[15, 47)$.

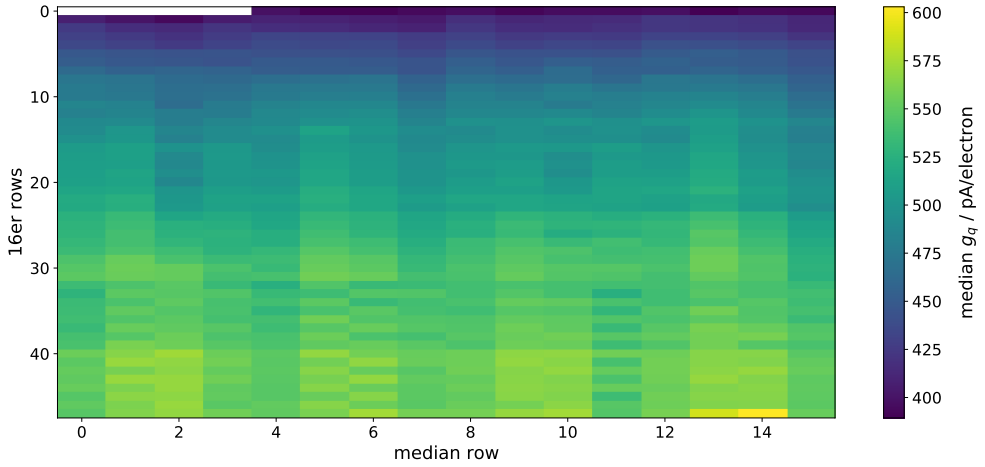


Figure A.62: Projection of the rows for module W67_IB stacked on each other in 16 steps. For the module, the small pixels are located from [0, 32] to [15, 47).

A.5 Correlation of Transconductance and internal amplification

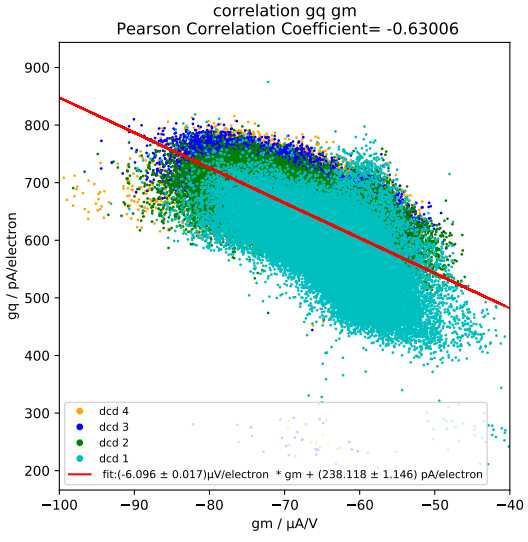
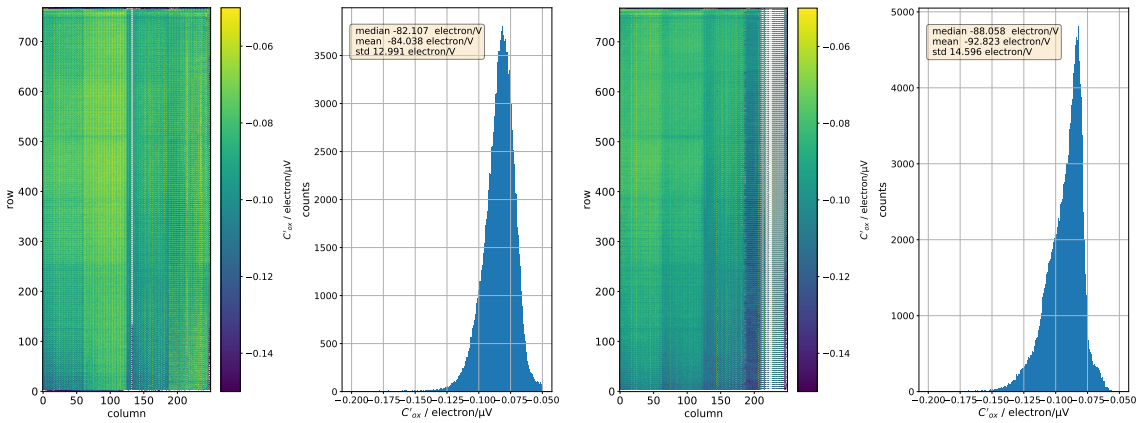


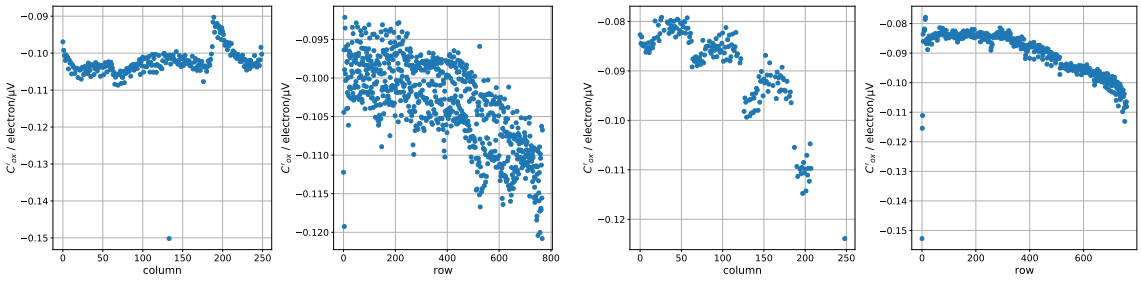
Figure A.63: Correlation between transconductance g_m and internal amplification g_q of Module W57_IB. The colour code indicates the different DCDs. The Pearson Correlation coefficient, gives a value on how correlated the both quantities are.

A.5.1 Oxide Capacitance



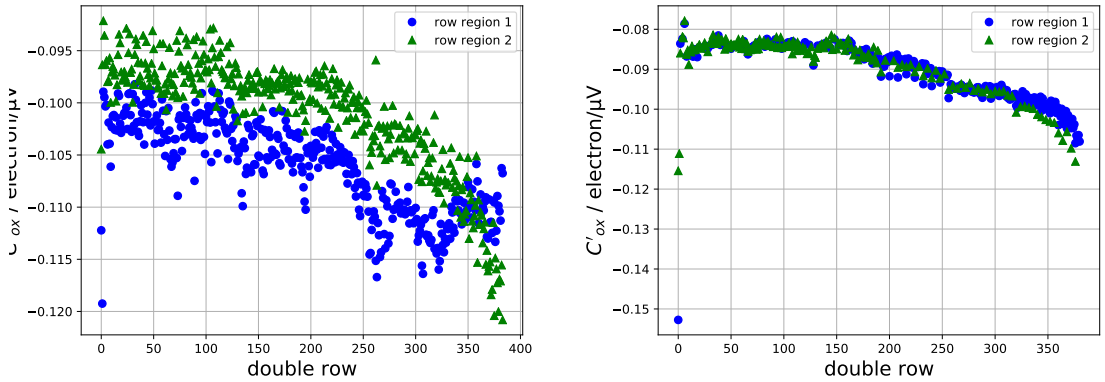
(a) Module W57_IB. (b) Module W67_IB.

Figure A.64: The values of the absolute oxide capacitance for each pixels are shown. In the left plot the values are distributed in the PXD9 matrix of the module. The absolute oxide capacitance is depicted for each channel via the color code on its geometrical position inside the DEPFET matrix. On the right the incidence of the values for each pixel is plotted.



(a) Module W57_IB. (b) Module W67_IB.

Figure A.65: Projection of values of the absolute capacitance along the column and the row axes.



(a) Module W57_IB.

(b) Module W67_IB.

Figure A.66: Projection of values of the absolute capacitance along double row axes where the two different double rows are marked.

Bibliography

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