Characterisation of the Final Components of the Belle II Pixel Detector and Energy Calibration using Source Measurements

Barbara Leibrock

Masterarbeit in Physik
angefertigt im Physikalischen Institut

vorgelegt der
Mathematisch-Naturwissenschaftlichen Fakultät
der
Rheinischen Friedrich-Wilhelms-Universität
Bonn

November 2017

I hereby declare that this thesis was formulated by myself and that no sources or tools other than those cited were used.

Bonn, ...
Date Signature

1. Gutachter: Prof. Dr. Jochen Dingfelder
2. Gutachter: PD Dr. Philip Bechtle

Contents

CHAPTER 1

Introduction

Since the time, when humans evolved above their basic instincts, they asked questions about the world surrounding them, came up with stories and creation myths to explain complex systems and processes to themselves. Furthermore, they started to perform experiments of sorts, investigating the materials and structures around them and eventually started to ask questions about the building blocks of matter and their combinations producing the structures of our environment.

In the western world, the first conclusive theory about the smallest building blocks was developed by Leucippus and his pupil Democritus in the 5th century BCE. They proposed all matter to be made of indivisible atoms, which could have different sizes and masses [1]. Today our concept of an atom largely differs from the atomists' ideas in ancient Greece. A few important steps on that development are shortly named here. Rutherford's atom model was proposed in 1911, seperating the heavy nucleus from small charged particles moving around it [2]. Murray Gell-Mann [3] and Georg Zweig [4] postulated quarks as constituting particles in hadrons like the proton in 1964. Experimentalists at the **S**tanford **L**inear **A**ccelerator **C**enter (SLAC) found those point-like objects in the proton in 1968. Many other theories and experiments were proposed and conducted in the 1960s. By the beginning of the 1970s, apart from many other aspects the model consisted of four quarks [5] and the Cabibbo matrix, preserving the universality of the weak interaction [6].

The fifth and sixth quark flavour known today were proposed by Makoto Kobayashi and Toshihide Maskawa in 1973 when expanding the Cabibbo matrix with its Cabibbo angle to the **C**abibbo-**K**obayashi-**M**askawa (CKM) matrix [7]. Their theory explained the previously observed [8] violation of *CP* symmetry. *C* and *P* denote the charge conjugation and parity symmetry. Thus, *CP* symmetry implies that the laws of physics are unchanged, when a particle is changed into its antiparticle while at the same time the spacial coordinates are inverted. Kobayashi and Maskawa believed that with two additional quarks *CP* violation could be explained. The CKM matrix is today the widely excepted unitary matrix explaining the strength of flavour-changing weak decays.

All of the above mentioned findings and many more are combined in the **S**tandard **M**odel (SM) of particle physics, the currently best fitting theory to explain the fundamental particles and their interactions of three of the four fundamental forces. It consists of six quarks as well as six leptons sorted into three so-called families each. Every family has similar characteristics as the other two, only differing in mass. Apart from those twelve fermions, there are four gauge bosons, called the interaction carriers as they are the carrier particles of the electromagnetic, the strong and the weak force. The last particle known in the SM is the Higgs boson, giving mass to the fundamental particles. However, even as the SM was proven at many occasions to work and describe the experimental findings accurately, there are still many challenges left. The large mass difference between the almost non-existing masses of the neutrinos and

the top quark mass which has about the same mass as a tungsten atom is so far unexplainable. The asymmetry of matter to antimatter in the universe is not understood. The occurrence of three families with the measured quantities cannot be explained. Maybe the most wondrous riddle is that the SM only accounts for about 5 % of interactions and matter in our known universe. [9]

There are two methods scientists use today to find out more about the universe. One is the cosmological approach trying to look as far back in time as possible hoping to discover in the periphery of our universe, what happend during the Big Bang. The second way is to build particle detectors to investigate the small scales at large energies. With the second approach, physicists try to reproduce the conditions at and shortly after the Big Bang. Furthermore, they aim for triggering rare decays which open up physics beyond the Standard Model, to find new areas and explanations about our surrounding environment.

One particle detector going to be looking for new physics is Belle II at the accelerator SuperKEKB. It is the upgrade of the Belle detector which proved the CKM theory with its *CP* violation phase [10]. Belle at the KEKB accelerator showed an asymmetry between matter and antimatter in B meson decays. However, this is insufficient to explain the dominance of matter over antimatter in our galaxy. Therefore, and for answers to the other aforementioned questions, high hopes are pinned on Physics beyond the SM. This new physic might be found in rare decays of B-mesons as small, unknown couplings or loop corrections, producing heavy new particles. To convincingly discover rare decays experimentally and seperate them from the background, large datasets have to be taken. For this reason, the KEKB is upgraded to the SuperKEKB with a luminosity fourty times higher than the predecessor. Hence, there will be more interactions in the beam collisions and thus, more recorded data. The increased luminosity and therefore higher signal rate and background of the accelerator makes the upgrade of the detector to Belle II necessary. It is in its commissioning phase now and is expected to start data taking in 2018. Especially, two layers of a newly developed **P**i**X**el **D**etector (PXD) are included as the innermost subdetector. It is made up of complex modules with a large DEPFET matrix and three different custom-made steering and readout chips. The DEPFET is a monolithic sensor type composed of a transistor with a pre-amplification in the pixel.

In this master's thesis, the final iterations of the matrix and chips were for the first time tested together in preparation of the module mass production. A set of four characterisation scans was performed, finding parameter spaces for the matrix voltages, the digitisation process, the chips' communication and for sending the data off the module. As the four modules for the commissioning detector and the first final modules are assembled already, those parameter scans were one of the final chances to find flaws in the chips. With the thus optimised system, energy and gain calibrations are performed. With the results of the former, the amplification of the DEPFET pixels is determined, while the latter is reapplied on the source data to increase the energy resolution and decrease the width of the peaks.

The achievements of Belle as well as the new Belle II detector and the SuperKEKB facility are explained in Chapter 2. The fundamental principles of semiconductor physics and field effect transistors are recapitulated and the thus following concept of DEPFETs is summarised in Chapter 3. These are followed by descriptions of the different module components and the PXD in Chapter 4 as well as the explanation of the used experimental setup with a demonstrator module in Chapter 5. The performed characterisations investigating the chips working parameter spaces can be found in Chapter 6, while the matrix characterisations, the energy as well as the gain calibration follow in Chapter 7.

CHAPTER 2

SuperKEKB and Belle II

2.1 SuperKEKB

The Japanese High-Energy Accelerator Research Organisation, KEK, operated the accelerator KEKB between 1998 and 2010 with the Belle detector at the interaction point. KEKB had a total circumference of 3 016 m. It was an e^+e^- collider running at the $\Upsilon(4S)$ resonance, producing $B^0\bar{B}^0$ and B^+B^- meson pairs. With symmetric beams colliding at the center-of-mass energy of the $\Upsilon(4S) = 10.58\,\text{GeV}$ the B mesons are produced at rest and would decay at the same position they were produced at. As one aim of Belle was to identify the decay products of a single B meson and seperate the two from each other, this is not a favourable situation. Therefore the accelerator ran at asymmetric energies with the electron beam energy higher than the energy of the positron beam which boosts the B mesons enough to observe a difference of $\Delta z \approx 200\,\mu\text{m}$ between the decay vertices. Because they produce a high amount of B mesons, accelerators of this kind are called B-factories. They search for rare new phenomena at medium energies but ultra-high luminosities. The instantanous luminosity L of KEKB was given with σ the interaction cross section, N the number of colliding particles and t the time period as

$$L = \frac{1}{\sigma}\frac{\mathrm{d}N}{\mathrm{d}t} = 2.11 \times 10^{34}\,\text{cm}^{-2}\,\text{s}^{-1} \tag{2.1}$$

which marks the current world record. In contrast, the Large Hadron Collider (LHC) at CERN investigates particles with large energies, accelerating them close to the velocity of light.

Amongst others, the accelerator KEKB and the Belle detector were built to confirm the CKM formalism and investigate *CP* violation. The latter was believed and is in the meantime experimentally found to be at least partly responsible for the asymmetry we observe in the matter-antimatter relation within our world and galaxy these days. Already with the data taken during the first years of operation, the effect of *CP* violation as described theoretically by Makoto Kobayashi and Toshihide Maskawa could be confirmed. The experimental discoveries lead to a Noble Prize in 2008 for the two theoreticians. Unfortunately even as the principles of *CP* violation are confirmed, the measured level is insufficient to explain the full amount of the observed matter-antimatter asymmetry. In addition to those findings, the Belle experiment found rare decays and CKM matrix elements were measured to considerably higher precison than before. But still many fundamental questions in the flavor sector are still unanswered. [11]

To get a better and deeper understanding of the CKM matrix and, furthermore, of the flaws within the Standard Model, investigation of rare decays beyond the Standard Model and high precision measurements of CKM matrix elements are necessary. Therefore KEKB is upgraded to SuperKEKB with an increase in the luminosity to $L = 8 \times 10^{35}\,\text{cm}^{-2}\,\text{s}^{-1}$, which is 40-times higher than the luminosity of

KEKB. A scheme of the SuperKEKB accelerator can be seen in Figure 2.1. It is built using the same accelerator ring as the previous one. The leptons are preaccelerated with linear accelerators, before they are injected in opposite directions in the two tubes of the synchrotron ring, which run in parallel. When reaching the intended energy, the beams collide within the volume of the Belle II detector. The higher luminosity compared to KEKB is achieved with a higher beam intensity and by reducing the beam width to a few nano meters (so-called *nano-beam solution*) in the interaction region.

Some questions regarding flavor physics are investigated with specialised experiments at the TeV mass scale at hadron colliders such as the LHC. However, the high-precision measurements of rare decays and CP violation in heavy quarks and leptons are necessary to reveal New Physics like the effects of new particles in higher order processes. Those are investigated in the cleaner environment of an e^+e^- collider, because in a hadron collision the amount of hadronic decaying possibilities overlay the interesting processes. Leptons have less possibilities to decay and recombine, therefore the environment for the investigated processes is cleaner. [9, 12]

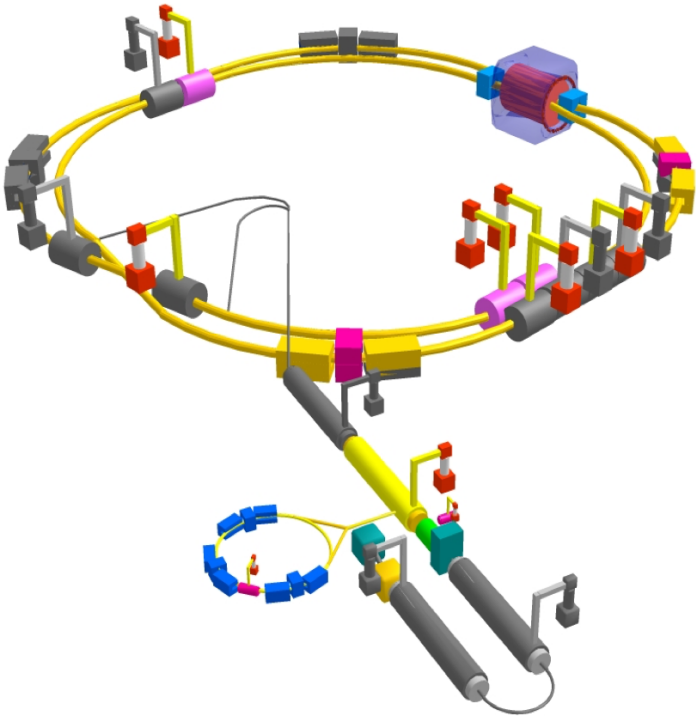


Figure 2.1: The accelerator SuperKEKB. The electrons and positrons are preaccelerated in linear accelerators seen in the lower part of the figure. After their injection into the ring, they are brought to the final velocities in two seperated tubes and then collided within the volume of the Belle II detector. [13]

2.2 Belle II

Because of the higher luminosity an upgrade of the Belle detector becomes necessary to cope with the higher background and larger amount of data. This upgrade is called Belle II. The detector is 7.5 m wide and 7 m heigh as can be seen in Figure 2.2. It sits at the same position within the accelerator ring as prior the Belle detector. Like many other particle detectors positioned within the collider's ring, Belle II is an onion-layered detector built around the interaction point. The interaction point is shown in the middle

of the figure with the beam pipes running towards it from both sides of the detector. Because the decay products are boosted, the detector is built asymmetrically. On the right side of the figure the forward direction can be seen, while the backward direction is to the left. The final state particles from the decays are detected and their properties measured by the different detector layers of Belle II. In the following paragraphs, every subdetector beginning from the outermost is shortly discussed. [13, 14]

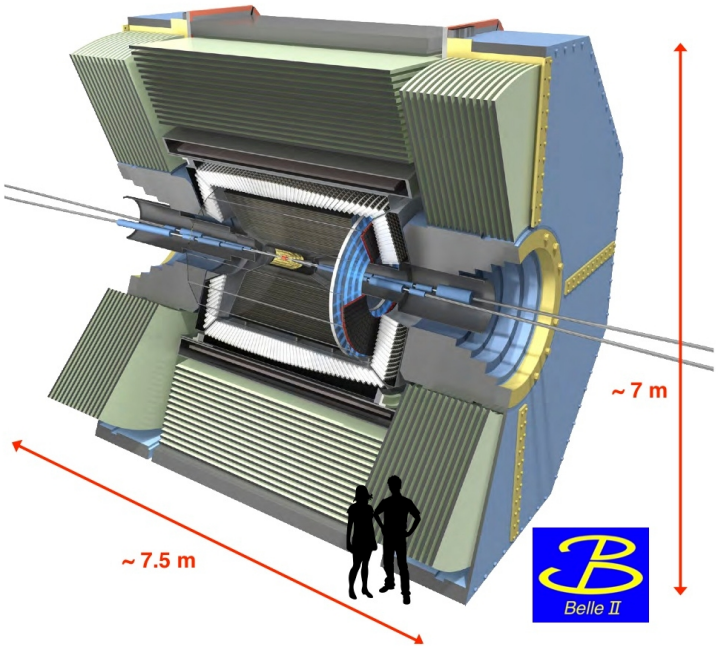


Figure 2.2: Cut through the Belle II detector revealing the subdetector layers compared to people's height.

K-long and Muon Detector

The muon and the K_L are both particles which travel a long distance inside the Belle II detector. The muon leaves tracks in other subdetectors due to electromagnetic interaction. However, it emits less bremsstrahlung than the electron in the detector system and its lifetime is longer than the tau's. Therefore, the other leptons are stopped or decayed by the time they would reach the outermost detector. A part of a track in the **K**-**L**ong and **M**uon (KLM) detector is therefore a distinguishing characteristic of a muon track. The K_L with a mass of 497.6 MeV decays mostly into three pions (m_π = 135 to 140 MeV). Therefore, within the decay only a small amount of kinematic energy is left for the three pions. This results in a long lifetime of the K_L. As the decay probability follows an exponential behaviour, many K_Ls will decay before they reach the KLM. For those not decaying previously, the KLM is designed to bring most of them to decay and detect them. To increase the decaying probability and therefore detection of the K_L, the KLM consists of 15 layers in the barrel part, 14 layers in the forward endcap as well as 12 layers in the backward endcap. The barrel layers, except the inner two, consist of Resistive Plate Counters (RPC). As their efficiency suffers with high background rates, the endcaps and the two inner barrel layers are instead equipped with scintillator strips. All layers are interspersed with thick iron plates, used as the flux return yoke of the 1.5 T solenoid encompassing all other subdetectors as well as as stopping material for muon and K_L. At some point the K_L collides with an iron nucleus and leaves a hadronic shower signal as well as all of its energy as a signature, distinguishing it from the continous track of a muon. [13, 14]

Electromagnetic Calorimeter

The **E**lectromagnetic **Ca**l**L**orimeter (ECL) is used to detect photons with high efficiency, determine precisely their energy and angular coordinates and identify electrons. Additionally, it detects K_L particles together with the KLM. The ECL is divided in three parts, the barrel region, the forward and the backward endcap. For the barrel part, crystals from the Belle detector are reused. Those are CsI(Tl) crystals of an average size of $6 \times 6 \times 30\,\mathrm{cm}^3$ and formed as truncated pyramids. In the endcaps, however, pileup is expected to severly decrease the energy and time resolution, therefore faster pure CsI crystals are used here. In total the ECL consists of 8 736 crystals. The readout electronics are changed compared to the Belle detector because they have to work at a larger frequency to cope with the higher data rate. The light output from the electromagnetic interactions within the crystals is read out by silicon PIN photodiodes. The deposited energies rank from a few MeV to a few GeV. [13–15]

Particle Identification System

The two subdetector parts responsible for the Particle Identification are the **T**ime **O**f **P**ropagation (TOP) detector and the **A**erogel **R**ing-**I**maging **CH**erenkov counter (A-RICH). The subdetectors analyse the Cherenkov light cones produced by charged particles. They are especially necessary to seperate charged kaon and pion signals from each other. In the barrel region, TOP counters made of quartz radiator bars measure both hit patterns and the time of propagation of internally reflected Cherenkov photons. From these values the spacial and time information of the corresponding particles are reconstructed. In the forward endcap, ARICH, consisting of aerogel radiators, identifies charged particles by 2-D Cherenkov ring images. Those images are read out by position sensitive photon detectors, capable of single photon detection inside a magnetic field in two dimensions. [13–15]

Central Drift Chamber

The **C**entral **D**rift **C**hamber (CDC) consists of 14 336 wires in a He-C_2H_6 gas volume of 5 760 liters. An electric field within the chamber is created by applying a high voltage to the wires. Passing charged particles ionise the gas, the resulting electrons are directed by the electric field towards the wires and create an electron avalanche in the stronger field around the wires, amplifying the signal. The wires detect the avalanche and send off a signal. The CDC reconstructs charged tracks and measures the corresponding particle's momentum as well as the energy loss within the gaseous volume of the detector. For slow particles, that do not reach the Particle Identification System, the CDC constitutes the sole identification system. It identifies particles based on deposited energy and the particle's momentum. [13–15]

Vertex Detector

The **V**erte**X** **D**etector (VXD) is responsible for accurate measurements of charged particle trajectories near the origin point. Thus, decay vertices may be reconstructed with high precision. The VXD is especially necessary for an exact measurement of the distance between different decay vertices. It has two subcomponents as shown in Figure 2.3, the **S**ilicon **V**ertex **D**etector (SVD) and the **P**i**X**el **D**etector (PXD). It consists of six layers in total. The four layers of the SVD are double-sided silicon strips in a so-called *Origami chip-on-sensor* orientation. The name of the concept comes from the fact, that the channels on the backside of the module are connected by small flexible fanouts bending around the edge of the module structure to be read out in front. This is done in order to achieve a high signal-to-noise ratio with fast shaping in the front-end electronics as well as to simplify the cooling process. The SVD adopts

as good characteristics "low mass, high precision, immunity to background hits, radiation tolerance and long-term stability" [13] from the previous SVD in the Belle detector. The SVD of Belle II increases the reconstruction efficiency for K_S decays to two charged pions due to the larger outer radius of the SVD in comparison to Belle. The PXD is an addition to the detector ensemble in comparison to Belle to cope with the high track density due to the increased luminosity. Through the additional pixel layers in short distance from the interaction point, the impact parameter resolution in the beam direction is improved by a factor of 2 for momenta below 1 GeV. The PXD consists of two layers of silicon pixels in the DEPFET design. The first layer sits at a distance of 14 mm from the interaction point and consists of eight ladders while the second layer is made up of twelve ladders at a radius of 22 mm. Each ladder is made of two modules including a pixel matrix and 14 **A**pplication-**S**pecific **I**ntegrated **C**ircuits (ASICs) to steer it and function as the front-end electronics before data is sent off the module. In chapter 4 the different parts of the PXD module are explained and discussed as well as the functionality and speciality of the DEPFET pixel matrix. [13, 15, 16]

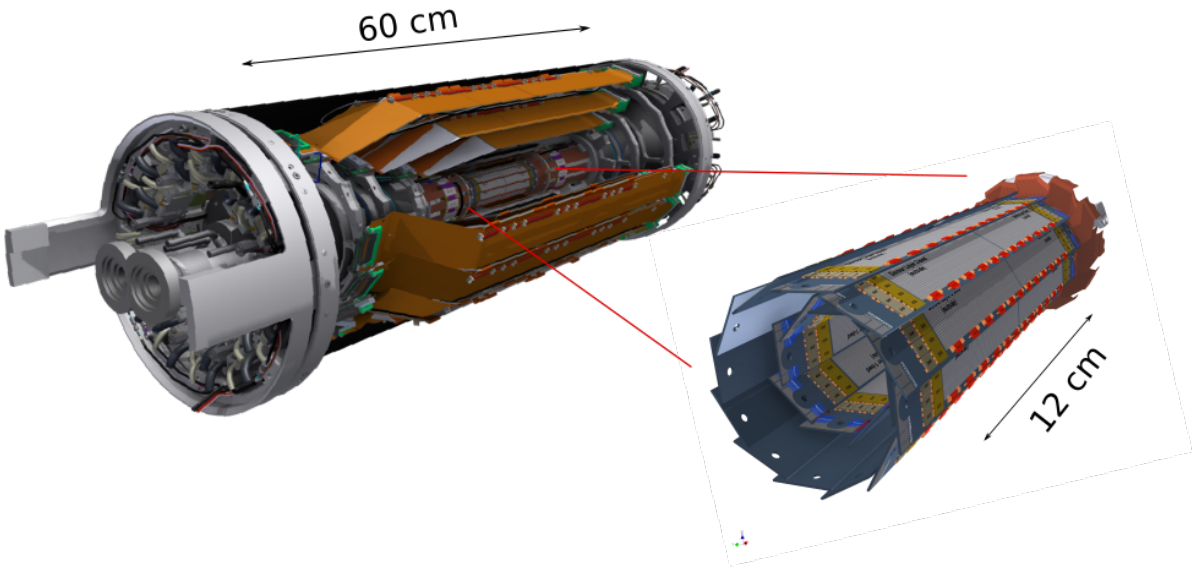


Figure 2.3: On the left side the complete vertex detector can be seen with the three outer layers of the silicon strip detector in orange and the innermost strip layer hidden beneath the others as well as the pixel detector included within. As the latter cannot be seen clearly it is enlarged on the right side. It consists of two layers with twenty glued ladders consisting of two modules each. The active region for the pixel layers reaches a length of 120 mm. [16]

CHAPTER 3

DEPFET pixels

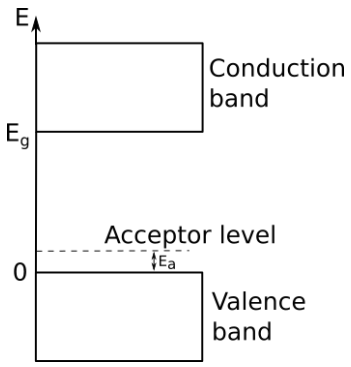
For a better understanding of the working principles of the DEPFET pixel detector a few basic phenomena have to be discussed first.

3.1 Principles of Silicon Semiconductors

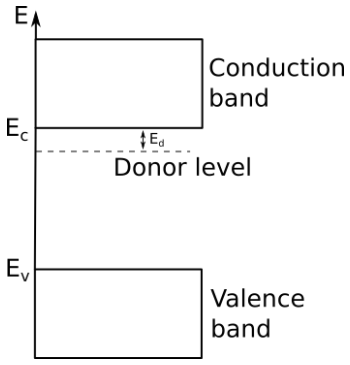
In this section the focus will be on silicon as this is used in the PXD modules. Silicon crystals are arranged in the so-called *diamond* lattice structure, meaning that every atom has four equidistant neighbours. The bond between two nearest neighbours is formed by two electrons, one from each silicon atom. In crystals the band structure gives the energy-momentum relationship. It consists of two different kinds of bands, the valence bands at energies where the electrons are firmly bound within their atoms and the conduction bands with electrons energized enough to leave the valence bands, leaving holes behind. Through this seperation of electrons and holes a conducting current is possible within the crystal. Between the different bands there is a bandgap that has to be overcome by the electrons in a single energetic jump before reaching the lowest conduction band. The bandgap at room temperature in pure silicon is 1.12 eV. To reduce this energy gap and create a better conductor due to more electrons jumping to the conduction bands, the silicon is doped with atoms either from the 13. or from the 15. group in the periodic table. The first option results in one electron too less for bonds with all four neighbouring silicon atoms, leaving one hole in the bonds. For the band structure this means that there is an impurity introduced at one fixed position within the bandgap close to the valence bands, schematically shown in Figure 3.1(a). The additional hole attracts electrons and the small energy gap enables them to break away from their nucleus. The silicon is called *p*-doped while the impurities are called "acceptor" atoms. The second doping case means that one electron is free of bonds in the crystalline structure, making it easier for this electron to leave its atom. In this case the negative impurity is placed close below the energetically lowest conduction band, shown in Figure 3.1(b). Therefore the electron can easily cross over the small gap into the conduction band. The silicon is then *n*-doped with the additional element being a "donor" atom. [17] A heavy doping is indicated by a +-sign while a weak doping is shown with a −-sign added to the letter indicating the type of doping.

3.2 Diodes

If two differently doped materials are put into contact next to each other, a *p*-*n* junction is created. Majority carriers close to the junction on both sides diffuse across the barrier. This results in electrons



(a) Simplified band structure for an acceptor doping, with E_g being the energy of the gap and E_a the difference between the valence band and the acceptor level of the introduced impurity. Adopted from [18].



(b) Simplified band structure for a donor doping, with E_v indicating the energy of the valence band, E_c the energy at the conduction band and E_d the difference between the conduction band and the introduced impurity. Adopted from [18].

Figure 3.1: Band structure models for doping with acceptor or donor elements.

diffusing from the n-doped side to the p-doped side as well as holes from the p-doped side to the n-doped part. Electrons will recombine with holes across the barrier and the the holes will recombine with electrons on the n-doped side. This creates a depleted region, free of mobile carriers but with a negatively charged acceptor region and a positively charged donor region. The resulting potential difference leads to a virtual current flowing in the opposite direction of the diffusing carriers. The resulting voltage without an external bias is called the built-in voltage V_{bi} and is calculated with

$$V_{\text{bi}} = \frac{k_B T}{e} \ln\left(\frac{n_{n_0} p_{p_0}}{n_i^2}\right)$$

where k_B is the Boltzmann constant, T the temperature, p_{p_0} the hole density on the p-side, n_{n_0} the electron density in the n-doped region, while n_i is the intrinsic carrier density. If an external current is applied at the junction it can either decrease or increase the depletion region. The first case is called a forward bias V_{f} where the p-side is connected to the positive electrode while the n-side is more negative. For the total potential difference between the p- and the n-side this results in

$$V_{\text{tot}} = V_{\text{bi}} - V_{\text{f}}$$

and therefore a reduction of the depletion region which can be overcome more easily by the electrons. The junction operates as a diode in forward direction. The opposite case is called reverse bias with the p-side at a negative potential $-V_{\text{r}}$ relative to the n-side which results in

$$V_{\text{tot}} = V_{\text{bi}} - (-V_{\text{r}}).$$

The negative electrode connected to the p-doped side of the junction sucks holes away from the junction as well as the positive electrode attracts electrons from the n-doped side. This results in an enlargement of the depletion region and thus, a higher barrier for the electrons to cross. The junction is now called a blocked diode. [18]

3.3 Sidewards Depletion

In the 1980s, E. Gatti and P. Rehak developed a new method of depletion called sidewards depletion [19]. The principle is shown in Figure 3.2. At the top and bottom of a n-doped bulk there are p^+-doped regions introduced. A negative voltage is applied there, creating two depleted zones around the contacts. When the voltage is further decreased, the two regions are getting wider and will touch in the middle of the silicon bulk. This results in the same situation as two diodes (np-pn) next to each other would create. The electrical field decreases linearly towards the middle, creating a potential minimum for electrons. If there are different voltages applied at the p^+-doped regions the minimum can be shifted to another position, preferably upwards. [19, 20]

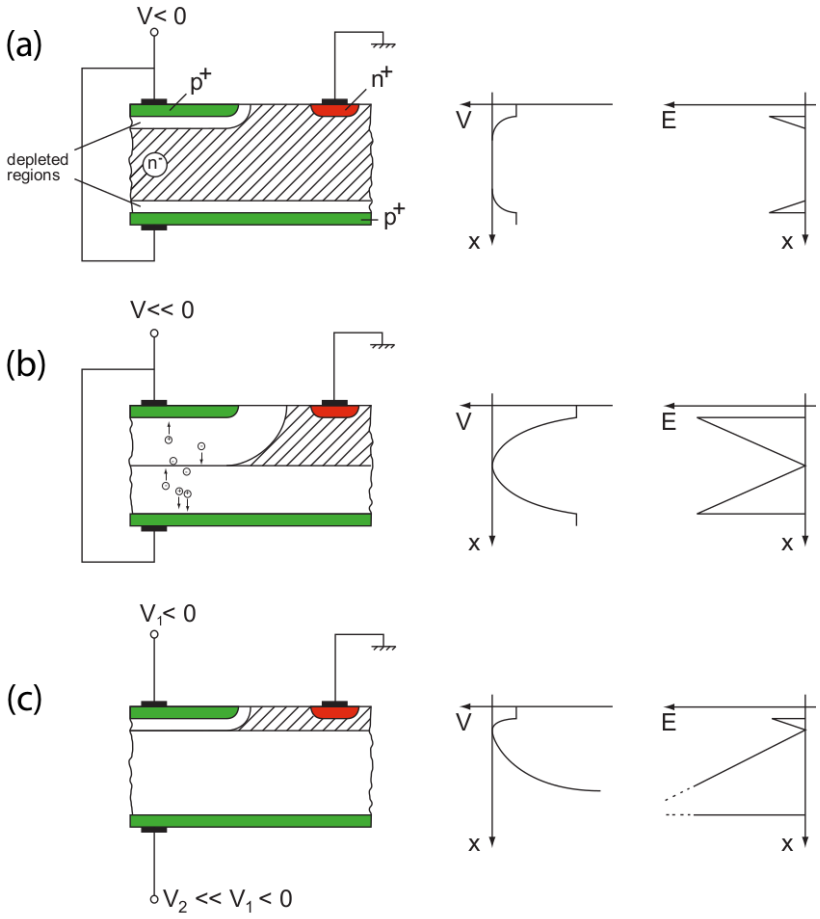
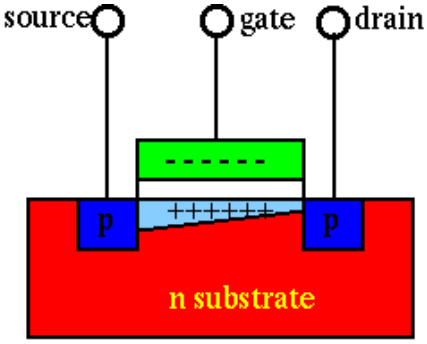


Figure 3.2: Principle of sidewards depletion with (a) a small introduced negative voltage, (b) an increased voltage forcing the depleted zones far enough to touch and then (c) moving the potential minimum by applying different voltages. [20]

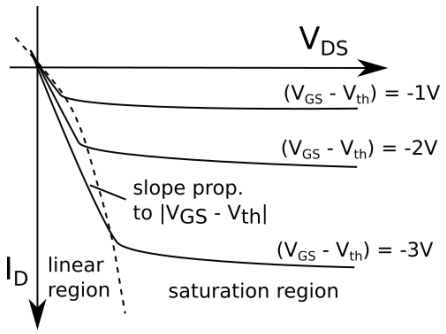
3.4 MOSFET

A MOSFET is a **M**etal-**O**xide-**S**emiconductor **F**ield **E**ffect **T**ransistor (FET), a 3-terminal device like shown in Figure 3.3(a). It consists of three electrodes, drain, source and gate, on top of a bulk. The latter is doped in the opposite way to both the source and drain electrodes. Both those electrodes are imbedded

in the bulk while the gate is seperated from the bulk by an insulating layer of SiO_2, and being positioned inbetween the source and drain electrodes. If a voltage is applied to the gate a small region in the bulk beneath the insulation layer is cleared of majority carriers. This enables a conductive current to flow between drain and source, controlled by the voltage applied at the gate. [21]



(a) A p-channel MOSFET device with p^+-doped source and drain which is switched on with a negative voltage at the gate. [22]



(b) The drain current I_D behaviour for increasing drain-source voltage V_{DS} at different gate-source voltages V_{GS} [21]

Figure 3.3: Composition and different stages of output-to-input behaviour of a MOSFET. On the left side a p-channel MOSFET can be seen, while the I_D to V_{DS} graph shows the relation between drain current and drain-source voltage of this MOSFET.

MOSFETs occur in different kinds, characterised by the polarity combination and the channel doping. In Figure 3.3(a) a p-channel MOSFET can be seen. It consists of p^+-doped source and drain electrodes which are surrounded by n-doped bulk silicon. The threshold voltage V_{th} where the transistor starts working depends on the type of MOSFET. For a depleted p-type MOSFET V_{th} is positive. As long as the gate electrode is kept positive, the transistor is switched off. When a negative voltage is applied to the gate electrode, the electrons as majority particles in the n-doped bulk are forced away from the gate electrode. Thus creating a carrier-free region below the insulation layer and furthermore a conducting channel between source and drain. The dependence of the resulting drain current I_D on the voltage V_{DS} between source and drain is for different gate voltages V_{GS} shown in Figure 3.3(b). There are three possible cases:

- $V_{GS} > V_{\text{th}}$:
  The MOSFET is switched off and there is no conductive current between source and drain.

- $V_{GS} < V_{\text{th}}$ and $\left|V_{DS}\right| < \left|V_{GS} - V_{\text{th}}\right|$:
  The MOSFET works in the linear regime where I_D is approximately proportional to V_{DS} and can be described through
  $$I_D = \frac{W}{L}\mu C_{\text{ox}}\left(\left(V_{GS} - V_{\text{th}}\right)V_{DS} - \frac{1}{2}V_{DS}^2\right) \tag{3.1}$$
  with the W as width of the gate, L the gate length, μ the carrier density and C_{ox} the oxide capacitance of the MOSFET. Within the linear regime the FET works like a resistor. The regime extends up to a voltage $\left|V_{DS\,\text{sat}}\right|$ where the drain current becomes almost constant and goes into saturation.

- $V_{GS} < V_{\text{th}}$ and $\left|V_{DS}\right| > \left|V_{GS} - V_{\text{th}}\right|$:
  The MOSFET works in saturation with a constant current output and no dependency on V_{DS}. The

resulting dependence can be described as

$$I_D = \frac{W}{2L}\mu C_{\text{ox}}\,(V_{GS} - V_{\text{th}})^2 \tag{3.2}$$

The FET's gain is described by the transconductance as the ratio of output current i_{out} to input voltage v_{in} given with

$$g_m = \frac{i_{\text{out}}}{v_{\text{in}}} = \frac{\partial I_D}{\partial V_{GS}} \tag{3.3}$$

[20, 21]

The DEPFET pixels are made up of depleted p-channel FETs and are discussed in more detail in the following section.

3.5 DEPFET pixel

A **DE**pleted **P**-channel **F**ield **E**ffect **T**ransistor (DEPFET) is in principle a MOSFET with gate, source and drain electrodes as described in section 3.4 on a sidewards depleted silicon bulk with an additional internal gate. The sidewards depletion as described in section 3.3 is achieved with only one pin on the surface of the modul. The technic is called *punch-through* and works because the high voltage applied to the pin first depletes a channel as direct connection to the completely p-doped backplane. Once the depleted part reaches the back of the pixel, the process is continued over the complete n-doped bulk in reverse direction. Through the high voltage applied, the potential minimum for the electrons can be shifted up to lay close beneath the insulation layer and the gate electrode.

The internal gate is a more strongly n-doped region directly below the external gate within the bulk where electrons are attracted to. Due to this concentration of the collected charge directly below the gate electrode the drain-source current is modulated and as a result amplified. As a charged particle passes through the pixel, electron-hole-pairs are created. The holes drift to the back side of the matrix while the electrons drift to the potential minimum created through the depletion process. They are then attracted by the internal gate, move sidewards and are collected within it. The charge collection process is done in switched-off mode, meaning that no drain current flows between drain and source. When the transistor voltage is dropped to the activation level below V_{th}, a current flows. The collected charge influences the gate voltage through capacitive coupling to the p-channel and changes it by

$$\Delta V_{GS} = \frac{\alpha q_s}{C} = \frac{\alpha q_s}{C_{\text{ox}} WL}$$

with q_s the collected charge, α the coupling constant close to 1 describing the losses due to stray capacitances, C as the coupling capacity and W, L and C_{ox} the width and length of the gate as well as the oxide sheet capacitance, as given in Equation 3.1. The change in the gate voltage also changes the drain current I_D in the saturation region as given in Equation 3.2 to

$$I_D = \frac{W}{2L}\mu C_{\text{ox}}\left(V_{GS} + \frac{\alpha q_s}{C_{\text{ox}} WL} - V_{\text{th}}\right)^2$$

The resulting amplification of the drain current is called g_q and the relevant quantity given for DEPFET sensors. It is calculated with

$$g_q = \frac{\mathrm{d}I_D}{\mathrm{d}q_s} = \alpha\sqrt{\frac{2\mu I_{\text{D}}}{L^3 W C_{\text{ox}}}}. \tag{3.4}$$

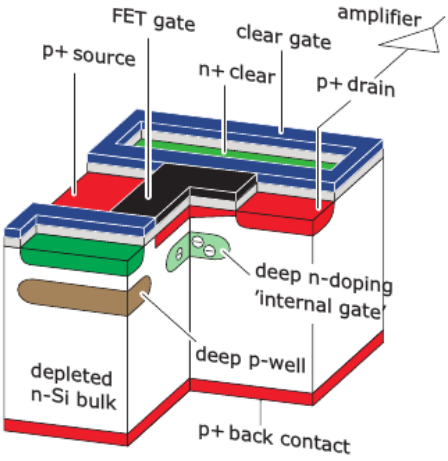


Figure 3.4: Schematic of a DEPFET pixel [13] viewing the gate, source and drain electrodes as well as the internal gate and the arrangement of clear towards the gates.

The expected amplification g_q is about 400 to 600 pA per electron at $I_D = 100\,\mu A$ which indicates the nominal operation.

However, as the electrons within the internal gate accumulate over time, the internal gate loses its attractiveness to new electrons created in the bulk, resulting in a loss of sensitivity of the pixel. To prevent this, the internal gate must be cleared after read out. In the collection phase the clear gate (shown in green in Figure 3.4) is switched off and shielded by a deep p implant. When the clear gate is switched on by applying a high positive potential, the electrons are attracted and move through the screening layer. The internal gate is cleared and set to collect new charges.

Through the small capacitance of the collecting internal gate is the DEPFET an excellent low-noise sensor type with equivalent noise charges of only a few electrons. [16, 20, 23]

CHAPTER 4

The Belle II Pixel Detector (PXD)

For the PXD as shown on the right side in Figure 2.3 40 PXD modules like the schematic one in Figure 4.1 are needed. A module has a sensitive part and **A**pplication-**S**pecific **I**ntegrated **C**ircuits (ASICs) as front-end electronics. In short, one module consists of

- the DEPFET pixel matrix,
- six steering ASICs called SWITCHER,
- four **D**rain **C**urrent **D**igitizers (DCD) with **A**nalog-to-**D**igital **C**onverters (ADC)
- and four **D**ata **H**andling **P**rocessors (DHP) which steer the other ASICs and are responsible for a first reduction of the collected data before sending it off the module.

The different parts of the module will be described in more detail in this chapter.

4.1 Pixel matrix

The DEPFET pixels as explained in section 3.5 are placed in a matrix of 250 columns with 768 pixels each. In total the matrix contains 192 000 DEPFET pixels. Four pixels together are shown as a schmatic in Figure 4.2. Two pixels share the same source electrode and those two connected transistors are surrounded by the clear gate, shielding the clear implants during the collection process. The clear implant (here in green) is orientated orthogonal to the drain-gate-source axis. The main part made up of the transistor and the clear implant is surrounded by a large drifting area. This ensures, that the electrons are collected in the pixel they were produced in and reduces charge sharing and electrons drifting into the neighbouring pixels.

All gates and clear implants of the pixels in one row are connected to two pipes running to a SWITCHER, one for the external gate signals and one for the clear ones. Hence, the pixels in one row can be steered together. Four rows make up one so-called *matrix gate* and are read out and afterwards cleared all at the same time before the next *gate* is switched on. This read out method is called *rolling shutter mode*. Within a column every fourth pixel is connected to the same circuit line going to the DCD, which is situated at the lower end of the pixel matrix. Therefore, four rows can be read out at once without mixing up the signals. When the voltage at the external gates of the pixels is droped, the DCDs read out the drain current flowing through each pixel.

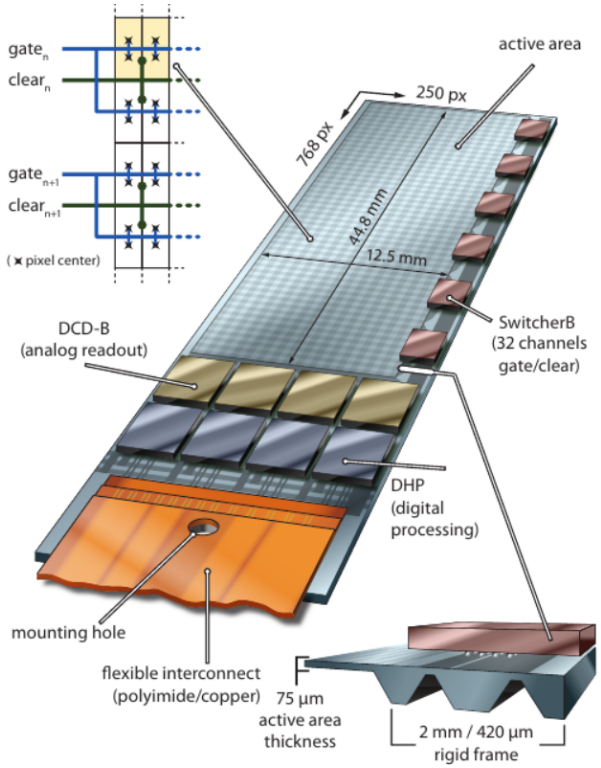


Figure 4.1: In the middle a schematic overview of an inner layer module for the PXD with a DEPFET pixel matrix, 14 ASICs and attached kapton can be seen. To the left the connections of the external gate and the clear gate are shown for a few connected pixels. In the right bottom corner a small part of the side view is shown where the thinning of the active parts and the thicker supporting structure can be seperated. [24]

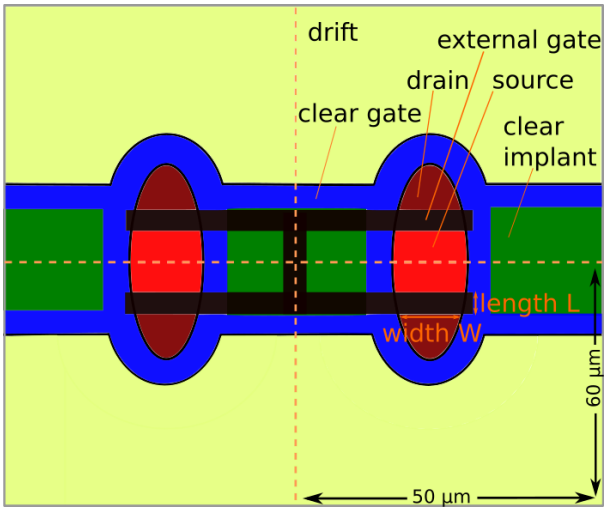


Figure 4.2: Four pixels of an inner module with the different gates and regions as a small example of the complexity of the pixel matrix. Two pixels share the same source electrode. The external gates as well as the clear implants are connected within one row.

4.2 Module

The latest generation of the module for the PXD in Belle II is called *PXD9 module*. With the pixel matrix the largest part of the module is covered. It is implemented within the silicon supporting structure of the module and covered with additonal layers for routing purposes between the pixels as well as the ASICs. As mentioned in the last paragraph, the pixels are connected row-wise to the steering chips, sitting on a balcony next to the matrix, and column-wise to the so called *end of stave* where the read out ASICs are situated. Due to the asymmetrical detector geometry, to the read out concept and the different sizes of the inner and outer layer, there are four different types of modules, which differ slightly in module and pixel sizes as well as the orientation of the steering ASICs next to the matrix. The inner module is 6.8 cm long and its width is 1.5 cm. The pixel sizes are 50 µm × 55 µm close to the interaction point and 50 µm × 60 µm under a larger incident angle from the interaction region. The outer module is 8.5 cm long while its width is 1.5 cm as well. As the total count of pixels is kept equal on both module types, the pixel sizes on the longer outer PXD module have to be increased to 50 µm × 70 µm and 50 µm × 85 µm. The different pixel sizes are partly due to the various incident angles when the module is within the detector. The part of the module that is furthest away from the end of stave is closer to the interaction point. There it is more probable that particles due to their angle only hit one pixel. The more inclined the path becomes towards the pixels further away from the interaction point, the more pixels are hit by one particle. The position of the main hit and the pixel with the most deposited energy can therefore be determined with analysis algorithms. Apart from the different sizes in the inner and outer layers, the most important distinguishing characteristic of the forward and backward modules is on which side of the matrix the balcony for the SWITCHERs is situated. One forward and one backward module are mounted face to face with the end of staves pointing in opposite directions. Thus, the SWITCHERs have to be mounted on different sides of the matrix. In general, the different modules look very similar. The matrix has the same amount of pixels, which are steered by the SWITCHERs, the data is digitised by the DCD, preprocessed by the DHP and then sent off to the backend electronics. The interconnection towards and off the module is realised via a flexible multi-layer kapton **P**rinted **C**ircuit **B**oard (PCB), transmitting signals and power to the module and sending data off. The modules are thinned down to 75 µm where the sensitive pixel matrix sits while the surrounding structure is kept thicker (500 µm) for mechanical stiffness, supporting the bump-bonded ASICs.

The read out of one complete frame of all 768 rows in 192 *gates* is for all four module types achieved in 20 µs. It can therefore be done in only double the SuperKEKB revolution time of 10 µs. The functionality of the various ASICs is explained in the following section 4.3. [16]

4.3 ASICs

The ASICs are responsible for the correct readout of the collected charge in the pixels. Before the readout and preprocessing worked as expected, a few iterations of every ASIC were necessary. The ones explained in the following are the final chips for the Belle II PXD modules. The communication between the ASICs is done via JTAG (**J**oint **T**est **A**ction **G**roup). It is used as the communication protocol to configure the system before data transmission. Within the configuration it is possible to decide whether the DCDs are included into the JTAG line, as the connections between each DCD and DHP in one pair are going both ways. For configuration purposes it can sometimes be useful to leave the DCDs out of the JTAG chain. However, for the full functionality of the detector they are included.

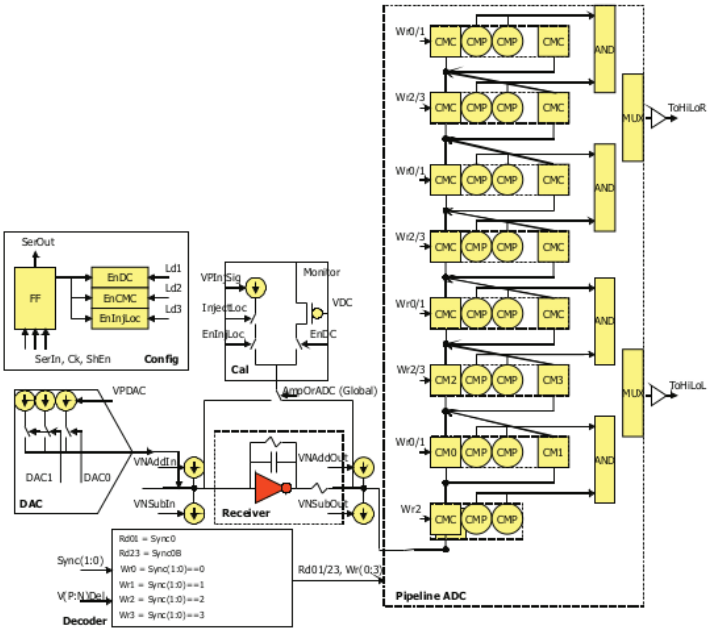


Figure 4.3: Circuit of one DCD channel showing the transimpedance amplifier (here called Receiver) in the middle of the figure and the pipeline ADC on the right. (For more information see [26]).

SWITCHER

Each of these analogue multiplexer chips controls the gate and clear voltage of 32 DEPFET matrix *gates*. The rolling shutter read out mode is done with the help of a shift register, addressing the channels sequentially. For this sequence, two high speed signals are used. The *Ser In* is a high level pulse shifted into the register. For a PXD matrix, there is only one high level signal wihin the shift register at a time. The *clock* takes care of shifting the signal through the SWITCHER. Therefore, only one gate is switched on at once. There are two more high speed signals controlling gate and clear gate, the *strobe gate* and the *strobe clear*. A negative gate signal is applied to switch a pixel on, a positive clear signal to pull the positioned charges out of the inner gate. The voltage swing within the SWITCHER can be up to 20 V. Internal register configuration is done with slow control signals using the JTAG protocol. The SWITCHER has to have a low current consumption because of cooling issues, but a fast reaction to signals to gurantee a smooth and fast readout process of the pixel matrix. The ASICs are produced by AMS in 0.18 µm HV CMOS technology. The final SWITCHER is internally called *SwitcherB18 v2.0*. [25]

DCD

The DCDs are placed at the end of the matrix, at the end of stave region, each taking up an area of 3 240 µm × 5 100 µm. Every one is equipped with 256 analogue channels with a **T**rans**I**mpedance **A**mplifier and an ADC of which 250 are connected to columns in the PXD matrix. Every DCD channel has a monitor line to which an external current source can be connected. There are over 25 DAC (**D**igital-to-**A**nalogue **C**onverter) values to regulate and control the functions of the DCD. The circuit of one DCD channel is shown in Figure 4.3.

The TIA is the analogue input stage of the ADC channel. It keeps the drain line on a constant potential, thus, increasing the readout speed, while reducing noise on the line. Further on, the digitisation of signals

from the matrix is done with 8-bit ADCs and sent off the DCD with 304.8 MHz (which means a data rate of 19.5 Gbit s^{-1} for one DCD-DHP pair). In addition, the DCD is able to perform an offset correction before digitisation. The currents from the matrix' pixels are composed of an offset, the transistor current, which is flowing even without deposited charge, and on top the amplification signal produced by the deposited charge. The offset is called *pedestal current*, which is different for every pixel, but expected to be approximately 100 µA. The signals are between 2 and 8 µA which corresponds to 1 to 4 MIPs (**M**inimal **I**onising **P**articles). As the ADC range is between 20 µA and 40 µA, there are two steps performed within the DCD to reduce the arriving current to fit the ADC range. The current of all pixels is first reduced by the same selectable amount, aiming to subtract the offset current. As this is not the same in every pixel, a 2-bit programmable current source afterwards adds different amounts of current to the pixel currents depending on how large the incoming current still is. Thereby, a compensation for large pedestal spreads is achieved. The latest DCD version is internally called *DCD4.2*. [16, 26]

DHP

The DHPs take up an area of 3 280 µm × 4 200 µm each and are placed in pairs with the DCDs at the end of stave. They are the module controllers, responsible for steering the other ASICs, thus, making sure that the data flow is continous. Furthermore, they are the interface to the backend electronics. As they have different tasks, the connections towards and going off the DHPs are sorted in the following by the different communication partners.

- **DCD**
  - **Towards** the DCD a steering clock signal *CLK* with a frequency of 304.8 MHz and a synchronising signal are sent.
  - The offset correction DACs of the DCD are steered by a 8×2-bit-bus.
  - ROW2_SYNC is there for synchronizing the DCDs. It is sent once every 128 clock cycles.
  - **From** the DCD the digitised data is received with a frequency of 304.8 MHz at 8×8-bit-bus input lines which results in a data rate of 19.5 Gbit s^{-1}.
- **Switcher**
  - **Towards** the SWITCHERs the DHP closest to the SWITCHERs sends a clock signal (*CLK*), which is synchronous with the DCDs digitisation signals. In addition the *Ser In* signal as well as the control signals for gate and clear are given to the SWITCHERs.
- **Backend Electronics**
  - **From** the backend electronics a global reference clock (*GCK*) at 76.2 MHz is sent as the main clock.
  - *TRG* is a trigger signal for the zero-suppressed readout (explained in the following paragraph).
  - **Off the module** the data is transmitted with differential **C**urrent **M**ode **L**ogic (CML) over a differential pair cable at a bit rate of 1.5 Gbit s^{-1}. As there are losses (e.g. skin effect, parasitic capacity) due to the high transmission frequency, a concept called *deemphasis* is introduced to reduce the negative effects. A more detailed explanation can be found in section 6.1.

The serialised data from the DCD is deserialised and written into a raw data memory ring buffer which can store the data of 1 024 full pixel rows. When the trigger arrives from the backend electronics the data processing starts. A data reduction from a rate of 19.5 Gbit s^{-1} coming from the DCDs to

1.5 Gbit s^{-1} data sent off the module for further processing is necessary. This reduction by at least a factor of 16 is achieved with the following steps. First a pedestal subtraction of previously stored pedestals is performed. Afterwards, zero-suppression of the data is done. Zero-suppression is the process ensuring that only information of pixels with a detected signal is sent off the detector. Every pixel, where no remaining signal is found after the pedestal subtraction, is discarded. Therefore a suppression of pixels with zero signal is carried out. The DHPs of the final generation are produced in 65 nm TSMC (**T**aiwan **S**emiconductor **M**anufacturing **C**ompany) CMOS technology and for the company name a T is added in the ASIC name. Therefore the DHP is internally called *DHPT1.2b*. [16, 27]

4.4 PXD

The pixel detector consists of 40 PXD modules in two layers. As shortly explained in the vertex detector paragraph of section 2.2, those 40 modules are ordered in two layers, with 16 modules in the inner layer and 24 in the outer layer. Two modules are glued together at the small side of the matrices opposite the readout ASICs and called a *ladder*. The ladders are firmly screwed to a metal holding structure on one side, while the screw on the other side sits inside of an elongated hole in the module structure to allow for temperature-dependent movements of the ladder. The readout ASICs sit on top of the metal structure. As they are the most power consuming parts of the module, the holding structure functions as a cooling block with liquid CO_2 running in small pipes through the metal. The full module's power consumption lies below 9 W, of which the active area produces $\approx$ 500 mW. This is achieved through the rolling shutter readout mode. Therefore the pixel matrix is only cooled by a circulated air flow.

CHAPTER 5

Hybrid 5

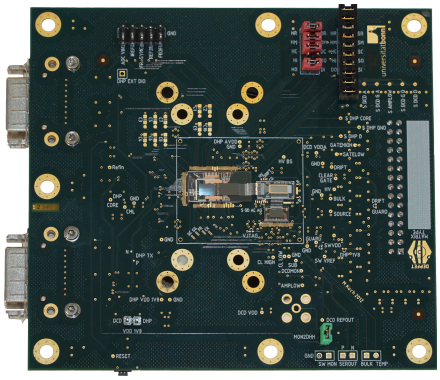
Before the final, fully assembled modules can be built, the components have to be tested individually as well as on small scale systems. The first tests are done with a probe card on the individual ASICs to see whether the electrical circuits are functional. After the basic validations are done in this way, the communication between the ASICs and the matrix are tested on a PCB (**P**rinted **C**ircuit **B**oard), the so-called *Hybrid 5*. The full PCB can be seen in Figure 5.1(a).

It offers space for a minimal full demonstrator system with a small matrix, steered by one SWITCHER, with one DCD to digitise the currents and one DHP for preprocessing before the data is sent off to the backend electronics. The ASICs are bump-bonded onto silicon wirebond adapters as they cannot go directly on the PCB. The matrix, however, is glued directly onto the PCB. Wirebond pads are built in. The adapters are glued on top of the PCB and connected to it, each other and the matrix with wirebonds. The DCD and DHP are put on the same adapter, connected with copper lines like it is done on the final PXD modules. At the position of the pixel matrix there is an opening in the PCB. This reduces the amount of material in the particles' path, therefore reproducing the situation of the final modules more closely.

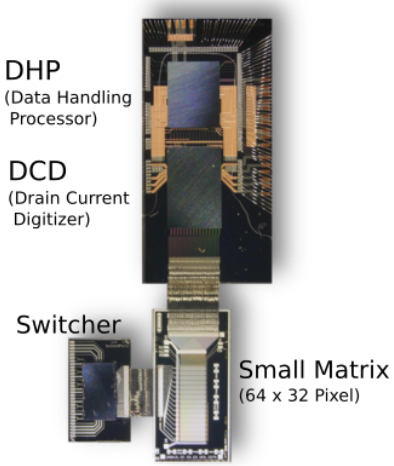
The Hybrid is powered via a connector by the company *Samtec*. Two Infiniband cables are used to connected the Hybrid to the DHE. The PCB offers probe points for all ASIC and matrix supply voltages as well as all control signals. Hence, the Hybrid is a thorough testing board for functionality and interaction of the PXD module components. This work presents results of the first tests of the system with with all final version ASICs as given in section 4.3 and a small PXD matrix with 32×64 small pixels. The pixel matrix W31 F00 has the same properties as the large final matrices. It is thinned down to 75 µm and was produced as part of the wafer number 31. The matrix is of the type ARR_ST_A_L5_Z55. Z55 means that the pixels are 50 µm × 55 µm in size. This corresponds to the small pixels of the inner module, see Section 4.2. L5 indicates a gate length of 5 µm.

5.1 Experimental Setup

The full experimental setup can be seen in Figure 5.2. It consists of the Hybrid as shown in Figure 5.1, externally powered with a custom-made **P**ower **S**upply (PS), and the backend electronics. The latter consists for this system of a breakout board and one DHE (**D**ata **H**andling **E**ngine). The breakout board's function is to enable a change from two Infiniband cables to one Infiniband and one Ethernet cable. This is necessary, because the most recent version of the DHE has only one Infiniband plug and one RJ45 plug. The breakout board was originally developed for JTAG boundary scans [28]. In this setup, it is used to convert between the different cable types. This is necessary due to placement constrains later in



(a) Hybrid 5 module with a small matrix, a SWITCHER, a DCD and a DHP.



(b) Closer look on tested ensemble, placed in the middle of the Hybrid 5 board.

Figure 5.1: Hybrid 5

the Belle II detector setup. The DHE provides JTAG configuration of the ASICs, fast control signals (CLK and TRG), and receives the module data from the DHP via a highspeed serial link at 1.5 GHz. The DHE sends the data per UDP (**U**ser **D**atagram **P**rotocol) over the Ethernet cable to the computer. The data is then stored on the computer and can be accessed for analysis purposes. More details on this can be found in Section 5.1.2.

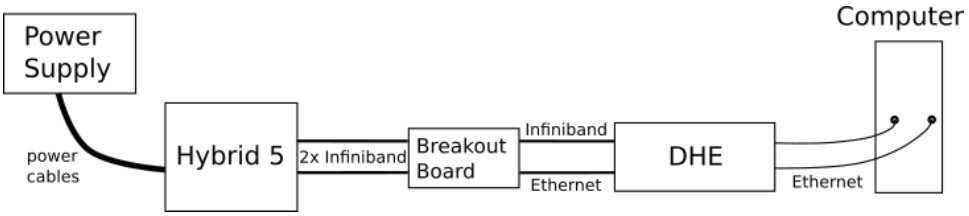


Figure 5.2: Schematic overview of the complete test system.

On the system a step-wise characterisation of the single components as well as the interconnection is performed and described in Chapter 6. In the beginning the parameters for an error-free data transmission off the module over a 15 m connection are optimised. Afterwards the communication between DCD and DHP is looked at, to make sure that no data is lost in a wrong sampling process. Furthermore, the functionality of the ADCs in the DCD has to be contolled and optimised. When the frontend electronics are working optimally, the matrix is investigated and parameter ranges for the pixel regulation are set before an energy and gain calibration can be achieved with various source scans. This second part of the investigations is documented in Chapter 7.

5.1.1 Matrix Investigations and Source Scans

For the matrix investigations and source scans the Hybrid is placed in a box of lead. It is mounted frontside down in a small aluminium housing to shield the matrix from light and stabilise the Hybrid's position. Thus, especially the Hybrid's front side is protected. There are two different kinds of measurement

methods due to the weight of the source surrounding cases and the activity of the sources themselves. The sources surrounded by light cases can be placed directly on top of the PCB. Therefore, the aluminium housing is opened only on the backside of the PCB, adhesive tape made of kapton is put over the electronic components, the source is placed directly on top of the PCB with the kapton as insulator between the two. A black cloth is put over the source and matrix to replace the light shielding effect of the housing's lid. The sources surrounded by a heavier case as well as those with a high activity cannot be put directly on the PCB. In the first case, they might damage the PCB and subsequently the matrix. In the second case, they are active enough to deposit more energy within the pixel as the readout system is designed for. As the intensity of radioactive decays decreases with the distance squared, the 2 cm distance created by placing the source on top of the aluminium housing lid reduces the intensity.

A schematic of the setup for source scans can be seen in Figure 5.3. The source is about 2 cm away from the matrix, showing the situation for the sources enclosed in heavy cases. The lighter source cases are placed directly on top of the PCB and the kapton tape.

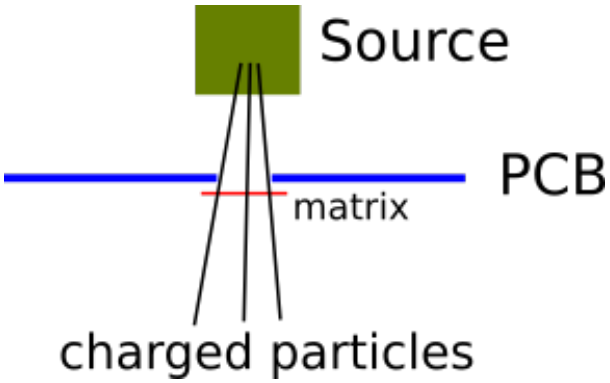


Figure 5.3: Schematic of the setup for the source measurements

5.1.2 Software

The software side of the Hybrid system is shown in Figure 5.4. The system is steered by a distributed control system called *EPICS* (**E**xperimental **P**hysics and **I**ndustrial **C**ontrol **S**ystem [29]). The Slow Control of all system components (PS, DHE, database etc.) is controlled by *EPICS*. Every setting is a variable and can therefore be read and changed within the control system. Those so-called **P**rocess **V**ariables (PVs) can be manipulated by python scripts as well as the GUI (**G**raphical **U**ser **I**nterface). All measurements as well as the analysis are done via python scripts as seen in the upper left hand corner of the figure. The GUI is shown with a screenshot on the right side. It opens up the possibility to change PVs, but also monitor the complete system at all times, because voltages and currents are updated in short time intervalls. The IOC server regulates everything in relation to EPICS, it makes the PVs available and constitutes the interface to the hardware (DHE). Variables are stored there and changes are going via the IOC Server. It communicates with the scripts as well as the GUI for all information regarding PVs. Changes in PVs representing ASIC registers only become active when the register contents are written via JTAG. JTAG writes only happen on request. The BonnDAQ software gets the measured data from the DHE via a UDP connection and stores it. Both, the IOC Server and the Bonn DAQ Server, are connected to the DHE with Infiniband cables. The Hybrid is connected to the configuration and readout system over two Infiniband cables. Those serve different purposes. One is used for the configuration of the system over an IPBus connection from the DHE, the other one for data transmission to BonnDAQ.

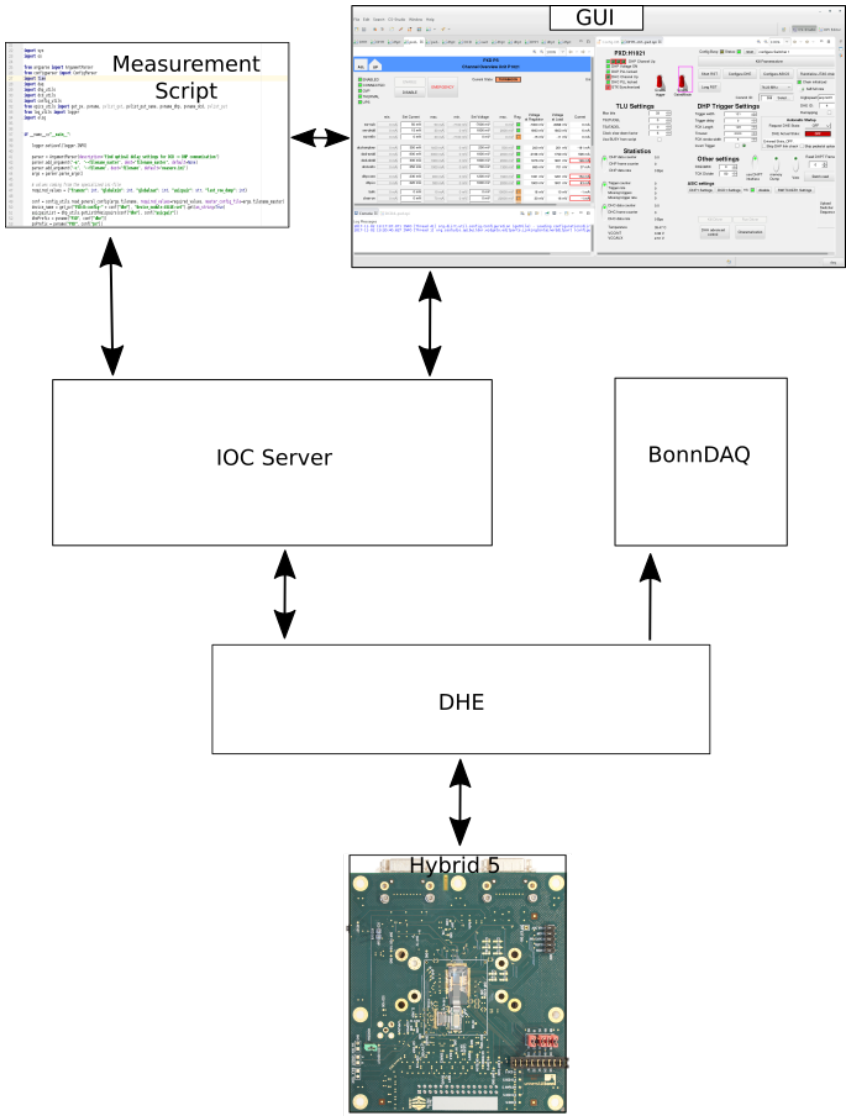


Figure 5.4: Schematic overview of the complete testing system

CHAPTER 6

Characterisation of Hybrid 5

This master's thesis is the first to investigate a fully assembled demonstrator module (Hybrid 5) with final components. While the different components underwent a long development process and various generations were necessary, many test procedures and scripts were developed over the last years within the *DEPFET collaboration*. Often intensive studies were done for single measurements. The developed scripts and routines were used for the following investigations, characterising single ASICs and the communication between them.

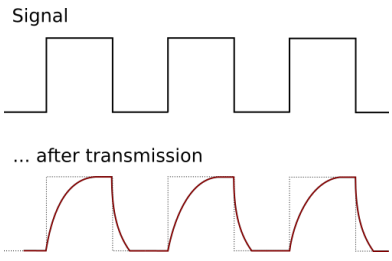
6.1 High-Speed Scan

As was mentioned in Chapter 5 already, the differential digital data has to be transmitted over a 15 m cable from the DHP to the backend electronics. In the Belle II experiment, the distance for the data transmission will be covered with an optical cable. Optical transmission is not subjected to the damping effects of electrical cables. It was therefore decided to be used, because with previous DHP generations it was not clear whether they would have the driving capability to transmit the data over the required distance in the end. In the lab setups and therefore for the following investigations an Infiniband cable of the same length was used. Anyway, this distance cannot easily be covered by a signal at 1.5 GHz frequency, because of degrading effects. In Figure 6.1(a) a sketch of a square wave signal is shown before and after transmission. After the transmission it is more distorted and after long distances it gets increasingly degraded up to the point of not being recognisable as a signal to the backend electronics anymore. In digital systems, only high and low level can be seperated. If the signal does not cross the related thresholds, it is received wrong. Therefore, the rising and falling edges have to be steep to assure an error-free transmission.

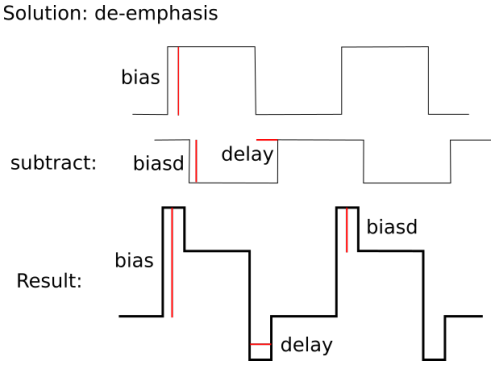
6.1.1 De-emphasis

The solution to transmit the signal over the required distance is shown in Figure 6.1(b). Before the differential signal goes through the transmitter on the DHP side, another differential signal is branched off. This parallel signal is delayed, inverted and the amplitude is modulated to be smaller, when it is merged back with the original signal. The delayed and inverted signal is added onto the original signal, creating a higher amplitude only at the beginning of the resulting signal (see Figure 6.1(b)). Therefore the slope of the rising edge of the transmitted signal becomes steeper and the received signal less distorted. Thus, the backend electronics detect the signal with a higher probability as there are less transmission errors occurring.

This approach leaves three parameters to be optimised. The amplitude at the beginning of the signal is called *bias*, the amplitude of the inverted signal *biasd* and the shift between the two signals *delay*. Different options for all three parameters are possible. There are 256 options for *bias* and *biasd*, because they are regulated by 8-bit DACs (**D**igital-to-**A**nalogue **C**onverters). For the *delay* variable four different values can be created by a certain number of inverters and reinverters slowing the signal transmission. To find the right settings, sweeps over all possibilities are performed and the stability of the link between frontend and backend electronics is thereby tested.



(a) Transmission over longer distances leads to a distortion of the signal after the transmission...



(b) ... which can be solved by the concept of de-emphasis. The three parameters determining the signal shape are indicated here. The sketch is adopted from [27].

Figure 6.1

6.1.2 Sweep Scan

The scan sweeps with given step sizes for all three de-emphasis parameters through the chosen parameter space. For every new setting, the high speed link is initialised. After a chosen time span the link is checked again. If it is still up, the link is noted down as stable for these parameters. If the link broke or could never be established, it is unstable. After the link is tested and its status recorded, the next parameter combination is set. In Figure 6.2, the results for a scan with 15 m Infiniband cable for the high speed transmission are shown for the longest *delay* setting with a step size of 15 for *bias* and *biasd*. The waited time span was 5 s. The white parts indicate that the link broke over those 5 s or could not be established at all. The yellow region indicates that the link is stable over this time and the measured amplitude between the low and the high signal level in arbitrary units is as large as possible in this measurement. This is indicated by the colour scale on the right side. If shorter *delays* are chosen, the possible parameter space shrinks down, because the two signals are less far shifted against each other. (Anhang?)

The possible amplitude can be investigated with so-called *eye diagrams*. Detailed analysis of the amplitude through this method can be found in [30], here only two examplary diagrams are shown in Figure 6.3. To generate them, different sequences for changes between the high and low level are produced. All those sequences are created by a pseudo-random generator in the DHP and stacked over each other by an oscilloscope. The triggering is done internally by the oscilloscope. Therefore only such diagrams can be produced where a structure in the data can be found by the electronics. For a thorough investigation of the difference between the low and the high level, the so-called *eye opening* is analysed. Figure 6.3(a) is an example for good settings, which produce a wide and symmetrical *eye*

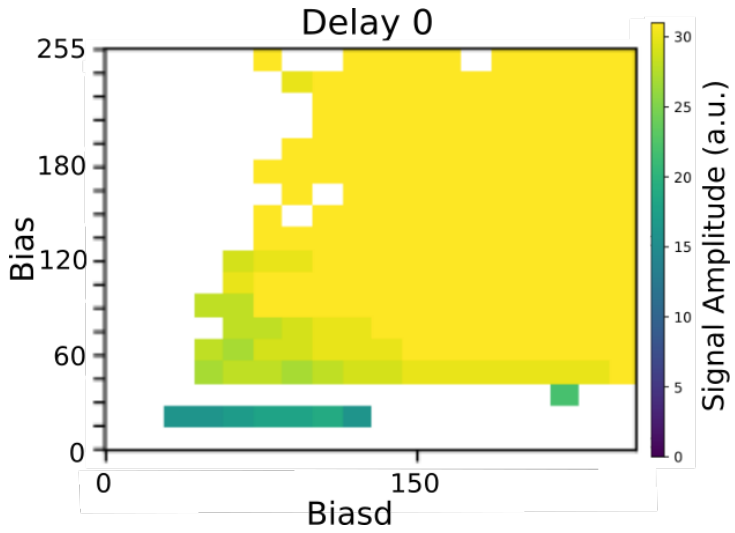
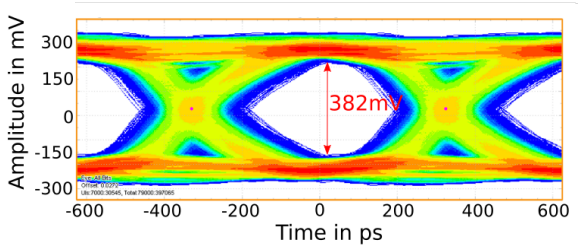
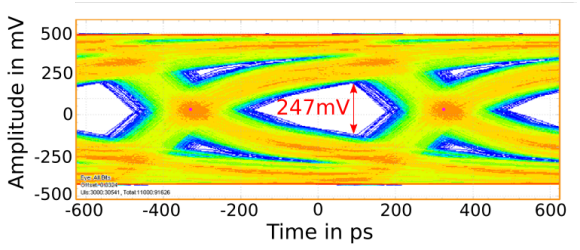


Figure 6.2: Sweep over full range of *bias* and *biasd* for *delay* = 0 and 15 m data cable. The yellow region corresponds to the largest amplitude measured and a stable link over the chosen time span of 5 s.

opening. The possible crossings from the low to the high data level and back are similar and steep. The parameter combination of *bias* = 255 and *biasd* = 200 is situated in the upper right hand corner of Figure 6.2. For Figure 6.3(b) *bias* = 80 and *biasd* = 0 are used. The parameter combination can be found in the white part on the left side of Figure 6.2. The eye diagram shows a wide spread of possible crossings between the low and high data level. The edges are not steep anymore and it takes longer before the other level is reached. The maximal amplitude is therefore smaller and decreases fast to both sides of the maximal opening. The development company *Xilinx* specifies 125 mV as the smallest *eye opening* for a well working system [31]. In general, a wide and symmetrical opening is more probable to indicate stable working conditions. Because those amplitude investigations take time for every chosen parameter combination, a High Speed link scan is done first to find possible parameter spaces. Within this preselection, single parameter combinations can than be checked in more detail. Previous measurements showed that a once found working setting can be used for other systems as well, thus, *eye diagrams* are not regularly necessary.



(a) For *bias* = 255 and *biasd* = 200 a maximal amplitude of 382 mV is measured.



(b) For *bias* = 80 and *biasd* = 0 a maximal amplitude of 247 mV is measured.

Figure 6.3

6.2 Delay Scan

The *Delay Scan* investigates the communication between DCD and DHP. The digitised data is transmitted from DCD to DHP. The sampling point in the DHP has to be chosen correctly to ensure an error free transmission. It can be shifted by a variable number of delay elements. The number of necessary elements is determined by the delay scan.

6.2.1 Communication DCD-DHP

In Figure 6.4(a), the connections between DCD and DHP are shown. The steering signals from the DHP to the DCD are a clock (CLK) and a synchronising signal (SYNC). In the other direction, there are 64 data lines from the DCD to the DHP. Every line is transmitting one bit of the 8-bit digitised output code of an ADC. 32 ADCs are connected to the same eight data lines, serially sending off their digitised data. There are two different kinds of delay elements. The *global delay* shifts the clock signal, which is sent to all ADCs, therefore shifting the data sending in all channels. The *local delay* elements, sitting at the DHP's end of every transmission line, take care of the individual adjustment in relation to each other. Every delay element consists of two inverters. The signal is inverted and afterwards re-inverted, taking advantage of the additional transit time the signal needs to pass through the inverters. There are 16 daisy-chained elements for both delay kinds and it can be freely chosen how many elements should be included in the signal path.

To determine which delay combination gives optimal results, a testpattern is sent many times from the DCD to the DHP. The sampled data in the DHP is read out and compared to the testpattern.

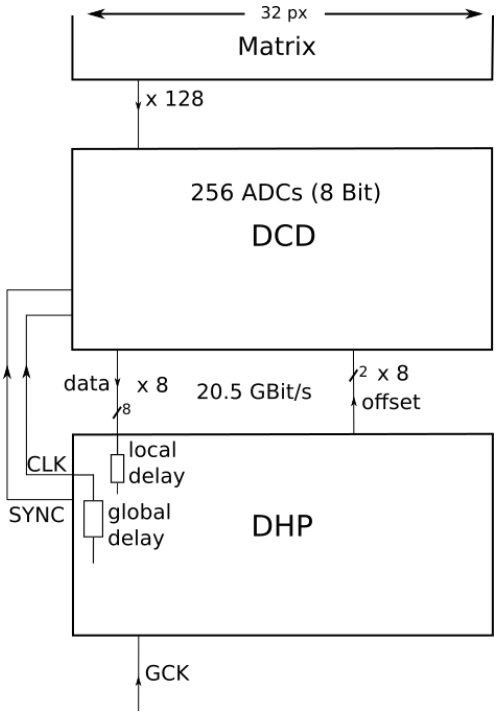
6.2.2 Results

The comparison between the recorded data and the testpattern is done bitwise and the number of wrong bits for every setting is recorded. For all 64 lines the *global delay* is plotted against the *local delay* like shown exemplary for Bit 0 in Figure 6.4(b). The colour code indicates the number of bit errors for the respective settings. The colour bar is cut off at two bit errors, because only parameter combinations without any detected communication error are working ones. The testpattern covers many different transitions between the high and low signal levels, but can never cover all possible combinations, because it is constrained to a length of 32 clock cycles by the DCD. Thus, possible bit errors might not be detected. However, as the best estimation for a sampling point, a setting in the middle of the 0-bit-band is chosen as working parameter set. In Figure 6.5 all 64 transmission lines are shown in an overview plot. The eight rows are labeled with the corresponding ADC numbers, 32 ADCs for each row. The eight columns correspond to the eight data lines, which are used by the 32 ADCs. The first column is the **L**east **S**ignificant **B**it (LSB), which represents the last one in an 8-bit digital number. The last column represents the **M**ost **S**ignificant **B**it (MSB), which is the position of 2^8 in an 8-bit digital sequence.

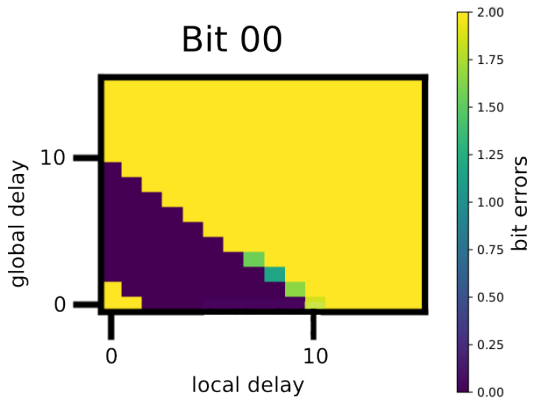
6.2.3 Diagonal Delay Scan

The band structure as seen in all subplots of Figure 6.5 is observed in every delay scan. Therefore, a new algorithm was developed, not scanning the full parameter space but only the values on the diagonal of the *global* and *local delays*. The configuration with identical *global* and *local delay* values as well as *global delay* = *local delay* + 1 are used. Thus, the following sequence is created:

$$(0,0),(0,1),(1,1),(1,2),...,(15,15)$$



(a) Communication between DHP and DCD as in the final PXD configuration. There are 64 lines between the frontend ASICs, which transmit the 8-bit digitised signals of 8 ADCs in parallel.



(b) Calculated bit error rate between testpattern and readout data for bit 0 at all possible settings for the *global* and *local delays*.

Figure 6.4: DCD-DHP communication

The scan is done in the same way as over all possible combinations, but much faster as only about 12 % of the parameter space have to be scanned. An example for all 64 transmission lines can be seen in Figure 6.6. The eight bits in one column are put into the same plot as they show the same significant bit and even in the full scan plots similarities in these plots can be found. The different ADC channels are indicated by the different colours. The bit error rate is plotted against the added *local* and *global delay* values. The wide range where the bit error rate equals 0 corresponds to the violet band in the full scan plots in Figure 6.5. The second plateau moving further on the x-axis indicates a shift by one readout cycle, while the third plateau means a shift by two readout cycles. The settings in the third plateau produce less bit errors as the chosen parameters for the second plateau. This is, because the testpattern often changes from 0 to 1 back to 0. A shift by one readout cycle produces therefore more bit errors as a change by two cycles. Like for the full parameter space the working parameter combinations lay in the middle of the 0-error-bit-plateau and every combination of *global* and *local delay* values resulting in a sum of 4 or 5 works.

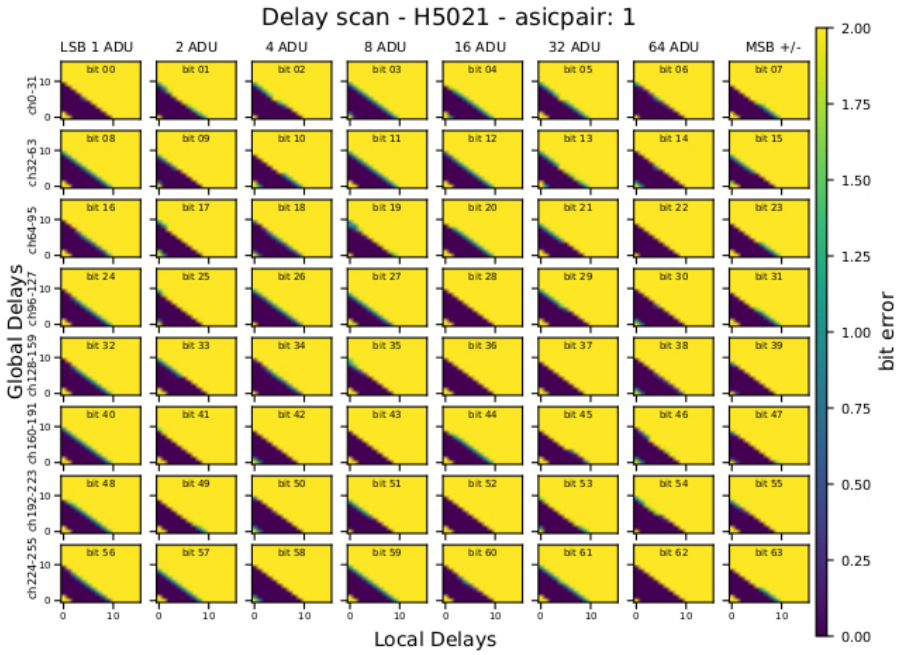


Figure 6.5: Calculated bit error rate between testpattern and readout data for all 64 lines and all possible settings for the *global* and *local delays*.

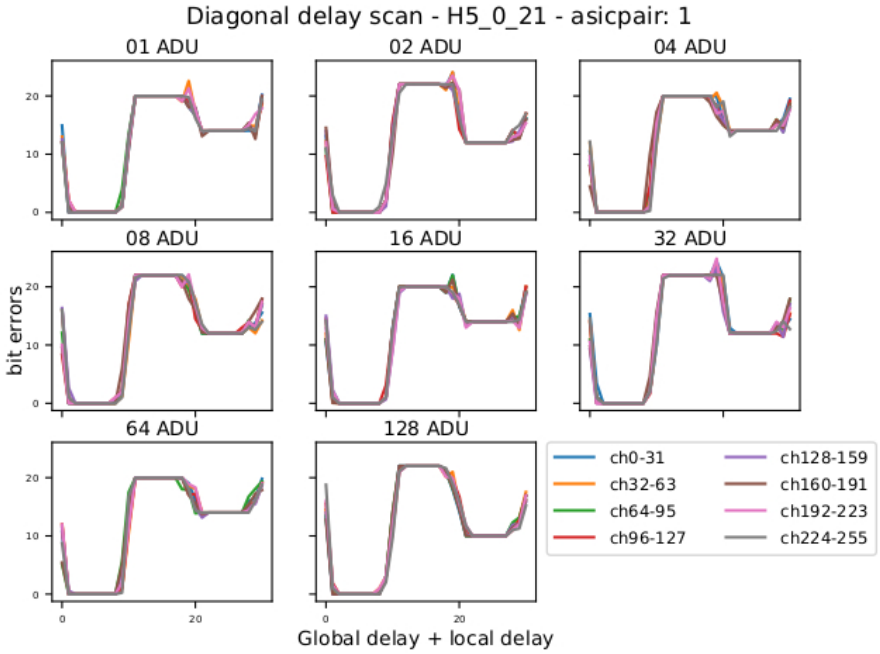


Figure 6.6: Calculated bit error rate between testpattern and readout data for all bits at those settings for the *global* and *local delays* which lay on the diagonal.

6.3 ADC Scan

To characterise the DCD's performance, a closer look has to be taken at the performance of every single ADC within the DCDs. The functionality of the ADCs is investigated by analysing the ADC transfer curves. Those are the ADCs output code measured against a known applied external current and look like the example in Figure 6.7. The external current can either come from a highly linear, finely tunable current source on the DHE or from the DEPFET transistors. In the first case, the current is injected before the TIA and can only be applied at one DCD channel at a time. The second possibility is faster, because all ADCs get a current at the same time, but the current is not as tunable and well-known as the one from the external source.

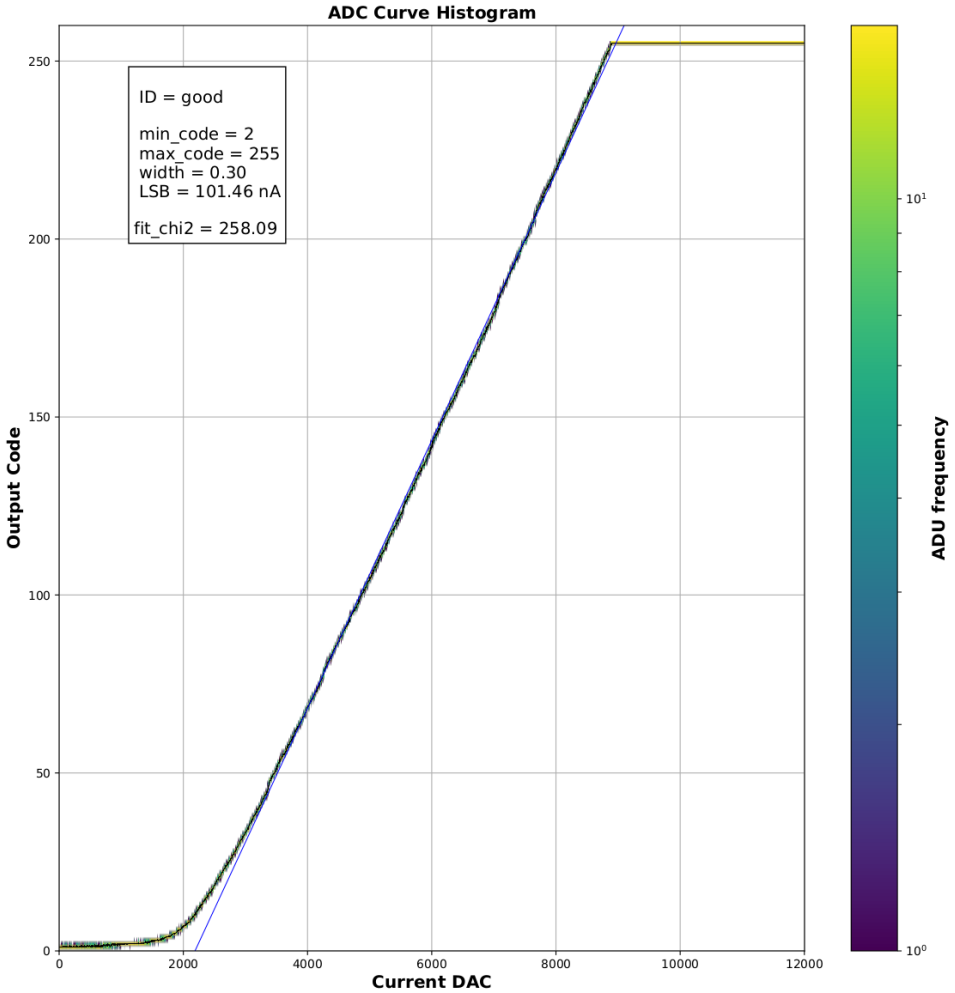


Figure 6.7: A good example of an ADC curve. A current DAC is connected and a known current injected into the ADC. The digital output code is recorded and used to characterise the dynamic range, linearity and noise of the ADC.

6.3.1 ADC curves

ADC transfer curves and therefore the performance of the ADCs are analysed for their dynamic range, linearity and noise. Measurements for every applied current are done multiple times and the average values of the output code o are calculated from those. The plots as shown in Figure 6.7 are two-dimensional histograms with the colour code indicating the number of times each bin on the ADC curve was recorded.

The output codes o are measured multiple times for one input current i. This is done to determine the level of electrical noise on the ADC curve. The Standard deviation σ_i as a function of the input current then gives the noise level from all output codes corresponding to the input value i. The overall noise σ of the ADC curve is therefore calculated as the median of all σ_i values. The so measured noise of the ADC combines the noise on the incoming signal with the noise introduced by the ADC itself.

As the DCD consists of 8-bit ADCs the natural output range lies between -127 and 127. Through a digital conversion, this is changed to a range of 0 to 255 to have the ADC value of 0 indicating no applied current. The input current is adapted to the range with subtracting a current by setting the *SubIn* DAC value. Therefore, every input current corresponds to a digital output code in the range 0 to 255. A higher input value means a higher output code. The ADC output code does not necessarily increase directly from a zero input onwards but can have a plateau before the output value starts to rise. The same also happens at the maximal value. Those bins in the plateau are the overflow and underflow bins. The range in which a correlation between an input current and an output code can be expected to be distinct, can vary depending on the ADC. The real input range covered by the ADC is called the *dynamic range* of the ADC and has to be roughly the same range as the expected input into the ADC. At the same time, the full output range of the ADC should be used to optimise the resolution. In Figure 6.7 the covered input range corresponds roughly to a range of 1 800 to 8 800 arbitrary units of current DAC. One current DAC step corresponds to 3.814 nA [32, 33]. The input range corresponds to currents between 6 865.2 to 33 563.2 nA.

The SubIn value corrects not only the difference in the ADC range but also subtracts large parts of the pedestal current before the analog signal enters the TIA and the ADC. The pedestal current is the drain current with values around 100 µA. The part of the pedestal current that is not subtracted can be measured (see Chapter 7). In this thesis the term "pedestal current" is used for the small rest amount after the subtraction.

In the dynamic range of the ADC curve, linearity is important to have a fixed difference in DAC currents corresponding to the same change in ADC output codes independent of the position on the curve. This saves an additional calibration for the output values. Deviations from the linear behaviour can be measured in two values. A local non-linearity is called a ***D**ifferential **N**on-**L**inearity* (DNL) while the discrepancy from a linear behaviour of all local deviations up to the currently observed DNL is given in the ***I**ntegrated **N**on-**L**inearity* (INL). When f_o denotes the number of occurences of the output code o and m is the calculated mean value of multiple measurements, which result in the output code o, then the DNL is given as

$$\mathrm{DNL}_o = \frac{f_o}{m} - 1 \tag{6.1}$$

which shows the local non-linearity for the output code o. The INL of the output code o is then simply the sum over all DNLs up to DNL_o,

$$\mathrm{INL} = \sum_{k}^{o} \mathrm{DNL}_k. \tag{6.2}$$

From the Equations 6.1 and 6.2 follows that a missing output code gets a DNL = −1 and a recurringly appearing code has a positive number. The optimal, because linear, case would be to have $DNL_o = 0$ for all output codes which then results in INL = 0 for the complete ADC curve. As this is not the reality, the INL_{pp} can be calculated as the difference between the maximal and minimal INL to determine the linearity over the whole ADC curve with

$$INL_{pp} = |\max(INL) - \min(INL)| \,. \tag{6.3}$$

6.3.2 ADC parameter

A detailed description on how the ADCs work can be found in [34] and will be outlined here in a simplified manner. The 8-bit pipeline ADCs digitise the input current through 8 cycles of comparing the input current to given thresholds and adding or subtracting currents depending on whether the input is too high or too low. After each comparison the resulting current is doubled and sent to the next cycle. Every stage in the ADC contains **C**urrent **M**emory **C**ells (CMCs) and comparators which contain several DACs and two bias voltages. Through optimisation and characterisation measurements over the last years a subset of important settings in the operation process of the ADCs could be determined. This subset consists of

- IPSource [DAC] - shifts the reference current of the comparators and therefore determines the dynamic range of the ADC.
- IPSource2 [DAC] - responsible for the working point of the transconductors. The value should by design be identical with IPSource.
- IFBPBias [DAC] - the biasing current of the transconductors. It determines together with IPSource the dynamic range and should by design be identical with the other DAC value.
- AmpLow [voltage] - the amplifiers ground potential in the current memory cells and the comparators.
- RefIn [voltage] - current dump and fixed potential reference at different nodes of the current cells and the comparators.

[34]

For those parameters one- and two-dimensional sweeps are performed in an experimentally established succession to determine working parameter ranges. The measurements were through a mistake only executed for the ADCs 0 to 251.

6.3.3 Results

All five parameters, DACs and voltages, are applied only once for the complete DCD and therefore the optimal settings are found when all ADCs work in the best possible way. For the parameter sweeps the following order was determined: First, AmpLow and RefIn are scanned and the resulting voltages are used for the second sweep over IPSource and IPSource2. The last parameter to be optimised is IFBPBias which is done in an one-dimensional scan while the results from the other scans are already applied. For all scans, all 256 ADC curves are analysed for the factors introduced before: dynamic range, noise, INL_{pp}, DNL and any other communication error that can occur, like bit errors. There are thresholds defined for every criteria, as Table 6.1 lists in detail.

criteria	sub criteria	minimal	maximal
range	-	< 30	> 240
DNL		1.3	-
	neighbours	-	0.8
	one neighbour	-	-0.8
INL_{pp}	-	-	10.0
noise error	-	-	1.5

Table 6.1: Thresholds for different ADC curve criteria, used to decide on the number of good working channels

Those passing a threshold are considered good working ADCs for this criteria, the ones that do not pass are considered non-working ADCs. The number of good working ADCs is added up and converted into a colour. Green corresponds to all or almost all ADCs passing the threshold for this criterium, red indicates only a third or less of the ADCs are fully working for the chosen parameter combination. Every criteria is documented in an overview plot for all parameter sweep settings. If an ADC passes the thresholds for all criteria, it is taken into the sum for the "product of all criteria" plot, which is the last one created. From the product of all criteria the working parameters can be determined. The settings with the highest number of good working ADCs are chosen.

In Figure 6.8 the sweep over AmpLow between 100 and 500 mV in steps of 50 mV and RefIn from 600 to 1 200 mV in steps of 100 mV is shown.

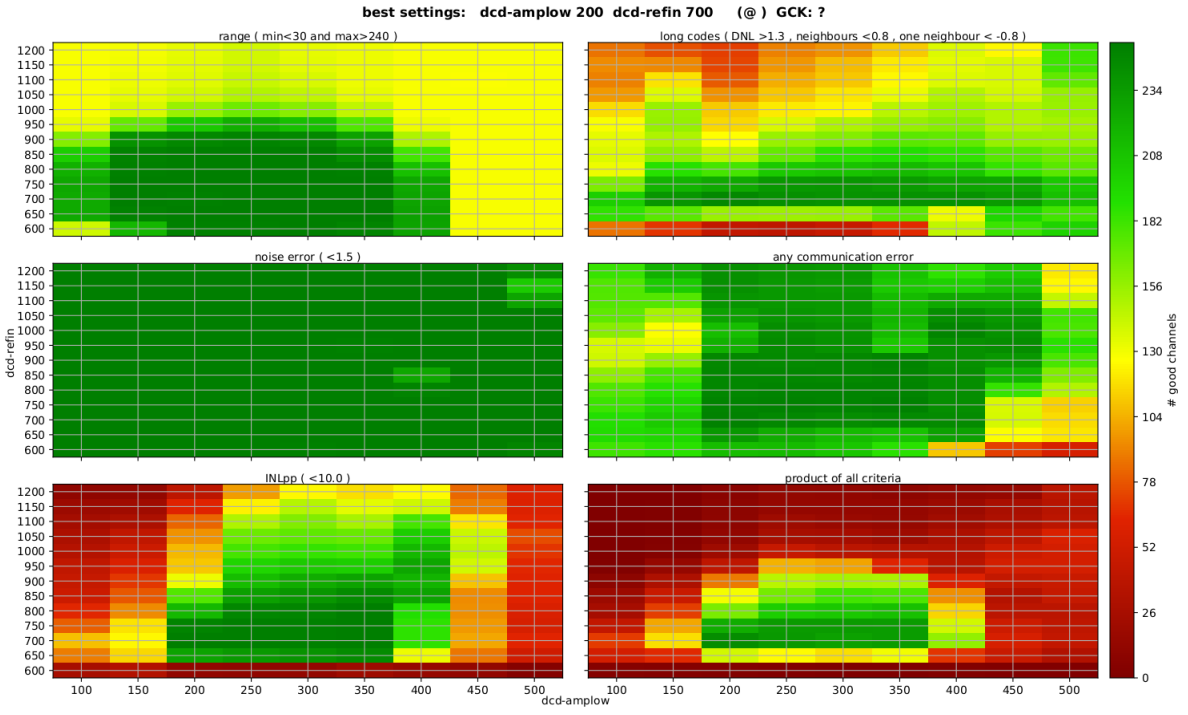


Figure 6.8: Parameter sweep over AmpLow-RefIn. For the five possible features the number of good channels is calculated and put into individual plots. The sixth plot shows the product of all criteria and an optimal setting is extracted, suggested and printed as the headline by the analysis script.

Five plots show the number of good channels for each parameter combination colour encoded. The last plot in the bottom right corner shows the result when all criteria are taken into account. Large regions of

the parameter space are excluded due to one or more criteria. But there are eight parameter combinations shown in a dark green. The number of working ADCs at these settings is spread between 220 and 243, as can be seen in the data sample. The best response with 243 ADCs is at AmpLow = 200 mV and RefIn = 700 mV. This is also given in the headline over the plots and will be set for the next sweeps.

The second scan is done for IPSource from 70 to 105 and IPSource2 between 55 and 95, both with stepsize 5. The results can be seen in Figure 6.9.

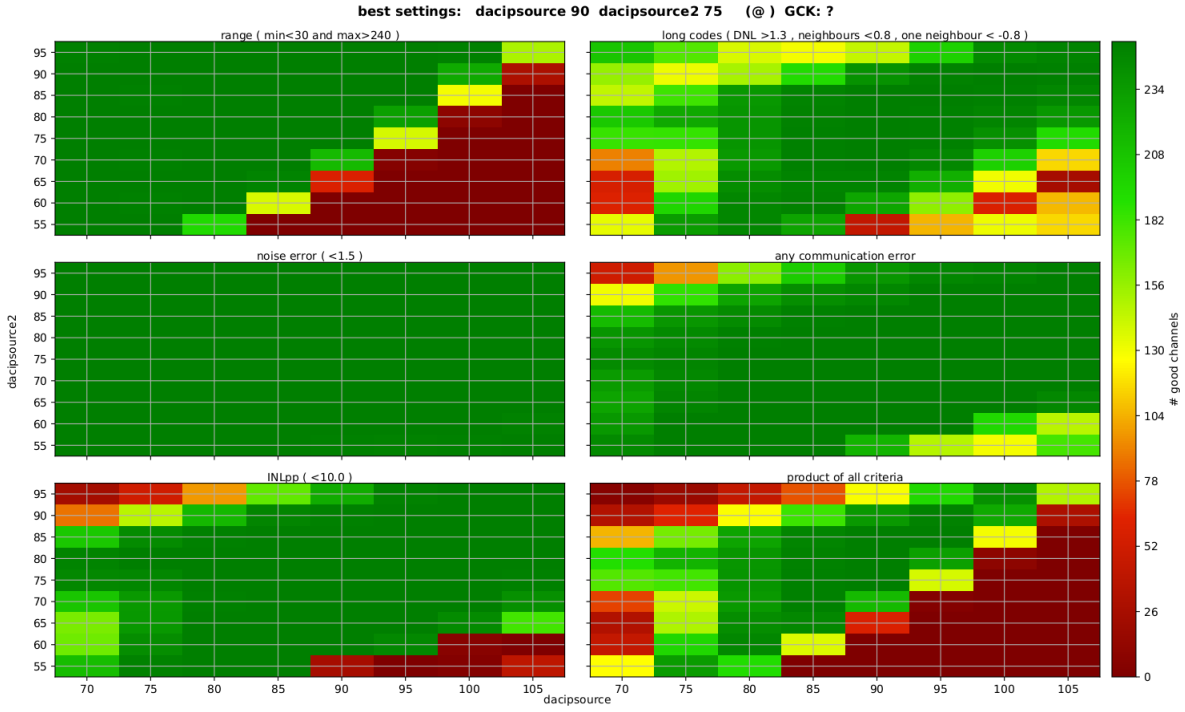


Figure 6.9: Parameter sweep over IPSource-IPSource2. For the five possible features the number of good channels is calculated and put into individual plots. The sixth plot shows the product of all criteria and an optimal setting is extracted, suggested and printed as the headline by the analysis script.

The plots are done for the same criteria as before and the colour code indicates again the number of good channels. In the sixth plot at the bottom right corner, a wider red area can be excluded completely, but there is a large region in the middle with many settings indicated in dark green, the darkest spots indicate that all ADCs are working as expected. The analysis script suggests to use IPSource = 90 and IPSource2 = 75 which is done for the last scan and further measurements.

The third scan is a one-dimensional scan over IFBPBias from 55 to 95 in steps of 5. The results of this are shown in Figure 6.10.

The number of good channels is here plotted on the y-axis while the IFBPBias value can be seen on the x-axis. Therefore, the results are given in a histogram where the colour code would not be necessary anymore, but is still indicating the number of good channels which can also be taken from the bin's height. The bins are always to the left of the IFBPBias value, they belong to. The value suggested by the analysis script is given with IFBPBias = 75, where all ADCs work within the thresholds.

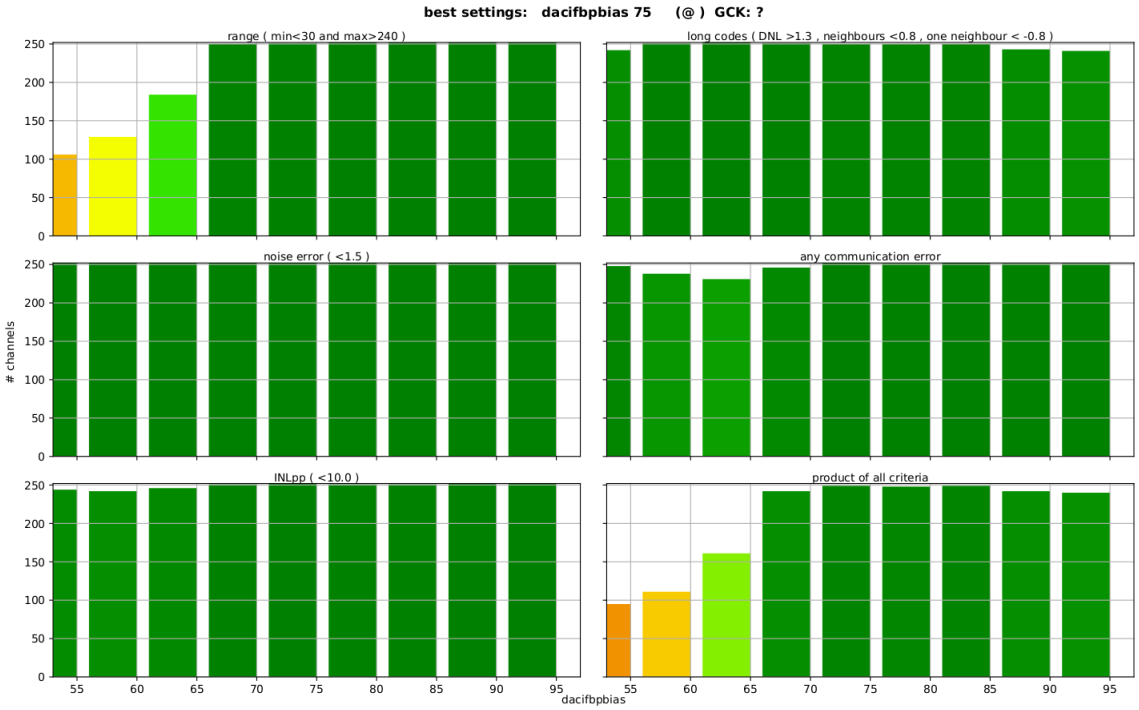


Figure 6.10: Parameter sweep over IFBPBias. For the five possible features the number of good channels is calculated and put into individual plots. The sixth plot shows the product of all criteria and an optimal setting is extracted, suggested and printed as the headline by the analysis script.

6.4 Conclusion

With the Hybrid 5 Setup, ASIC investigations were successfully done at GCK = 76.2 MHz. First, the DHP was examined in more detail, finding suitable parameters for the error-free transmission of the digitised data to the backend electronics at 1.5 GHz. A large parameter space was found for the longest *delay* setting, from which the combination of *bias* and *biasd* can be chosen. The delay cannot be chosen as freely, because the possible settings for the other two parameters decrease rapidly with shorter delays. As the amplitude between high and low signal level is only given in arbitrary units, the more detailed measurements were shortly discussed. The aim with these *eye diagrams* is, to find a large and symmetrical opening between the two signal levels. In such a case, the probability for a stable link over a long time is higher. The second step in the characterisation was the communication between DCD and DHP. To synchronise the sending and sampling of the digitised data, delay elements are used. Scans over the full parameter space were performed as well as the diagonal delay scan developed. The latter only scans over the diagonal of the full parameter space, thus, the time required for a scan can be reduced to about 12 %. Any combination of *global* and *local delay*, summing up to 4 or 5 can be chosen. The last investigations done of the ASICs are the optimisation of the ADC settings. A subset of parameters was identified in previous measurements within the collaboration. Those five parameters were sweeped in two-dimensional and one-dimensional scans and the number of ADCs satisfying the selection criteria was determined for every setting. The parameter combination with the most working ADCs was chosen. It is listed in Table 6.2.

The sweep over AmpLow and RefIn is the only one of the three, in which no setting could be found where all ADCs were working. This might originate in wrong settings for IPSource and IPSource2 during

Parameter	result	# good ADCs
AmpLow	200 mV	243
RefIn	700 mV	243
IPSource	90	252
IPSource2	75	252
IFBPBias	75	252

Table 6.2: Results for the investigated subset of ADC parameters used for all further measurements

the first sweep. It was not further investigated here as with the later sweeps settings were found for which all ADCs fulfilled the criteria.

With those results from the characterisation, the system can be used for matrix investigations, source measurements as well as energy and gain calibrations.

CHAPTER 7

Calibration of DEPFET Matrix

For the calibration of the matrix, first a characterisation is needed to find stable working parameters. The matrix characterisation consists of a pedestal investigation and a working point definition with a radioactive source. Afterwards, an energy calibration of the matrix and a gain calibration of the individual pixels is done.

7.1 Pedestal Scan

As exlained previously in the Chapters 4 and 6 the current of every pixel mainly consists of the drain current from the transistor. Most of it is subtracted by the SubIn setting. The remaining part is the pedestal current and differs from pixel to pixel. It takes up a part of the ADC range. To ensure, that there is a wide enough range for the signal left in the ADC, investigations of the pedestal current are necessary.

7.1.1 Relevant matrix parameters

A set of different parameters determines the functionality and range of the pixels pedestals.

- **HV** is the High Voltage responsible for the depletion of the *n*-doped bulk of the DEPFET pixel from the backside of the matrix. This is done through the process of sidewards depletion (explained in section 3.3). The voltage is applied at a contact on the front side. Therefore, the depletion reaches the backside through the *punch-through* mechanism as explained in section 3.5.
- **Drift** describes a negative potential, which is applied row-wise between the transistors. The drift region is indicated in Figure 4.2. It guides the electrons in the direction of the internal gate. If drift is not negative enough, the charges will not be collected completely or not fast enough before the pixel is read out. The charges would be lost.
- **Gate Off** is the positive voltage of the external transistor gate during the charge collection, while the pixel is not read out.
- **Gate On** is the negative voltage applied to the external gate to switch the pixel starting the readout process.
- **CCG** is short for **C**ommon **C**lear **G**ate. It encloses the transistors and the clear implant and seperates both from each other and from the drift region. It supports the clear process, because the

applied voltage enables a current to flow below the clear gate and cross through the deep p-well surrounding the clear implant. A detailed schematic can be seen in Figure 4.2.

- **Clear Off** is a positive voltage applied at the clear implant during charge collection. It needs to be low enough in order to not attract electrons.
- **Clear On** is a high positive pulse signal, applied to remove the electrons from the internal gate. It is high enough to provide an attractive signal for the electrons even through the p-well shielding the clear implant.

Apart from the above described voltages applied at the matrix' pixels some of the ADC parameters influence the pedestal current as well. The role of SubIn was discussed in Section 6.3. The other parameter influencing the pedestal current is the gain introduced by the ADC channel. Both parameters were not changed during the scans, except for the cases were it is indicated differently.

7.1.2 Measurement

From previous measurements within the collaboration it is known that the most significant changes are found by sweeping hv against drift and ccg against clear off as those parameters depend on each other. Operation values for the other parameters were determined in the collaboration before and used for the scans here without investigating them anew. Those can be found in Appendix A.2.

For the measurements the Hybrid is placed within the aluminium housing as explained in section 5.1.1 to shield the matrix against light radiation. Thus, the pedestal scans investigate the single pixel behaviour as well as the functionality of the complete matrix in its basic state. Sweep scans are performed either for hv against drift or for ccg against clear off. The scans are not linked or performed in a certain order. For all four voltages, standard settings exist. These are −70 V for hv, −5 V for drift, 0 V for ccg and 5 V for clear off. During the sweep scan of the respective other pair, the standard values for two of the four voltages were applied. Therefore, the standard values were checked by the pedestal scans as well as a thorough investigation was performed for restricted parameter spaces. While the sweep scan is running over the given range, the output of every ADC, the ADC value, is measured. For every parameter combination, a 2D-plot as an overview over the matrix is created and a histogram with the number of pixels is plotted against the ADC value. An example for hv at −70 V and drift at −5 V is shown in Figure 7.1.

The distribution of the recorded ADC values, shown to the right of the figure, can be analysed. For this, a gauss curve given by

$$g = y \cdot \exp\left(\frac{-(x-m)^2}{2 \cdot \sigma^2}\right) \tag{7.1}$$

with y the highest value, m the central value and σ the width of the distribution is fitted to the data. In the Figure it can be seen, that with the given settings the pedestal distribution is recorded fully within the range of the ADCs and is located at the lower end of it. This is the favoured behaviour, because here enough space within the ADC range is left to detect a signal while no pedestal signals are below the ADC range.

From the gauss fit different values can be calculated. First, the central value of the distribution as well as, second, the width of the distribution. Those give an idea of where the pedestals are within the ADC range and how wide the distribution is. Furthermore, two limits are introduced. For the upper limit the 99.5th percentile is calculated, meaning that 99.5 % of the data can be found below the limit. The lower limit is at the 0.5th percentile. Both limits applied together leave 99 % of the measured pedestals

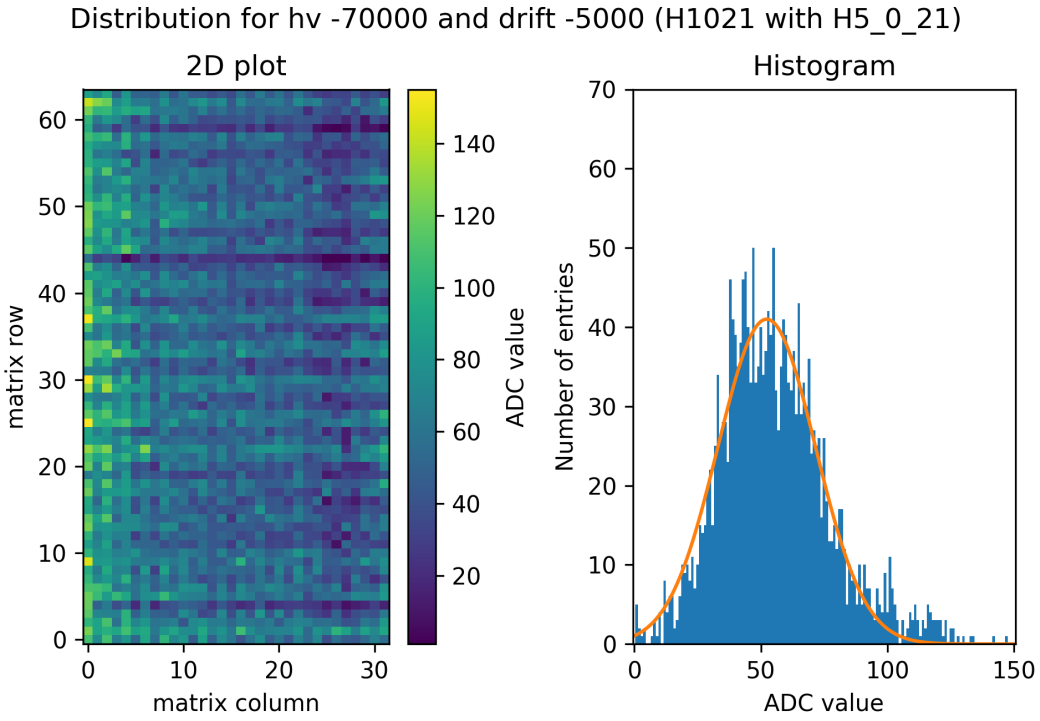


Figure 7.1: The pedestal distribution for hv at −70 V and drift at −5 V. On the left side the matrix rows and columns are shown, the colours indicated by the colourbar on the right side stand for the ADC values. On the left side the distribution in regards to the ADC value is histogrammed.

included in the distribution. This way, especially ADC values with a small number of entries are taken out of the width calculation. Such ADC values can be seen in Figure 7.1 around the ADC value of 150. The last aspect considered is the total amount of bad pixels. This is the number of pixels which are out of range for the current settings. A pixel is considered bad in the analysis, if the number of entries for this pixel is below 5 or above 200.

The central value of the gauss fit, the width of the gauss, the width including 99 % of the pedestals and the number of bad pixels are calculated and shown in overview plots for the sweeped parameter space. The results for sweeps of hv between −80 and −60 V and drift between −7 and −3 V can be seen in Figure 7.2 while the results for ccg from −1 to 1 V and clear off from 2 to 8 V are viewed in Figure 7.3. For both scan types, the overview plots of the analysed pedestals are ordered in the same way. The central values of the gauss fit are shown in the upper plot on the left side, while the widths of the gaussian are plotted next to it. In the second row, the widths including 99 % of the pedestals can be seen on the left, the number of bad pixels for all parameter combinations are to the right.

For the hv-drift scan in Figure 7.2 the central value is found between 30 and 85 ADC values, while the width of the gauss function is located between 17 and 25 ADC values and the width of the distribution including 99 % of the measured pedestals spreads between 85 and 135 ADC values. In all three plots, a corresponding behaviour can be seen for the same parameter combinations. In the lower left hand corner of all three plots the highest values can be found. Thus, a high central ADC value goes along with wide distributions. The higher the pedestal distribution is situated within the ADC range, the less of the ADC range is left for the detection of a signal. Therefore, the parameter settings with the highest central and width values are not considered stable voltages. This triangular region reaches from the lower left hand

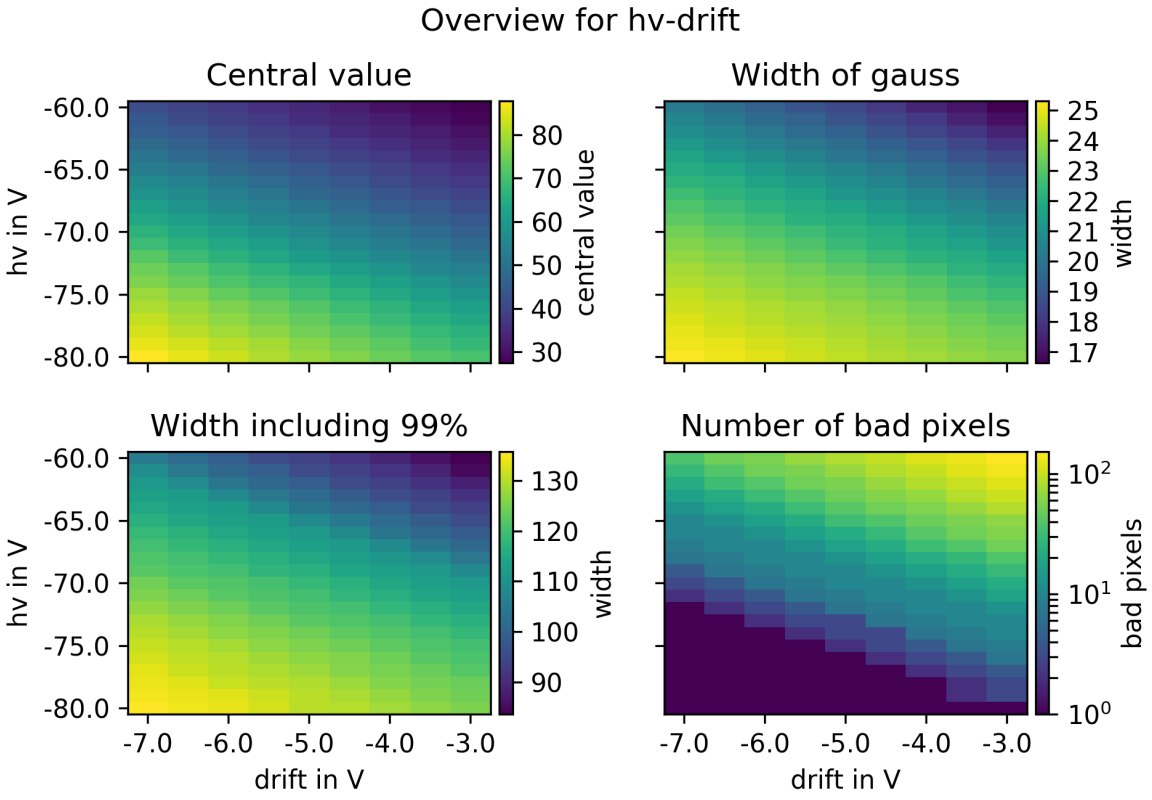


Figure 7.2: Overview for the sweeping scan over hv and drift. SubIn = 40. The detected pedestal values are analysed for the position of the central value of the gauss function, the width of it, the width including 99 % of the pedestals and the number of bad pixels.

corner up to the diagonal connection between the pedestal points of (−7 V, −70 V) and (−6 V, −80 V). In the plot indicating the number of bad pixels, these settings show the lowest amount of bad pixels. The inspection of the plot raises limits rather on the opposite side of the parameter space. With higher, more positive values of both parameters the number of bad pixels increases. The parameter settings within the triangular area, including the combinations of the more positive of the investigated hv values with more positiv drift values, with 20 to 105 bad pixels cannot be used for the measurements. It seems that the range defining a good pixel is chosen to small at least for the lower limit. That is indicated by the compliance of the highest central values with the smallest number of bad pixels. In the other settings, there are probably too many pixels at the lower end of the distribution which send a current with less than 5 ADC values. The following results can be drawn from the overview plots for the hv vs. drift scan: The diagonal band between the two triangular regions discussed before consists of reasonable voltage combinations. The proposed standard settings of hv at −70 V and drift at −5 V are verified with the setup. These are further investigated in the source measurements in Section 7.2.2.

For the ccg-clearoff scan the situation looks similar, but the pedestal distributions in general are smaller and they are located lower within the ADC range. The central values can be found between 15 and 45 ADC values, while the width of the gauss varies from 8 to 19 and the width including 99 % of the pedestal distribution is found between 40 and 100 ADC values. The highest values are again found for the more negative voltage combinations in the lower left hand corners of all three overview plots. The triangular region can be found between the settings (2 V, −1 V), (2 V, 0 V) and (5 V, −1 V). This region

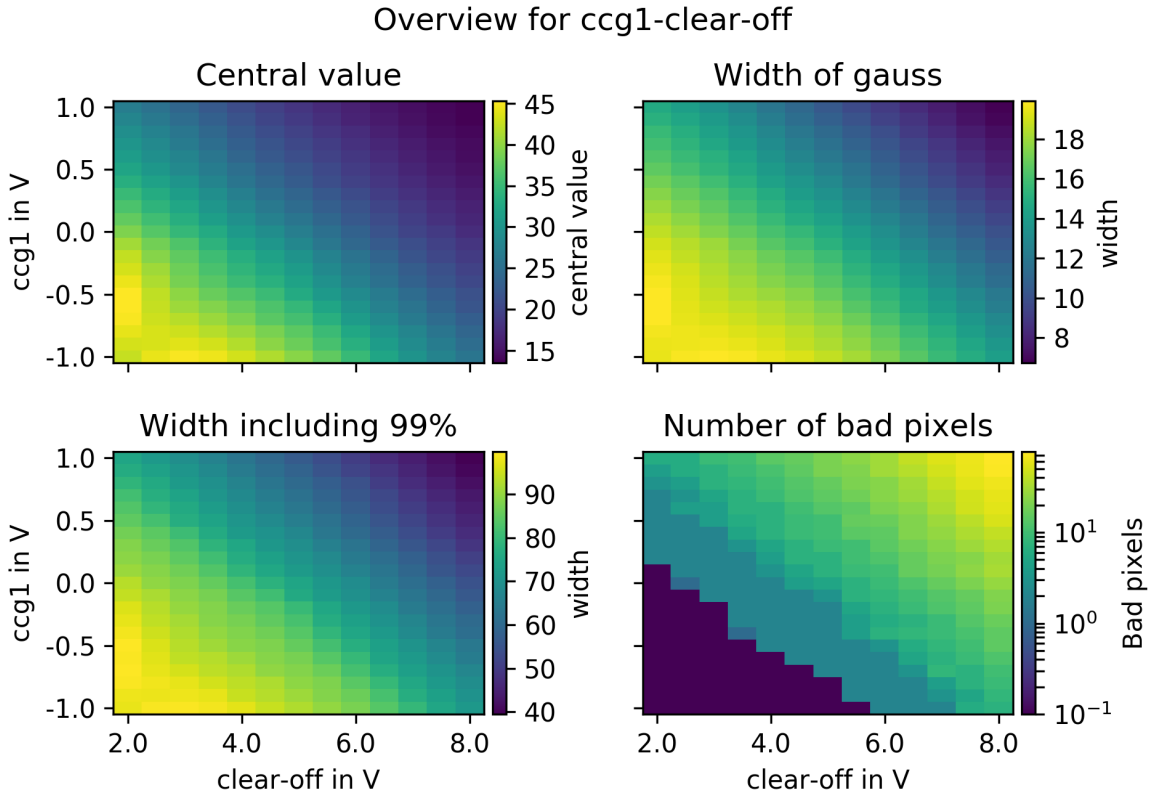


Figure 7.3: Overview for the sweeping scan over ccg and clear off. SubIn = 40. The detected pedestal values are analysed for the position of the central value of the gauss function, the width of it, the width including 99 % of the pedestals and the number of bad pixels.

corresponds again with the lowest numbers of bad pixel which are below 1 pixel. Only a small region in the upper right hand corner is neglected due to the number of bad pixels being above 20. A wide band of parameter settings is left as supposedly well working voltage combinations. The standard values of 0 V for ccg and 5 V for clear off are close to the middle of it.

As mentioned before, the SubIn regulates what part of the drain current is left after subtracting the main part. Therefore, the pedestal distribution is influenced by the choice of the SubIn value. To validate this presumtion, Figure 7.4 shows the analysis for ccg and clear off with a SubIn value of 39 instead of 40 (as used for the Figures 7.2 and 7.3). The colour distribution of the plots, except for the bad pixels, is very similar, but as the scale on the colour bar indicates, the complete pedestal distribution is shifted to higher values. This is expected, as a smaller SubIn value means less current is subtracted. Especially on the number of pixels considered bad the changed SubIn value has a huge impact. The range of settings producing less than 1 bad pixel is more than doubled. Thus, with the higher SubIn value more ADCs get input at the lower end of their range. Partly, this is intended as it leaves more space within the ADC range for an incoming signal, but the analysis of the bad pixels indicates that the SubIn value has to be handled more carefully and determined before every one of the succeeding source measurements.

In general, it is positive, that the pedestal sweeps over the whole of the tested parameter spaces were done at one SubIn value and with one ADC channel gain. The gain of the channel is created by the relation of two resistors used to convert the current into a voltage and then back into a current. As SubIn and gain are stable over the sweep, it is not necessary to determine them anew for every setting,

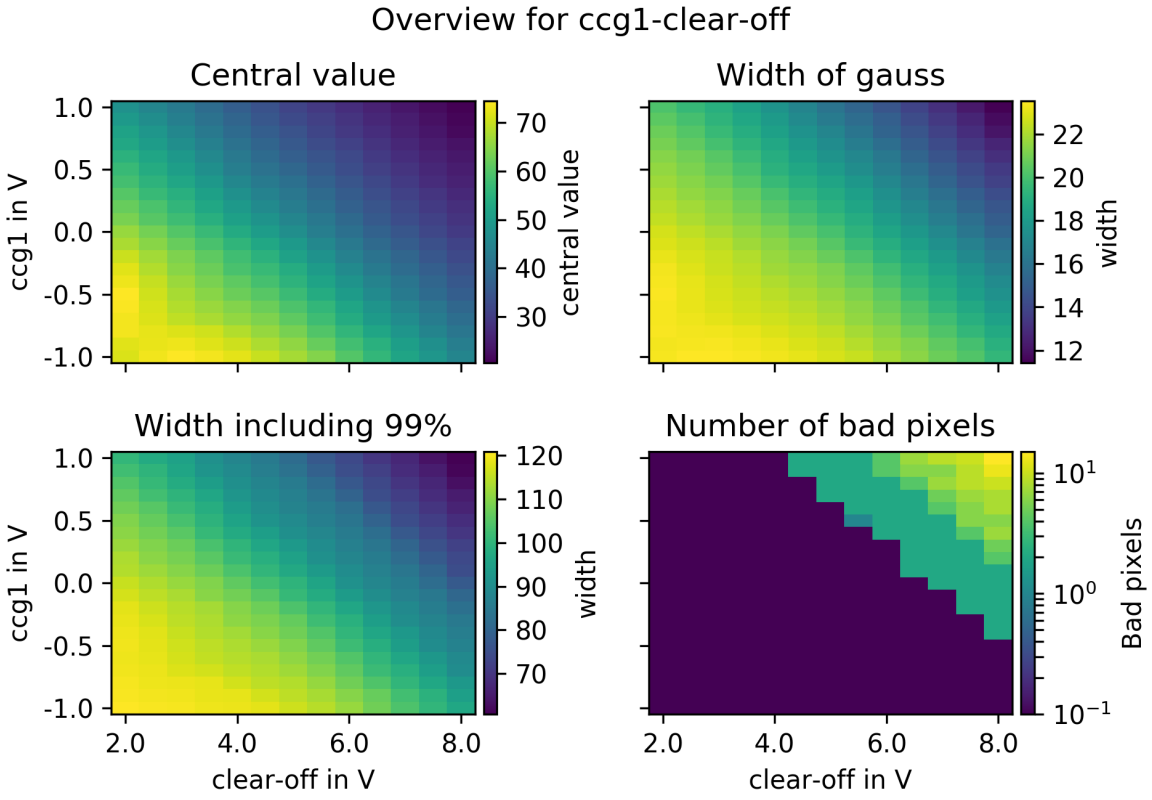


Figure 7.4: Overview for the sweeping scan over ccg and clear off. SubIn = 39. The detected pedestal values are analysed for the position of the mean, the standard deviatian and width of the distribution as well as for the positions of the 99.5 %- and the 0.5 %-limit and the total amount of noisy instances during the measurement.

even within these wide scan ranges. This reduces the amount of parameters that have to be identified before a measurement. With the pedestal investigations alone, no definitive conclusions about stable conditions can be drawn. Only possible ranges were established. To get more indicators for the right matrix operation voltages, investigations with a source are done.

7.2 Source Scan

The aluminium housing containing the Hybrid is put into a lead box as explained in Section 5.1.1. First, a ^{90}Sr source is used to find optimal voltage settings for the matrix. The measurement is expected to confirm the ranges found in the pedestal scans or even reduce them. With the verified voltage choices, an energy calibration of the pixel matrix can be done. Eight different γ sources are measured and known peak positions in the energy spectrum are used for an energy calibration of the matrix. Some sources are measured with sufficiently high statistics to conduct a single pixel analysis of the distributions. With the analysis results of all pixels, gain maps for the complete matrix are created and reapplied on the measured data. As a result, the width of the peaks are expected to become smaller and the energy resolution of the detector increases. In detail, the steps and results for those processes are documented in the following.

7.2.1 Measurement process

All source scans are carried out in a similar fashion. The first step is the determination of a suitable SubIn value by sweeping through a given SubIn range. The values are tested after each other with 10 raw data frames taken (one frame is one complete readout of the matrix) and analysed until the central value of the distribution is found to be above 40 ADC values. The distribution in these pre-measurements contain pedestal current and signal. For the voltage sweeps with the strontium source, the SubIn value is determined before every measurement with a new parameter combination. In the pedestal scans a lower and upper limit of 5 and 200 were given to determine the ADC range for good pixels. The lower limit is included into the measurement routine of the source scans as a threshold and can be chosen. Only data above the threshold is saved. This is done to reduce the amount of recorded noise. During the data taking the data is saved as raw data. A charged particle passing through the sensitive matrix area often deposits energy in different pixels. Therefore, clustering the data is the first step of the analysis. Neighbouring pixels with hits at the same time are called a cluster. Within the clustering, noisy pixels are determined and masked to reduce noise on the dataset. Sometimes, pixels are always noisy and therefore completely masked out, but there are more cases with pixels being pertly noisy. Those pixels are masked out for the frame in which they were found noisy as well as the one before and the one afterwards. The further analysis of the data includes a hitmap showing the distribution of hits over the matrix, the number of entries for every ADC value and the number of entries for different cluster sizes. For those sources with high statistics taken, the single pixel distributions are fitted with gauss peaks. Investigations are done, comparing the different distributions of seed signals, data of all clusters including the multipixel clusters and data only from single pixel clusters. Gain factors are calculated for every pixel by dividing the expected peak energy in keV by the measured peak in ADC values. In the following only the main analysis results are shown and discussed.

7.2.2 Matrix voltage investigation

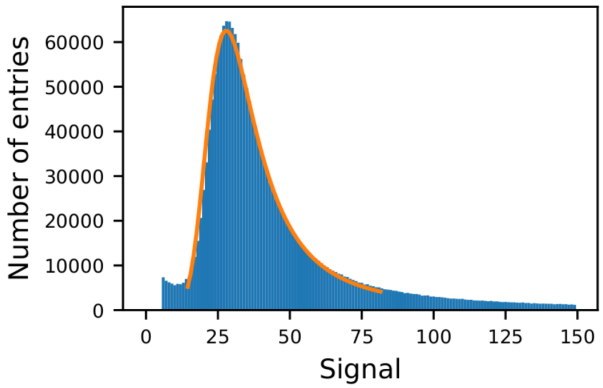


Figure 7.5: Langau distribution of the strontium isotope ^{90}Sr measured with the DEPFET pixel matrix in ADC values. The MPV gives the most probable value of the distribution while sigma indicates the width at half maximum.

The strontium isotope ^{90}Sr is radioactive and decays via β^- radiation. It is used to investigate the uniformity of the matrix's response to radiation. As the amount of emitted energy is continous in the case of β radiation, the expected spectrum is a landau distribution given by

$$p(x) = \frac{1}{\pi} \int_0^\infty \exp\left(-t \ln t - xt\right) \sin\left(\pi t\right) \mathrm{d}t.$$

which is given with simplified assumptions of charged particles passing through matter. Within the analysis of energy distributions, the landau distribution is shifted and scaled to fit the measured data. [20] At the same time, irregularities and noise in the pixels and the readout electronics introduce a gaussian component. The function expected to be best fitting to the data set is a landau folded with a gaussian function. This reproduces the effects of the detector on top of the emitted energy spectrum. The measured distribution can be seen in Figure 7.5 where such a so-called langau distribution is fitted to the data. The two parameters investigated in the following are the **M**ost **P**robable **V**alue (MPV) and the width of the gauss component. The MPV gives the peak value and is in a landau distribution different from the mean value as the long tail shifts the latter towards the right within the distribution. The width of the gaussian part is called sigma in Equation 7.1. Both values can be used to analyse the used parameter settings.

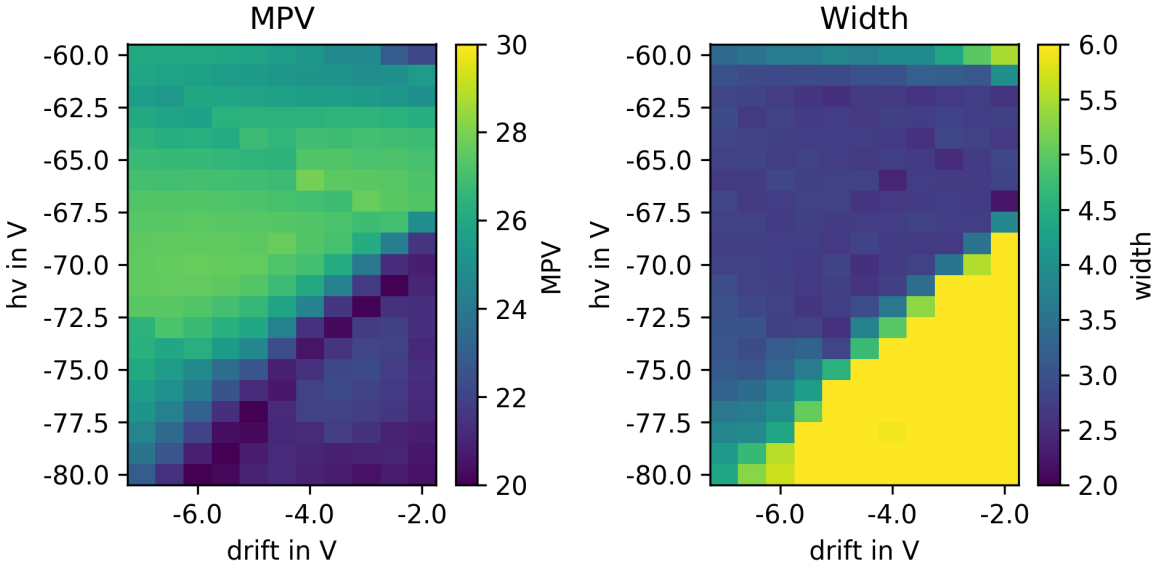


Figure 7.6: Results for MPV and width of the gauss function of a sweep over hv and drift. On the left, the results for MPV are shown, while on the right the results for the width can be seen.

For a hv-drift sweep scans the analysis for MPV and the width can be seen in Figure 7.6. The scan is done over the same voltage ranges as for the pedestal investigation. On the left the MPV is indicated by the colour scale. On the right the width is given in the same way. In the right hand bottom corner of both plots, there is a distiguishable triangular area. The MPV for those settings is lower than for the others while the width is larger, which means that the distribution is wider as well as the MPV is shifted to smaller ADC values. For the most positive hv voltages measured, a similar behaviour can be observed. This can be explained by the functions, which the hv and drift voltages have in the pixels. As exlained in the beginning of this chapter, hv is the voltage to steer the depletion and the position of the potential minimum in the matrix. If it becomes too positive, the pixels will not be fully depleted. Meanwhile, drift is the potential directing the electrons towards the internal gate. If the drift potential becomes too positive, it does not reject the electrons anymore. This has two effects on the distribution. First, the electrons do not move to the internal gate fast enough to be read out. The charges are lost for the signal

detection and the detected signal is located at a lower ADC value. Second, the amount of charge drifting too slow or not at all towards the internal gate differs. This results in a wider range of ADC values read out of the pixels and therefore the distribution becomes wider. The hv voltage is out of range for the most positive value measured within the scan. In this case the pixels are most probably not fully depleted and the position of the potential minimum is not at the position of the internal gate. Therefore, the produced charges are not directed to the internal gate by the field within the pixel.

The results from the ^{90}Sr source scan over hv and drift are the following: The settings within the triangular region in the bottom corner and the most positive values for hv measured, cannot be used. Apart from that, any value above the triangular region, at hv voltages between −72 to −63 V, in the middle of the plots seems to be usable. Taking into consideration the results from the pedestal scans, a parameter space in the middle of the total scan values is left. It is located roughly between the data points (−7 V, −70 V), (−4 V, −64 V) and (−3 V, −67 V). The standard parameters are still within the range and can be used for measurements and further investigations.

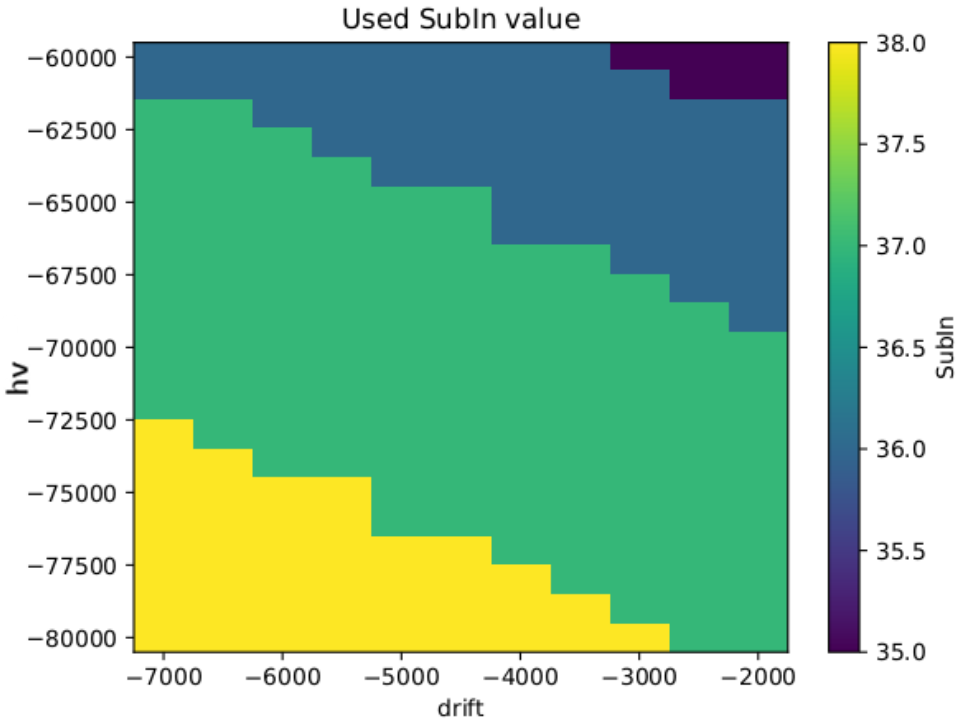


Figure 7.7: For different settings various SubIn values have to be used and thus are determined before every measurement. The ones used for the measured hv and drift combinations are shown here.

Apart from the excludable voltage settings, a second curiosity can be observed especially in the measurements for MPV. There are diagonal lines running in the opposite direction to the triangular structure in the lower corner. The same distribution is found when investigating the SubIn values used for the settings. This is shown in Figure 7.7. When it is compared to Figure 7.6 it is clearly comprehensible that the diagonal lines are at the same positions as the changes of the SubIn value. A possible explanation is, that the output of the ADCs in the DCD depends slightly on the SubIn value.

For ccg and clear off, a similar measurement was done and the results can be seen in Figure 7.8. The measured range for clear off is smaller here than in the pedestal scan. To both sides of the range two values less are measured than previously. The excludable parameter space is not as large as in the hv-drift sweeps, but at least for the clear off voltage a highest limit was found. At a clear off voltage of 6.5 V the

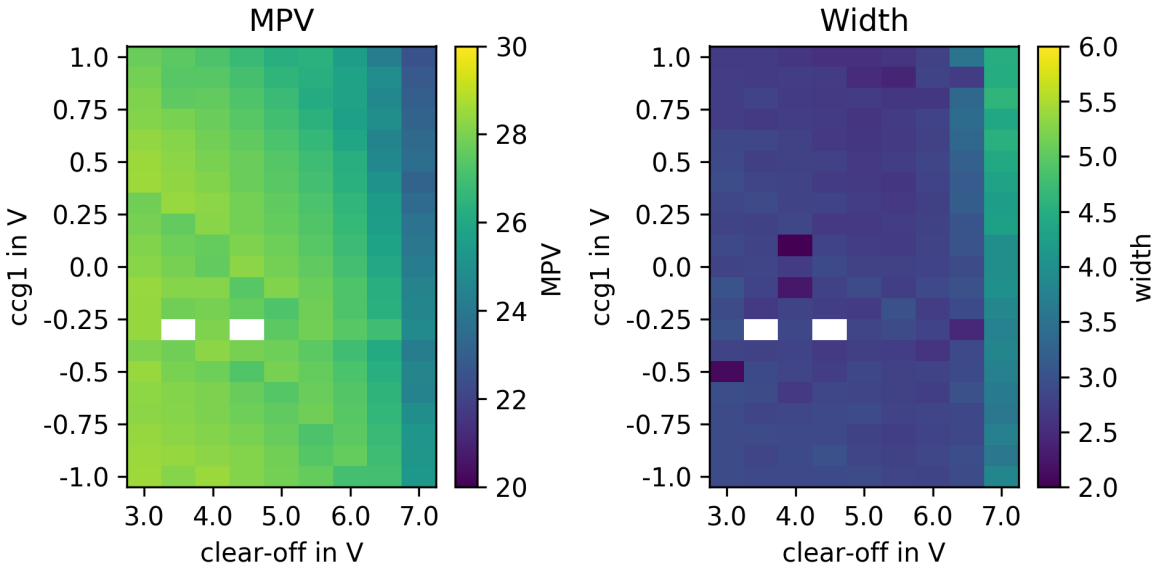


Figure 7.8: Results for MPV and width of the gauss function of a sweep over ccg and clear off. On the left, the results for MPV are shown, while on the right the results for the width can be seen.

MPV decreases to smaller ADC values, while the width increases. The functions of the two voltages as explained in the beginning of this chapter are the following. The ccg potential is applied at a gate structure to direct the electrons to the clear gate during the clear process by weakening the *p*-well around the clear. The clear off voltage is applied at the clear implant during the charge collection. If it becomes too positive, while the ccg potential influences the *p*-well too much, electrons will move to the clear implant before they are collected in the internal gate. They are lost for the detected signal. In contrast, if clear off becomes too negative, it can come to back injection of electrons into the internal gate, because the clear voltage is not attractive enough in relation to the internal gate. This behaviour was not observed in the scan range taken. Especially for ccg it is important, that the matrix response does not change over a wider change of settings. As the voltage is applied at a gate structure, it is more sensitive to radiation damages. A wide range of possible settings for ccg means that smaller damages through radiation will not change the matrix response. The two white dots indicate that something went wrong during the measurement of the data. There is too much data recorded for those settings, that the analysis could not be carried out as for the other datasets.

Combined with the results from the pedestal scans, all settings above the line between (2 V, 0 V) and (5 V, −1 V) as well as below clear off voltages of 6.5 V can be used for measurements. The standard voltages are located well within the range and are therefore verified by the scans.

7.2.3 Energy Calibration

An energy calibration of the DEPFET matrix is necessary to confirm that the pixels respond linearly within a wider range of energies and that there is no large, inexplicable offset. If irregularities and different behaviour in various energy ranges would be found, the output of the matrix cannot be attributed to a fixed energy anymore. For the energy calibration, eight γ radioactive sources with their prominent peaks between 6 and 60 keV are used. These are iron, americium, copper, rubidium, molybdenum, silver,

barium and terbium. The first two are directly decaying sources. ^{55}Fe is decaying with γ-radiation. The K-L_3 and the K-M_3 transitions are close together and are measured at one energy. The transitions result from electrons in the shells further out dropping to the innermost "K" shell. The transitions to the innermost shell are normally the ones with the smallest amount of energy in the radioactive spectrum of the respective element. The K-M_3 peak's amplitude reaches about 15 % of the K-L_3 transition. Conversions to the Siegbahn notation can be found in [35]. ^{241}Am decays via the α decay with a smaller γ ray component. Only the γ-radiation is used for the calibration. For the other six sources a *variable energy X-ray source* from *Amersham International* is used. There is ^{241}Am used as a primary source, sitting at the top of the *X-ray source* case. The radiation is directed through a window onto another source. The other materials are installed on a turnable lower level within the case. Therefore, the chosen material can be brought beneath the window. The material is excited by the americium decay and decays via fluorescence with its individual K-L_3 and K-M_3 transition energies. The literature values [36–38] for the used elements are listed in Table 7.1.

Source	transition	energy/keV	combined peak/keV	measured peak/ADC values
^{55}Fe	K-L_3	5.9		8.84 ± 0.10
Cu	K-L_3	8.04	8.17	11.77 ± 0.08
	K-M_3	8.91		
Rb	K-L_3	13.37	13.61	19.80 ± 0.10
	K-M_3	14.97		
Mo	K-L_3	17.44	17.77	25.83 ± 0.14
	K-M_3	19.63		
Ag	K-L_3	22.10	22.53	32.44 ± 0.15
	K-M_3	24.99		
Ba	K-L_3	32.06		46.58 ± 0.14
	K-M_3	36.55		
Tb	K-L_3	44.23		64.95 ± 0.15
	K-M_3	50.65		
^{241}Am	γ byproduct	59.5		85.07 ± 0.07

Table 7.1: Radioactive γ transitions of the eight used sources. For copper, rubidium, molybdenum, silver, barium and terbium the used isotopes are not given, because the americium decay excites the material which decays via fluorescent radiation. The used isotope is probably the naturally most occurring one.

Measurements with the listed elements are carried out over different time intervals, depending on the activity of the source and the purpose of the dataset. Those elements used for the gain calibration later on were measured for longer times, to collect enough data in every single pixel. The energy distributions of the measured sources are documented in Figure 7.9. In the figures, the ADC values are called ADU which stands for **A**rbitrary **D**igital **V**alues. There is no difference between the two names. Gauss functions as given by Equation 7.1 are fitted to the prominent peaks.

For the energy calibration, the central values in ADU of all elements are taken from the gauss fits and plotted against the literature values of the transition energies in keV. A linear fit is applied to the values. The resulting plot can be seen on the left in Figure 7.10. On the right the respective residuals of the fit are plotted.

The result from the fit is, that 1.44 ± 0.01 ADC values correspond to 1 keV. With this result, the amplification g_q can be calculated. The amplification is given by $\frac{\mathrm{d}I}{\mathrm{d}q}$ as explained in Section 3.5. Therefore, next to the slope, the drain current and the number of created electron-hole pairs is needed. The latter

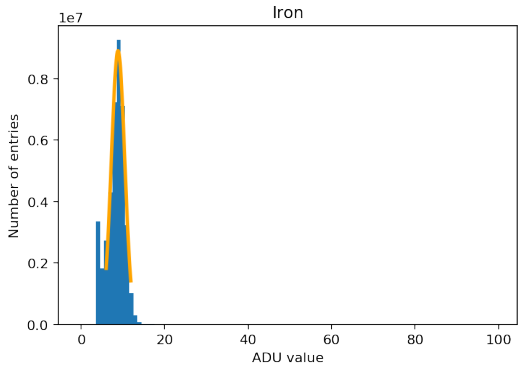
can be calculated with the following consideration: The production of one electron-hole pair at room temperature in silicon requires (3.67 ± 0.02) eV [39]. Therefore 272 electron-hole pairs can be produced by a particle depositing the energy of 1 keV within the pixel. The drain current in nA per ADC value is known from the ADC scans shown in section 6.3. It is called I_{ADC} for further use and given by $I_{\mathrm{ADC}} = (116.18 \pm 0.47)\,\mathrm{nA\,ADU^{-1}}$.

The amplification is with those values calculated to

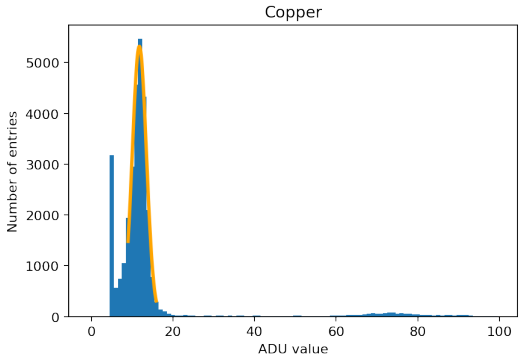
$$\begin{aligned}\frac{\mathrm{d}I}{\mathrm{d}q} = g_q &= 1.44\,\frac{\mathrm{ADU}}{\mathrm{keV}} \cdot 110.92\,\frac{\mathrm{nA}}{\mathrm{ADU}} \cdot \left(272\,\frac{e}{\mathrm{keV}}\right)^{-1} \\ &= (613.45 \pm 8.99)\,\frac{\mathrm{pA}}{e}. \end{aligned} \tag{7.2}$$

The expected range given in section 3.5 is between 400 and 600 pA per electron. Therefore, the calculated value exceeds the expected range. The uncertainty of 1.5 % comes from the fit uncertainties, the varying current output of the ADCs and the variation on the number of produced electron-hole pairs by a certain amount of energy.

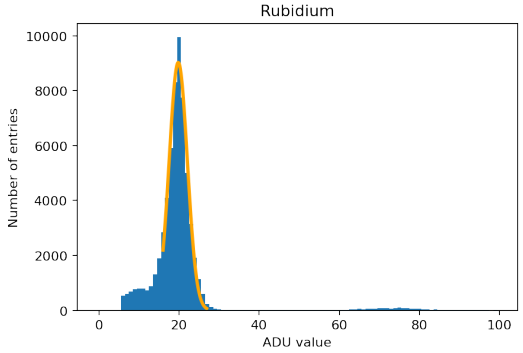
This is an higher amplification than previous measurements with the last generation of DEPFET pixels. Those were for example carried out by Florian Lütticke [40] or Benjamin Schwenker [41]. In the first case, pixels with a gate length of 6 µm were used and an amplification of (453 ± 5) pA per electron were measured. In the other one, two matrices consisting of pixels with the same gate length as the ones used here, 5 µm, were investigated. The results were (510 ± 25) pA and (570 ± 25) pA per electron. The higher amplification is mainly explainable with the thicker sensor. The earlier generations had pixel matrices with 50 µm silicon material, while the final generation is 50 % thicker. As a result, higher signals are expected.



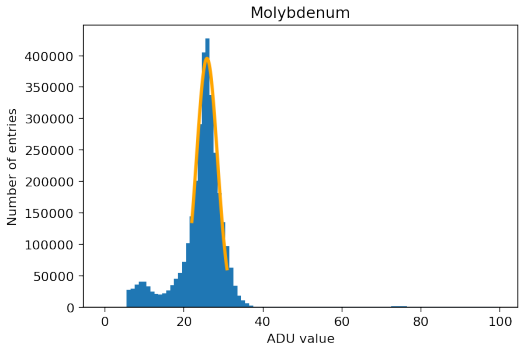
(a) The distribution for iron is fitted with a gauss, peaking at 8.84 ± 0.10 ADC values



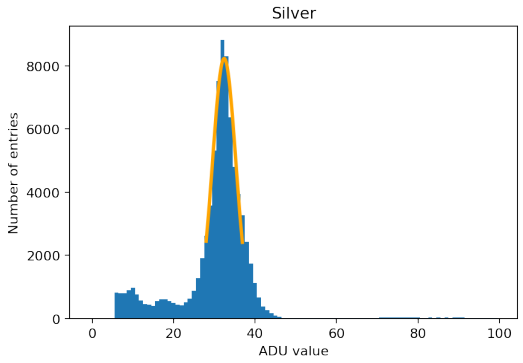
(b) The distribution for copper is fitted with a gauss, peaking at 11.77 ± 0.08 ADC values



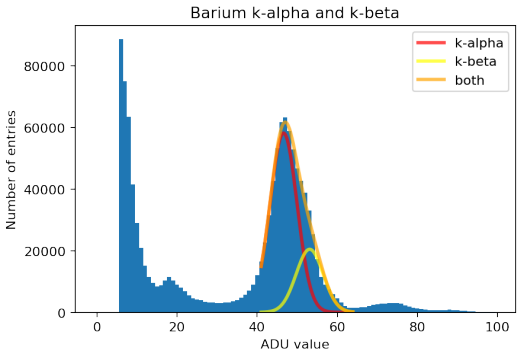
(c) The distribution for rubidium is fitted with a gauss, peaking at 19.80 ± 0.10 ADC values



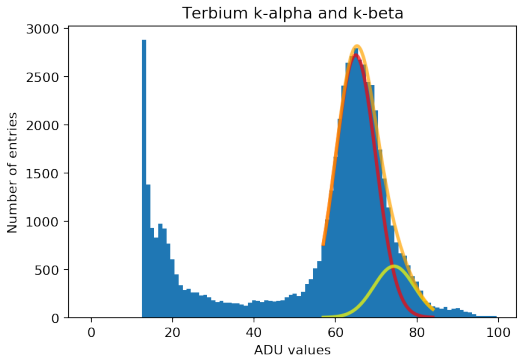
(d) The distribution for molybdenum is fitted with a gauss, peaking at 25.83 ± 0.14 ADC values



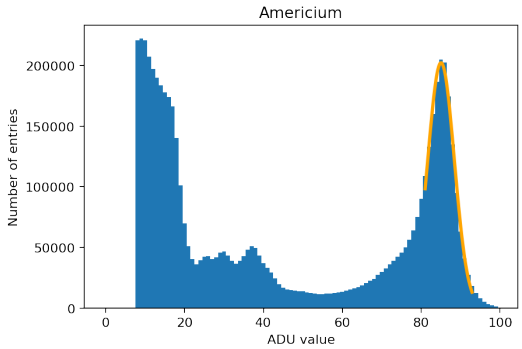
(e) The distribution for silver is fitted with a gauss, peaking at 32.44 ± 0.15 ADC values



(f) The distribution for barium is fitted with a gauss over both transition lines, peaking at 46.58 ± 0.14 ADC values. For the energy calibration the value for the K-L_3 transition is used.



(g) The distribution for terbium is fitted with a gauss over both transition lines, peaking at 64.95 ± 0.15 ADC values. For the energy calibration the value for the K-L_3 transition is used.



(h) The distribution for americium is fitted with a gauss, peaking at 85.07 ± 0.07 ADC values

Figure 7.9: Results of the source scans

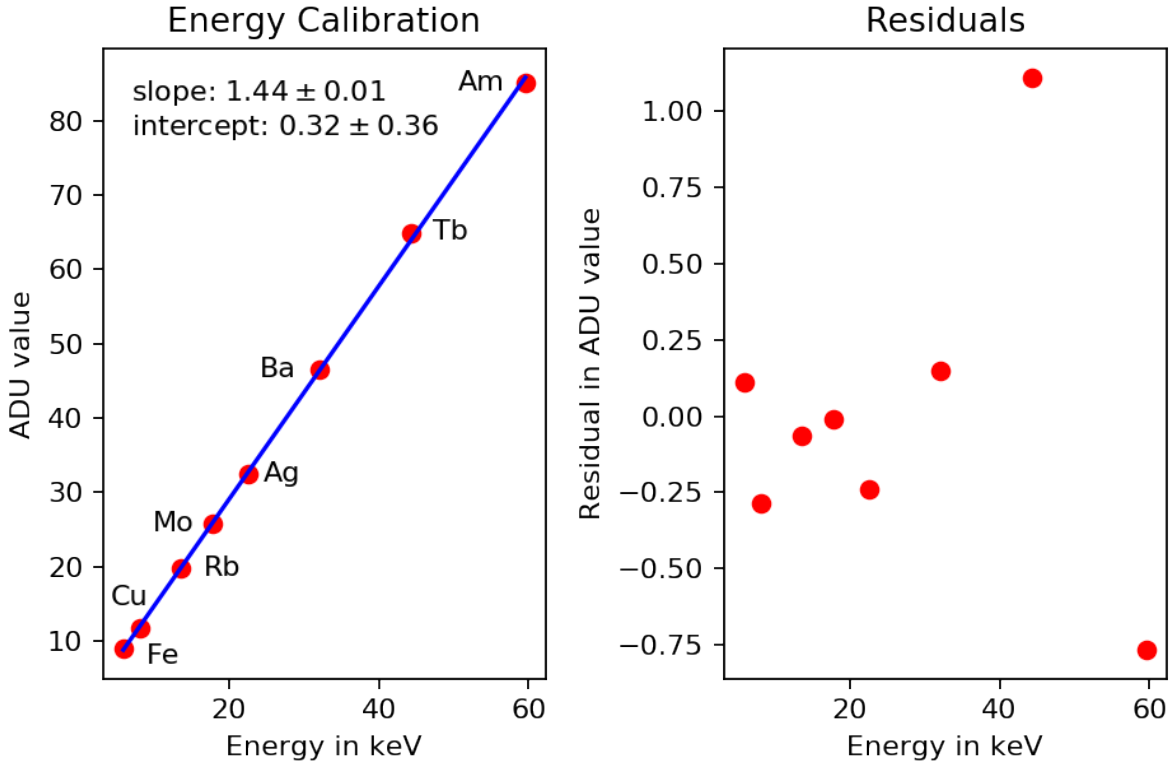


Figure 7.10: Energy calibration with the mean values of the eight measured γ-sources.

7.2.4 Gain

As mentioned before, a gain calibration is performed. This is done to find differences in the gain behaviour of the 2 048 single pixels as well as to reduce them. Therefore, an equalisation of the matrix response to a certain extent can be achieved. Different gain values do not influence the width of the peaks anymore and the energy resolution is increased. The measurements are done in the same way as for the energy calibration and were carried out along with them. Especially sources with high activity were chosen to be measured with higher statistics and then used for the energy as well as the gain calibrations. The sources used for the gain maps were americium, terbium, silver and molybdenum. To the distributions of every pixel, gauss fits are applied like it was done for the distributions of the complete matrix. The central values of the gauss fits are recorded. An example of those single pixel distributions of molybdenum can be seen in Figure 7.11.

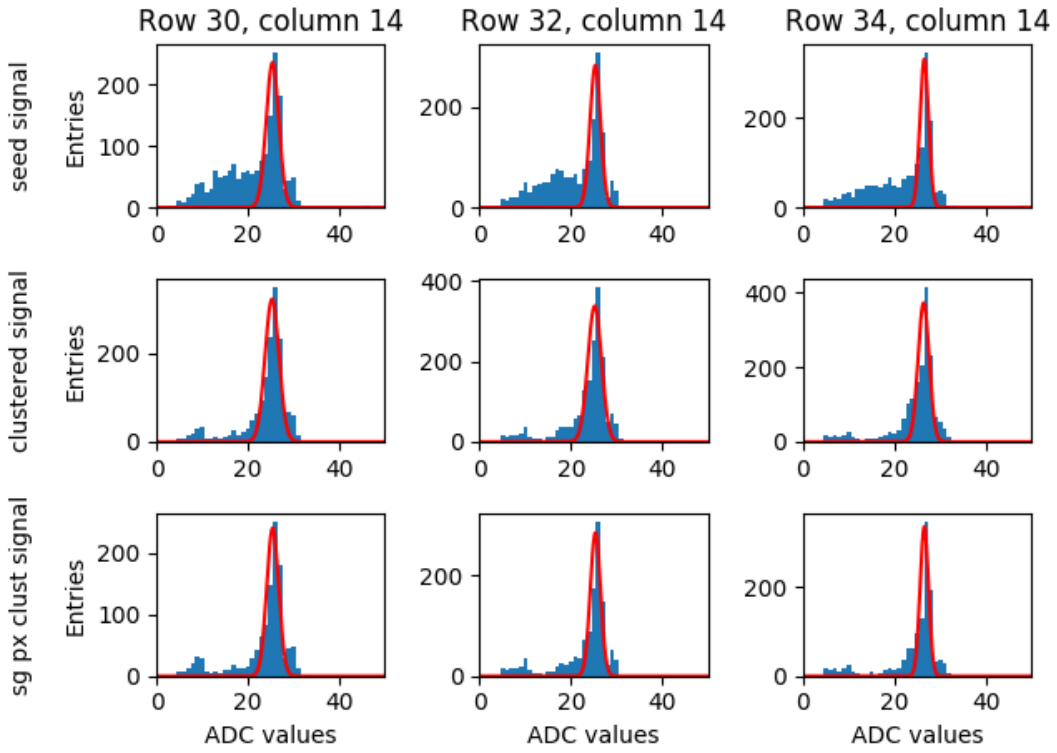
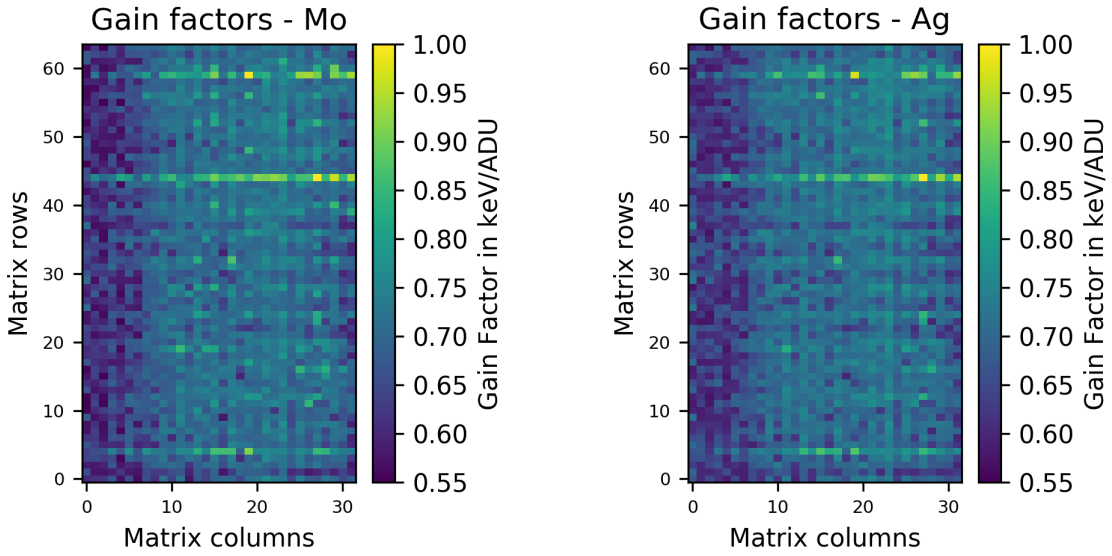


Figure 7.11: For molybdenum the three different readout versions are shown for three different pixels. In the first row the seed signal data is shown. This can be seen by the larger entries left of the peak. In the second row clustered data without other cuts are plotted. Therefore, multi pixel and single pixel clusters are added together. In the third row only the single pixel clusters are shown. The difference between the second and the third row can be seen, when the amplitude of the peaks is considered. There are less recorded hits when only single pixel clusters are considered.

The distributions shown in the figure are representing three different cases for the same three pixels. The first row shows the seed signals, which are the largest fraction of a recorded cluster. This includes all instances where only this pixel was hit, but also multi-pixel clusters where the largest signal fraction was detected in this one. In the second row, multi pixel clusters including single pixel clusters are shown. For

clustered data, all signals recorded by the pixels within a cluster are added together and attributed to the pixel with the seed signal. In the third row only the single pixel clusters of these pixels are used. The differences of the three can be seen in the plots. In the plots of the seed signals, there are entries left of the distinguishable peak which are the seed signals of multi pixel clusters. Those cannot be observed in the second and third row. The difference between those is the amplitude and the width of the peaks. The datasets for the single pixel clusters are smaller, but the width of the peaks is decreased as well. As the gain maps should reduce differences between the pixels, interference effects are minimised. Therefore, only the data from the single pixel clusters is used for the gain maps.

The literature peak value is divided for all pixels by the fitted one to get the gain factor. Those factors are plotted for all four investigated elements. In Figure 7.12 the gain distributions of molybdenum and silver can be seen, while Figure 7.13 shows them of terbium and americium. All pixels of the matrix are shown. The colour code indicates the gain factor.

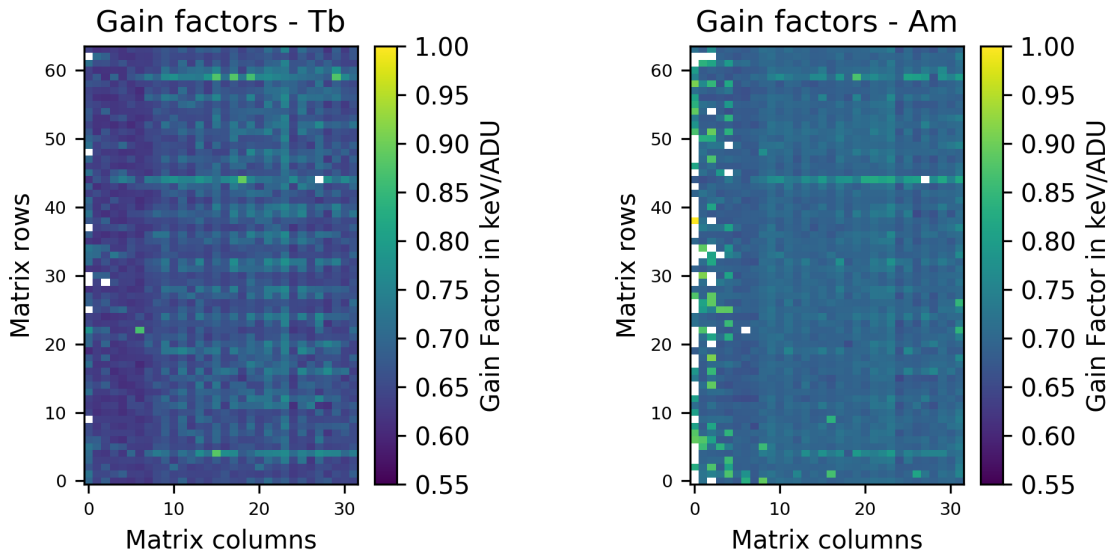


(a) Gain map of molybdenum.

(b) Gain map of silver

Figure 7.12

The K-L_3 transition energies for molybdenum and silver are at 17.44 keV and 22.10 keV. The K-L_3 transition line of terbium is located at 44.23 keV, the main peak of americium at 59.5 keV. That the transition energies of molybdenum and silver as well as of terbium and americium are close together, can also be seen in the gain map plots. They look very similar regarding the one in the same energy range, but different from the other two. While the most gain factors for molybdenum and silver are above 0.75, for terbium and americium many gain factors are between 0.6 and 0.8. Therefore, the range of gain factors seems to be different depending on the energy of the transition. A second observation made in the plots of the gain factors for terbium and americium is, that not for all single pixel distributions a gain factor was calculated. This comes from the fact, that a gauss function could not be fitted to the distribution of those pixels. To reduce fit errors and fluctuations by acknowledging the different gain behaviour of molybdenum and silver in regard to terbium and americium, two gain maps are created out of the four. One with the values from molybdenum and silver, the other one for terbium and americium. Both sets are reapplied on the recorded data and compared with the distribution without gain calibration.



(a) Gain map of terbium.

(b) Gain map of americium

Figure 7.13

For terbium and silver the three differently analysed distributions are shown in Figures 7.14 and 7.15. First, the uncorrected distribution, in the middle the one with the gain map from terbium and americium applied, while on the right the one with the gain map created from molybdenum and silver is shown. For the uncorrected distribution the energy calibration is used. Therefore, the x-axis is calibrated and shown in keV. In all three plots the central value m of the peak is given with the error resulting from the fit as well as the width s.

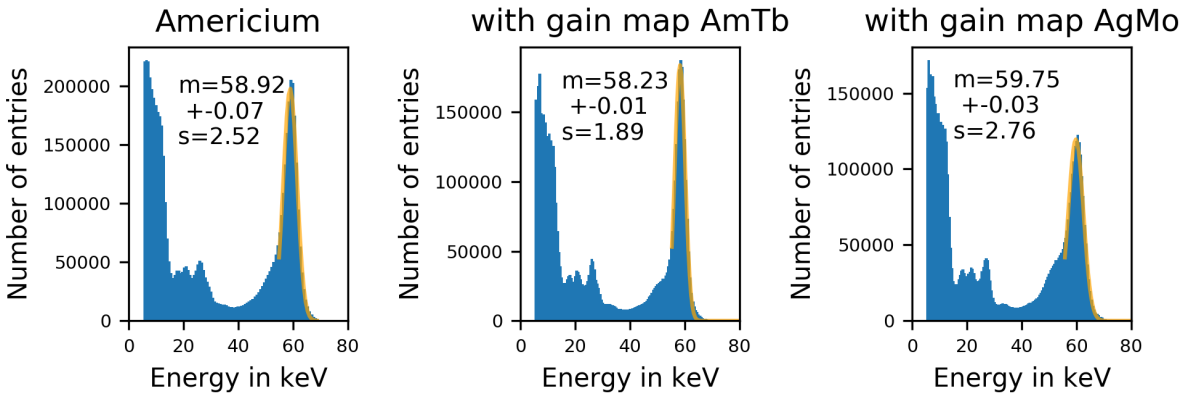


Figure 7.14: The uncorrected distribution of terbium is on the left side, in the middle is the same distribution corrected with the gain map from terbium and americium, while to the right the corrections with the gain map produced from silver and molybdenum is shown. Both corrections increase the energy resolution.

For terbium, both corrections by the applied gain maps show that the peak for the K-M_3 transition is

clearly distinguishable from the main peak of the K-L_3 transition. This is not the case in the first plot, without the gain calibration. Small differences can be seen between the distributions corrected by the gain factors from americium and terbium in contrast to those from molybdenum and silver. The peak, where the gain map including the material itself is applied, has a smaller width. Therefore, this gain calibration is a bit more accurate than with the two elements at the lower energy range. This is as expected from the difference in the gain factors seen before.

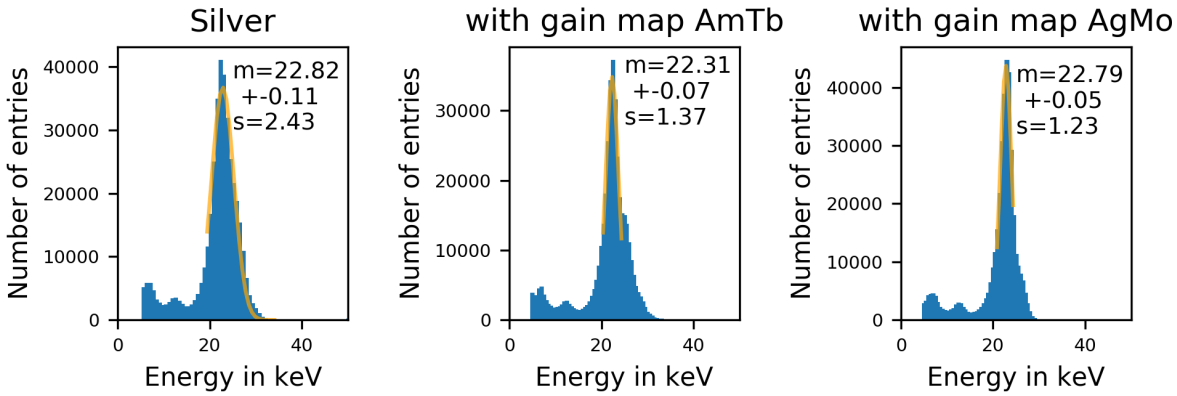


Figure 7.15: The uncorrected distribution of silver is on the left side, in the middle is the same distribution corrected with the gain map from terbium and americium, while to the right the corrections with the gain map produced from silver and molybdenum is shown. Both corrections increase the energy resolution.

Figure 7.15 shows the corrections in comparison to the non-corrected distribution for silver. Here, the same aspects can be seen as before for terbium. Both corrections show a definite improvement over the non-corrected case. The smaller K-M_3 transition peak cannot be seen as clear as for terbium. However, a difference of the entries in contrast to the shape of the gauss fit on the right side of the K-L_3 peak can be observed in both corrected distributions. The width of the gauss fit is again smaller in the case where the gain factors from the same element were used. The corrected distributions for the other elements can be found in appendix A.3.

The americium spectrum is analysed in more detail in Figure 7.16. To correct the distribution as best as possible with the measurements performed, the gain map from americium and terbium is used. In Figure A.5, the central value of the gauss fit to the most prominent γ peak of the spectrum at 59.5 keV is found at (58.23 ± 0.01) keV. Its difference to the actual value is 1.27 keV. This is a worse result than from the fit to the uncorrected distribution. Therefore something must have gone wrong in the analysis and correction with the gain map from americium and terbium. However, some of the peaks at the lower end of the spectrum can be seperated better than in the uncorrected dataset. Next to the prominent line at 59.5 keV, the γ radiation peak of americium at 26.3 keV can be seen. With a linear error on the peak position due to the mistake in the gain map assumed, the peak seen in the data should be off by 0.56 keV. This might be consistent with the peak seen. The lines at approximately 20.7 keV and 17.7 keV are transition lines from ^{237}Np, which is the decay product of americium. The line at 20.7 keV indicates the L_2-N_4 transition line, while the one at 17.7 keV shows the L_2-M_4 transition. Both lines align rather well with the peak position which supports the theory of a linear error dependence resulting from the correction mistake while applying the gain map. The amplitude of the peaks from neptunium depends on the age of the source. Neptunium has a lifetime of 2.1×10^6 years and therefore accumulates over time. The positions of the peaks are taken from [37].

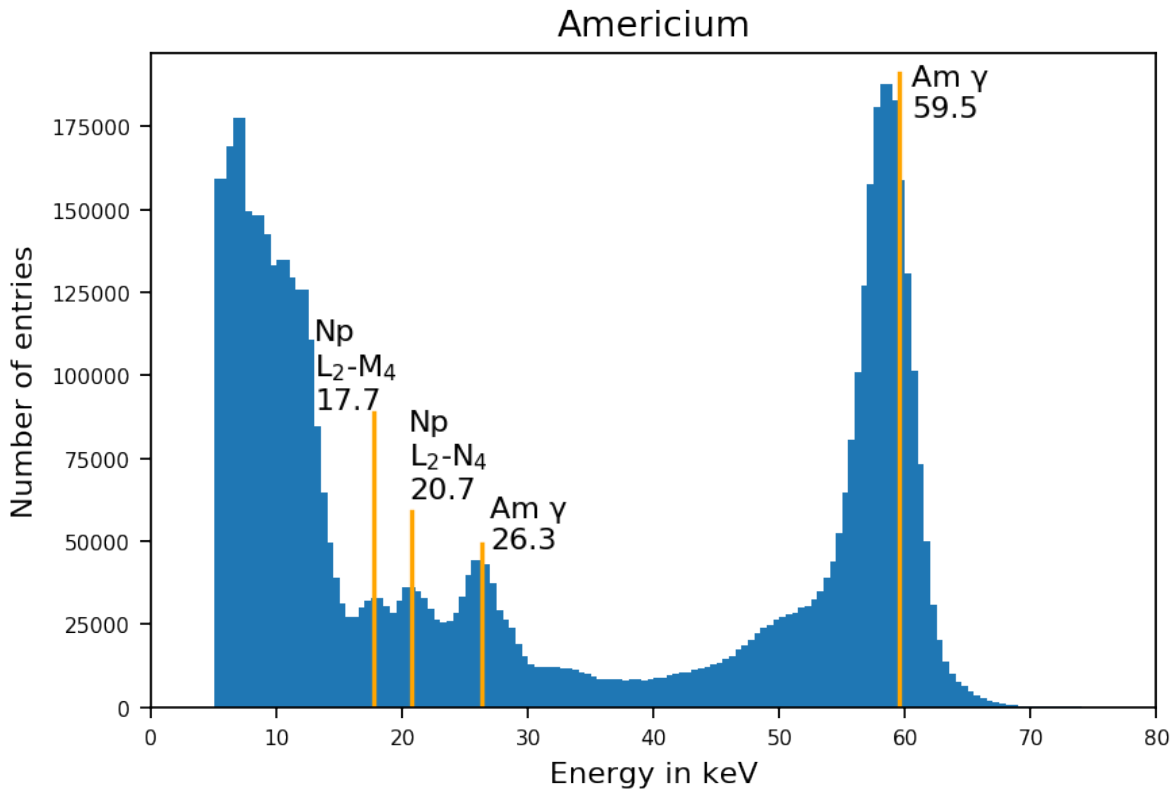


Figure 7.16: Transition lines of the americium spectrum which can be seen in the distribution corrected by the AmTb gain map. Next to the prominent 59.5 keV line, the transition lines at 26.3 keV, 20.7 keV and 17.7 keV [37] can be distinguished.

The conclusion to be drawn from the gain investigations is, that an improvement of the distributions could be achieved as seen by the direct comparisons as well as with the corrected and analysed spectrum of americium. The peak widths are not completely caused by noise but can be optimised to a certain extent. Therefore, the detector can be calibrated more than previously done. For different peak energies used to obtain a gain map, different gain factors are found. As the energy calibration showed a linear reaction, something else must cause the varying factors.

It could be considered using gain calibrations for simulations. With the gain factors some effects are corrected which result in a wrong read out of a current. This might also affect the position, where the crossing particle was detected. With a simulation it could be investigated whether a gain calibration reduces the possible recording of charge sharing aspects. This could increase the probability to find the position more precisely at which a charged particle crossed the detector.

CHAPTER 8

Conclusion

The PXD has been developed for the Belle II experiment at the SuperKEKB accelerator. The modules of the detector consist of a DEPFET pixel matrix and three different chips. The latter are responsible for steering the matrix readout, digitising the analogue currents and preprocessing those, before sending it off to the backend electronics. The components had to be tested before the final modules are assembled, to ensure their functionality and the correct communication on the module. After individual tests of the chips, a demonstrator system called Hybrid 5 was used to investigate a minimal set of final matrix and chips and determine working parameter spaces.

First, characterisations were done, testing for stable matrix voltages, the digitisation of the analogue currents, the communication between the chips and the transmission of the data to the backend electronics. Second, a calibration of the matrix was done with different radioactive sources. In all characterisation scans, stable conditions were found, often even a wide range of settings to choose from. The matrix voltages found by the characterisation were confirmed to work fine with the continuous spectrum of a Strontium source, resulting in the expected Landau shaped distribution.

With the optimal working parameters defined, an energy calibration of the system with final components was done for the first time. Eight γ-sources with their prominent peaks at energies between 6 and 60 eV were used and a linear relation between the measured energies was found as expected. Furthermore, with the energy calibration it was possible to calculate the amplification of the DEPFET pixels. The resulting amplification $g_q = (613.45 \pm 8.99)$ pA per electron is higher than all previous measurements of it.

With high statistics in some source scans, single pixel distributions were investigated for the first time. With these, two gain maps were created. One map at lower peak energies around 20 keV with silver and molybdenum, and another one at higher peak energies around 50 keV with americium and terbium. When reapplied on the recorded data, the energy resolution is increased and the width of the peaks becomes considerably smaller.

For americium, a detailed analysis of the lower peaks was performed on the gain corrected data. Previously, a clear distinction of the peaks in the distribution was difficult. With the corrections through the gain map, three additional peaks can be distinguished.

In the results of the pedestal investigation as well as the gain calibration maps similar effects were observed. Those are not expected and it could be interesting to investigate in detail where they come from. In addition, different combinations of matrix voltages might be examined for dependences. With wider ranges than chosen in this thesis, more extreme effects might be found.

The gain maps were only applied to the distributions of the γ sources used in the measurements. It would be interesting to apply it to the strontium distribution, investigating the improvement in the energy resolution on this different kind of distribution.

With the results of this master's thesis as well as previous detailed measurements on matrix and chips, the mass production of the final modules for the PXD in Belle II was started. The smaller pre-detector is in commissioning since September 2017. The first data taking is expected in the first half of 2018.

Bibliography

[1] Leucippus and C. Taylor,
The Atomists, Leucippus and Democritus: Fragments : a Text and Translation with a Commentary,
Phoenix (Toronto, Ont.).: Supplementary volume, University of Toronto Press, 1999 (cit. on p. 1).

[2] E. Rutherford, *The scattering of alpha and beta particles by matter and the structure of the atom*,
Phil. Mag. Ser. 6 **21** (1911) (cit. on p. 1).

[3] M. Gell-Mann, *A Schematic Model of Baryons and Mesons*, Phys. Lett. **8** (1964) (cit. on p. 1).

[4] G. Zweig, *An SU_3 model for strong interaction symmetry and its breaking; Version 2*, (1964)
(cit. on p. 1).

[5] S. L. Glashow, J. Iliopoulos and L. Maiani, *Weak Interactions with Lepton-Hadron Symmetry*,
Phys. Rev. D **2** (1970) (cit. on p. 1).

[6] N. Cabibbo, *Unitary Symmetry and Leptonic Decays*, Phys. Rev. Lett. **10** (1963) (cit. on p. 1).

[7] M. Kobayashi and T. Maskawa, *CP-Violation in the Renormalizable Theory of Weak Interaction*,
Progress of Theoretical Physics **49** (1973) (cit. on p. 1).

[8] J. H. Christenson et al., *Evidence for the 2π Decay of the K_2^0 Meson*, Phys. Rev. Lett. **13** (1964)
(cit. on p. 1).

[9] M. Thomson, *Modern Particle Physics*, Cambridge University Press, 2013 (cit. on pp. 2, 4).

[10] K. Abe et al., *Observation of Large CP Violation in the Neutral B Meson System*,
Phys. Rev. Lett. **87** (2001) (cit. on p. 2).

[11] B. Golob, S. Hashimoto and M. Hazumi, eds., *Physics at Super B Factory*, 2010,
URL: `https://arxiv.org/pdf/1002.5012.pdf` (cit. on p. 3).

[12] KEK, *SuperKEKB and Belle II*, 2017, URL: `www.belle2.org/project` (cit. on p. 4).

[13] Z. Dolezal and S. Uno, eds., *Belle II Technical Design Report*, 2010,
URL: `https://arxiv.org/abs/1011.0352v1` (cit. on pp. 4–7, 14).

[14] Belle II, *Belle II*, 2017, URL: `belle2.jp/detector` (cit. on pp. 5, 6).

[15] T. Konno, *Status and prospects of the Belle II experiment*,
Journal of Physics: Conference Series (2015) (cit. on pp. 6, 7).

[16] C. Kiesling and H.-G. Moser, eds., *The PXD Whitebook*, unpublished, internal, 2017
(cit. on pp. 7, 14, 17, 19, 20).

[17] S. Sze, *Physics of Semiconductor Devices*, 2nd ed., Wiley, 1981 (cit. on p. 9).

[18] U. Mishra and J. Singh, *Semiconductor device physics and design*, Springer Netherlands, 2008
(cit. on p. 10).

[19] E. Gatti and P. Rehak,
Semiconductor Drift Chamber - An Application of a Novel Charge Transport Scheme,
Nuclear Instruments and Methods in Physics Research (1984) (cit. on p. 11).

[20] H. Kolanoski and N. Wermes, *Teilchendetektoren*, Springer Spektrum, 2016 (cit. on pp. 11, 13, 14, 46).

[21] P. Horowitz and W. Hill, *The Art of Electronics*, 2nd ed., Cambridge University Press, 1989 (cit. on pp. 12, 13).

[22] R. Wang, *Metal-Oxide-Semiconductor Field-Effect Transistors*, 2017, URL: `http://fourier.eng.hmc.edu/e84/lectures/ch4/node13.html` (cit. on p. 12).

[23] M. Porro et al., *Spectroscopic performance of the DePMOS detector/amplifier device with respect to different filtering techniques and operating conditions*, Nuclear Science, IEEE Transactions on **53** (2006) (cit. on p. 14).

[24] M. Koch, *Development of a Test Environment for the characterisation of the Current Digitizer Chip DCD2 and the DEPFET Pixel System for the Belle II Experiment at SuperKEKB*, PhD thesis: University of Bonn, 2011 (cit. on p. 16).

[25] P. Fischer, I. Peric and C. Kreidl, *SwitcherB18 (Gated Mode) Reference Manual*, 2012 (cit. on p. 18).

[26] I. Peric, *Production ASICs: DCDB4.1 and DCDB4.2 Reference Manual*, 2016 (cit. on pp. 18, 19).

[27] M. Lemarenko, L. Germic and T. Hemperek, *Data Handling Processor Manual*, 2016 (cit. on pp. 20, 26).

[28] P. Leitl, *JTAG Boundary Scan of the Belle II Pixel Vertex Detector*, MA thesis: University of Munich, 2015 (cit. on p. 21).

[29] Argonne National Laboratory, *Experimental Physics and Industrial Control System (EPICS)*, URL: `http://www.aps.anl.gov/epics/` (cit. on p. 23).

[30] L. Germic, *Phd thesis*, unpublished (cit. on p. 26).

[31] Xilinx, *Virtex-6 FPGA Data Sheet*, DC and Switching Characteristics (cit. on p. 27).

[32] B. Paschen, *internal communication* (cit. on p. 32).

[33] F. Lütticke, *internal communication* (cit. on p. 32).

[34] P. Wieduwilt, *Optimization of the front-end read-out electronics for the Belle II DEPFET Sensor*, MA thesis: University of Goettingen, 2016 (cit. on p. 33).

[35] R. Jenkins et al., *Part VIII. Nomenclature system for X-ray spectroscopy (Recommendations 1991)*, (1991) (cit. on p. 49).

[36] Amersham International Limited, *Variable energy X-ray source code AMC.2084* (cit. on p. 49).

[37] C. Chong et al., "Gamma ray spectrum of Am-241 in a back scattering geometry using a high purity germanium detector", *Proceedings of INC '97 - International Nuclear Conference: a new era in Nuclear Science and Technology - the challenge of the 21st century*, Malaysia: Malaysian Inst for Nuclear Technology Research MINT, Bangi, Selangor, Malaysia, 1997 (cit. on pp. 49, 56, 57).

[38] E. Hussein, *Handbook on Radiation Probing, Gauging, Imaging and Analysis*, Springer Netherlands, 2003 (cit. on p. 49).

[39] R. Pehl et al., *Accurate determination of the ionization energy in semiconductor detectors*, Nuclear Instruments and Methods **59** (1968) (cit. on p. 50).

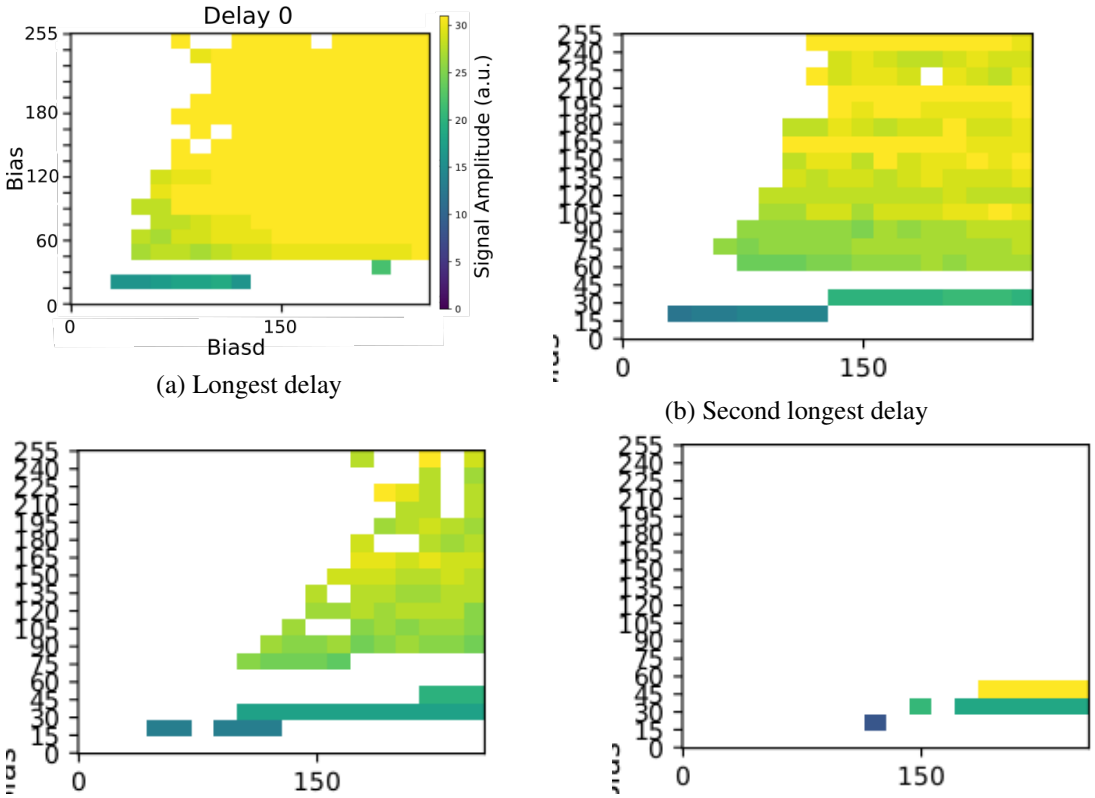
[40] F. Lütticke, *Development of Pixel Modules for the Belle II Detector*, unpublished, PhD thesis: University of Bonn, 2017 (cit. on p. 50).

[41] B. Schwenker, *Development and validation of a model for the response of the Belle II vertex detector*, PhD thesis: University of Goettingen, 2014 (cit. on p. 50).

APPENDIX A

Useful information

A.1 HS link with different delays



(a) Longest delay

(b) Second longest delay

(c) Second shortest delay

(d) Shortest delay

Figure A.1: Shorter delay options reduce the number of possible settings.

A.2 List of Matrix and DCD Parameters

Matrix parameter	Setting
bulk	10 000 mV
source	6 000 mV
gate off	5 000 mV
gate on	−2 500 mV
clear on	19 000 mV
DAC	**Value**
IPDel	127
ITCP	30
ITCPL	30
IPSourceCasc	64
IFBRef	64
INMOS	120
VNSubIn	40
VTCSFN	60
VNDel	127
RefNWell	64
IAmpPBias	60
VPMOS	120
gain	En90

Table A.1: Matrix and DCD parameters for pedestal and source measurements.

A.3 Gain corrections

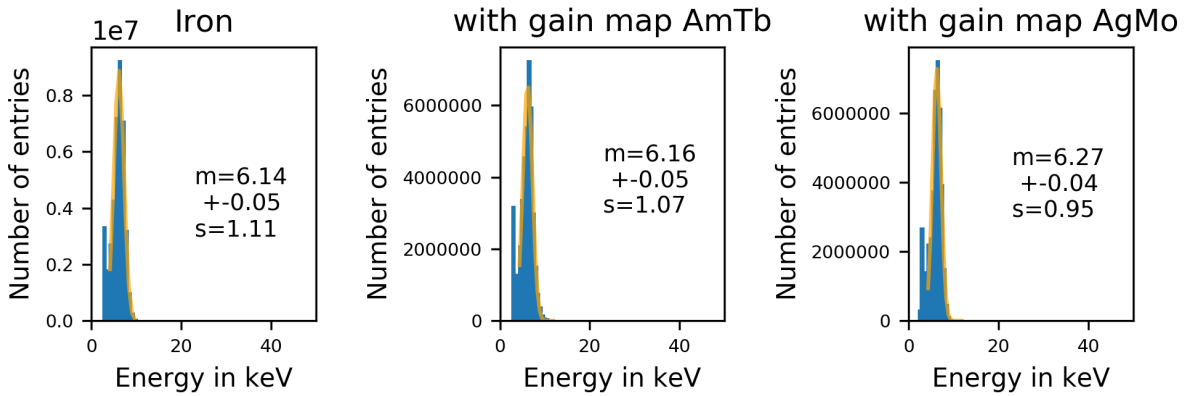


Figure A.2: The uncorrected distribution of iron is on the left side, in the middle is the same distribution corrected with the gain map from terbium and americium, while to the right the corrections with the gain map produced from silver and molybdenum is shown. Both corrections increase the energy resolution.

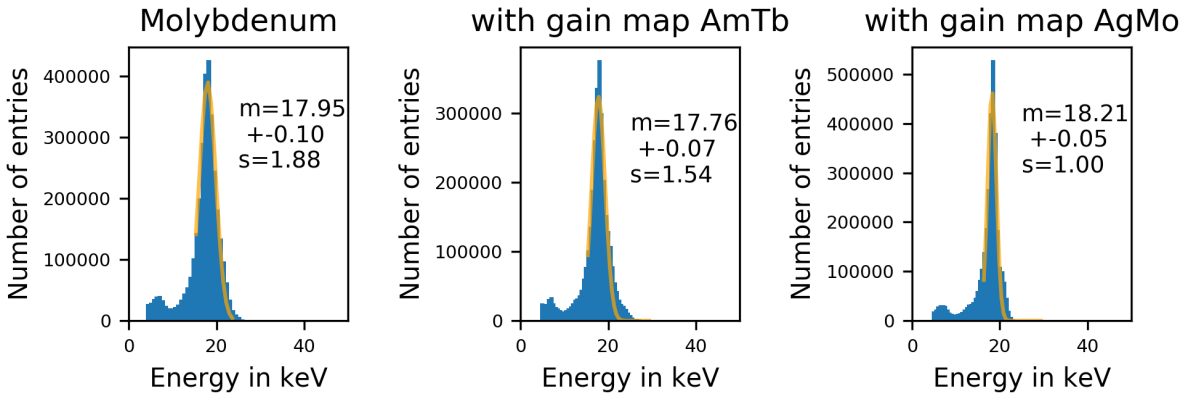


Figure A.3: The uncorrected distribution of molybdenum is on the left side, in the middle is the same distribution corrected with the gain map from terbium and americium, while to the right the corrections with the gain map produced from silver and molybdenum is shown. Both corrections increase the energy resolution.

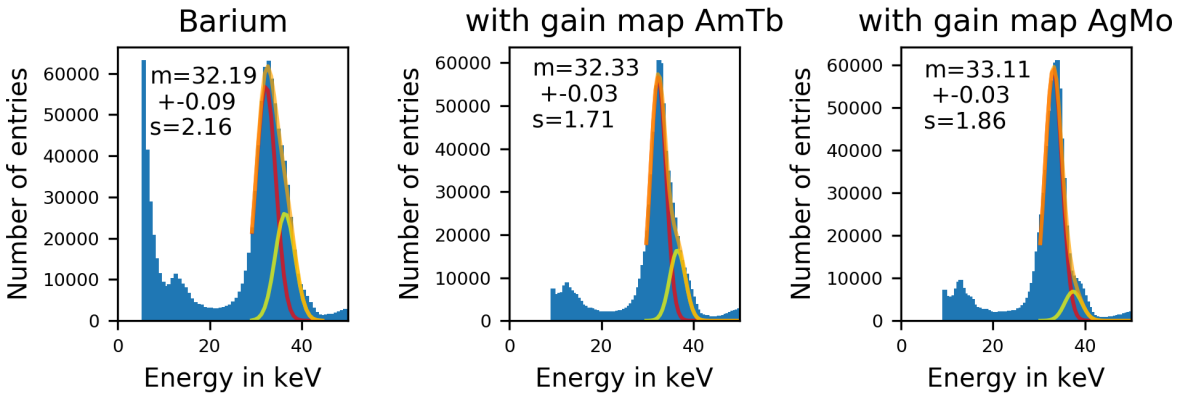


Figure A.4: The uncorrected distribution of barium is on the left side, in the middle is the same distribution corrected with the gain map from terbium and americium, while to the right the corrections with the gain map produced from silver and molybdenum is shown. Both corrections increase the energy resolution.

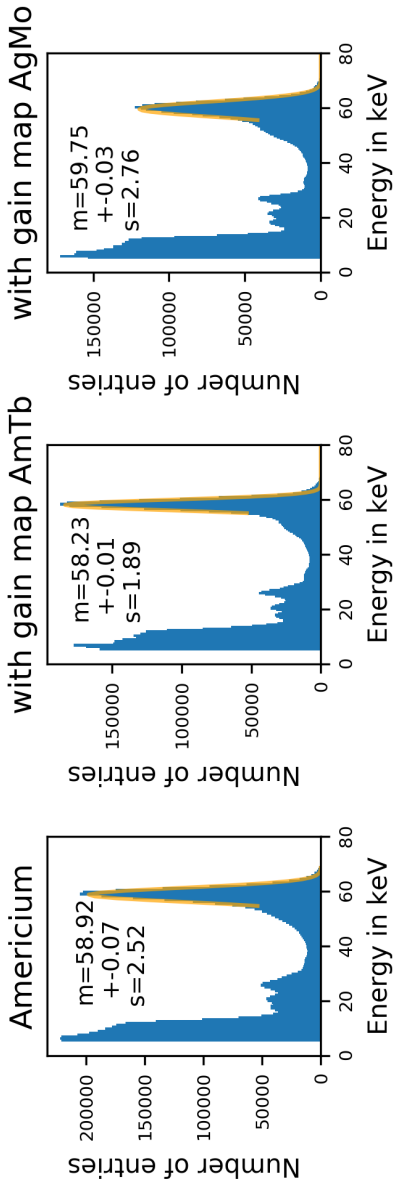


Figure A.5: The uncorrected distribution of americium is on the left side, in the middle is the same distribution corrected with the gain map from terbium and americium, while to the right the corrections with the gain map produced from silver and molybdenum is shown. Both corrections increase the energy resolution.

List of Figures

List of Tables

Acknowledgements

I would like to thank, first of all, Professor Dr. Jochen Dingfelder for giving me the opportunity to write my master's thesis in his group on the Belle II Pixel Detector. I learned a lot during the last year about working in a collaboration, about difficulties and delays (in more than just the received results) in measurement processes and about myself. I enjoyed being part of the group.

Secondly, I would like to thank Dr. Philip Bechtle who kindly agreed to read and evaluate my master's thesis as the second referee. I am grateful for the uncomplicated procedure.

Third, I would like to thank Carlos Marinas for his help on the talks I gave during the last year. Thanks for rearrangements, transition sentences and in general tips and tricks. Special thanks for the time, you took before the colloquium for explanations and practice talks.

I thank Botho Paschen for relating to my problems to grasp the many different aspects of the complex system and bringing them together to a working ensemble in my head. For giving understandable answers and often explaining a bit more than I could phrase in a question. I thank you for insisting in the beginning, that I take the time to complete the programming tutorial. I think, it helped me a lot later on.

I thank Florian Luetticke for his support in most aspects related to programming and always finding the bugs I could not. Thanks for many evenings, weekends and nights spend in the institute harmoniously working, especially during the last weeks. Thanks for bearing with my repeated and sometimes not just once rephrased questions, when I still did not understand this or that connection. And thanks for the ice cream.

I thank Leo Germic for his explanations and sketches on data transmission and de-emphasis and sometimes discussions on completely different topics.

Thanks to the SiLab people for talks, cake and recreational activities.

Ich danke meiner Familie, die mich während meines Studiums und darüber hinaus immer unterstützt hat. Mir bedeutet eure Anteilnahme und euer Interesse viel. Danke dafür. Auch meinem Freundeskreis, seien es nun die physikbegeisterten Menschen, die mich sicherlich durch die ein oder andere Vorlesung gezogen haben, oder Freunde außer- und innerhalb des Studiums, die auch mal für anderweitige Ablenkung und Beschäftigung sorgten, gilt mein Dank. Beides hätte und möchte ich nicht missen. Grazie mille!

Last but not least, I could not have finished this thesis without music. Especially the fantastic soundtrack to the movie *The Guardians of the Galaxy* as well as the music by *Mark Knopfler*, *Talco* and the *Piccola Orchestra Avion Travel* accompanied me during many hours of coding and writing. It made everything at least seem easier. Thank you very much!