Investigation of gated mode operation of the Belle II pixel detector

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I hereby declare that this thesis was formulated by myself and that no sources or tools other than those cited were used.

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CHAPTER 1

Introduction

Where do we come from? How was the universe created? Particle physicists have been researching to figure out answers to these questions. Curiosity was a driving factor for them, trying to understand the foundation our universe is built on, to see which fundamental forces govern the universe. The Standard Model of particle physics has been successful so far in describing and predicting interactions between particles. Great achievements have been made by particle physicists in the last decades, expanding and verifying the Standard Model. Nonetheless the current Standard Model is not flawless. It is unable to answer fundamental questions like how did the universe begin? Or why does the universe consist of matter? Thus new more precise experiments are conducted in an attempt to discover new physics, physics currently not contained in the Standard Model. As better and bigger particle accelerators are commissioned and built detectors need to advance as well to keep up with the new requirements.

1.1 A short history of insights

Every particle has its own antiparticle. If a particle interacts with its corresponding antiparticle, they annihilate. In the Fifties of the last century people believed that both particle and antiparticle are governed by the same laws. The common belief was that after mirroring charge and spatial coordinates (CP-symmetry), one would be able to apply the same laws to the antiparticles as to particles. Yet in the following years this belief was shaken when violations of this symmetry were discovered. After CP-violation in Kaon systems was observed by James Cronin and Val Fitch the year 1964, theoretical physicists struggled to explain this disparity [1]. It took nearly ten years until Kobayashi and Maskawa found the solution to this problem in 1972. They solved the problem of asymmetry by postulating the existence of two new elementary particles the top (t) and bottom (b) quarks [2]. With earlier work from N. Cabibbo this lead directly to the discovery of the Cabibbo–Kobayashi–Maskawa matrix (CKM matrix). The CKM matrix describes the strength and probability of flavour changing weak decays. This approach, which allowed them to integrate CP-violation into the Standard Model of particle physics, was the cue for a search for new particles. Finally, in 1977 the bottom quark was first observed at Fermilab, serving as a first step to verify their theories[3].
More than 30 years later, at the beginning of this century, large parts of the CKM matrix were well investigated, but scientists were still aspiring to prove the theories of Kobayashi and Maskawa completely. The final breakthrough arrived in the late 1990s when electron colliders which featured high luminosity were built. Two famous experiments which investigated CP-violation are the BaBar experiment in California and the Belle experiment in Japan. Their accelerators, the so-called B-factories, were designed to study CP-violation appearing in B mesons. These mesons are of interest because their lifetime, though

very short, is still comparatively long compared to other heavy mesons. If CP-symmetry was preserved, one would expect B and $\bar{B}$ mesons to have the same lifetime. To detect even slight differences in lifetime very precise measurements of the lifetime were necessary (further information on B-factories can be found in [4]).
Within the framework of the Belle experiment electrons and positrons are collided with a centre of mass energy of 10.579 GeV. This is equivalent to the mass of the $\Upsilon(4S)$ resonance, which consists of a **b** and $\bar{\mathbf{b}}$ quark. The $\Upsilon(4S)$ decays into B-mesons consisting of a **b** and a **u** or **d** quark. The lifetime of B mesons is in the order of $(1.519\pm0.007)\cdot10^{-12}$s[5]. This lifetime causes B mesons to decay before they enter the detector, which makes detection by conventional methods difficult. In order to work around this problem different energies for electron and positron beams are used. The positron beam is accelerated up to 3.5 GeV while the electron beam is accelerated up to 8 GeV[6]. This way the created mesons are boosted in direction of the electron beam. Instead of measuring the lifetime directly it becomes possible to measure the distance travelled by the mesons and deduct their lifetime from this information. A difference in the distances travelled by the meson and antimeson can be translated to a different lifetime and thus a violation of CP symmetry. There are plans for a follow-up experiment which will be called Belle II experiment. This follow-up experiment comes with a drastic increase in peak luminosity of the KEKB accelerator from 2.108×10^{34} cm^{-2} s^{-1}[7] to a design value of 8×10^{35} cm^{-2} s^{-1} ([8] p.21). Furthermore the KEKB accelerator will be upgraded and renamed to SuperKEKB. By comparison the design luminosity at LEP (Large Electron-Positron Collider), which was optimised for high energies rather than luminosity, was only 16×10^{30} cm^{-2} s^{-1} ([9] p.2). This upgrade of the accelerator and especially the increase in luminosity will make a complete redesign of the Belle detector mandatory.
One performance measure in detectors is vertex resolution[1]. Being able to distinguish secondary vertices of particles with a short lifetime from the primary vertex is a requirement for the Belle II vertex detector. With the redesigned modern Belle II detector it could become possible to look for new physics in loop processes in SuperKEKB, due to the large luminosity even rare decays could be studied with a sufficient number of events. Furthermore studies at SuperKEKB could discover new particles which appear in heavily suppressed decays. Finally the discovery of new physics is expected of current experiments at large hadron accelerators like the LHC in CERN. The new SuperKEKB accelerator could serve to investigate these events with high statistics. One of the goals of Belle II is to research particles with a short lifetime. To research these kinds of particles the ability to distinguish the interaction point from secondary vertices is crucial. An important part of modern vertex detectors is the pixel detector. Pixel detectors offer good intrinsic resolution[2], while being able to cope with high amounts of ionising radiation and the ensuing high occupancy. Thus the innermost layer of particle detectors is often made of pixel detectors. In the redesign of the Belle detector a pixel detector will be added. The Belle II detector will use the **DE**pleted **P**-Channel **F**ield **E**ffect **T**ransistor (DEPFET)[10] technology. In section 2 this work will discuss what a pixel detector is in and in section 2.1 elaborate details of the DEPFET technology.
The research part of this thesis is further divided in two parts. Chapters 4 and 5 will deal with optimising the electronics connected to DEPFET. While chapter 6 will investigate a new mode of operation for DEPFET.

[1] A vertex is the point in space where particles, in case of the KEKB accelerator electrons and protons, collide. This point is also called primary vertex or interaction point. When particles are created displaced from the primary vertex, this point is called secondary vertex. A secondary vertex occurs when a particle created in the primary vertex decays.
[2] Intrinsic resolution indicates how well a detector can resolve where it has been hit.

1.2 The Belle II detector

The Belle II detector is built in layers. Each layer is responsible for acquiring different information about the particles passing the detector. A superconducting solenoid magnet creates a magnetic field of roughly 1.5 T to bend the tracks of charged particles passing the detector. The different layers in the Belle II detector include, starting from the outermost layer moving to the interaction point:

K_L and muon detector (KLM): This part of the detector is responsible for detecting K_L (long kaons) and μ (muon). While muons do not interact strongly and do not lose enough energy to be stopped in the detector, K_L create hadronic showers in this detector and are stopped here.

Electromagnetic calorimeter (ECL): Most particles created in Belle II are stopped in this part of the detector. It measures mass and energy of electromagnetically interacting particles.

Particle identification system (PID): This part of the detector is mainly responsible for differentiation between kaons and pions. It relies on Cherenkov light to accomplish this.

Central drift chamber (CDC): This part of the detector is filled with gas. When a charged particle passes it creates electron-ion pairs, which when attracted to charged wires create particle cascades. Furthermore the CDC is responsible for tracking, momentum measurement and triggers the VXD.

Silicon vertex detector (VXD): The innermost part of the detector is mainly responsible for distinguishing primary and secondary vertices. Furthermore hits are used for a precise track reconstruction close to the interaction point.

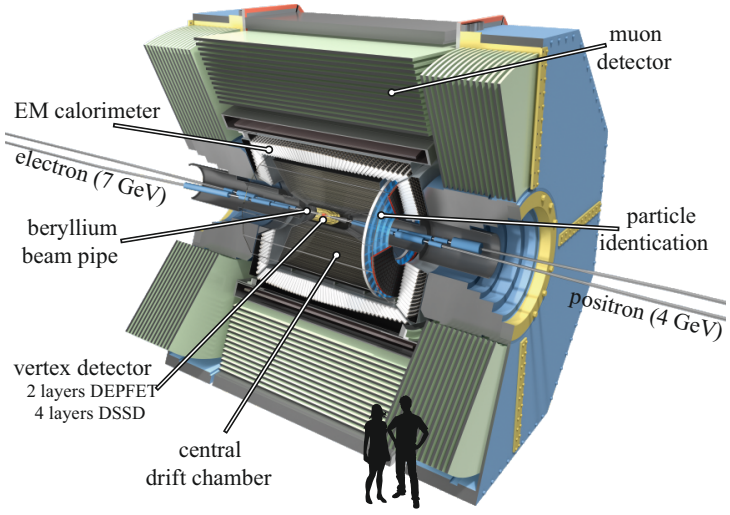


Figure 1.1: Sketch of different layers of the Belle II detector [11].

Vertex detector performance

The important parameters for the vertex resolution can be understood from a simple two-layer detector model. The vertex resolution (σ_{vertex}) of such a detector with two layers, with layer 1 being the inner and

layer 2 the outer layer, is described by ([12] p.272):

$$\sigma_{\text{vertex}} = \left(\frac{r_1}{r_2 - r_1}\sigma_2\right)^2 + \left(\frac{r_2}{r_2 - r_1}\sigma_1\right)^2 + \sigma_{\text{MS}}^2.$$

In this formula r_1 is the distance between inner layer and beam line and r_2 is the distance between the outer layer and the beam line. The variable σ_1 and σ_2 are the intrinsic resolutions of the inner and outer layer. Finally σ_{MS} represents the decrease in resolution due to multiple scattering.
The effects of multiple scattering are proportional to the material budget ($\sigma_{\text{MS}} \propto 1/\sqrt{\text{x}/\text{X}_0}$). The parameters with the strongest influence on the vertex resolution are the distance of the innermost layer from the interaction point (r_1), the intrinsic resolution of the innermost layer (σ_1) and the material measured in radiation lengths (x/X_0). In addition, a higher number of detector layers provides more interaction points and better track reconstruction.

The Belle II vertex detector

To allow for precise vertex reconstruction the Belle II vertex detector has six layers of two different silicon detector technologies. The two innermost layers are DEPFET pixel detectors and the four outermost layers are strip detectors called DSSD (Double-Sided Silicon Strip Detector). Strip detectors allow for excellent spatial resolution (in the case of the Belle experiment strip pitches of 22.5 to 76 µm ([13] p.3)) and good time resolution (shaping time of 1 µs ([14] p.132). A downside to the strip technology is that it is challenging to deal with multiple hits. If more than one particle hits the detector at once the position of the hit becomes ambiguous and ghost hits appear[3], hit to track association becomes difficult. In the Belle experiment the length of one strip was fairly large with strip length of 25.6 to 77.7 mm([13] p.3). That is why closest to the interaction point a pixel detector (PXD) will be used in the Belle II experiment (definition see section 2). PXD layers will be placed at a distance of 14 mm and 22 mm ([8] p.78). Pixel detectors have more readout channels and the small size of pixels makes multiple hits in one read out channel less likely. This makes it possible to place them closer to the interaction point. Strip detectors are placed at the outer layers of VXD. The DSSD will be placed at an inner radius of 38 mm and an outer radius of 140 mm from the interaction point ([8] p.139).
The pixel sensor type used in Belle II is called DEPFET. Due to the large number of read out channels DEPFET and pixel detectors in general produces large amounts of data. The pixel detector used in this thesis is produces data rates of up to 1.28 Gbit/s ([15] p.12). The total data rate produced by the PXD is expected to amount to up to 58 Gbit/s in the Belle II experiment. To reduce the data stream the 4 layers of DSSD are used. Because their environment is less severe and their integration time is lower than that of DEPFET they can be used to define regions of interest for the innermost two pixel detector layers. As especially the pixel detectors are very close to the interaction point, it is crucial for the material budget to be low and the detector to be as thin as possible. This prevents multiple scattering which leads to measurement errors in the other layers of the tracking detector. This thesis investigates properties of the DEPFET pixel detector.

[3] Further information on the advantages and disadvantages of strip technology can be found in [12].

CHAPTER 2

The Belle II pixel detector

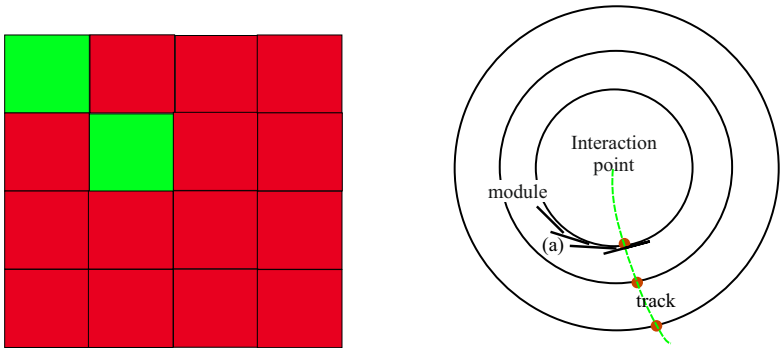


Figure 2.1: To the right, many detector modules (a) are positioned circularly around the interaction point. A particle passes the detector. On the left is a schematic picture of a pixel matrix. The green squares show which pixel cells in the grid recorded a hit. The information which pixels have been hit allows particle track reconstruction.

A pixel detector is a device used for position dependent measurements. The basic idea is to align a large number of individual pixel sensors to a grid. Those grids of particle detectors are placed circularly around the interaction point covering as much of the full 360° angle as possible, to leave the least space possible for particles to leave the detector undetected. Figure 2.1 displays such a pixel detector and how the information from pixel detectors is used for track reconstruction.
In a pixel detector each pixel is a fully functional sensor. The simplest type of silicon pixel sensor is a pn-diode. If a large enough reverse voltage is applied, the sensor is fully depleted, and very little current flows. But an ionizing particle passing through the detector will deposit energy which will result in the creation of electron hole pairs. These electron hole pairs will move according to the field created by the depletion voltage which will result in a current pulse. Measuring this current pulse provides information on how much energy has been deposited and when the ionizing particle interacted with the sensor.

2.1 DEPFET pixel

The **DE**pleted **P**-Channel **F**ield **E**ffect **T**ransistor (DEPFET) is a silicon based detector. DEPFETs foundation is a p-channel MOSFET structure integrated on a fully depleted n-type silicon bulk. Below the MOSFET structure, just separated by a few micro meters from the external gate, is a strong n^+ implantation, the so called internal gate.

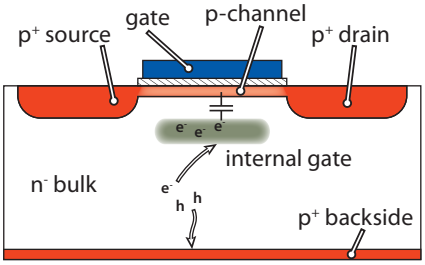


Figure 2.2: DEPFET's main component is a MOSFET structure integrated on a fully depleted bulk. The p-channel couples to the internal gate[11].

A charged particle passing through the detector will create electron hole pairs. Holes will be attracted to the p^+ backside, while electrons will be attracted to and collected inside the internal gate. The internal gate couples to the p channel by inducing mirror charges. These mirror charges change the width of the p-channel. Thus the amount of collected charge in the internal gate has an influence on the transistor current and measurements of the transistor current will yield information on the amount of collected charge. The coupling between internal gate and p-channel causes an internal amplification of the signal. The technique of internal amplification allows for excellent signal to noise ratio. The whole process is displayed in figure 2.3. As the readout in DEPFET is non destructive charge stored inside the internal gate can be sampled any time, so charge does not need to be measured as soon as it is created. Furthermore no read out electronics need to be placed directly on top of DEPFET. Thus the detector can be build more thinly and as the readout electronics, which need active cooling, are located outside the acceptance region, gas injection cooling is sufficient to dissipate the heat generated by DEPFET [16].

2.1.1 Charge collection in DEPFET

The internal gate is a strong n^+ implantation right below the external gate. When in operation the complete DEPFET sensor is depleted. Depletion causes the internal gate to become positively charged. Thus the internal gate forms a potential minimum and is attractive for free electrons.
Due to the high luminosity in the Belle II experiment, the DEPFET detector needs a fast integration time. This also has an influence on charge collection. Charge needs to be collected before the next readout is done. But with the potential minimum created by the internal gate as the only mechanism for charge collection charge which is created at the edges of the pixel might not be collected in time before the next readout. Furthermore, charge created close to the edges might travel to a different pixel. As electrons diffuse until they reach a field with sufficient strength and drift to an internal gate. In conclusion just relying on the internal gates attraction to collect all electrons within the bulk is not enough. For that reason, mechanisms for quick and reliable charge collection are implemented in DEPFET. These mechanisms are sidewards depletion and a drift voltage.

Sidewards depletion

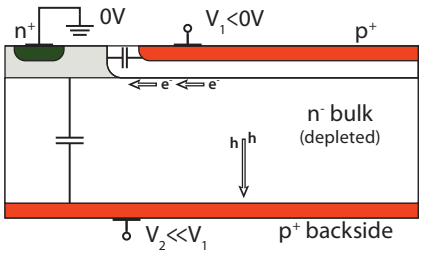


Figure 2.3: Depletion regions from top and bottom of the detector overlap close to the top, forming a potential minimum. [11].

If one wants to be able to create free charge carriers within the DEPFET, the bulk needs to be depleted. If one were to deplete a DEPFET pixel from one side, all newly created charge would be extracted from that contact. However, for DEPFET free charge carriers should go to the internal gate. That is why DEPFET is depleted from two sides using the so called sidewards depletion. Prerequisite are two p contacts at the top and bottom of the pixel and an additional n contact placed close to the edge of the pixel. The two p contacts are set on a potential which is negative in regard to the n contact. Depleted areas start to form around both p contacts. If their voltages are chosen high enough these two depleted areas will overlap, forming a potential minimum. This potential minimum can be moved within the pixel depending on how much larger or smaller one of the two voltages is compared to the other. If this potential minimum is moved to the same height as the internal gate it assists charge collection.

Drift voltage

Charge created in border areas of a pixel takes longer to drift to the internal gate than charge created in more central regions. To ensure all charge is collected in the short time between readout cycles, an additional drift voltage is implemented. This drift voltage is applied close to the edges of each DEPFET pixel. It is a negative voltage which pushes electrons closer to the central region of the DEPFET pixel. This also decreases the chance of electrons drifting to neighbouring pixels.

2.1.2 Charge removal from DEPFET

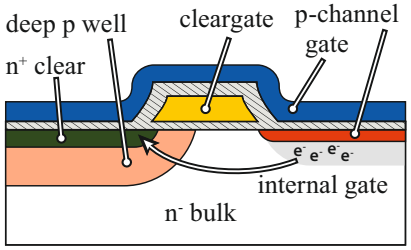


Figure 2.4: Clear contact, clear gate and a deep p implant form a MOSFET structure[11].

Over time leakage currents and more and more charged particles interacting with the detector, would start filling the internal gate. This would continue until the internal gate is completely filled with electrons. The consequence being the loss of attraction to free charge carriers. Hence a mechanism is needed to remove charge from the internal gate. In DEPFET a process called clear is used to remove the collected charge from the internal gate and any leftover charge in the detector. Two additional contacts are required for the clear. One contact is the clear contact, which is used to extract charge from the DEPFET pixel. This contact is realised in form of a n^+ implant. To prevent charge from travelling to the clear contact instead of the internal gate, during charge collection or read out, the clear contact is shielded by a deep p implant. The second contact is called clear gate. Together with the internal gate, deep p implant and clear contact, the clear gate forms a MOSFET structure. This MOSFET structure is reverse-biased to prevent any charge being lost within the clear contact. To clear a DEPFET pixel a large positive voltage is applied to the clear contact. Simultaneously the external gate is switched to on. This lowers the potential barrier between internal gate and clear. As a result, charge is able to punch through the potential barrier created by the deep p implant. The required contacts are displayed in the schematic in figure 2.4.

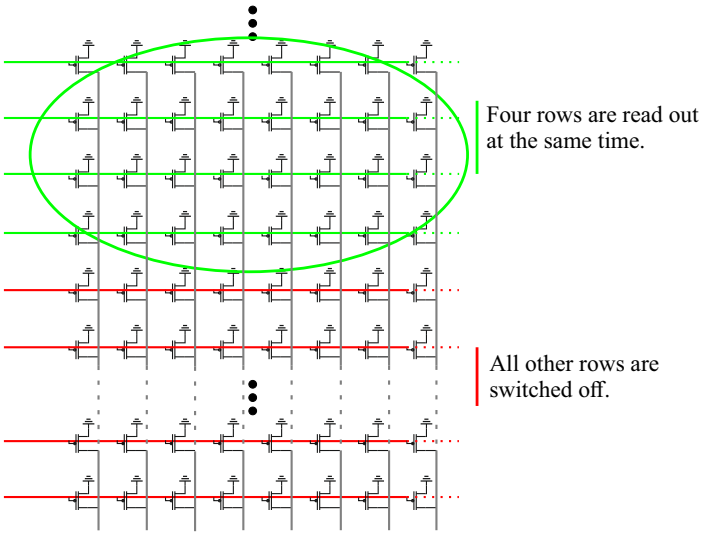


Figure 2.5: Rolling shutter readout of a DEPFET matrix. Simplified sketch, no drain lines are shared between pixels which are read out at the same time.

2.2 DEPFET matrix

In order to reduce material budget and decrease the amount of data generated, the DEPFET detector is not read out as a whole. Rather DEPFET employs a slightly modified rolling shutter mode. In a simple rolling shutter mode pixels are read out row by row, starting from the top. In this readout scheme there can only be one active row, all other rows must be switched off. This allows a reduction of the number of drain lines required to read out the pixel, because each column can share one drain line. The advantage of this read out scheme is that the material budget created by cables is drastically reduced. The downside of this readout scheme is speed. Compared to reading out the matrix directly, the full integration time of the matrix is much longer and given by the number of rows multiplied by the time required to read out one row ($t_{tot} = N_{row} \times t_{1row}$).
The rolling shutter mode used in DEPFET is a slightly modified version of the simple rolling shutter mode. Instead of reading out row by row, DEPFET reads out four rows at once. This allows for reasonable integration times in the order of 20 µs [17] while keeping material budget and power consumption to a minimum ($t_{tot} = \frac{N_{row}}{4} \times t_{1row}$). DEPFETs rolling shutter mode is displayed in figure 2.5. To integrate the matrix each pixel follows the ensuing algorithm:

Charge collection phase:
1. Gate voltage is set to a positive value (off state).
2. The detector starts collecting charge in the internal gate.

Sampling phase:
1. Gate voltage is set to a negative value (on state).
2. Wait until the current in the drain contact has settled.
3. Sample the drain current.
4. Raise voltage on the clear contact, to remove charge from the internal gate.
5. Lower clear voltage to allow charge collection to begin anew.

During the charge collection phase the detector is sensitive for incoming particles. While during the sampling phase the amount of electrons within the internal gate is measured. The matrix is read out and

cleared continuously, so after a fixed amount of time each pixel is read out. It is of special importance to choose the sampling point well. If the signal is measured too early the pixel's drain current might not have settled yet, if measured too late there is a risk of measuring during or after the clear. If the sampling point is chosen correctly, the drain current depends solely on the number of electrons stored in the internal gate. The change of current for a given change in number of electrons stored within the internal gate is called gain. The gain can be calculated with:

$$g_q = \frac{\partial I}{\partial q}.$$

In my bachelor thesis I determined the gain of a PXD 6 matrix to be $(431 \pm 4)\,\mathrm{pA/e^-}$ h−pair. For further explanation on how to obtain gain see [18]. The matrix used in this thesis is a PXD 9 Belle II prototype.

2.3 The DEPFET half ladder

In the Belle II experiment the DEPFET matrices will be organized in modules. The DEPFET modules for the Belle II pixel detector are entities that combine an active area with DEPFET pixels with the required steering and readout chips on one module. Figure 2.6 shows a half ladder featuring an array of 250×768 pixels. The steering **a**pplication-**s**pecific **i**ntegrated **c**ircuits (ASICs) are bump-bonded at the side of the stave, while the readout ASICS are placed at the end of the module. The ASICs used in the module are:

Switcher: The Switcher chip is responsible for selecting the active row. Gate and clear voltages are controlled with the Switcher.

DCD: The **D**rain **C**urrent **D**igitizer (DCD) is responsible for converting the output signal of the matrix to a digital signal.

DHP: The **D**ata-**H**andling-**P**rocessor (DHP) is responsible for data reduction, buffering of data and steering and synchronisation of the other ASICs.

Four rows of the DEPFET matrix in the half ladder are connected to one electrical row (gate) of the Switcher forming 192 gates. Altogether six Switchers are used to steer the matrix. Thus each Switcher has 32 gate and clear outputs.
A half ladder has 4 DCDs with 256 input channels each, which send the digitized data to 4 DHPs for further processing.

2.4 Gated mode

The improved superKEKB accelerator will use a continuous injection scheme. Every 20 ms [17] a e^+ or e^- bunch will be refilled. The newly injected particles will produce large background and need roughly 3 ms [17] to cool down. The background is caused by the smeared out momentum of newly injected particles. These newly injected particles oscillate around the ideal bunch position or they are lost completely, creating signal while they pass the detector. This poses a special challenge because the integration time of DEPFET is in the order of 20 µs while bunches pass the interaction region every 10 µs [17]. This background from newly injected bunches coupled with the high data rates from the high luminosity could potentially lead to the detector data becoming unreliable and faulty. In order to make the DEPFET detector blind while these noisy bunches pass by a new mode of operation was suggested. This new mode will be called gated mode. Goal of this mode of operation is to suspend normal charge

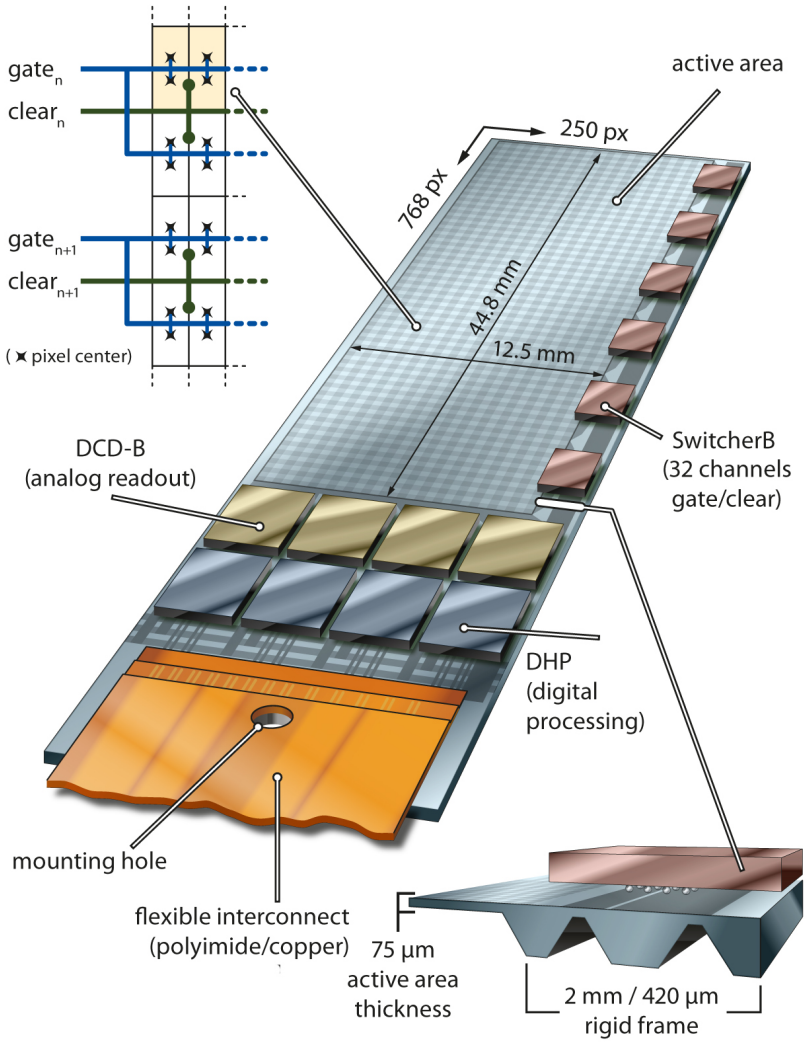


Figure 2.6: A half length silicon module from the inner layer of the PXD[11].

collection whenever a noisy bunch passes the detector. Gated mode is based on the clear process of DEPFET. To put a pixel into gated mode the voltage at the clear contact is raised to a high voltage. At the same time the external gate is switched to off state. This maintains a potential barrier which charge from the internal gate cannot pass. On the other hand charge created in the bulk is not affected by this potential barrier and is extracted into the clear contact. Hence charge within the internal gate is preserved, while newly created charge is removed. This principle was proven to work in measurements by E. Prinker [19].

Switching the detector in and out of gated mode in a time frame which is lower than the integration time poses special challenges. The whole electronics chain needs to be flawless to not corrupt data. The timing for switching in and out of gated mode needs to be precise. Else there is a risk of measuring during the passage of a noisy bunch. Furthermore as few bunch crossings as possible should be gated, to measure as many physic events as possible. Thus optimising the electronics is a first step, before dynamic enabling and disabling of gated mode can be achieved.

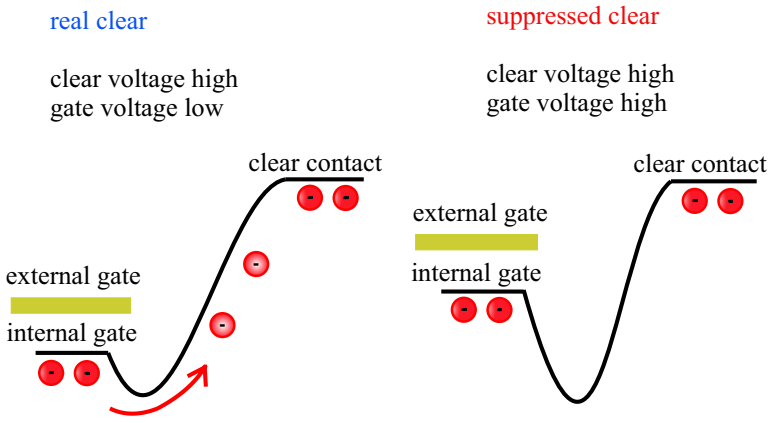


Figure 2.7: In contrast to a normal clear in gated mode the external gate is turned off when clear is put to a high potential.

2.5 Radiation damage

When ionizing radiation enters a silicon lattice there are two ways it can interact with atoms. The radiation can interact with the electrons of the atoms, creating electron hole pairs in the process. The effects of this kind of interaction are reversible. The created electron hole pairs are what is measured in a silicon detector, they give information on the energy of the particle passing the detector. The other way radiation can interact with the atoms is by interacting with the nucleus (or the whole atom) directly. This can cause permanent changes to the silicon lattice.
The PXD will get irradiated by multiple processes which incluse synchrotron radiation and beam-gas Coulomb interactions. The main contribution to the background in the Belle II experiment will stem from fermions (mainly electrons and positrons)[20]. The main background stemming from the 4-fermion final state radiation:

$$e^+e^- \rightarrow e^+e^- + f^+f^-$$

This process is the main contribution to background, because being a quantum electrodynamic process it is luminosity dependent [21]. The dose rate at the experiment is luminosity dependent and is expected to be 5.4 kGy/year[1] for the outer layer of DEPFET and 20 kGy/year for the inner layer. Simulations and measurements predict that the damage done to the bulk will be small [20]. The largest effects will stem from surface damage. The radiation will create electron hole pairs in silicon dioxide layers. Silicon dioxide is used as an insulator in **m**etal–**o**xide–**s**emiconductors (MOS). In DEPFET the off voltage for the gate is positive. If the isolating silicon dioxide is irradiated electron hole pairs will form. The electrons are attracted to the positive gate voltage, while the holes move towards the silicon bulk.
However, the mobility of holes is much smaller than that of electrons. Thus, while electrons are swept out of the silicon dioxide in picoseconds, holes take seconds to travel to the silicon interface (at room temperature). There the holes form deep long-lived trap states, which can persist for hours or up to years [22].
The holes cause shifts in noise, threshold and transconductance [20].

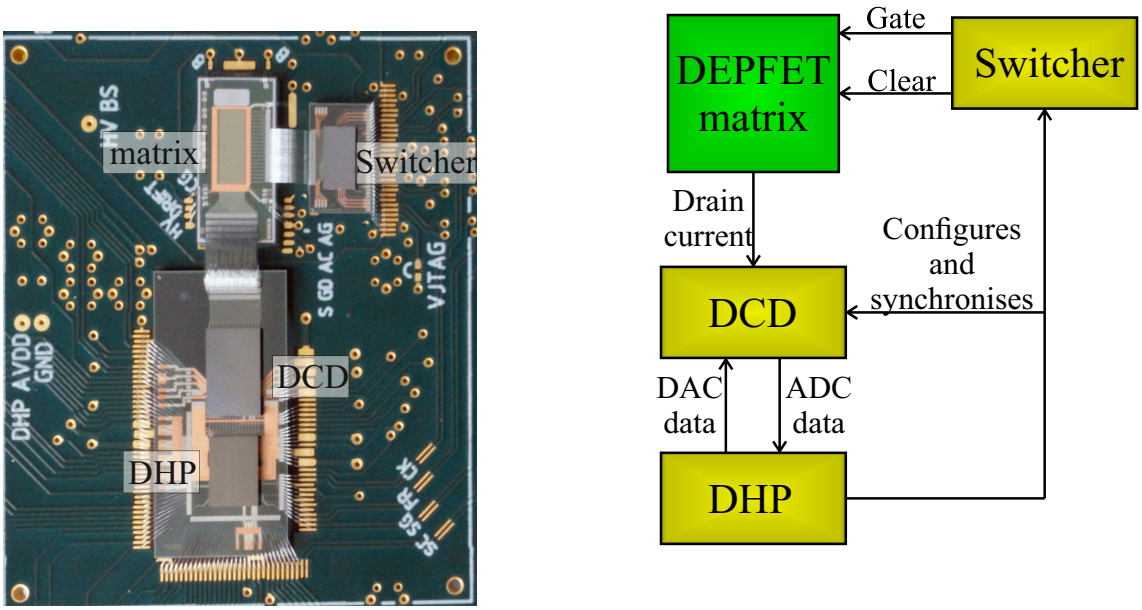
[1] One year is equal to the snowmass year of 10^7 s.

CHAPTER 3

Test setup

The following chapter describes the setup which was available to test the DEPFET system. The small testboard which houses the DEPFET matrix will be introduced. Furthermore the functionality of the FPGA board which is the link to the lab computer is explained. Finally a setup used for position dependent measurements will be described.

3.1 Hybrid 5 board



(a) Photo of Hybrid 5 components.

(b) Sketch of Hybrid 5 electronics.

Figure 3.1: Overview over Hybrid 5 electronics.

The DEPFET sensor used in this thesis was a short prototype consisting of 64×32 DEPFET pixels. The small matrix is installed on a Hybrid 5 testboard. The Hybrid 5 board is a test board featuring ASICs similar to the ones which will be used in the final experiment. The Hybrid 5 board used in this thesis featured a single DHP, DCD and Switcher. The versions of the ASICs installed on the Hybrid 5 board

with the id H5.007, which was used in this thesis, are DHPT1.0, DCDBpp and Switcher B gated mode. The standard configuration which was used to operate the DEPFET matrix and ASICs can be found in table B.1 in the appendix. The Hybrid 5 board is connected to a custom-made power supply which was built at the LMU in Munich. It is able to provide all relevant voltages for the DEPFET sensor and ASICs. An overview over the components of the Hybrid 5 board is given in figure 3.1(a) and figure 3.1(b). This Hybrid 5 board is connected to a **D**ata-**H**andling-**E**ngine (DHE), which is the link to the lab computer, via two InfiniBand cables.

3.1.1 DHP

The DHP was designed in Bonn by T. Hemperek and H. Krüger[15]. The DHP is responsible for controlling the Switcher and DCD. Furthermore the data rate is strongly reduced in the DHP. To achieve this reduction of data rate the DHP only sends data when it is requested by a trigger signal. In addition, the data the DHP sends is zero suppressed. Meaning only information about pixels which show a signal significantly larger than their base signal is sent to the computer. The data reduction and noise filtering is done in three steps.

1. The base signal of all pixels, also called pedestal value, is subtracted from the measured signal. The pedestal values need to be measured and programmed into DHP memory beforehand.

2. Noise which affects all values of a gate, so called common mode noise, is filtered. This is done by using the two parse average method. In this method the average of all data values is computed. Large values are replaced with the average value. Then the average is calculated again. This average is the common mode and subtracted from all data in the measured gate.

3. The data which has been corrected for its base value and common mode noise is checked against a threshold. Information on the pixels above threshold is sent to the computer.

This data contains information on the measured values and position of all pixels above threshold. The data is tagged with information, if common mode correction, pedestal subtraction and threshold were applied. Furthermore information on the chip which measured the data and an ID in which readout frame the data was measured are sent.
The various registers of the DHP containing information on pedestals and other system variables can be configured using JTAG[1]. Commands choosing the mode of operation (gated mode or normal) as well as when to start the readout of the matrix from the top are received across a trigger line.

3.1.2 Switcher

The Switcher is responsible for controlling the gate and clear voltages of the DEPFET-Matrix. The Switcher has two high voltage switches for clear and gate voltages:

The high clear voltage is called ClearHigh and switches the clear on, the low clear voltage is called ClearLow and switches the clear off. The high gate voltage is called GateOff and switches the external gate off, the low gate voltage is called GateOn and switches the external gate on.

The Switcher has 32 gate and 32 clear lines, which can be used to control 128 matrix rows. In case of

[1] **J**oint **T**est **A**ction **G**roup is a protocol which allows the prgramming and debugging of integrated circuits and computer chips directly within the circuit.

Hybrid 5 only 16 of those lines are connected. The rows in the DEPFET-Matrix are activated in a fixed order, which is controlled by a shift register which is running along rows. This shift register is controlled by a serial input (short: SerIn) which is connected to the DHP. When a logical one is put in SerIn, this one is the signal for the Switcher to start operation. Subsequently the logical one is clocked through the shift register, activating the rows in order.
The Switcher has two memory regions for readout sequences. The first memory region contains the normal readout sequence, the second one contains a gated mode sequence. If the Switcher receives the veto signal it switches into the second memory block. As soon as no veto signal is registered the Switcher goes back to normal readout. It resumes by reading out the gate which would have been read out, if the Switcher stayed in the first memory block for the full duration. The Switcher is located next to the DEPFET-Matrix at the side of the module, see figure 3.1(a).

3.1.3 Drain Current Digitizer

The **D**rain **C**urrent **D**igitizer (DCD) handles the conversion of analogue DEPFET-Matrix signals to digital signals. Each chip has 256 channels of which 128 are connected to the DEPFET-Matrix in case of Hybrid 5. The 128 channels are organized in 4 column pairs with 32 channels each. Each of these channels has an input dynamic range in the order of 16 µA[23]. The signal is converted in an **a**nalogue **d**igital **c**onverter (ADC) with a precision of 8 bits. Which gives a total of 2^8=256 ADC codes to work with. More details on the DCD will be explained in section 4.1.

3.2 DHE and DHH

The **D**ata-**H**andling-**E**ngine (**DHE**) is placed between computer and the Hybrid 5 board in the electronics chain. It is the link between the Software interface installed on the computer and the rest of the system. The DHE is responsible for generating the DHP system clock and controls the Hybrid 5 system with trigger signals. Those trigger signals are created with an 80 MHz clock by the DHE. Four trigger signals are created and sent to the Hybrid 5 board:

Frame sync: Serves to synchronise frames[2] and is the signal for the DHP to start integration from the beginning.

Trigger: Is the signal for the DHP to start sending data. The DHP only sends data, if it receives a trigger signal.

Veto: Is the signal to go into gated mode operation.

Reset: If the reset signal is sent the whole system is reset.

Those four signals are encoded in an 8 Bit Manchester code[3] and then transmitted to the DHP on a trigger line with 80 MBit/s. Thus, commands are transmitted with an effective speed of 10MHz. Hence, one expects a delay between command issue and completion. It is possible to program set sequences of trigger signal within the DHE. Length and timing of the different control signals within the DHE can be set in steps of the DHE reference clock. An adapter card for the DHE exists. This card allows it to read out the veto, frame sync and DHP trigger signals. In addition, the adapter card has a connector which allows for triggering of a laser with the DHE. This allows for programming of operation sequences in

[2] The package of data obtained after reading the full matrix out once is called frame.
[3] In Manchester encoding a 1 is encoded as 10 and a 0 as 01. This way the arriving signal is DC-balanced by default.

which the laser is shot with precise timing relative to the internal operations of the system.
The DHE features its own current source, with a scope of 248 µA which can be divided in 65000 steps. This current source can be used to inject currents into individual DCD channels. This gives the capability to observe the DCDs response to a known input current. Measurements using the DHE current source are used to optimise DCD parameters.
The DHE is part of the **D**EPFET **H**andling **H**ub (DHH). In the final experiment the DHH will contain multiple DHE, one for each module. The Hybrid 5 system used in this thesis only uses one DHE.

3.3 Software

The most important part of the Software framework are four **E**xperimental **P**hysics and **I**ndustrial **C**ontrol **S**ystem (EPICS) servers. These EPICS servers store the current state of the system. All parameters and voltages are stored inside **p**rocess **v**ariables (PV). The parameters are linked directly to the DHE, power supplies and the Hybrid 5 board. If any value is changed in the server, the corresponding value in the part of the system is changed accordingly! Communication with the servers can be done directly from the linux terminal with the commands **`caput`**, to change a variable, and **`caget`**, to read out a variable. As a more convenient solution a widget collection was developed in CS-Studio which provides a graphic interface to access all important system parameters. The EPICS PVs can also be modified within a python script. A collection of python scripts exists within the collaboration. These scripts range from basic building blocks for creating more advanced scripts to scripts which can optimise some parameters of the system automatically. The DCD optimisation done in this thesis relied on a script which can be configured to probe a freely selectable number of DCD channels with previously chosen voltages and parameters.

3.4 Laser scan

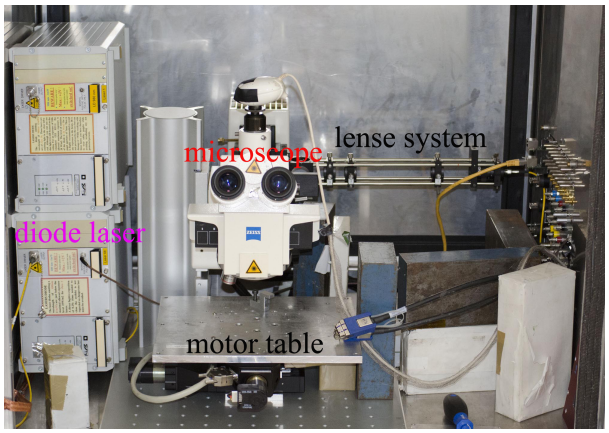


Figure 3.2: Content of the aluminium box.

With a laser scan position dependent measurements can be conducted. These scans can be used to verify the behaviour across large parts of the DEPFET matrix. The Hybrid 5 board is placed, with its back facing upwards, on top of a motor table. With the motor table position of the Hybrid 5 can be adjusted in steps of 0.5 µm. The laser is triggered with a pulse generator. Laser pulse length, intensity and repetition rate can be controlled from the pulse generator. The pulse generator is set to fire the laser

as long as an external trigger is present, which is provided by the DHE adaptercard.
The laser light is directed to a fiber coupler with optical fiber cables. From there a system of lenses directs the light into a microscope. The microscope focuses the laser beam on the DEPFET matrix. It is possible to view the laser beam with the microscope and confirm the position of the laser beam on the matrix.
Because DEPFET is sensitive enough to detect daylight the Hybrid 5 together with the laser, optical system and motor table are placed within an aluminium box of 1 m^3. The pulse generator remains outside to allow access to the laser configuration. Figure 3.2 shows a photo of the system. In figure 3.3 a sketch of the important components for the laser scan is shown. Measurements are started from the computer.

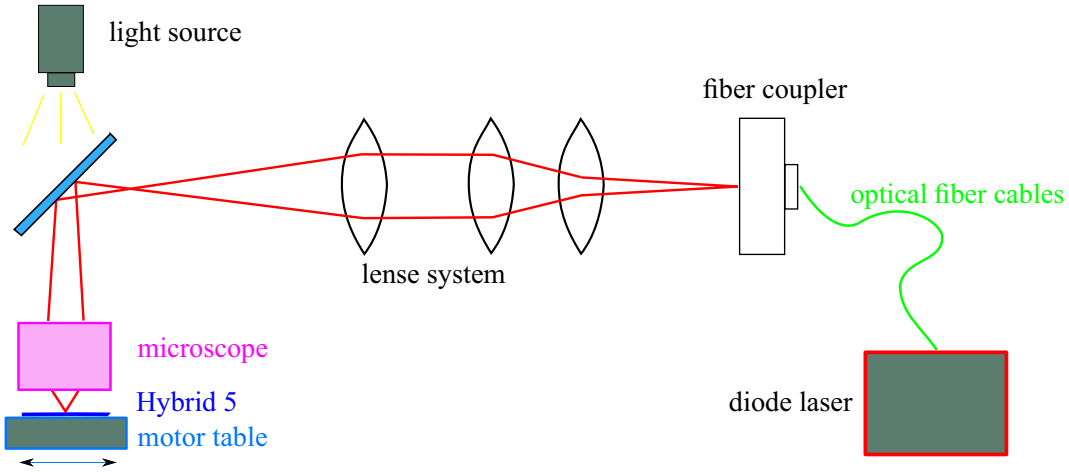


Figure 3.3: Sketch of the laser setup (derivative of [24]).

With the computer laser pulse length can be controlled via the DHE adapter and the illuminated position via the motor table.

CHAPTER 4

DCD-optimisation

This chapter will explain how analogue signals are converted to digital signals in the DCD. Important parameters are introduced which indicate the quality of an analogue to digital conversion. Finally the DCD performance is optimised using the introduced methods.

4.1 The Drain Current Digitizer readout ASIC

The Drain Current Digitizer (DCD) is mounted right next to the matrix and responsible for digitizing the output signal of the matrix. The design of the current electronics called DCDBpp, able to cope with the ensuing high radiation and with the required sampling rate of 50MHz, was created by Ivan Perić [23]. Former versions of the DCD were designed as cyclic ADCs, but the version used in this thesis was a pipeline ADC.
The pipeline ADC is sketched in figure 4.1 on the left and consists of blocks. Each of the blocks contains two Current Memory Cells (CMC) and two comparators. The current memory cells feature a reference current (R) which can be added or subtracted from the saved signal. DEPFET uses eight blocks in its DCD. Starting from block 0 the conversion is done as follows:

block 0: The analogue signal from the detector is saved in both CMCs. The comparators are connected to the first cell. One comparator compares the signal to a high threshold (h), the other one to a low threshold (l). If the signal is larger than the high threshold, then the reference current is subtracted from the signal in both cells. Consequently if the current is smaller than the low threshold, the reference current is added. Finally, if the signal is in between thresholds nothing is changed. After altering the saved currents with the reference current, the sum of both CMCs currents is written in the first cell in block 1. Then roughly 20ns later the second cell in block 1 is set to the same value. As for the comparators they switch their output signals to one once their condition is fulfilled. Thus the output codes are for input currents being higher than high threshold (h = 1, l = 0), smaller than low threshold (h = 0, l=0) and in between thresholds (h = 0, l = 1).

block 1: First the sum of both currents saved in the two CMCs from block 0 is saved in the first CMC of block 1. Then the same current is saved in the second CMC while the first CMC is evaluated using the two comparators. According to the results the reference current is added, subtracted or disabled in both CMCs. Finally the sum of both CMCs currents is written to the first CMC in block 2. After roughly 20ns the same current is written to the second CMC in block 2.

The procedure for blocks 2, 3 and so forth is the same as described for block 1. The resulting output signal after one block is displayed in figure 4.1 on the right. The final conversion result is D. It is obtained

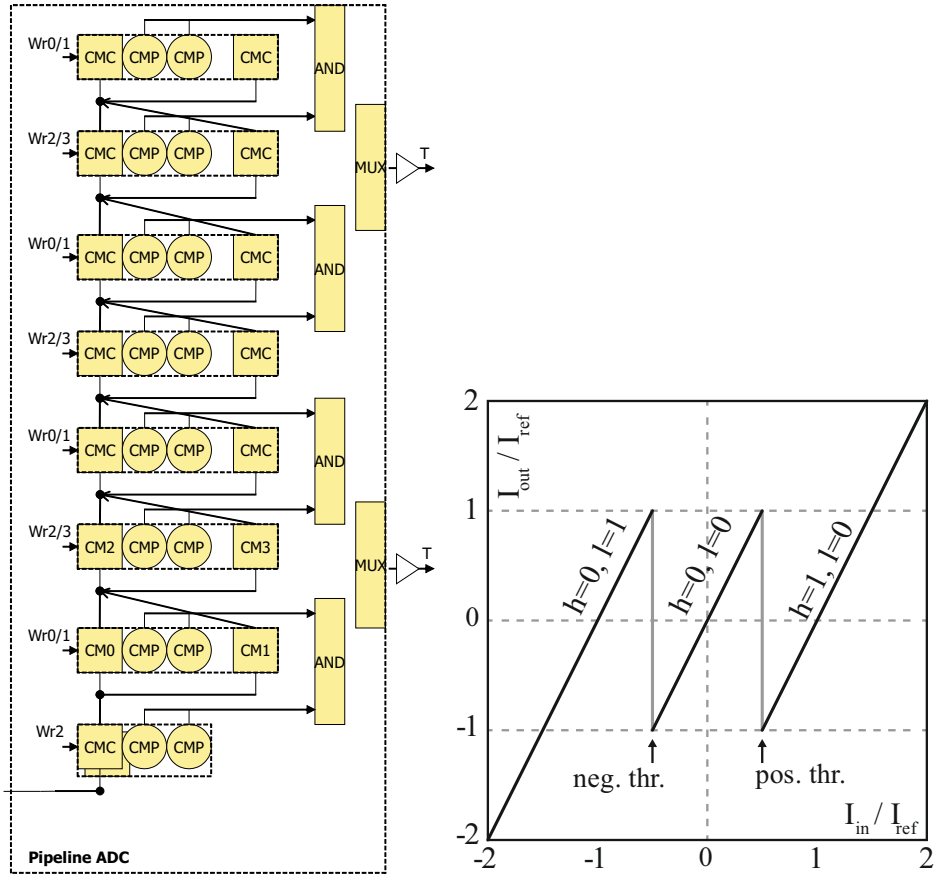


Figure 4.1: On the left sketch of the pipeline ADC used in this thesis[25]. On the right input signal after a single conversion stage [11].

as follows: $D = 2^7(h_7 - l_7) + \ldots + 2^0(h_0 - l_0)$. Therefore the analogue input signal is encoded in one of -255 to 255 digital values. Thus the digital precision of the ADC is given by the number of blocks plus one, with each block adding one bit to the output code and the way the final result is calculated adding another bit. The original signal can be reconstructed with $I_{signal} = D\frac{R}{128}$ Because further signal processing and data transfer is simplified by encoding the signal with a number of bits which is a power of two (2^x), the **L**east **s**ignificant **B**it (LSB) is discarded. Thus leaving eight bits within the range -127 to 127.

4.1.1 The CMC

The CMC is an essential part of DCDBv3. It is responsible for saving the sampled input signal from the DEPFET. The main components of the CMC are a capacitor, an amplifier and a transconductor. Figure 4.2 shows a circuit diagram of the CMC. To sample the signal from the DEPFET matrix Sw1 (switch 1) is closed and the input current I_{in} travels through node number 2 charging the capacitance C_f. The resulting voltage is stored by opening Sw1. The transconductor (TC in figure 4.2) keeps the voltage across C_f constant. The stored voltage is fed into the CMP via node 3. There it is compared with the high and low threshold. The high threshold is a current of 7 $\times$ IPSource, while the low threshold is 5 $\times$ IPSource. Depending on the result of the comparison a current of ($6 \times$ IPSource $\pm$ $2 \times$ IPSource) is added to the stored signal. The current IPSource is a current generated from the voltage VPSource. Then

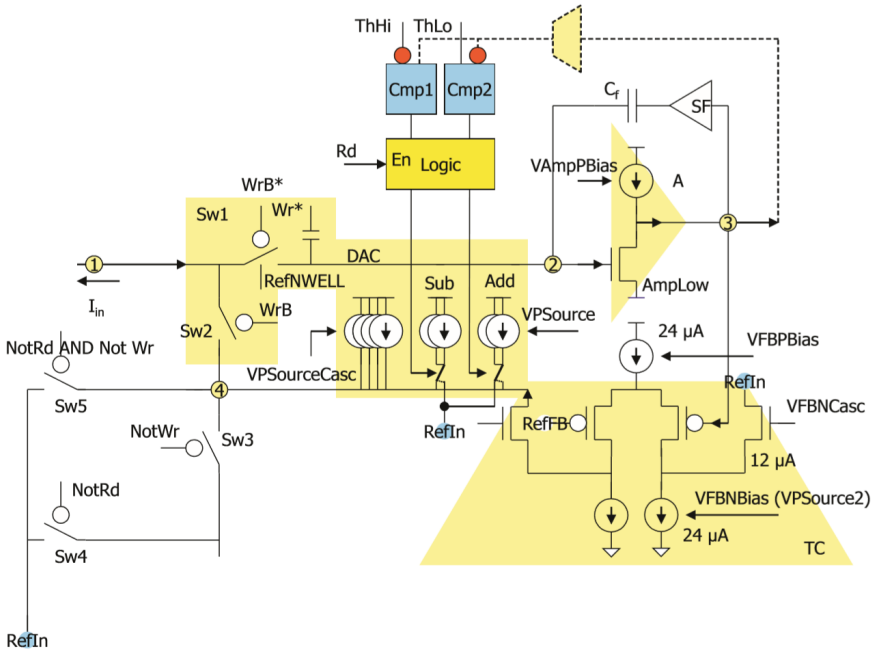


Figure 4.2: Sketch of the CMC used in the pipeline ADC [25].

the current is fed into the next stage of the ADC.
In chapter 4 the DCD will be optimised. The parameters which are optimised are IPSource, IPSource2, AmpLow and RefIn. These parameters fulfil the following functions:

IPSource: This parameter plays a central role in converting the analogue signal to a digital signal. The thresholds in the CMP and the reference current in the CMC are both derived from IPSource.

IPSource2: Is derived from VPSource2 and among the parameters responsible for the range of input signals the ADC can handle.

AmpLow: Is the ground potential for the transistor used in the amplifier of the CMC. Its main purpose is to lower power consumption by providing a higher ground potential.

RefIn: Is the bias voltage and serves as reference potential throughout all ADCs in a DEPFET module.

The IPSource and IPSource2 parameters are important because they influence the DCD performance strongly. But they can be configured for every DCD chip individually. In contrast the RefIn and AmpLow parameters are shared between all DCDs on one module. Thus settings are needed for this parameter which perform well for all DCDs on the ladder.

4.2 General analogue to digital conversion

When an analogue signal is converted to a digital signal, information is lost. The reason for this is limited precision. Analogue signals are a continuous range of signals and contain a theoretically unlimited amount of possible values, while a digital representation has a fixed set of discrete values. Thus each increase in digital code by one corresponds to a jump in analogue signal. This smallest increase in

analogue signal which can be described digitally is called LSB.
Ideally the LSB width would remain the same over the whole range of the analogue input signal. This would result in a transfer function with a staircase shape in which each step has the same width and height.
In a real transfer function step size does vary.

4.2.1 Differential nonlinearity

The **D**ifferential **N**on**L**inearity (DNL) describes the difference between real step width and ideal step width of one LSB. It is defined as:

$$\mathrm{DNL}(i) = \frac{\mathrm{V_{in}}(i+1) - \mathrm{V_{in}}(i)}{\mathrm{V_{ideal\ LSB}}} - 1$$

In this formula $\mathrm{V_{in}}(i)$ represents the input voltage belonging to the digital code i and $\mathrm{V_{in}}(i+1)$ the one belonging to the next larger digital code which occurs $(i+1)$. The variable $\mathrm{V_{ideal\ LSB}}$ corresponds to the ideal step width of one LSB. In an ideal analogue to digital converter (ADC) the DNL remains constant at 0 LSB, because the transition values are spaced one LSB apart. The digital output can take a total of 2^N values, where N is the number of bits available to encode the output in. The total amount of possible output values is called **f**ull **s**cale **r**ange (FSR). If the spacing of transitions is not equal 1 LSB, DNL is

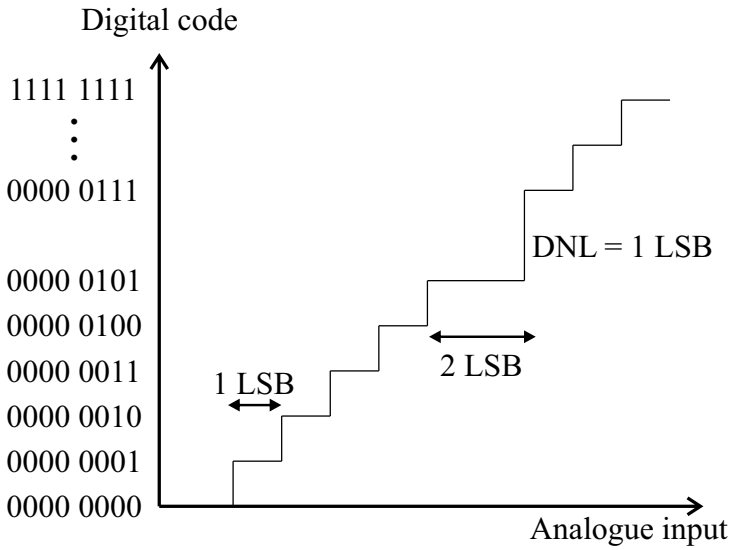


Figure 4.3: Analogue to digtial conversion and determination of DNL code.

different from 0 LSB. In figure 4.3 there is a jump from digital code 0000 0101 to 0000 0111. In this ADC the digital code 0000 0110 would never occur. A code which does not occur in the ADC output is called “missing code”. Consequently with one less code the FSR would be limited. At the value where the missing code occurs the DNL has a value of 1 LSB. If two digital codes where missing right after each other DNL would take a value of 2 LSB. Consequently DNL can be used to determine how many digital codes are missing and where those codes are missing.

4.2.2 Integral nonlinearity

The **I**ntegral **N**on**L**inearity (INL) describes the deviation of the transfer function from a straight line. There are different approaches how to calculate INL, in this thesis the best straight-line approach was used. In this approach a straight line is fitted to the transfer function. This allows to obtain information on the y-axis intercept (offset) and slope (gain). The INL is determined after both static offset and gain errors have been corrected. It can be calculated with:

$$\mathrm{INL(i)} = \left| \frac{\mathrm{V_{in}}(i) - \mathrm{V_0}}{\mathrm{V_{ideal\ LSB}}} - i \right|$$

In this formula $\mathrm{V_{in}}(i)$ represents the analogue value belonging to the digital code i and $\mathrm{V_0}$ the minimal analogue value belonging to the digital output code consisting of all zeros. The variable $\mathrm{V_{ideal\ LSB}}$ corresponds to the ideal step width of one LSB. Summing up all INL values gives the total deviation of the measured ADC curve to the ideal one.

4.3 Method of optimisation

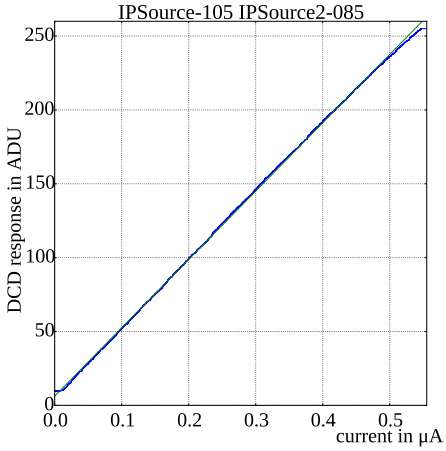


Figure 4.4: Transfer of a test current into digital code.

The figure of merit for analogue to digital conversion is the ADC curve, which is measured by feeding a set of known input currents into a DCD channel. Figure 4.4 shows an ADC curve which was measured for close to optimal settings. ADC curves are represented by a 2-dimensional histogram. The x-acis bins show the analogue input while the y-axis bins represent digital output code. ADC curves are tested for quality using four criteria:

Range: The range of ADC values, calculated as largest ADC value minus smallest ADC value contained in fit. This criteria detects limitations to FSR.

Linearity: Linearity of the ADC value's[1] rise with input current, calculated as $\chi^2_{\mathrm{reduced}}$. This is the representation of INL used in this thesis.

[1] ADC values are given in **a**nalogue **d**igital converter **u**nits (ADU).

Noise: How likely the same input current will give rise to the same ADC value, calculated as standard deviation of all ADC values measured at an input current.

Missing codes: Missing codes lead to jumps in the ADC curve. Missing codes are obtained from DNL. In the calculation a code only counts as missing if two or more consecutive ADC codes are missing.

DNL is calculated by summing up how often each ADC code occurs. The occurrence of each ADC code divided by the average occurrence of each ADC code gives the DNL. The calculation for missing codes only considers consecutive missing ADC codes, because a single missing ADC code would not impede operation. To not cut into signal the threshold is usually set more than one ADU lower than the lowest pedestal value of any pixel. Thus a single missing code would, if it was close to the value set as threshold, just function as an additional offset. However, multiple consecutive codes could mask an event which otherwise would be regarded as a hit. To prevent this case of consecutive missing codes an additional test is used. In this test the DNL is checked for large steps. A large DNL step occurs when a lot of successive ADC codes are missing. For the optimisations done in this thesis the test looks for any occurrence of three or more successive missing codes.

To determine the optimal set of IPSource, IPSource2, AmpLow and RefIn parameters multiple scans are conducted. The four parameters are divided into two parameter sets, in each scan one set is investigated. Meaning in each scan two parameters are measured against each other while the remaining parameters are set as constant. These two parameters are scanned over a number of channels. An optimal operating

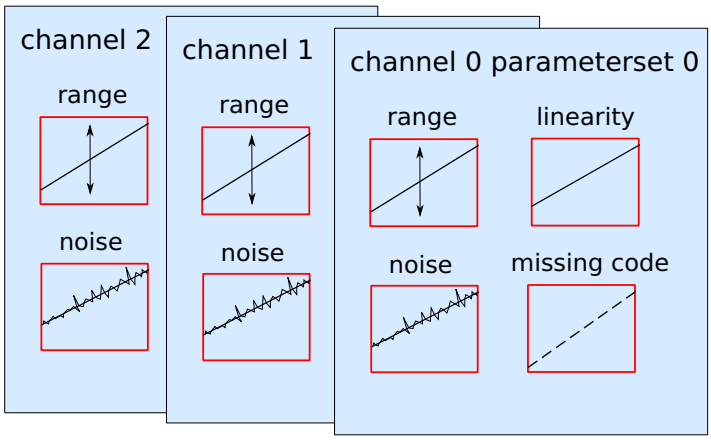


Figure 4.5: At each configuration a set of tests is conducted. The number of unsuccessful tests over all measured channels is calculated.

point is reached when as many channels as possible show acceptable curves. It is more important for as many channels as possible to work correctly than for individual curves to be as good as possible. Considering that a not functioning channel represents a whole area on the matrix which does not work correctly.
To determine the optimal operating point constraints are defined for each of these tests. The ADC curves of all tested DCD channels are evaluated. A test is counted as passed successfully by a channel if the constraints are met. If the constraints are set too strictly bad DCD channels will be unable to meet the requirements even with their optimal parameter set. If the criteria for passing a test are set too laxly, the optimisation is going to be dominated by bad channels and lots of configurations will show up as

optimal configuration. The values used for the optimisation in this thesis were obtained looking at past measurements, estimating up to what degree we could expect bad channels to perform.
Once one has set a standard for the four tests on range, linearity, noise and missing codes one counts for each combination of parameters how many tests were not passed successfully across all channels (compare to figure 4.5). The algorithm to calculate the optimal operating point searches for the configuration with the lowest amount of tests not passed. Then it checks all parameter combinations to check if there was a test with similarly good results. If there are multiple parameter combinations with close to optimal results, configurations whose parameters are close to the optimal configuration in parameter space are also factored in. These neighbouring configurations are weighted by distance from the ideal configuration. Finally the optimal operating point is the point which passed the most tests or, if there is multiple good points, the one which has the best surroundings. Like the consideration of similar voltages/currents close to the optimal configuration point, the software was designed to also allow additional criteria. One additional criteria which was used for all optimisations in this thesis is additional weight. It is used if all measured DCD channels did not pass a certain test. This weight serves as an insurance to warrant that this configuration is not chosen as the optimal operating point. The criteria used for the tests are summed up in table B.2.

4.4 Measurements

After defining the method for optimisation (see section 4.3) the next step is to approach the optimal configuration point with successive measurements. For this thesis scans were done in the IPSource-IPSource2 set and in the AmpLow-RefIn set. The methodology was an iterative approach:

1. Conduct a 2D scan for one parameter set.
    - Set the parameters which are not scanned to the last obtained optimal values and keep them fixed for the duration of the scan.
    - Measure the two parameters in the parameter space in reasonable boundaries.
    - Obtain optimal values for the two parameters.
2. Conduct a 2D scan in the next parameter space.
    - Set the parameters which are not scanned to the last obtained optimal values and keep them fixed for the duration of the scan.
    - Measure the two parameters in the parameter space in reasonable boundaries.
    - Obtain optimal values for the two parameters.
3. Repeat until the values for all the parameters converge or the number of errors hits 0.

For the first scan, as there weren't any measured optimal points yet, the parameters which were not scanned were all set to standard values. Standard values are the ideal values of the last DCD which was optimised. The standard values used in this measurement were obtained during the irradiation campaign in Karlsruhe and they represent stable values which could produce good results throughout the whole irradiation campaign! How these values were obtained and more detailed analysis will be provided in chapter 5.

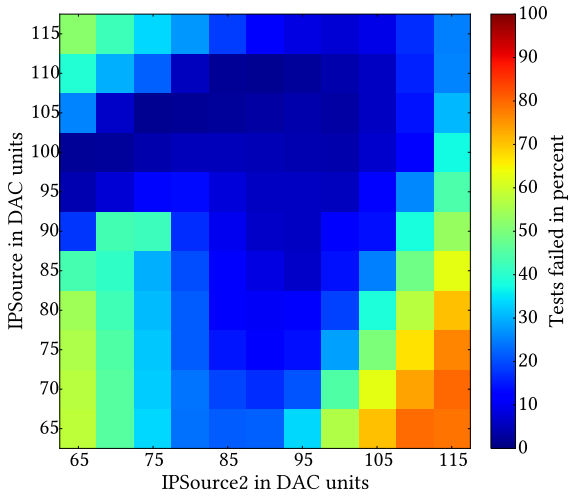


Figure 4.6: Scan in IPSource-IPSource2 parameter space. At each configuration a set of tests is conducted. The number of unsuccessful tests over all measured channels is calculated.

4.4.1 First parameter sweep: IPSource vs IPSource2

The parameter set scanned in the first scan is IPSource- IPSource2. For this scan IPSource is varied between 65 and 115 DAC units in 5 DAC units steps. IPSource2 is varied between 65 and 115 DAC units in 5 DAC units steps. The range for the scan of these parameters was chosen by considering the position of the optimal operating point measured for different DCDs in the past. The optimisation is displayed in figure 4.6. The electronic optimisation calculates the optimal point as:

IPSource = 105 DAC units

IPSource2 = 85 DAC units

Figure 4.6 shows that the DCD does not work correctly, if IPSource or IPSource2 are chosen too small. Looking at single curves for the bad configurations one observes missing codes. This is displayed in figure 4.9.
If IPSource or IPSource2 are set to large values the ADC curve displays missing codes as shown in figure 4.8.
If IPSource is set to 90 DAC units and IPSource2 is set between 70 and 75 DAC units, strong noise is seen across all channels. This heavy noise is displayed in figure 4.11.
Finally, if one of the parameters IPSource and IPSource2 is too large and the other too small the result is a limited range, refer to figures 4.7 and 4.10 for visualisation.
In conclusion if one or both of the two parameters IPSource or IPSource2 are chosen too large or too small the resulting curves no longer satisfy the standards of the tests. The DCD works best if both IPSource and IPSource2 are close but not the same in value. The optimal configuration is displayed in figure 4.12.

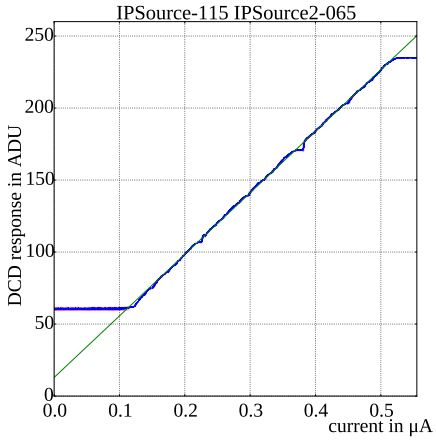


Figure 4.7: Large IPSource and small IPSource2 result in a limited range and missing codes.

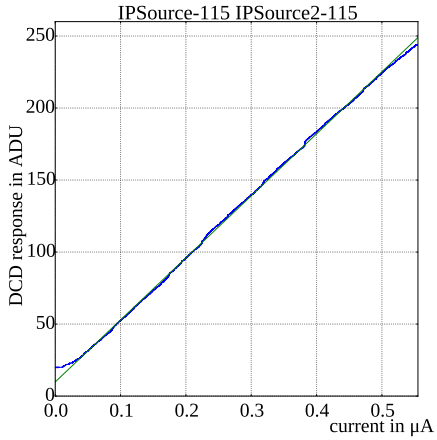


Figure 4.8: Large IPSource and large IPSource2 result in missing codes.

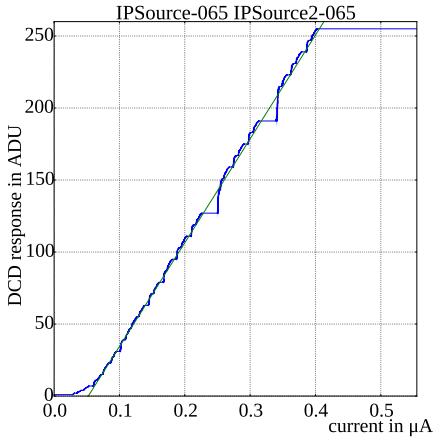


Figure 4.9: Small IPSource and small IPSource2 result in missing codes.

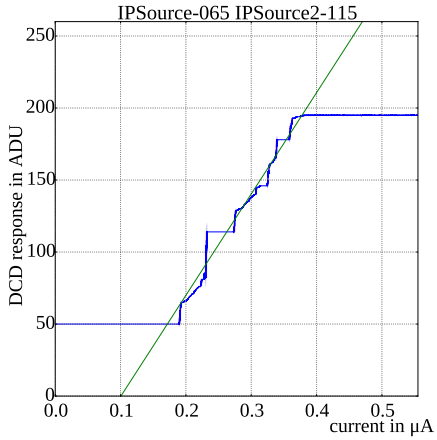


Figure 4.10: Small IPSource and large IPSource2 result in a limited range, nonlinearities and missing codes.

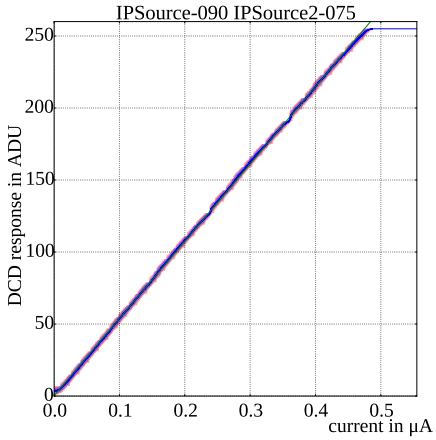


Figure 4.11: At certain voltages the noise increases drastically.

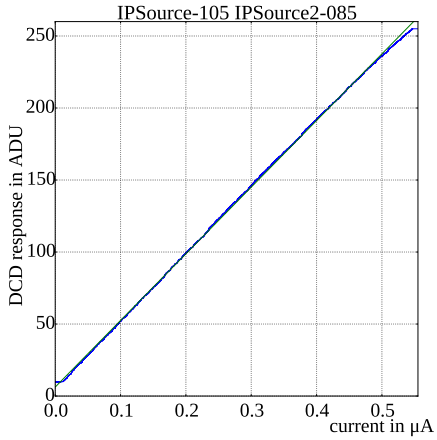


Figure 4.12: At the optimal operating point there are no major problems.

4.4.2 Second parameter sweep: AmpLow vs RefIn

The second parameter space to be scanned is the AmpLow-RefIn parameter set. For this scan the AmpLow voltage is varied between 100 and 500 mV in 50 mV steps. The RefIn voltage is varied between 800 and 1 000 mV in 25 mV steps. These voltages are chosen by considering the position of the optimal operating point determined in previous DCD optimisations. The constraints on the RefIn voltage were set quite tight. The ADC performance is expected to not depend strongly on AmpLow and RefIn. The reason being AmpLow and RefIn are reference potentials which do not play a major role in converting the signal from analogue to digital. Thus the parameter restraints were chosen too tight for curves with strong errors caused by a bad RefIn voltage to appear. The parameter restrains were chosen tight to allow for quick scan times. The optimisation is displayed in figure 4.13. IPSource and IPSource2 were set to the optimal values obtained in the previous scan. Again, the bottom right part of this figure shows the

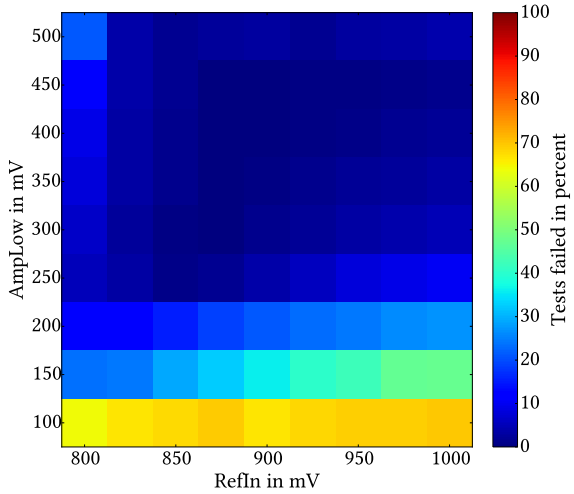


Figure 4.13: Scan in AmpLow-RefIn parameter space. At each configuration a set of tests is conducted. The number of unsuccessful tests over all measured channels is calculated.

summary of all tests across all measured channels. The software calculates the optimal point as:

$$\text{AmpLow} = 400\ \text{mV}$$
$$\text{RefIn} = 900\ \text{mV}$$

Figures 4.14 to 4.17 show different extreme cases. As reference voltages one would not expect strong dependencies between the two parameters. But some dependencies are visible in figure 4.13. If AmpLow and RefIn are chosen as large values this results in a slightly limited range of the ADC curve and an increase in noise (see figure 4.15).
If AmpLow and RefIn are chosen as small values this results in bad linearity of the ADC curve and missing codes (see figure 4.16).
If RefIn is large and AmpLow is small then noise increases (see figure 4.14).
Finally if RefIn is small and AmpLow is large missing codes appear (see figure 4.17).
The optimal configuration is displayed in figure 4.18.

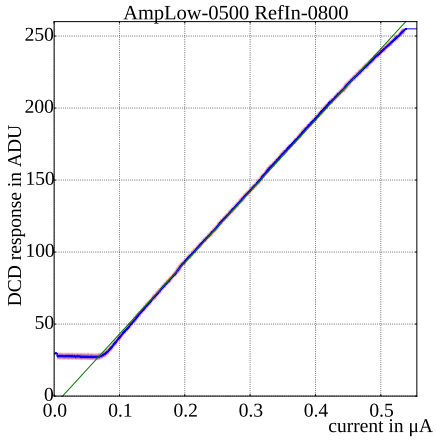


Figure 4.14: Small RefIn and large AmpLow result in high noise.

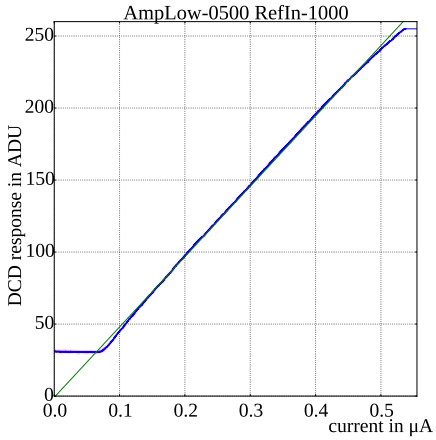


Figure 4.15: Large RefIn and large AmpLow result in slightly limited range and increased noise.

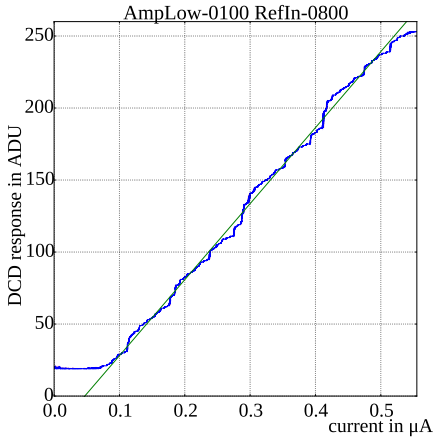


Figure 4.16: Small RefIn and small AmpLow result in missing codes.

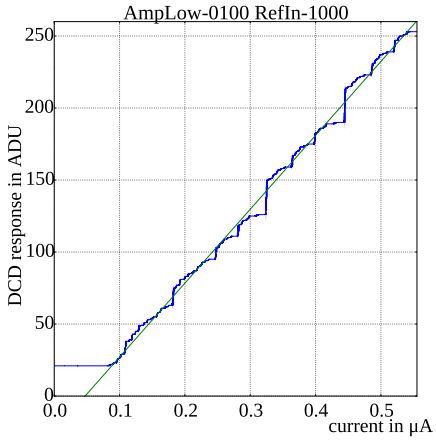


Figure 4.17: Large RefIn and small AmpLow result in strong occurrences of missing codes.

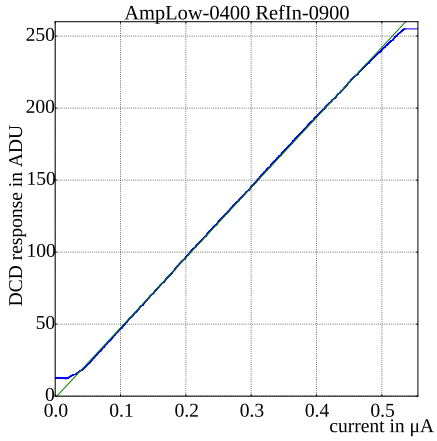


Figure 4.18: At the optimal operating point there are no major problems.

4.4.3 Iterative parameter scan

The IPSource-IPSource2 and AmpLow-RefIn parameter sets are scanned alternatingly. Also for these scans IPSource is varied between 65 and 115 DAC units in 5 DAC units steps. IPSource2 is varied between 65 and 115 DAC units in 5 DAC units steps. For the AmpLow-RefIn scan the AmpLow voltage is varied between 100 and 500 mV in 50 mV steps. The RefIn voltage is varied between 800 and 1 000 mV in 25 mV steps. The two optimisations are displayed in figures 4.19 and 4.20. Using the electronic

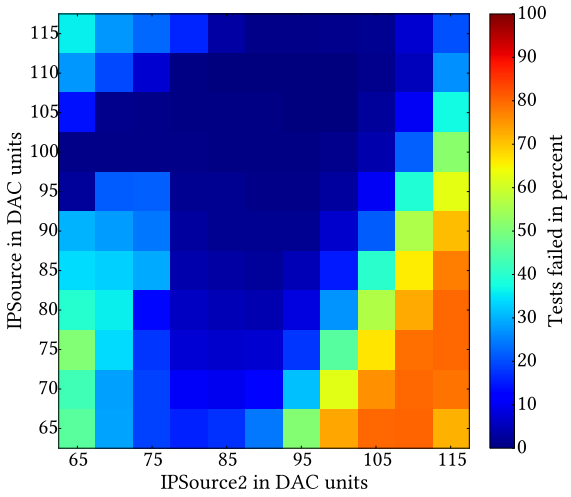


Figure 4.19: Scan in IPSource-IPSource2 parameter space. AmpLow was set to 400 mV and RefIn to 900 mV.

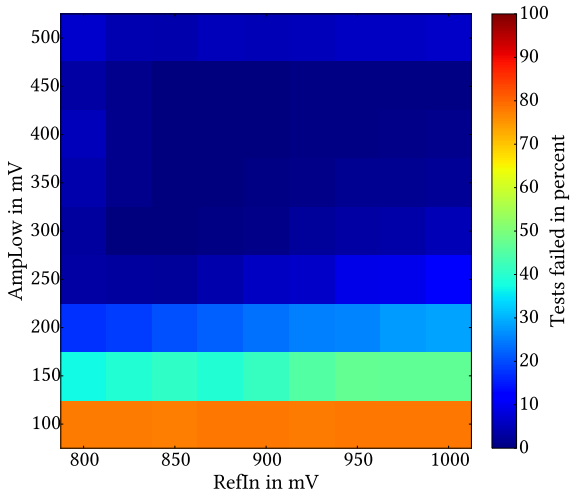


Figure 4.20: Scan in AmpLow-RefIn parameter space. IPSource was set to 105 DAC units and IPSource2 to 95 DAC units.

optimisation on these two scans the optimal points are calculated as:

$$\text{IPSource} = 105 \text{ DAC units}$$
$$\text{IPSource2} = 95 \text{ DAC units}$$

$$\text{AmpLow} = 400 \text{ mV}$$
$$\text{RefIn} = 875 \text{ mV}$$

Both measurements show multiple points where all tests were successfully passed. The optimal configuration of the IPSource and IPSource2 parameters showed no errors. The configurations directly bordering to this configuration showed any errors in at most 3 (of 64 measured) channels. Making this configuration very stable. In addition, with RefIn voltages between 800 and 1 000 mV and AmpLow voltages between 250 and 450 mV the quality of the analogue to digital conversion is good. Thus a large parameter space is available for optimal settings for RefIn and AmpLow.

CHAPTER 5

Irradiation campaign

In the Belle II experiment the PXD will be placed close to the interaction point. Thus the PXD will face strong x-ray radiation. Both the DEPFET sensor the ASICs will need to withstand irradiation of up to 2 Mrad/year (in Si units 20 kGy/year)[20]. It is of great interest how irradiation will influence the ideal working point of the ASICs. Ideally constant tweaking of the operation parameters should be prevented. A set of parameters with which the ASICs perform satisfactorily independent of irradiation should be found. In the March 2016 irradiation campaign in Karlsruhe the DEPFET ASICs were irradiated up to 4 Mrad (in Si units 40 kGy) [26]. This chapter will analyse the behaviour of the DCD under irradiation, using the measurement data from the Karlsruhe campaign. Unless scanned the parameters were set to:

AmpLow: 300 mV

RefIn: 950 mV

IPSource: 90 DAC units

IPSource2: 90 DAC units

The rest of the parameters was set to standard values. In the course of the irradiation campaign the device was irradiated first, up to a certain point. Then the parameters AmpLow, RefIn, IPSource and IPSource2 were checked for their optimal value. Also the response of all the channels was measured. To solely observe effects related to the ASICs, no matrix was connected in the Hybrid 5 used for the measurements of this chapter[1].

5.1 Optimising the AmpLow and Refin parameters

The AmpLow voltage is varied between 100 and 600 mV and the RefIn voltage between 800 and 1 200 mV. The step size and number of channels measured does vary between scans, which is due to time constraints. The measurement data for AmpLow and RefIn is evaluated using the same method which was used in chapter 4. The ideal operation point can be determined when consulting figure 5.1. The figure shows the percentage of tests which were not passed. So a high percentage represents a bad set of parameters. When the DCD is unirradiated there is a wide range of voltages which allow good performance. But as soon as the DCD is irradiated the working area becomes much smaller. As soon as irradiation is increased to 20 kGy or larger there is no configuration where all channels operated

[1] ID number of the Hybrid 5 is H5.005.

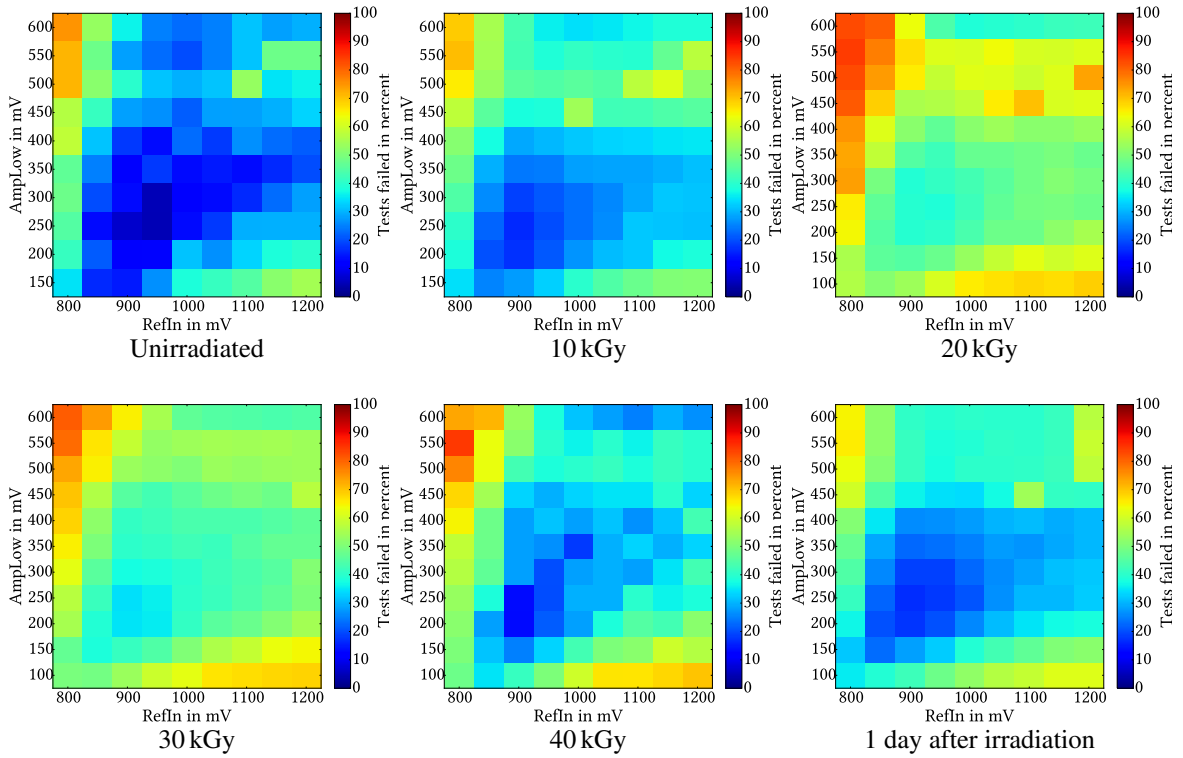


Figure 5.1: Ideal operation point in AmpLow-RefIn plane after different doses. The percentage of tests which were not passed is listed. Blue areas represent good configurations.

flawlessly in all tests. This is in part because the DCD performs worse across all channels with irradiation, but also because in this particular DCD some channels stopped working completely. The cause were communication problems between DCD and DHP, due to failing data links. For a dose of 30 kGy, the DCD does not perform worse than it does for a dose of 20 kGy. When irradiated up to 40 kGy, the DCDs performance increases compared to the measurement at 30 kGy. This behaviour is expected for the type of surface damage the DCD recives and was already observed in previous measurements [20].
The purpose of the tests which are applied to the measured data is to narrow down the voltages the DCD performs best at. Thus the DCD not passing 30 % of the tests does not mean it will not work 30 % of the time. Nevertheless looking at the voltages the DCD performs best at for each irradiation dose, one is able to define voltage ranges in which the DCD performs well for all doses. Varying the RefIn voltage between 850 and 1 000 mV and the AmpLow voltage between 200 and 350 mV gives good results for all doses. After irradiating the DCD up to 40 kGy and then waiting for one day the performance of the DCD is close to the level it was at when the DCD was not yet irradiated.
As AmpLow and RefIn voltage will be shared between all DCDs on one module in the final experiment this working area should overlap with the one measured in chapter 4 in figure 4.20. There is sufficient overlap between the two DCDs and to operate close to optimal settings the RefIn voltage should be between 850 and 1 000 mV and the AmpLow voltage between 250 and 350 mV.

5.2 Optimising the IPSource and IPSource2 parameters

The IPSource parameter is varied between 50 and 120 DAC units and the IPSource2 parameter also between 50 and 120 DAC units. As the AmpLow-RefIn optimisation and the IPSource-IPSource2 optimisation were run right after each other, between irradiation steps, the same time constraints apply. Thus step size and number of channels measured does vary between scans. The measurement data for IPSource and IPSource2 is evaluated using the same method which was used for the AmpLow and RefIn measurement and in chapter 4. Figure 5.2 shows the performance of the DCD for different

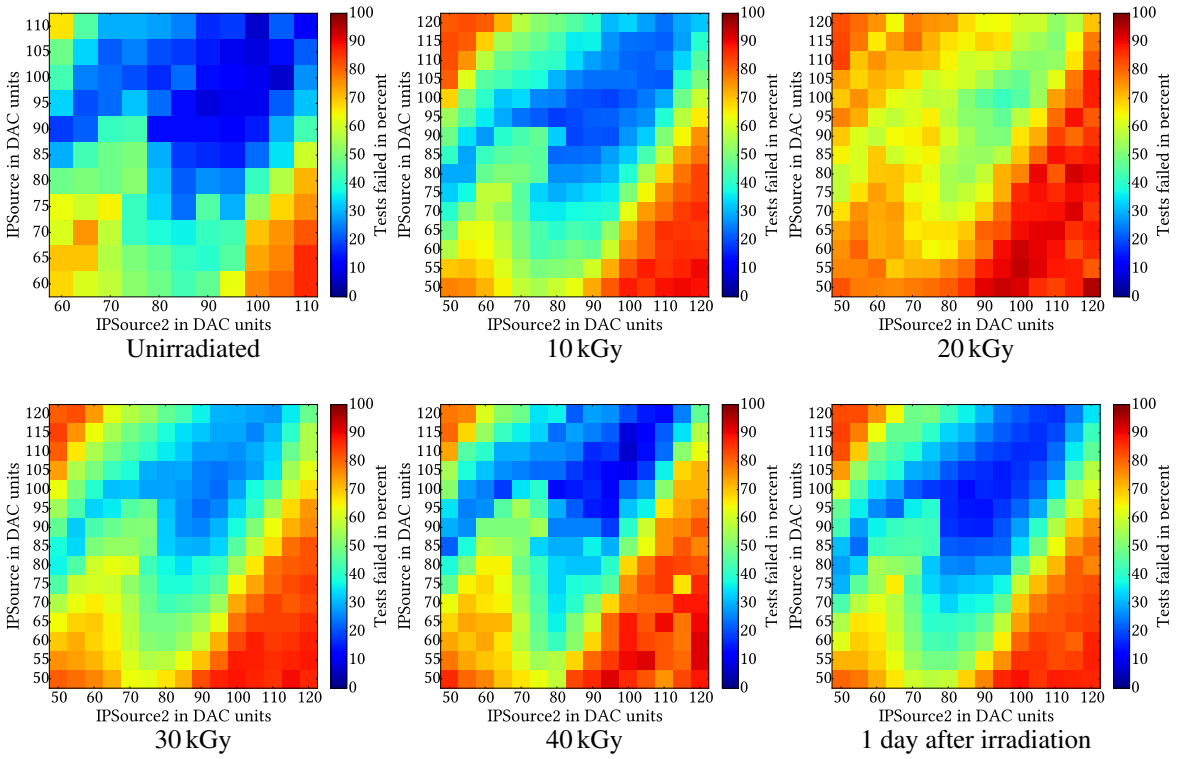


Figure 5.2: Ideal operation point in IPSource-IPSource2 plane after different doses. The percentage of tests which were not passed is listed. Blue areas represent good configurations.

doses, depending on IPSource and IPSource2. The unirradiated DCD performs best if both IPSource and IPSource2 are between 85 and 105 DAC units. When the DCD is irradiated the DCD performance worsens with increasing irradiation up to a dose of 20 kGy. When the DCD is irradiated to a dose of 30 kGy or more it starts to recover. After bringing the DCD back to Bonn it recovers to the point of performing similar to an unirradiated DCD after a day.
For optimal performance IPSource and IPSource2 should be larger than 80 DAC units. At the same time there should not be a difference larger than 5 DAC units between the two parameters. A suggestion for an optimal operation point would be setting IPSource to 100 DAC units and IPSource2 to 95 DAC units.

5.3 Continuous irradiation

For the last irradiation step from 30 kGy to 40 kGy a number of channels is monitored during irradiation. At set time intervals ADC curves are taken for these channels during irradiation. From these ADC curves

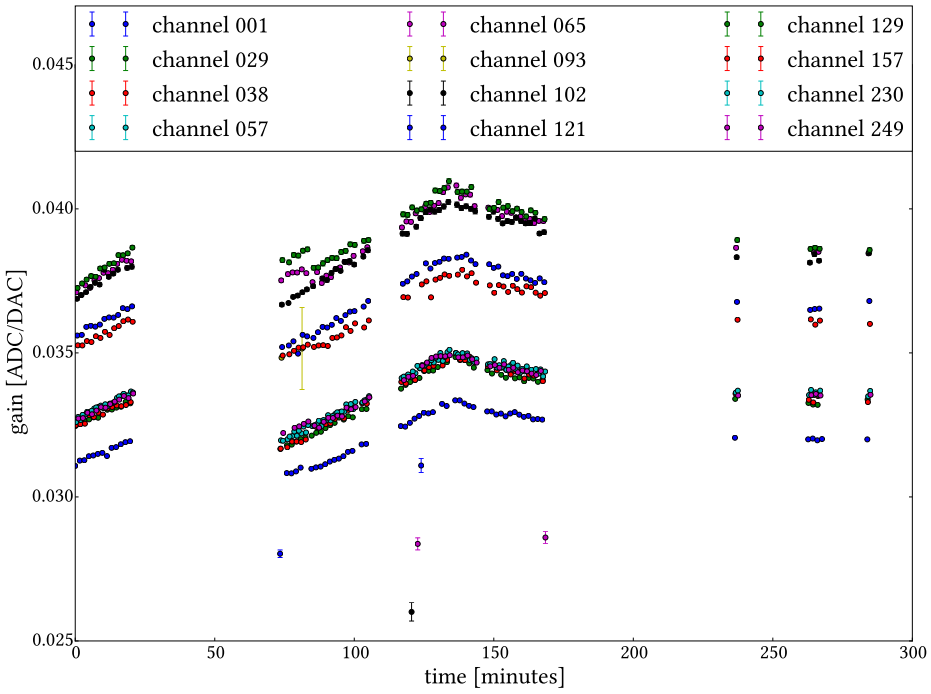


Figure 5.3: Gain measured against time. The DCD is irradiated during the measurements.

gain and noise is extracted for each channel. Figure 5.3 shows how gain changes over time. Up to 25 min gain increases. Then the system was restarted. At 75 min the first measurements after the restart are conducted. Some of the radiation damage to the DCD was already healed by annealing at that point [22]. Hence the gain is slightly lower than before the restart. After 140 min the DCD is no longer irradiated. In conclusion gain increases with increasing dose, after irradiation stops gain decreases over time. Thus an increase in gain with increasing radiation can be expected for the final experiment, as the dose absorbed in in this measurement is equal to half a year of operation at the Belle II experiment.

Figure 5.4 shows the same measurements for the same channels over time. For this figure noise was extracted from the measured ADC data. There is no strong increase of noise across the observed doses visible. Noise does increase by 0.01 to 0.02 ADU, but does not decrease after irradiation stops. The cause for this increase could lie in not perfectly stable temperatures. With thresholds set at 4 ADU an increase in noise at this level is unlikely to hinder the experiment. Consequently, considering the radiation levels of 20 kGy/year at the Belle II experiment, a strong increase in noise of the ADC data which stems from the DCD is not expected.

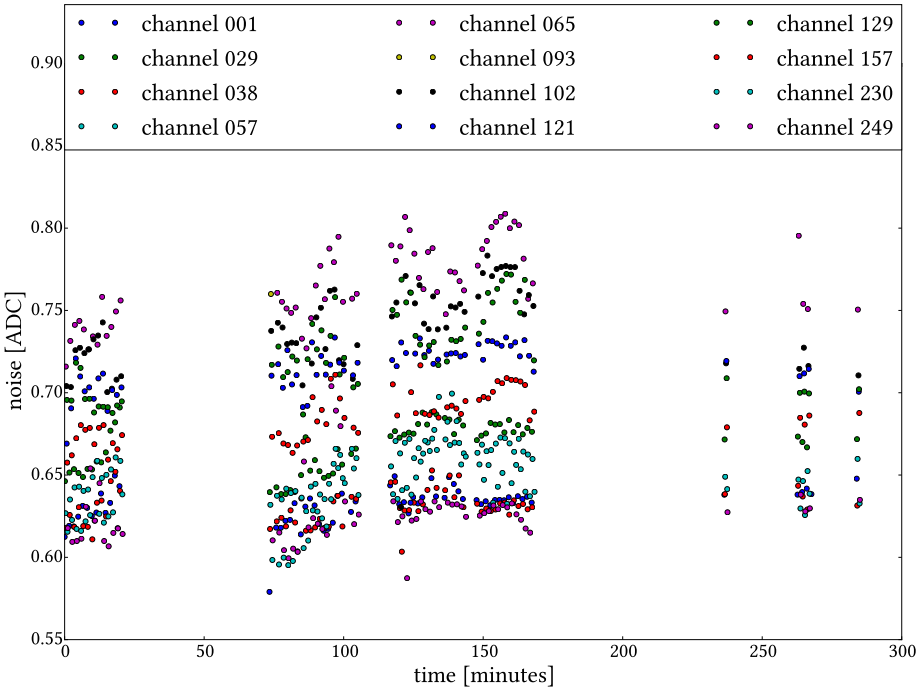


Figure 5.4: Noise measured against time. The DCD is irradiated during the measurements.

CHAPTER 6

Gated mode

The goal of the measurements in this section is to understand and verify different aspects of gated mode operation. In section 6.1 the different readout cycles for normal and gated mode operation are explained. Furthermore the system internal timings that are relevant for gated mode operation are measured.
In section 6.2 the dead time of the detector is determined. Moreover the ability of gated mode to retain the charge stored within the internal gate is quantified. In addition the ClearLow, ClearHigh and GateOff parameters are optimised for gated mode performance.

6.1 Oscilloscope measurements

Before the Hybrid 5 board is placed under the laser, the functionality of the Switcher sequences needs to be confirmed and the internal timings measured. To achieve this a Hybrid 5 testboard without matrix is used. The identification of that Hybrid 5 is H5.005. The last two gates of the Switcher were probed and displayed on an oscilloscope.

6.1.1 Normal readout

The first measurement probes the normal readout from DEPFET it is displayed in figure 6.1. In normal readout the signal is sampled first. Then the internal gate and bulk are cleared of charge by applying a large voltage to the clear contact. Finally clear voltage is lowered to off state and then gate voltage is raised to off state. In conclusion DEPFET behaves as expected in this measurement. The oscillation of the voltages is due to incorrect termination impedance. The whole process of reading out and clearing the four rows of pixels (one gate) takes roughly 100 ns. With reference clock speed set to 76.33 MHz. Slower clock speeds would result in longer readout time.

6.1.2 Gated mode operation

Remeasuring the same gate for gated mode operation with readout one obtains the picture displayed in figure 6.2. In gated mode operation with readout the clear voltage is high at all times, while the gate voltage is in off state. Thus charge is removed from the bulk, but not the internal gate. Only when a gate is read out does the clear voltage switch back to off state. During readout the clear voltage stays low. Thus no clear is applied and internal gate and bulk retain their charge. Just looking at the voltages applied gated mode with readout works correctly.

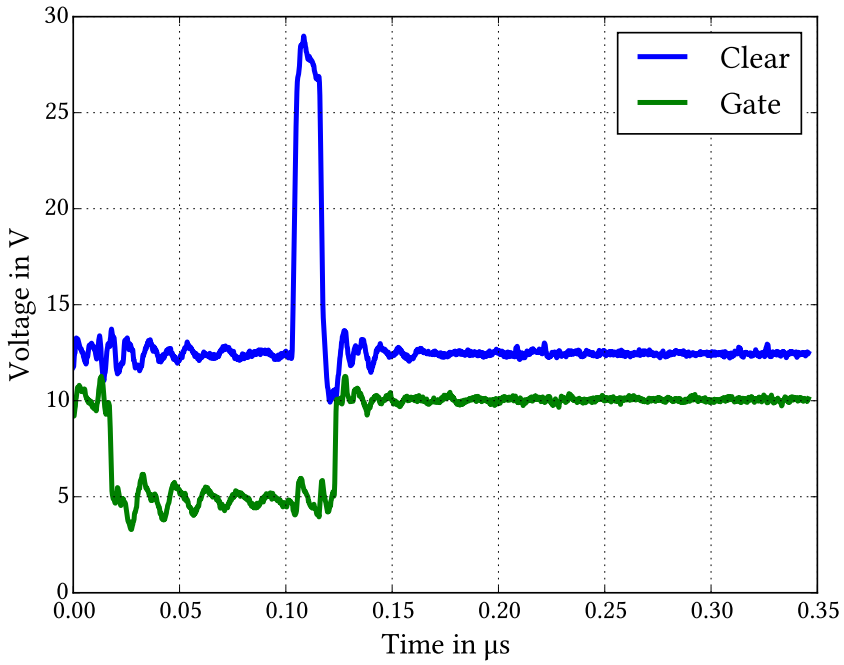


Figure 6.1: Normal readout of one gate in DEPFET.

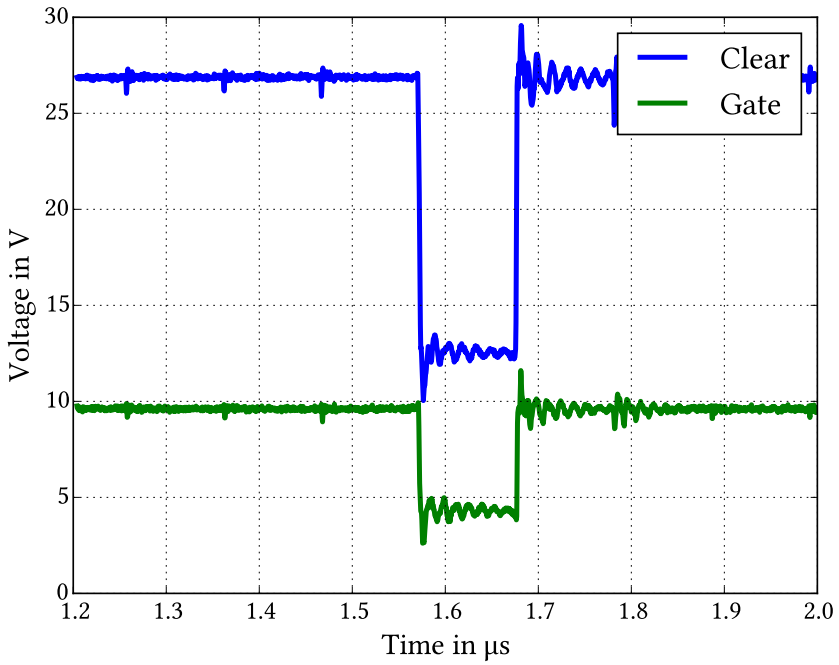


Figure 6.2: Gated readout of one gate in gated mode with readout for DEPFET.

6.1.3 Time required to read out one gate

A more precise measurement of the time one gate is active is displayed in figure 6.3. The switcher

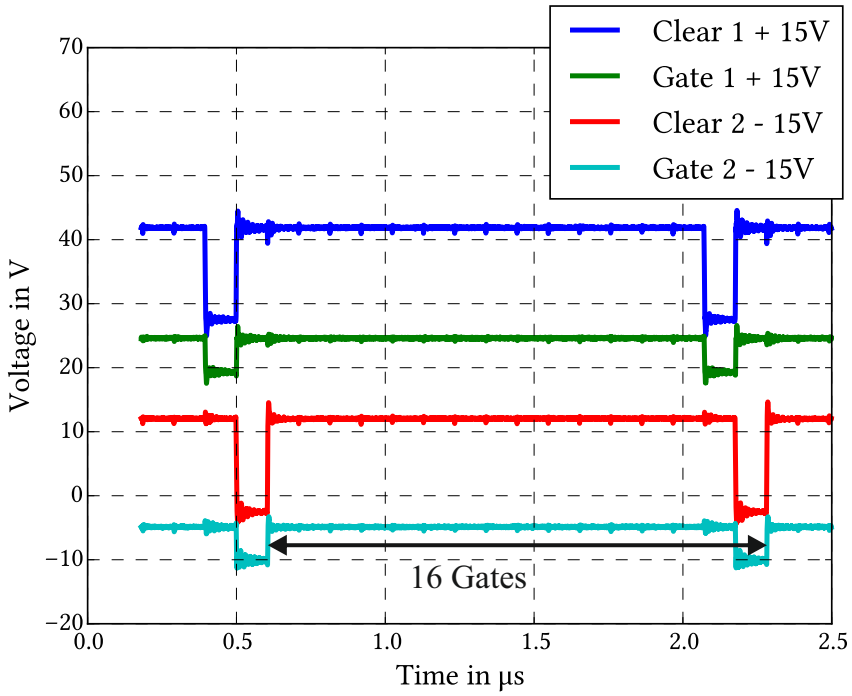


Figure 6.3: Output signal of the last two gate and clear lines of the Switcher. Before a gate is read out a second time the other 15 gates are read out.

switches on the gate voltage of the gates in order. After reaching the end of the matrix it resets and starts again from the beginning. The Hybrid 5 matrix used in this thesis has 16 gates. Consequently the time between a certain gate being switched on (or off) for the first time to that same gate being switched on (or off) again, is 16 gates long.
In figure 6.3 this behaviour was used to determine how long it takes to read out one gate. For this measurement the time interval between two points with the same voltage on the rising edge was determined for Gate 1 and Gate 2 voltage. The rise time of the oscilloscope used (model: MSO4104B) is 350 ps [27]. This is also a worst case estimate on the error of the measurement. In addition, to minimise the reading error, the picture was zoomed in on the rising edges. The results are:

Gate 1:

$$(500.3 \pm 0.4)\,\text{ns} \xrightarrow{(1\,677.0 \pm 0.5)\,\text{ns}} (2\,177.3 \pm 0.4)\,\text{ns}$$
$$\Rightarrow \Delta T_{1\,\text{Gate}} = (104.81 \pm 0.03)\,\text{ns}$$

Gate 2:

$$(604.9 \pm 0.4)\,\text{ns} \xrightarrow{(1\,677.0 \pm 0.5)\,\text{ns}} (2\,281.9 \pm 0.4)\,\text{ns}$$
$$\Rightarrow \Delta T_{1\,\text{Gate}} = (104.81 \pm 0.03)\,\text{ns}$$

It takes (1 677.0 ± 0.5) ns from the end of the first complete matrix readout cycle to the end of the second complete readout cycle for both gates. Dividing that number by 16 to obtain the time it takes to read out one gate gives (104.81 ± 0.03) ns. Summing up the result for both gates one obtains a readout time of (104.81 ± 0.03) ns/gate[1]. To make sentences which contain the time it takes to read out N gates (with N being a natural number) more readable, this thesis will call this time interval just "N gates" in short. The DHE reference clock was set to (76.33 ± 0.01) MHz. In theory this would result in a gate length of (104.81 ± 0.02) ns [28].
During the more complex gated mode measurements with a laser the setup which was used, was unable to maintain a permanent link with the DHP using the (76.33 ± 0.01) MHz clock[2]. Without a link to the DHP, data is not transmitted to the computer. To be able to conduct measurements involving the DHP and the matrix the reference clock is slowed down. The clock is slowed down enough to ensure any potentially observed error is due to gated mode not working correctly and not caused by communication errors. The clock frequency of 62.5 MHz is well tested with the Hybrid 5 board used in this thesis, thus

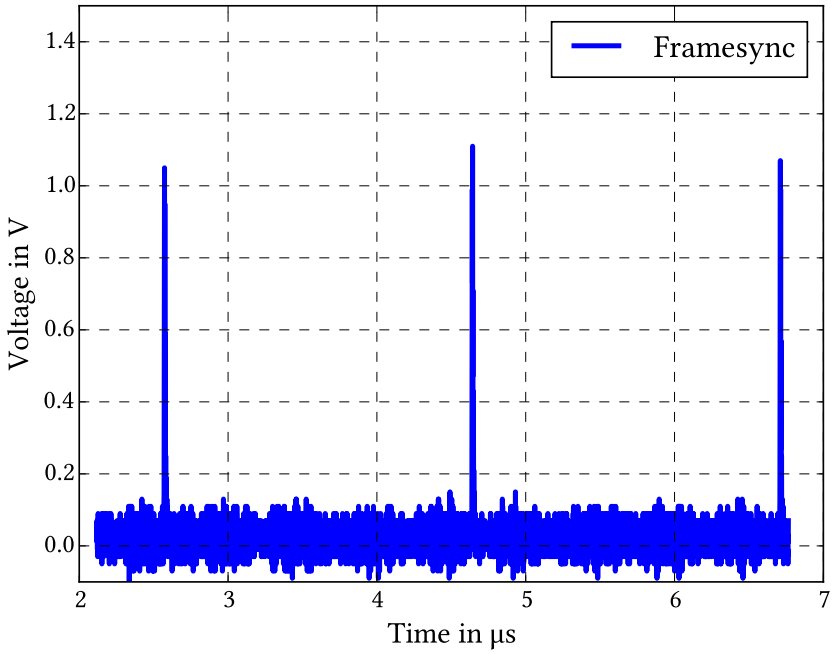


Figure 6.4: Framesync is sent every 16 gates. Thus 32 gates are between the two outermost framesync signals.

this frequency is chosen. As the readout time measurements with the faster clock speed proved successful, the measurement is repeated with the slower clock speed to determine the exact clock frequency.
To determine the exact clock frequency the framesync signal shown in figure 6.4 is probed. The Hybrid 5 board has a connector to probe the framesync signal, as it is being transmitted from the DHP to the Switcher. Thus compared to probing gate and clear voltages this has the advantage that the time to read out one gate can be measured directly on the Hybrid 5 which was used for later gated mode measurements. The framesync signal is sent once at the start of every readout cycle. Thus it is sent every 16 gates. Using

[1] The error remains unchanged as it stems from the oscilloscope rise time and is systematic.
[2] The used Hybrid 5 had the identification H5.007.

the time difference between framesync signals to calculate the time it takes to read out one gate gives:

1. framesync to 3. framesync:

$$(2\,572.9 \pm 0.4)\,\text{ns} \xrightarrow{(4\,137.9 \pm 0.5)\,\text{ns}} (6\,710.8 \pm 0.4)\,\text{ns}$$

$$\Rightarrow \Delta T_{1\,\text{Gate}} = \frac{(4\,137.9 \pm 0.5)\,\text{ns}}{32\,\text{gates}} = (129.31 \pm 0.02)\,\text{ns/gate}$$

With the slower clock one gate is (129.31 ± 0.02) ns long. Using this number the time equivalent of 1 GCK (short for one reference clock cycle) can be calculated using:

$$\frac{\text{Time to read out one gate}}{\text{Number of GCK in one gate}}.$$

Hence one clock cycle is $(129.31 \pm 0.02)\,\text{ns}/8 = (16.164 \pm 0.003)$ ns long and results in a clock speed of (61.86 ± 0.01) MHz.

6.1.4 DHE memory timing

When programming the DHE one is able to influence four different signals. While the DHE trigger signal is for internal use within the DHE, the DHP trigger and veto signals are sent to the DHP and the laser signal to the laser.
To measure possible delays between the programmed signals, all four signals are set to start at memory

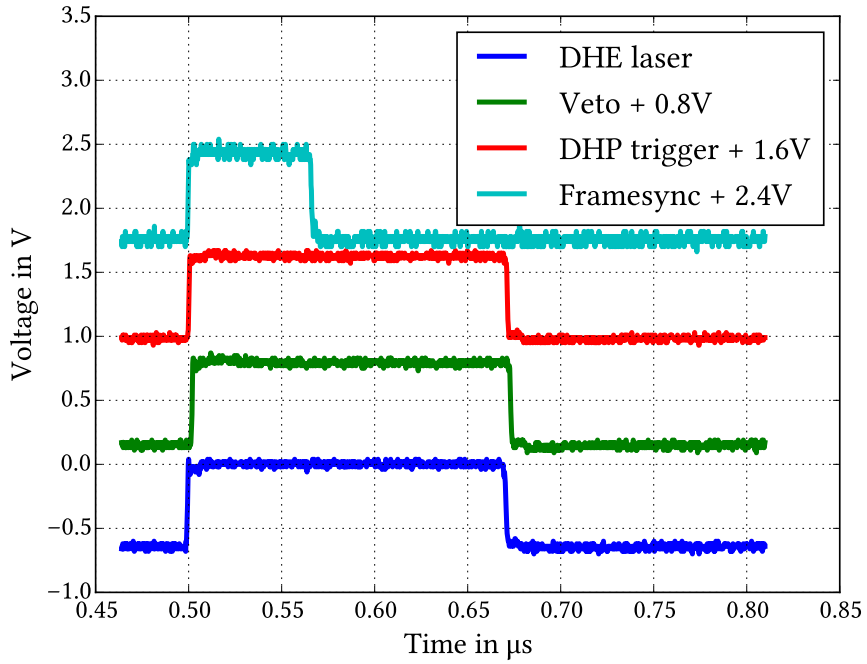


Figure 6.5: The four programmable signals which can be read out with the DHE adapter card start at the same time.

position zero. All signals are set to the same length. The DHE trigger is an internal signal and was not measured in this thesis. It serves to power internal counters within the DHE and does not play a major

role in gated mode operation. The DHP trigger, veto and laser signals can be read out with the DHE adapter-card. In addition the DHE adapter also grants access to the framesync signal, as it is sent from the DHE. The measurement displayed in figure 6.5 shows the output signals of the DHE adapter. The internal signals start with no larger time delay than (4.0 ± 0.4) ns. Thus all the signals have the same length and start at the same time. The signals which are sent to the DHP have to go through the DHP trigger line. There the signals are encoded and new commands can only be issued once per gate. Thus the DHP receives new commands from the DHE only once every (129.31 ± 0.02) ns. As this time interval is much larger then the shift of 4 ns between the internal signal gated mode operation is not influenced.

6.1.5 DHP trigger line

The commands issued by the DHE are Manchester encoded on the DHP trigger line. Each word contains four bits, which are encoded as reset, veto, trigger and framesync. As a special case the idle word 01010101 is not used, but replaced by 00011101, which is more easily recognizable by the system. After the first two bits are transmitted the receiving end knows, whether to expect a new command.
The DHP trigger line is clocked in sync with the DHE reference clock. Although the speed is reduced to 1/8, due to one word consisting of 8 bit. This effectively reduces the speed of the DHP trigger line to $\frac{62.5\,\mathrm{MBit/s}}{8} = 7.8\,\mathrm{MBit/s}$.

Delay due to DHP trigger line

This measurement shows how long it takes for a signal from the DHE to influence the switcher. The DHP trigger line, the Switcher clock and the veto signal from the DHE adapter card are measured. The system clock was set to 62.5 MHz. At (696.3 ± 0.4) ns the veto signal is switched on. In the next word on the DHP trigger line this information is sent to the DHP[3]. As the veto signal can be programmed per reference clock cycle, the timing between veto signal switching on and this information being sent on the DHP trigger line can vary. Thus the time difference between the DHP receiving the signal from the DHP trigger line and the signal taking effect in the switcher is measured. In figure 6.6 the veto signal was used to activate the second Switcher memory block. This block contained the command for the Switcher clock to stop.

The time required to go into gated mode is:

$$(879.2 \pm 0.4)\,\mathrm{ns} \xrightarrow{(105.1 \pm 0.5)\,\mathrm{ns}} (984 \pm 65)\,\mathrm{ns}$$
$$\Rightarrow \Delta T_{\mathrm{GM\ activate}} = (105 \pm 65)\,\mathrm{ns}$$

After (879.2 ± 0.4) ns the command to go into gated mode is completely uploaded into the DHP. Finally after (984 ± 65) ns the switcher clock stops in this case signalling the start of gated mode operation. The large error is caused by the inability to judge when exactly the Switcher clock stopped. Thus half a gate which is also half a Switcher clock cycle is assumed as error. Therefore going into gated mode took (105 ± 65) ns in this case. This is a little under the time it takes to read out one gate (129 ns). In conclusion at least one gate worth of time needs to be reserved for gated mode to activate.

[3] There are exceptions to this. If a signal is switched to on less than 3 reference clock cycles before the next word starts, the information is delayed by one more word.

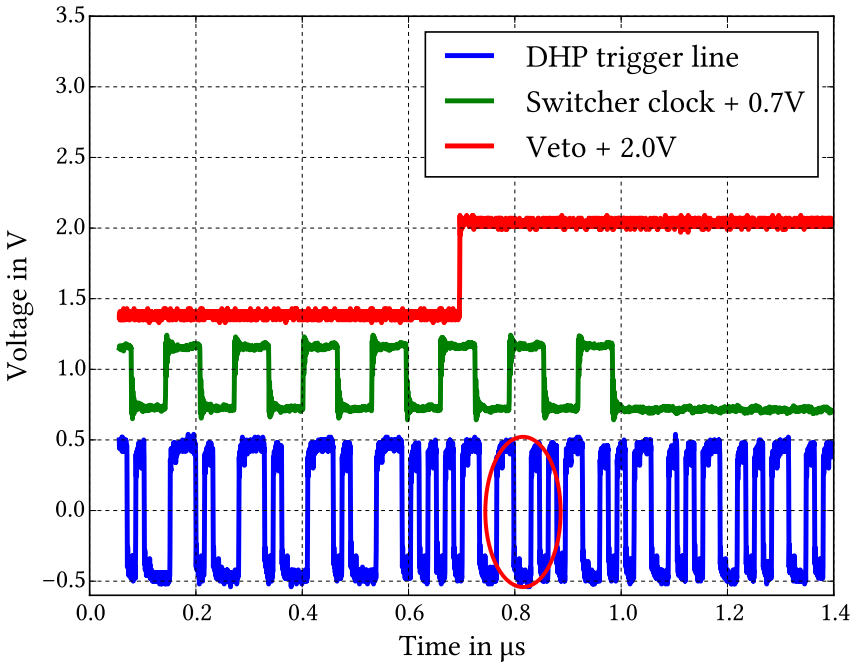


Figure 6.6: Veto signal is raised to high, this information is transmitted across the DHP trigger line and finally the switcher starts gated mode operation. The red circle marks the transmission of the veto signal across the DHP trigger line.

Delay from DHE to DHP trigger line

Measurements were conducted to figure out when the DHE signal is recognised on the DHP trigger line and the minimal length of the DHE signal which is still recognised. The DHP trigger, measured from the DHE adapter card, is compared with the signal on the the DHP trigger line. In these measurements a signal which is 1 GCK long was programmed at different memory positions. These memory positions were from 0 to 15, increasing memory position by one for each measurement. First looking at the measurement on the left in figure 6.7 one observes that the DHP trigger is sent on the DHP trigger line the gate after it was switched to on. In contrast for the figure 6.7 on the right, the DHP trigger is sent two gates after it is switched to on. This shows that it is enough to switch one of the programmable signals on for 1 GCK, for it to be registered by the DHP.
In general if shifted by 8 GCK a signal is transmitted one word earlier or later across the DHP trigger line. Nonetheless a signal programmed in the DHE memory needs to be active at least 3 GCK before the next word is sent across the DHP trigger line, to be transmitted in that word. If there is just 1 or 2 GCK difference then the signal is delayed for one more gate. This is the reason why at memory position 5 in figure 6.7 the DHP trigger is transmitted one gate later[4] than at memory position 4.
In appendix A in figure A.2 further memory positions of the 1 GCK long DHP trigger pulse are displayed. Moreover, in appendix A in figure A.1 the transmission of the veto signal was measured. It shows the same behaviour as the DHP trigger signal. For the gated mode measurements in section 6.2 the first memory position that was written was memory position 5. Therefore one avoids the initial shift of one gate after 5 GCK. Thus any signal programmed into the DHE memory, if shifted by 8 GCK, will cause a

[4] The first memory position is 0. Thus memory position 4 is the 5th memory position.

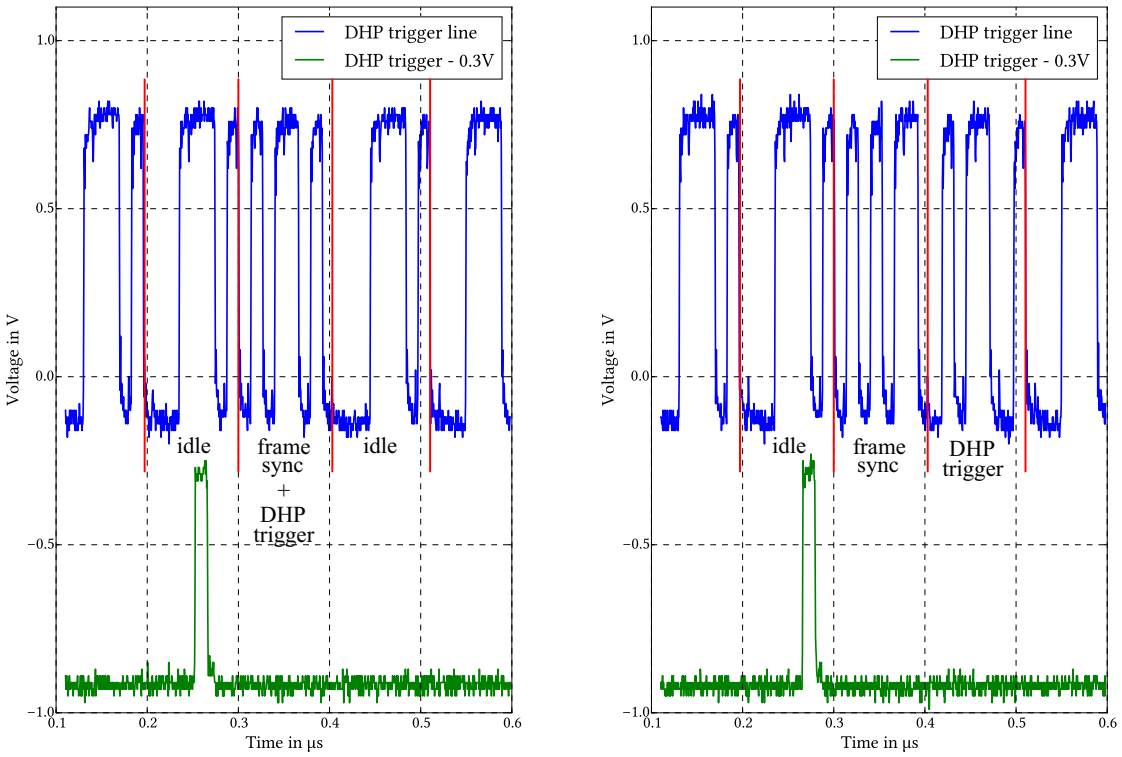


Figure 6.7: The DHE trigger displayed with DHP trigger line. On the left DHP trigger was 1 GCK long and written in DHE memory position 4. On the right left DHP trigger was also 1 GCK long, but written in DHE memory position 5.

shift of one gate.
With this knowledge one can also predict the time required until a programmed signal is uploaded into the DHP memory. Figure 6.7 shows that 18 GCK are required to upload the DHP trigger to the DHP. Those 18 GCK are caused by the logic block and remain unchanged, if the reference clock speed is altered. Using this one obtains for the 62.5 MHz clock:

$$\text{Time to read out one gate} \times \text{time to upload from DHE to DHP in GCK}$$
$$(16.164 \pm 0.003)\,\text{ns} \times 18\,\text{GCK} \;=\; (290.95 \pm 0.05)\,\text{ns}$$

Thus for the measurements in this thesis it takes (290.95 ± 0.05) ns to upload the signal into the DHP memory. In the final experiment it is known beforehand when the detector needs to be in gated mode because the detector is synchronized with the accelerator. Therefore the time to upload the DHE signal into the DHP memory can be neglected.

Delay on the laser

The laser setup is controlled by a function generator. This function generator is connected to the DHE adapter. The function generator is set to fire when the output signal from the laser connector on the DHE

adapter is high. Looking at figure 6.8 the laser is delayed by (30.5 ± 0.5) ns relative to the input signal.

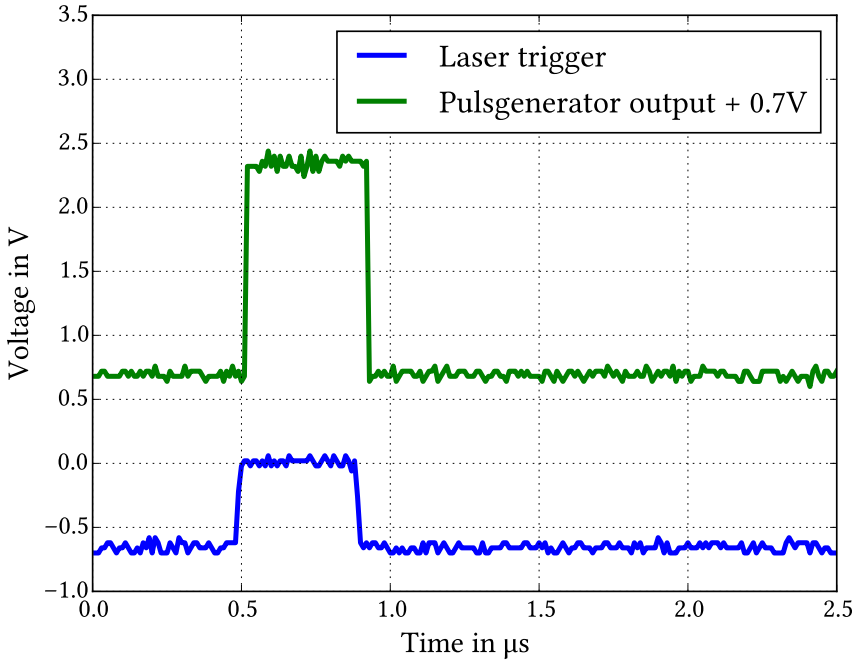


Figure 6.8: The laser shoots less than one gate after the laser signal is switched on.

This is less than one gate and needs to be considered when calculating delays, but does not hinder gated mode measurements.

6.2 Gated mode measurements with a laser

For the measurements presented in this section the DEPFET detector is installed in the laser setup and the switcher sequence in Switcher memory B is set to gated mode. The firmware which was installed on the DHE used for this thesis does not support a continuous gated mode. In this firmware the content of the DHE memory is executed once. This poses a challenge because during normal operation DEPFET is just triggered to read out the matrix once (also called frame). But sensible gated mode measurements require more than one frame. A simple measurement would be to shoot a laser onto the matrix during gated mode operation and then check how much charge was injected into the matrix despite gated mode shielding in the next frame. To make measurements which involve more than one frame feasible it is possible to program a DHP trigger in the DHE memory, which is longer than one frame. When the trigger is longer than one frame the matrix is continuously read out, until the trigger stops. In case of the small Hybrid 5 setup the reduced number of rows compared to the final design for the Belle II experiment allows to read out the full matrix multiple times, without data loss. In the following measurements the matrix was triggered so that it is read out for four times in succession.
To ease working with the data the frames were recorded without any pedestals, threshold or common mode correction applied. Any corrections were applied manually to the measured data and were not done by the DEPFET system. In figure 6.9 the general outline of the DHE memory sequence used in this

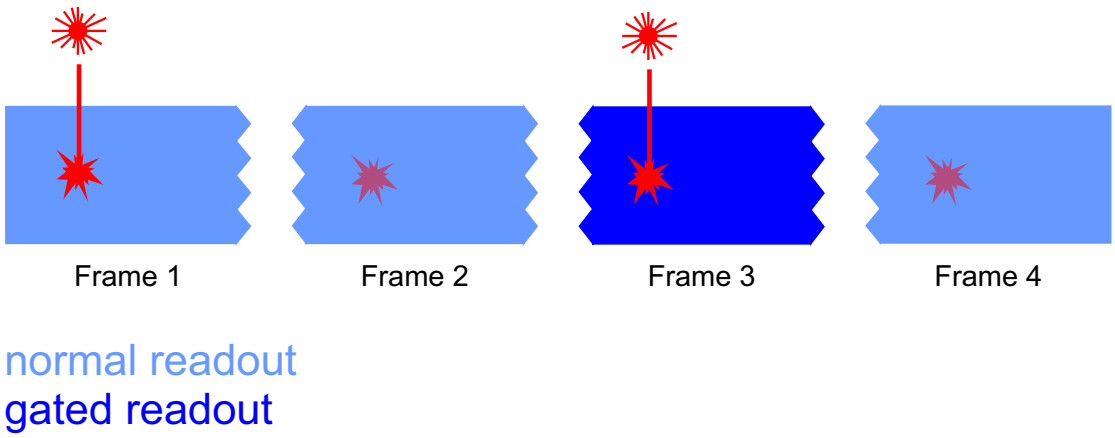


Figure 6.9: The laser is shot twice, once in the first frame and then again during the third frame.

thesis is displayed. In this sequence four frames are recorded[5], while the laser is shot twice. Once the laser is shot during normal operation in the first frame. And a second time the laser is shot during gated mode operation in the third frame. The second and fourth frame maintain normal operation and serve as reference frames. As it was observed that the DHP trigger programmed into the DHE memory takes effect one frame later then its memory position would suggest, the DHP trigger is switched to on with a delay of one frame (128 GCK) with respect to veto, DHE trigger and laser. The veto sequence in the third frame is programmed to be 49 GCK long. This ensures that the veto signal will be on for 7 gates. On the one hand this is because leaving the signal on for 1 GCK is enough to ensure it gets transmitted across the DHP trigger line. On the other hand leaving the signal on for 50 GCK could potentially veto the matrix for 7 gates or 8 gates, depending on the phase relation. Using a veto signal which is shorter than 16 gates ensures that not all the pixels are read out during gated mode.

[5] This means the DHP trigger was put to on state for $16 * 4 = 64$ gates or $16 * 4 * 8$ GCK = 512 GCK.

6.2.1 Time required to go into gated mode

The purpose of the first measurement is to decide how long it takes for DEPFET to switch in and out of gated mode. To measure this the DHE memory is programmed in accordance with figure 6.9. The veto sequence is set at a fixed position starting when readout of the third frame starts and lasting for 7 gates. The time the laser is shot is then delayed with respect to the time the veto sequence starts. Thus the laser shifts through the whole sequence. Two measurements are conducted. In the first measurement the laser is shot in a pixel which is in the lower half of the matrix within the region which is read out during the gated mode sequence. The second measurement is done shooting the laser into a pixel in the last gate on the upper border of the matrix. This second pixel is not read out during the gated mode sequence.

Measurement for pixel in gated area

For the first measurement the important frames are the third and fourth frame. There are four cases which can occur when the laser is delayed:

- If the laser is shot into the pixel before gated mode was activated, then the injected charge is read twice. Once in the third frame during gated mode with readout and then again in the fourth frame during normal readout, because pixels are not cleared during gated mode with read out.
- The laser is shot into the pixel after gated mode was activated. The internal gate of the pixel is shielded from additional charge. Thus no signal should be visible in the third and fourth frame.
- The laser is shot while the pixel is read out and during gated mode. While a pixel is read out the voltage on the clear contact is low. Consequently, the pixel is not shielded. The signal is read out twice, once in the third frame during gated mode and again in the fourth frame.
- The laser is shot into the pixel after gated mode was deactivated. In this case the pixel was already read out during this frame. Consequently, the signal should only appear in the fourth frame. This case is equivalent to firing the laser during normal operation.

Because the fourth frame contains all relevant information it is used to display the results for this measurement. Figure 6.10 shows the response of the pixel the laser was shot at. In the appendix figure A.3 shows the response of the area the laser was shot at in more detail[6]. The laser pulse which was used to create this measurement was 2 GCK (or (32.328 ± 0.006) ns) long.
Starting from the first measurement looking at measurements where the laser was shot with increasing delay, one observes the full signal for the first 32 GCK delays. This means charge is shot before gated mode started and preserved until the fourth frame! For the delay settings of 33 GCK and 34 GCK the signal is weaker. The reason being the finite length of the laser pulse. Part of the laser pulse is shot when the pixel is already gated, while another part is able to deposit charge before gated mode is fully activated.
At delay setting 35 GCK gated mode is fully activated. Until at delay 55 GCK the signal is visible again. As already mentioned this is because the pixel is inside the gated area and while it is being read out no shielding is active. The laser pulse is visible for 10 GCK. This response is smeared out because of the finite length of the laser pulse. To determine how much time the readout requires it is necessary to establish when readout started and when it ended. When the full signal is visible in the fourth frame it is

[6] Information on the columns was omitted, instead just the column of the pixel which was hit by the laser is displayed. On the x-axis the row which is read out is displayed. The title of each of the subplots shows by how much the laser signal was delayed compared to the veto signal.

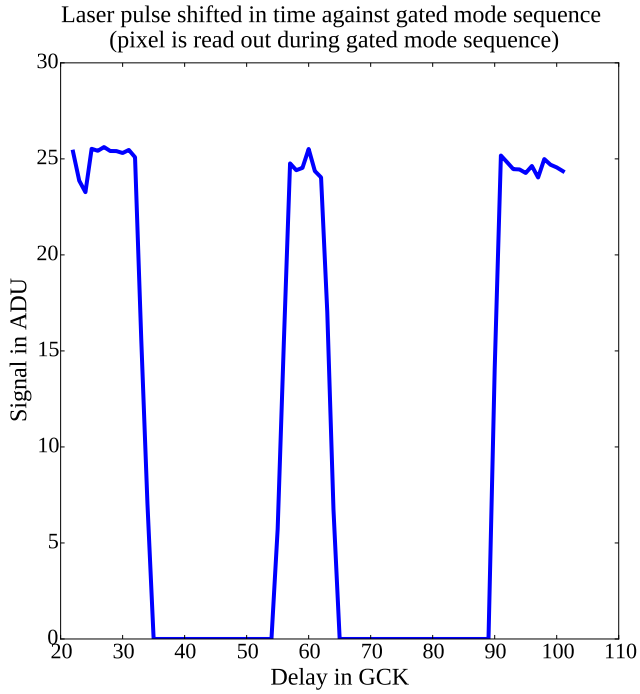


Figure 6.10: The laser is fired onto a pixel which is read out during gated mode operation. The laser is delayed against the veto signal. The fourth frame is used to check when gated mode was active.

because the starting point of the laser pulse is after the starting point of the readout sequence. When the signal is no longer visible the starting point of the laser is after readout finished. Consequently readout took 65 GCK − 57 GCK = 8 GCK, which is in agreement with the results obtained in the measurements with the oscilloscope (see 6.1.3).
Going to higher delays, again the laser is already visible starting from 90 GCK due to finite laser length. The laser signal is fully visible starting from 91 GCK. Which is also the point in time at which gated mode is deactivated. The programmed length of the gated mode sequence was 7 gates, using start and end point of the sequence for a consistency check, one obtains:

$$\frac{91\,\text{GCK} - 35\,\text{GCK}}{8\,\text{GCK/gate}} = 7\,\text{gates}.$$

Hence gated mode is active for the expected amount of time. Using the delay of $(35.0 \pm 0.5)\,\text{GCK}$[7] to calculate the time it takes to activate gated mode one obtains:

$$\text{Time to go into gated mode} \times \frac{\text{Time to read out one gate}}{\text{Number of GCK in one gate}} =$$
$$(35.0 \pm 0.5)\,\text{GCK} \times \frac{(129.31 \pm 0.02)\,\text{ns}}{8\,\text{GCK}} = (565 \pm 8)\,\text{ns}.$$

This does not take into account any of the measurements with the oscilloscope. Considering the delay on the laser signal (30.5 ± 0.5) ns and the delay caused by uploading the signal into the DHP (290.95 ± 0.05) ns a corrected value for how long it took for gated mode to activate for this particular

[7] One measures in steps of 1 GCK. Consequently the precision is also 1 GCK.

pixel is calculated:

$$(565 \pm 8)\,\text{ns} - (290.95 \pm 0.05)\,\text{ns} + (30.5 \pm 0.5)\,\text{ns} = (305 \pm 8)\,\text{ns}.$$

Thus it takes (305 ± 8) ns to switch this particular pixel into gated mode. As the measured gated mode sequence is exactly 7 gates long switching out of gated mode for this particular pixel takes less than 1 GCK. This is not the time it takes for the matrix to go in and out of gated mode though. To calculate this time one has to consider the pixel outside the gated area as well.

Measurement for pixel outside gated area

For the second measurement the important frame is the third frame. Considering that the observed pixel is in the last gate of the matrix and gated mode is active for the first 7 gates, this can be deducted when looking at the cases which can occur when the laser is delayed:

- If the laser is shot onto the pixel before gated mode is activated, the injected charge is preserved during gated mode and read out at the end of the third frame during normal operation.
- The laser is shot onto the pixel after gated mode was activated. The internal gate of the pixel is shielded from additional charge. Thus no signal should be visible in the third frame.
- The laser is shot onto the pixel after gated mode was deactivated. In this case the pixel is also read out in the third frame during normal operation.

Because the third frame contains all relevant information it is used to display the results for this measurement. Figure 6.11 shows the response of the pixel the laser was shot at. In the appendix figure A.4 shows the response of the area the laser was shot at in more detail[8]. The laser pulse which was used to create this measurement was 2 GCK long.
At a delay of 42 GCK the start of the laser pulse is no longer visible and gated mode is fully active. Because this pixel is not read out it stays active until the delay is 99 GCK compared to the veto signal. Using these two numbers to calculate the length of the veto sequence one obtains:

$$\frac{99\,\text{GCK} - 42\,\text{GCK}}{8\,\text{GCK/gate}} = 7.125\,\text{gates}.$$

The pixel is gated 1 GCK longer than programmed. A possible explanation for this could be the finite time it takes to go out of gated mode. Which could cause the gated mode sequence to stay active for 1 GCK longer than expected.
Utilising the information obtained from the pixel on the bottom half of the matrix and the one on in the last gate the time required to go in and out of gated mode for the whole matrix can be calculated. In the case of going into gated mode the pixel from the last gate took longer than the one from the first half of the matrix. The additional time it takes for the last gate to switch into gated mode is calculated with:

$$[(42.0 \pm 0.5)\,\text{GCK} - (35.0 \pm 0.5)\,\text{GCK}] \times \frac{(129.31 \pm 0.02)\,\text{ns}}{8\,\text{GCK}} = (113 \pm 11)\,\text{ns}.$$

[8] Information on the columns was omitted, instead just the column of the pixel which was hit by the laser is displayed. On the x-axis the last gate is displayed. The title of each of the subplots shows by how much the laser signal was delayed compared to the veto signal.

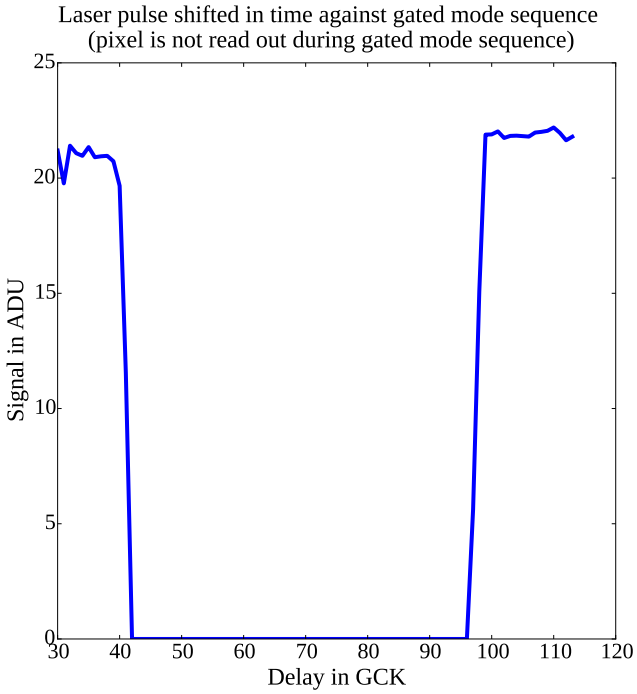


Figure 6.11: A pixel which is not read out during gated mode is observed. The laser is delayed against the veto signal. The fourth frame is used to check when gated mode was active.

The time to activate gated mode for the full matrix can be calculated by adding the additional time it takes for the last gate to switch operation modes:

$$(113 \pm 11)\,\text{ns} + (305 \pm 8)\,\text{ns} = (418 \pm 14)\,\text{ns}.$$

Hence it takes (418 ± 14) ns to switch the complete small matrix into gated mode. The additional time it takes to switch the upper half of the matrix into gated mode compared to the lower half stems from the Switcher. Internally the Switcher is divided in four parts. In the small matrix two of these parts are connected. One to the upper and one to the lower half of the matrix respectively. The (113 ± 11) ns represent the delay caused by the two Switcher parts not switching the matrix into gated mode at the same time. Under the assumption that the delay between Switcher parts is the same for the whole matrix, one can calculate a possible time to switch the large matrix into gated mode. This time would be $3 \times (113 \pm 11)\,\text{ns} + (305 \pm 8)\,\text{ns} = (644 \pm 34)\,\text{ns}$. Under this assumption going into gated mode would take roughly 5 gates for the large matrix used in the modules which utilises the full Switcher.
The additional time it takes the last gate to go out of gated mode compared to the pixel inside the gated area can be calculated with:

$$[(99.0 \pm 0.5)\,\text{GCK} - (91.0 \pm 0.5)\,\text{GCK}] \times \frac{(129.31 \pm 0.02)\,\text{ns}}{8\,\text{GCK}} = (129 \pm 11)\,\text{ns}.$$

By adding the time for the lower half pixel and the time for the last gate, one obtains the full time required to go out of gated mode:

$$(129 \pm 11)\,\text{ns} + (0 \pm 7)\,\text{ns} = (129 \pm 13)\,\text{ns}.$$

Thus it takes (129 ± 13) ns to go out of gated mode for the small matrix. Assuming each of the four parts of the Switcher requires the same amount of time to switch out of gated mode, one is able to calculate the time to go out of gated mode operation for the large Belle II matrix. This time is given by $3 \times (129 \pm 11)$ ns + (0 ± 7) ns = (387 ± 34) ns. Thus the large matrix would require 3 gates to go out of gated mode operation.

In the Belle II experiment it will be known when a noisy bunch will pass the detector and when the DEPFET detector will need to be in gated mode operation. Thus gated mode operation will be timed, so that the matrix is fully gated when the noisy bunch passes the detector. Consequently the time in which the detector is unable to measure data is given by the time the DEPFET matrix itself takes to go in and out of gated mode plus the length of the gated mode sequence itself. Which is the additional time a pixel in the upper half of the matrix takes to switch into and out of gated mode compared to a pixel in the bottom half of the matrix. In case of the small matrix used in this thesis, the time required by the matrix to go in and out of gated mode is:

$$(129 \pm 11)\,\text{ns} \;+\; (129 \pm 11)\,\text{ns} \;=\; (258 \pm 16)\,\text{ns}.$$

Thus in case of the small matrix used in this thesis the time in which one could not measure would be given by (258 ± 16) ns plus the time spent in gated mode.
Transferring these results to the large matrix which will be used in the full modules during the Belle II experiment, would correspond to the following time to switch in and out of gated mode:

$$3 \times (129 \pm 11)\,\text{ns} \;+\; 3 \times (113 \pm 11)\,\text{ns} \;=\; (726 \pm 47)\,\text{ns}.$$

Thus, under the assumption that the delay between Switcher parts is the same, the DEPFET detector will be unable to measure for (726 ± 47) ns plus the time spent in gated mode.

6.2.2 GateOff-ClearHigh influence on gated mode

When gated mode is active the height of the potential wall shielding the internal gate and how effective charge is removed from the bulk depends on GateOff and ClearHigh. To measure the ideal working point the two voltages GateOff and ClearHigh are varied against each other. It is important to consider the performance of the device in normal and gated mode operation. For both modes of operation the GateOff voltage should be as small as possible to create as little heat as possible by switching the gate on and off. ClearHigh in normal operation should be high enough to remove all charge stored within the internal gate. During the gated mode operation, ideally no charge should travel from the internal gate to the clear contact. This sets an upper limit on the ClearHigh voltage. The laser intensity is set so that the signal is roughly equal to two minimum ionising particles passing the same pixel, which should happen only very rarely during the Belle II experiment [9].

Charge preservation

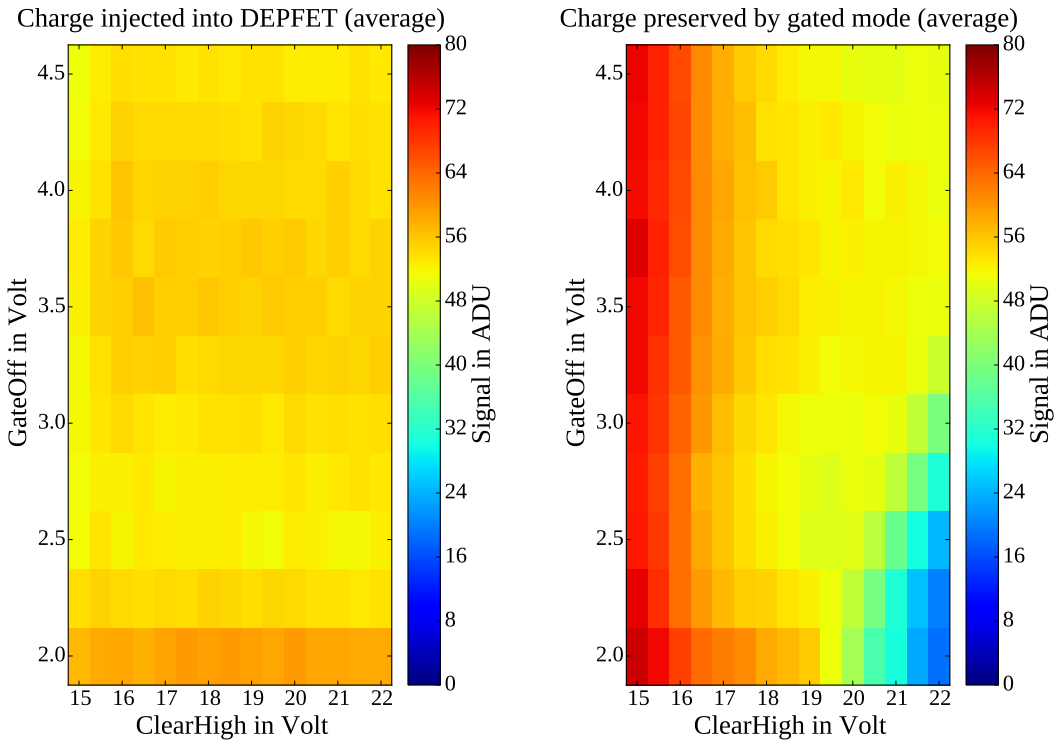


Figure 6.12: On the right charge preserved during gated mode operation. On the left reference how much charge was injected. Both measured in dependence of GateOff and ClearHigh voltages.

The sequence from figure 6.9 is used to measure the ideal working point in the GateOff-ClearLow parameter space. The first and third frame are used to optimise gated mode. In the first measurement the laser is shot shortly before gated mode operation starts, then the pixel is read out after 7 gates of gated mode operation. Figure 6.12 displays the first (left) and the third (right) frame. The figure on the right side shows how much charge was measured after the gated mode operation. The figure on the

[9] The signal one minimum ionising particle will create in the Belle II experiment is estimated to be roughly 30 ADU [29].

left side shows DEPFET during normal operation. During normal operation and shortly before the start of gated mode operation, the laser was shot both times at the same pixel and with the same intensity. Therefore the left figure in figure 6.12 serves as a reference frame, displaying how much charge was injected. One would expect that if ClearHigh is chosen too small during gated mode operation, not all charge is extracted from the bulk and some reaches the internal gate. In this case, since no laser was fired during gated mode operation, the increase in signal for ClearHigh voltages below 20 V is most likely due to charge pileup[10]. For ClearHigh voltages above 20 V combined with GateOff voltages below 2.5 V one

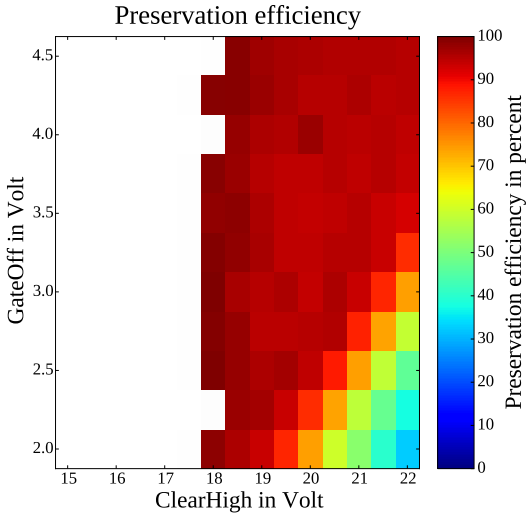


Figure 6.13: Preservation efficiency plotted against the GateOff and ClearHigh parameters.

observes a slight decrease of the signal after gated mode. This is because the relation between ClearHigh and GateOff voltage approaches the case of a real clear.
The measured signals can be converted into an efficiency using:

$$\eta_{\text{preservation}} = \left(\frac{I_{\text{gated-p}}}{I_{\text{signal}}} \right)$$

In this equation $\eta_{\text{preservation}}$ is the preservation efficiency and $I_{\text{gated-p}}$ is the signal which is measured at laser position, after the laser was fired shortly before the start of gated mode operation. The variable I_{signal} corresponds to the signal which was measured at the same position during the reference measurement in normal operation. Figure 6.13 displays the resulting preservation efficiency. Any points with a preservation efficiency over 100 % are left blank, as those points indicate incorrect functionality of the detector and charge pileup. If GateOff is set to 3 V or larger and ClearHigh larger than 18 V almost all configurations show a preservation efficiency larger than 90 %.

Charge shielding

The goal of this measurement is to determine how much charge reaches the internal gate despite gated mode shielding. The measurement uses the DHE sequence introduced in figure 6.9. The laser is fired in the third frame during gated mode operation and afterwards the signal is sampled. Ideally no charge should be injected into the internal gate and the signal should be 0 ADU. If sufficient charge was already

[10] In normal operation, if ClearHigh is chosen too small, not all charge is removed from the detector during clear. This leads to a pileup of charge, which eventually fills the internal gate completely.

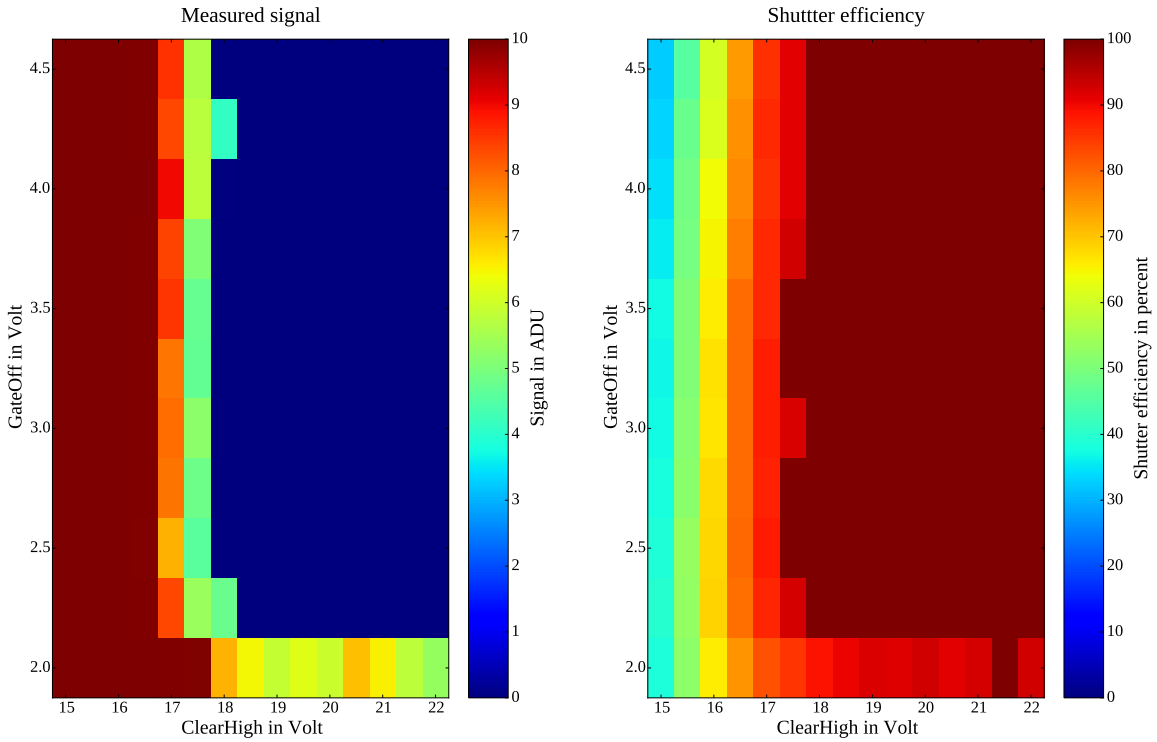


Figure 6.14: The left figure shows charge measured in ADU after laser was fired during gated mode operation. The right figure depicts the resulting shutter efficiency.

collected within the internal gate, even slight increases in collected charge might shift a pixel above threshold. Thus no threshold is applied for this measurement to detect even slight changes in the internal gate. For each configuration a shielding efficiency is calculated by:

$$\eta_{\text{shield}} = \left(1 - \frac{\mathrm{I}_{\text{gated-s}}}{\mathrm{I}_{\text{signal}}}\right).$$

In this equation η_{shield} is the shutter efficiency and $\mathrm{I}_{\text{gated-s}}$ is the signal which is measured at the laser position, after the laser was fired during gated mode operation. The variable $\mathrm{I}_{\text{signal}}$ corresponds to the signal which was measured at the same position during the reference measurement in normal operation. The shutter efficiency is the efficiency with which gated mode prevents additional charge from reaching the internal gate.
In figure 6.14 the results of the shielding efficiency measurement are summed up. The results are similar to the preservation efficiency measurement. If GateOff is chosen equal or larger than 2.5 V, the shielding around the internal gate works correctly and no additional signal is measured.
When ClearHigh voltage is chosen smaller than 18 V the clear process does not work correctly and charge piles up in the internal gate. To determine the ideal working point both preservation and shielding efficiency need to be considered. Else a configuration where gated mode approaches a real clear could be mistaken for one with good shielding efficiency or a configuration with no clear at all for one with good preservation efficiency. Looking at the performance shown by DEPFET in the two measurements, the ideal working point is placed at ClearHigh 19 V and GateOff 3 V. ClearHigh is chosen so that the

clear voltage is as low as possible while still being able to clear the internal gate completely. Similarly GateOff is chosen as low as possible, but with a small safety margin to guarantee correct functionality of the DEPFET sensor.

Increased pedestals

When optimising the DEPFET sensor an additional thing to consider are the pedestals. The quick switching of the clear voltage between potentials of up to 22 V (in this measurement) and a low potential of 6 V has an influence on the pedestals. Shortly after gated mode ends there are a number of pixels which show a signal significantly over threshold. This causes an increase in noise hits. Figure 6.15 shows

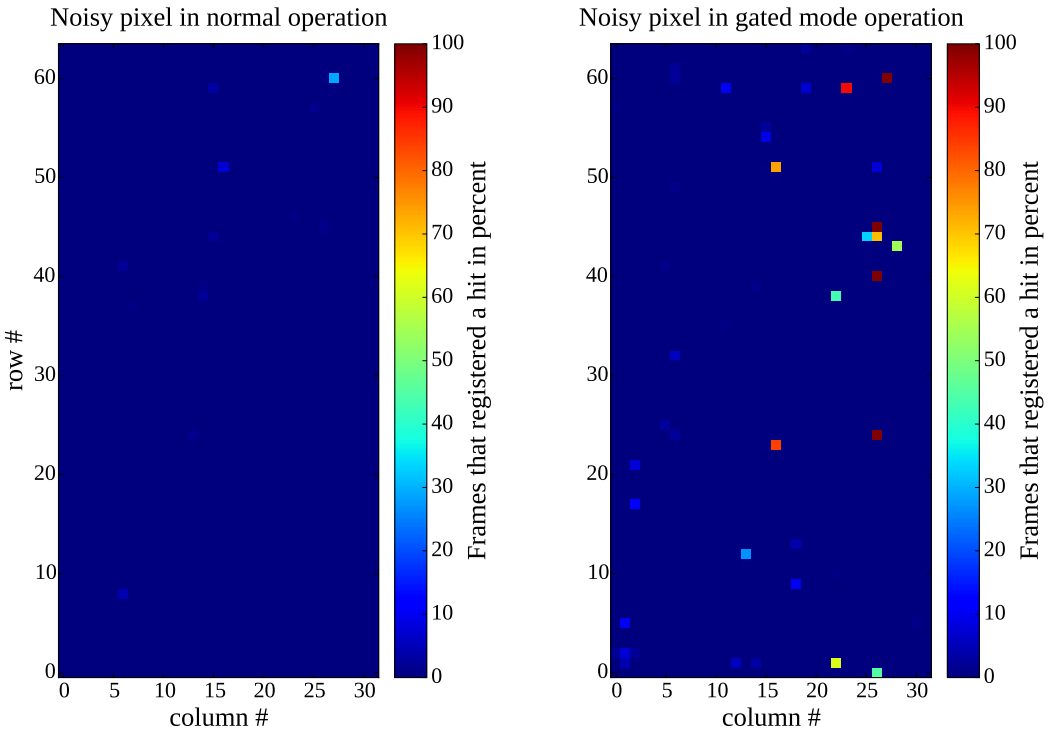


Figure 6.15: Percentage of frames in which that particular pixel fired. On the left normal operation, on the right normal operation right after gated mode ended.

how often each of the pixels registered a hit. On the left hand side the second frame, after the laser was fired, is displayed. On the right hand side the fourth frame, after gated mode ended, is displayed. An increase in occupancy compared to the frame, which was not in direct succession to a frame with gated mode operation, is visible. This increase can in part be traced back to the switching of the clear voltages, which change across the whole matrix during gated mode operation. To check the influence of ClearHigh and ClearLow on noise and gated mode performance further measurements are conducted.

6.2.3 ClearLow-ClearHigh influence on gated mode

There is coupling between the clear and the drain lines. The quick shifting of the clear voltage when gated mode is activated and deactivated has an influence on the drain lines and causes a change in pedestals. This shift in pedestals can partly be removed by common mode correction. But some pixels show strong

increase in their pedestal value, which causes them to register a hit without any charge being injected from the outside. Increasing ClearLow and decreasing ClearHigh lessens the backlash of switching between high and low voltage on the drain lines. In theory this should lessen the variation of pedestals. Figure 6.16 shows the noise occupancy which was observed, measuring in the frame right after gated

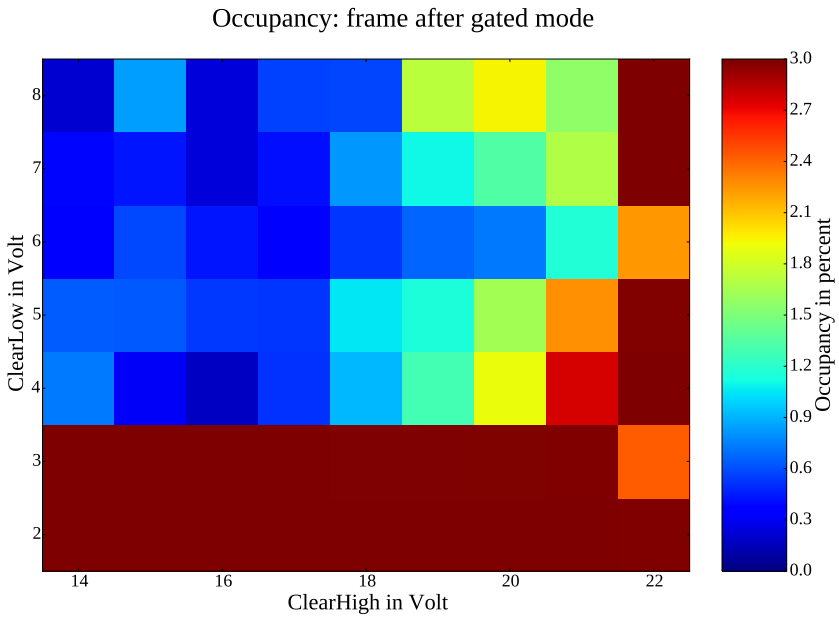


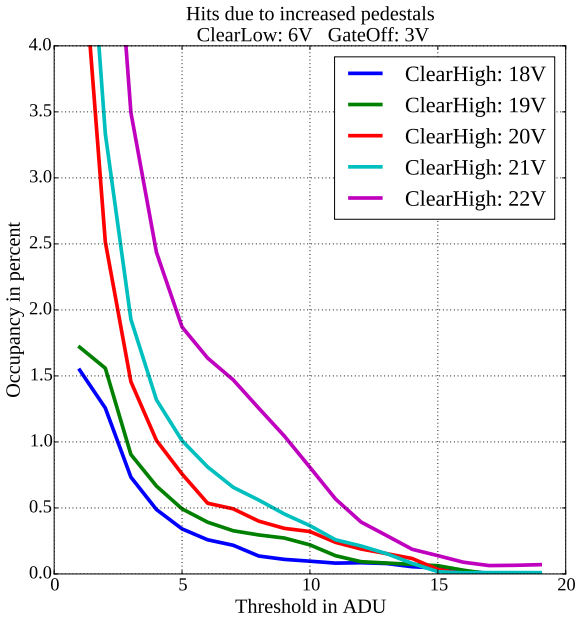
Figure 6.16: The figure shows the occupancy in the next frame right after gated mode ended.

mode ended. Threshold was set to 4 ADU in this measurement. In the last measurement campaign which optimised the DEPFET sensor voltages, the DESY testbeam in November 2015 the configuration ClearLow 5 V and ClearHigh 20 V was used. This campaign did not include measurements for gated mode. Comparing this configuration with the results from figure 6.16, one observes over 1.5 % noise occupancy for the testbeam configuration. But increasing ClearLow from 5 V to 6 V garners good results. In addition ClearHigh is decreased from 20 V to 19 V. This decreases the number of registered hits by a factor of 1/2, while the detector still works correctly in normal operation.

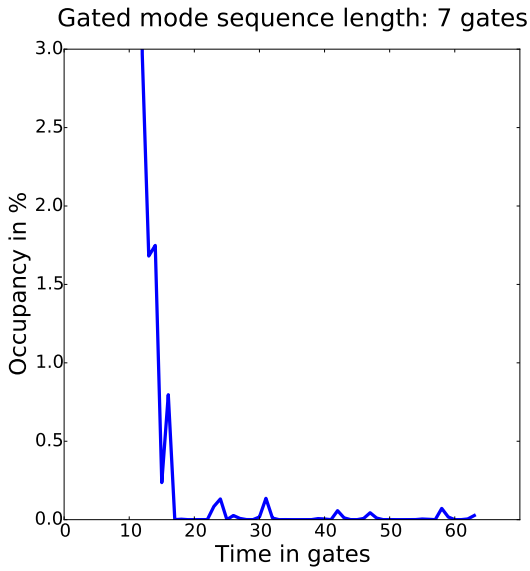
6.2.4 Investigation of gated mode fluctuations

After choosing a setting with fewer noise hits, investigations are started, how the signals which caused those noise hits are distributed. In case of noise distributed in the lower energy range an increase in pedestals could potentially eliminate the major part of noise. Figure 6.17(a) shows the relation between occupancy and threshold, measuring in the frame after gated mode. The statistical errors are smaller than line thickness. The trend of the curves appears to be exponential. For ClearHigh voltages above 19 V the occupancy shows a strong increase for low thresholds (figure 6.17(a)). The maximum occupancy the PXD can cope with is 3 % the expected occupancy caused by all sources is 0.4 hits /μm^2s. Assuming a pixel size of 50×55 μm^2 this results in an occupancy of 2.2 % [30][11]. The occupancy caused by background sources is estimated to be (1.28 ± 0.03) %[31]. Consequently in the long run, the occupancy caused by the increased pedestals needs to be below 0.8 %. Otherwise the detector is unable to process any hits and information on new hits is lost. Keeping the optimal operation point ClearHigh 19 V and

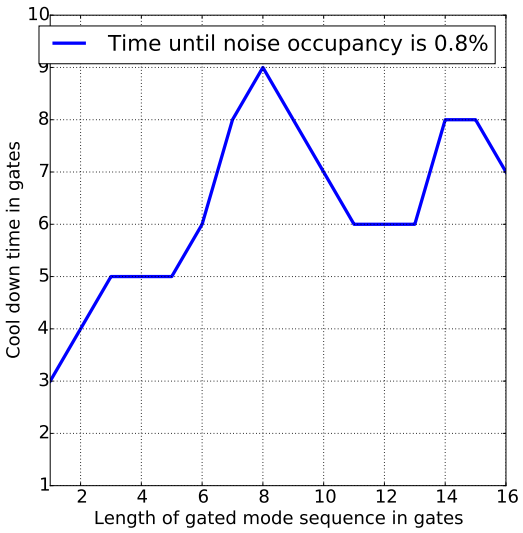
[11] The assumed pixel size is the size of the pixels of the PXD9 matrix used in this thesis.



(a) Occupancy in the next frame right after gated mode ended for different threshold and ClearHigh settings.



(b) Occupancy of each gate during and after gated mode.



(c) Time until occupancy decreases to 1 % in number of gates read out.

Figure 6.17: Steps to figure out noise occupancy and cool down time of the DEPFET matrix.

adding a threshold of 4 ADU yields an occupancy of (0.699 ± 0.002) %. The error is purely statistical and does not take any systematic errors into account. This leaves over 1 % occupancy for physics.
The next step is a measurement to find out how many gates worth of time are required until the pedestals of the detector have settled down. The threshold was set to 4 ADU. The limitation of 3 % occupancy per

frame stems from the DHP. However the DHP can handle short bursts of occupancy of over 3 %, due to buffers. Nonetheless this thesis assumes that the system is cooled down until occupancy reaches 0.8 %, before data taking resumes. Factoring in the buffers of the DHP, this leaves enough room to process hits without the risk of data loss. In the measurement the DHP is triggered for four frames. The gated mode sequence is activated at the beginning of the first frame to observe as many gates of cooldown as possible. Figure 6.17(b) shows the occupancy of each gate which is read out during the four frames. The statistical errors are smaller than line thickness. The gated mode sequence was 7 gates long, the same length which was used for the previous measurements. The gate number on the x-axis is increasing but, as the matrix has only 16 gates, the same gates are measured four times. During and right after gated mode is active a strong increase in occupancy is visible. It takes (15.0 ± 0.5) gates for the occupancy to fall below 1 %. Thus not counting the length of the sequence itself the matrix needs (8.0 ± 0.5) gates to cool down.
Further investigations have the goal to determine if the number of gates read out in gated mode has an influence on how long pedestals fluctuate. The length of the gated mode sequence is varied between 1 gate and 16 gates in steps of 1 gate and the number of gates which are read out until the active gate has less than 0.8 % occupancy is determined. The results are displayed in figure 6.17(c). For short sequences of length 1 to 8 gates the cooldown time increases with increasing sequence length. Looking at longer gated mode sequences the cooldown time remains at roughly the same level. This saturation effect might be related to the limited number of gates available or to one of the capacitances between the clear connection and one of the other connections fully charging. Overall the system takes (6 ± 2) gates or (760 ± 207) ns on average to switch into gated mode. According to this measurement waiting for (9.0 ± 0.5) gates would ensure that the active gate has an occupancy of less than 0.8 %. More detailed pictures showing the occupancy at each gate can be found in the appendix in figure A.5. That figure shows the occupancy which each gate sees for different lengths of gated mode sequences.

6.2.5 Position-dependent measurements

The final laser measurement for gated mode is a position-dependent measurement. Once the system is optimised the goal of position-dependent measurements is to verify if shutter efficiency and charge conservation depend on the position where free electrons are released. Measuring with a laser allows for precise control where charge is released on the back of the detector, but is unable to release charge deeper within the bulk.
For the position-dependent measurements the same DHE sequence which is displayed in figure 6.9 is used. For this measurement the detector is divided into a grid. During the position-dependent laser scan the detector is moved so that the laser hovers over different points of the grid, while the laser remains stationary. For each grid point the laser is fired twice, once during normal and once during or shortly before gated mode operation. Thus the shutter efficiency and charge conservation can be measured. In the measurements in this thesis common mode correction, pedestal subtraction and threshold were disabled in the DHP settings and done manually.

Shutter efficiency

For the shutter efficiency measurement the detector was moved under the matrix in steps of 5 µm in both x and y direction. To calculate the shutter efficiency, pedestals were subtracted and common mode correction applied to the data. However, to measure the shutter efficiency no threshold was applied. This

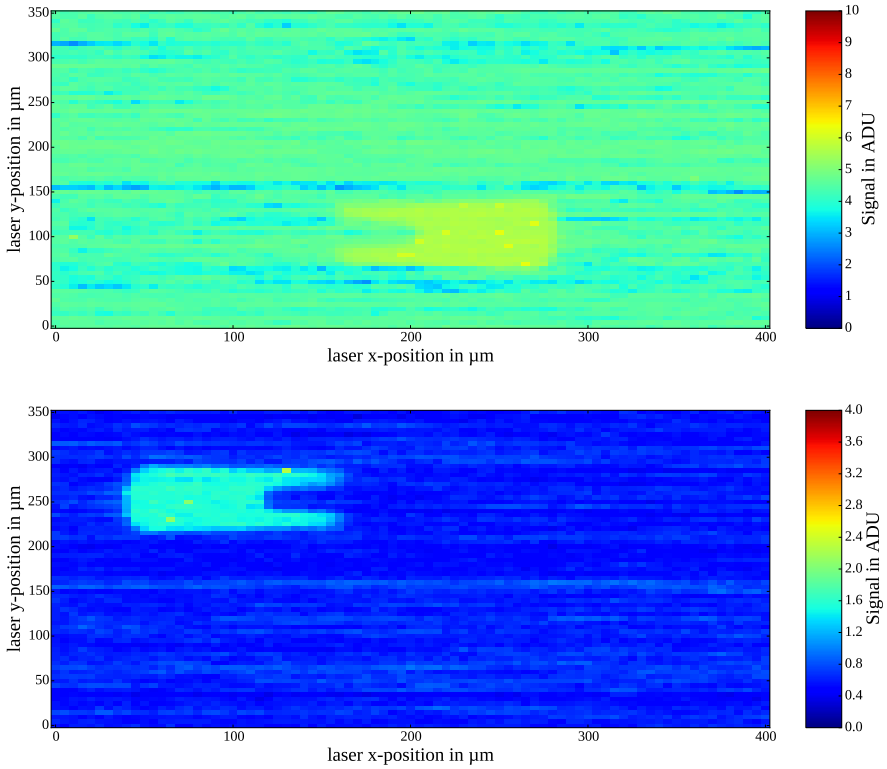


Figure 6.18: Top plot shows the average signal of a pixel for all laser positions. The bottom shows the same but for a different pixel. Figures illustrate non uniform change of pedestals after gated mode operation.

is due to the expected signal being close to 0 ADU, which is caused by the internal gate being shielded

while the laser is fired. Only slight changes in signal are expected, due to failed shielding. Because of omitting the thresholds a lot of additional hits are introduced in the matrix (see figure 6.17(a)). This noise causes the shutter efficiency to appear worse than it is. Hence, to limit the influence of noise on the measured shutter efficiency, the seed signals[12] are used to determine the shutter efficiency.
The additional noise hits, which are observed after gated mode operation, are caused by a shift in pedestal value of the pixels. Figure 6.18 shows the signal registered for each laser position for two pixels. The base value of the figure corresponds to a new pedestal value the pixel has after gated mode. The new base values of each pixel are calculated and used as new pedestal values. After a cooldown period the pedestal value falls back to its original value. The area where the signal is slightly increased corresponds to the pixel or a neighbouring pixel being hit. The signal of the two pixels remains almost equal, no matter if the pixel is hit in the center or a region which boarders on the next pixel. A possible explanation is that newly created charge, which is not successfully removed, stays within the bulk and forms a charge cloud as soon as gated mode becomes inactive. This charge cloud can spread to all bordering pixels equally. However, further measurements are necessary to understand this phenomenon. The top two graphs in

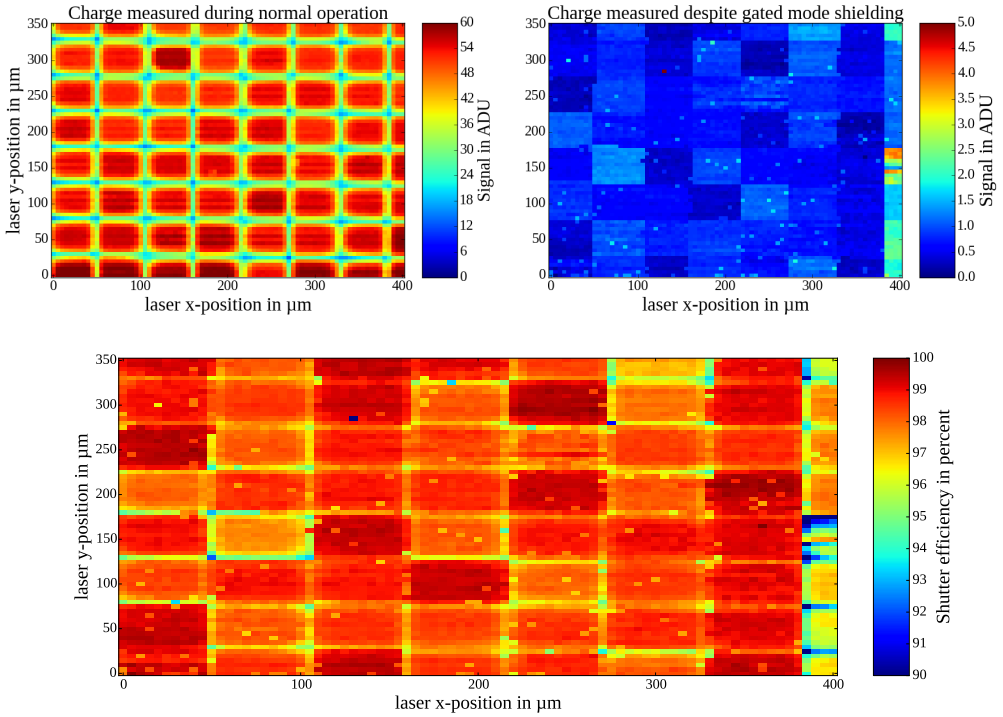


Figure 6.19: Top left reference how much charge was injected. Top right charge measured despite shielding from gated mode operation. Bottom shows the resulting shutter efficiency.

figure 6.19 show how much charge is injected into the observed pixel at the laser position and how much charge reaches the internal gate despite shielding. Looking at the top right side of figure 6.19 pixels seem to behave homogeneously.
In conclusion charge injected at the pixel boarders is not shielded any better or worse, but the additional threshold seems unable to completely get rid of differences in pedestal values. Overall the shutter

[12] When a laser is shot between pixels the created electrons are divided between two or more pixels. The seed pixel is the pixel with the largest signal.

efficiency across all measured pixels is:

$$(98 \pm 1)\,\%$$

Thus the shielding efficiency is close to a 100 %, which will allow gated mode to decrease the effects of noisy bunches strongly. Furthermore it appears that the shielding efficiency does not depend on the position where charge is injected into the matrix.

Preservation efficiency

For the preservation efficiency measurement the detector was moved under the matrix in steps of 5 µm in both x and y direction. In the preservation efficiency measurement the laser was shot shortly before gated mode has activated. After the gated mode sequence the pixel is read out in normal operation. Ideally the potential wall between internal gate and clear contact would preserve all charge within the internal gate. In reality not all charge is preserved, as some tunnels from the internal gate to the clear contact. For the preservation efficiency measurement pedestal subtraction, common mode correction and threshold were applied. Figure 6.20 sums up the results from the preservation efficiency measurement. The seed

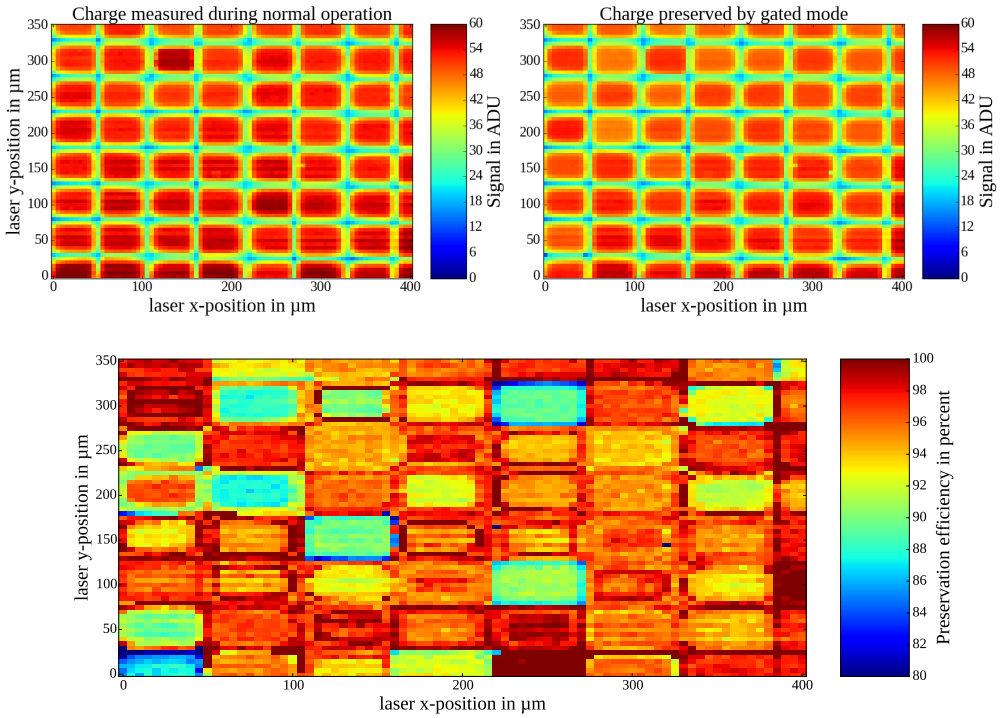


Figure 6.20: The top left shows charge measured in ADU after laser was fired during gated mode operation. The top right shows the remaining charge after gated mode operation. The bottom depicts the resulting preservation efficiency.

signal[13] was used to create the plots. The figure on the top left depicts the charge measured when the laser is fired during normal operation. In the top right figure the laser is fired shortly before gated mode operation and the signal of the seed pixel is read out afterwards. The pedestal values were adjusted for fluctuations caused by gated mode. Thus the figure shows how much charge is preserved during gated mode operation. The bottom figure shows the resulting preservation efficiency which is obtained by dividing the signal measured after gated mode operation by the reference signal. There are differences in preservation efficiency between pixels in the order of 5 % which could in part be caused by pedestal fluctuations, which were not filtered successfully (see figure 6.17(a)). If the laser is shot close to a pixel border the efficiency increases. The reason for that lies in the potential of the internal gate. When the external gate is switched off a positive potential is applied. This raises the potential of the internal gate, which couples to the external gate, and creates a potential barrier between clear contact and the internal

[13] When a laser is shot between pixels the created electrons are divided between two or more pixels. The seed pixel is the pixel with the largest signal.

gate. This potential barrier shields the charge stored within the internal gate (see figure 2.7). Electrons stored within the internal gate lower the potential of the internal gate and influence the potential barrier. Thus less charge within the internal gate lowers the probability for electrons to tunnel through to the clear contact. As there are fewer electrons[14] stored within the internal gate of the seed pixel if the laser is shot close to a pixel border, the preservation efficiency increases. Taking the average of all laser positions the resulting preservation efficiency is:

$$(96 \pm 5)\,\%.$$

The preservation efficiency is close to a 100 %. As the amount of electrons in the internal gate influences the preservation efficiency, it is not fully position independent. But for all laser positions the preservation efficiency stays above 80 %. Furthermore, the preservation efficiency is not subject to strict requirements. As long as a signal which would have been recognized as a hit is still larger than the threshold after gated mode operation, the requirements are met. As the preservation efficiency increases for smaller numbers of collected electrons, this should be the case.

[14] The rest of the charge is shared with bordering pixels.

CHAPTER 7

Summary and Outlook

The KEKB accelerator is being upgraded to create B mesons in e^+e^- collisions at a higher luminosity. The higher particle rate creates the necessity to upgrade the Belle detector to the new Belle II detector. The detector and ASICs need to withstand the ensuing radiation at the experiment.
The refilling of bunches during superKEKB operation will cause noisy bunches. The pixel detector needs to be able to filter out the noisy bunches. This filtering is accomplished by gated mode operation. It preserves the charge within the internal gate while preventing any additional electrons from reaching the internal gate.

The analogue to digital conversion of the DCD was tested, using the DHE current source. The goal was to develop new quick algorithms to ease future DCD optimisation. A DCD was optimised using the newly developed algorithms and methods the ideal parameters were found to be:

$$\text{IPSource} = 105 \text{ DAC units}$$
$$\text{IPSource2} = 95 \text{ DAC units}$$

$$\text{AmpLow} = 400\,\text{mV}$$
$$\text{RefIn} = 875\,\text{mV}$$

The stability of the ideal operation point was tested under irradiation. For that purpose a second DCD was irradiated up to 40 kGy. The ideal operation point remained stable during the irradiation. Both DCDs could be operated close to optimal settings with the same AmpLow and RefIn voltages.

The behaviour of the ASICs and the DEPFET was investigated using an oscilloscope. The goal was to understand how different internal signals influence operation and what steps need to be undertaken to switch DEPFET into gated mode dynamically. The important timings between internal components were measured using the 62.5 MHz reference clock. Measurements to determine how much time is required to upload the veto command to the DHP ((290.95 ± 0.05) ns) and for the Switcher to go into gated mode were conducted. Furthermore the delay between issuing the command to fire the laser and the laser firing was measured. The timings were determined to be:

DHE-DHP: (290.95 ± 0.05) ns

DHE-Laser: (30.5 ± 0.5) ns

DHP-Switcher: (105 ± 65) ns

After achieving gated mode operation, measurements were conducted to investigate the properties of gated mode. The time required to switch the DEPFET sensor into gated mode was measured directly by shooting the laser onto the matrix. Using the numbers from the oscilloscope measurements the time to go into gated mode was determined to be (418 ± 14) ns, starting from the moment the veto signal is uploaded to the DHE memory. Furthermore the time to go out of gated mode was determined to be (129 ± 13) ns. Finally the deadtime of the small PXD9 matrix used in this thesis was determined to be:

$$(258 \pm 16)\,\text{ns} + \text{time spent in gated mode} + (760 \pm 207)\,\text{ns}$$

With the first component stemming from the time which is required to go in and out of gated mode and the last term being added to ensure noise occupancy is at a level which does not influence data taking. The operation voltages of the DEPFET sensor were optimised to improve gated mode performance. The shielding and preservation efficiency were optimised by determining the ideal operation point in the GateOff and ClearHigh parameter space. In addition the amount of noise hits was reduced by optimising the ClearLow and ClearHigh parameter space. The suggested voltages were determined to be:

GateOff: 3 V

ClearHigh: 19 V

ClearLow: 6 V

Finally position dependent measurements were conducted with the laser. The laser scans contain information on the homogeneity of the shielding and preservation efficiency across the detector surface. The results of the measurements were for the shielding efficiency:

$$\eta_{\text{Shield}} = (98 \pm 1)\,\%.$$

While the result for the preservation efficiency was:

$$\eta_{\text{Preservation}} = (95 \pm 3)\,\%.$$

The measured efficiencies should warrant that with threshold applied the charge stored within the internal gate is preserved and no additional hits are registered. There is a good chance that gated mode operation will be used in the Belle 2 experiment. The measurements were successful overall.

It is unlikely that gated mode will be used right from the start of Belle II operation. Only higher occupancy will create the necessity to filter noisy bunches. Thus there is time to further investigate gated mode operation. Future measurements could research how the charge stored within the internal gate influences preservation efficiency and how the charge injected influences shutter efficiency. Furthermore capacitances between drain and clear lines could be investigated to figure out their influence on the increased noise occupancy. Measurements concerning dead time with the final Belle II DEPFET modules were already conducted by the time this thesis is being written, but are still unpublished.

Appendix

APPENDIX A

Gated mode

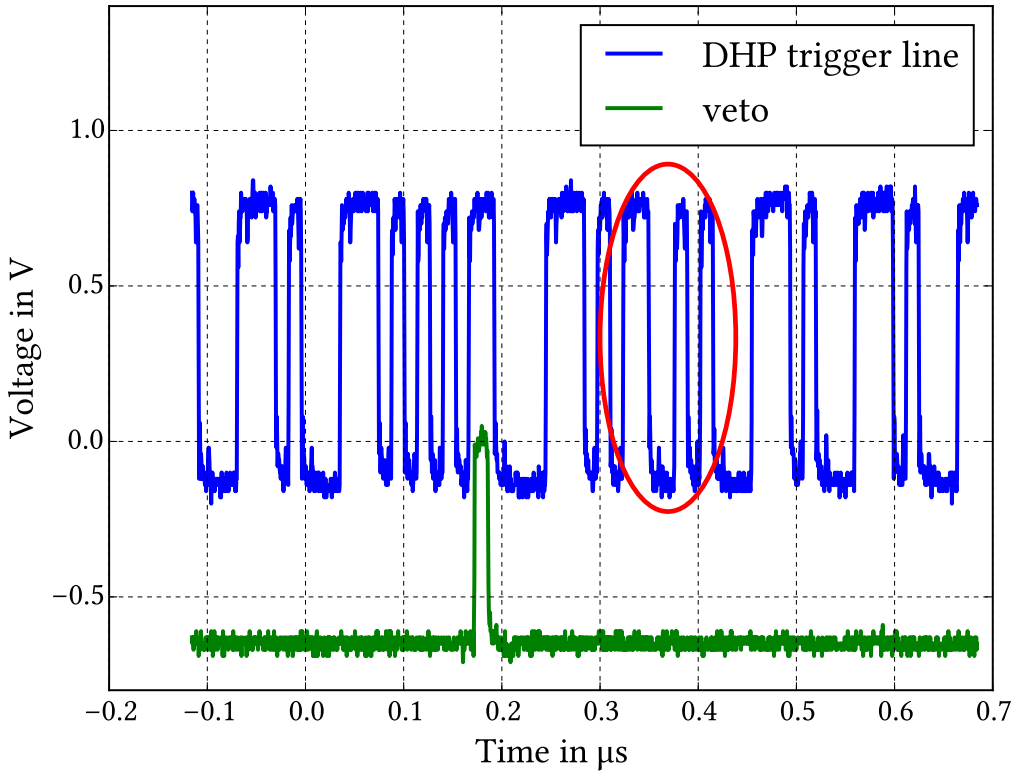


Figure A.1: When sending the veto signal across the DHP trigger line, the system behaves just as it did with the DHP trigger.

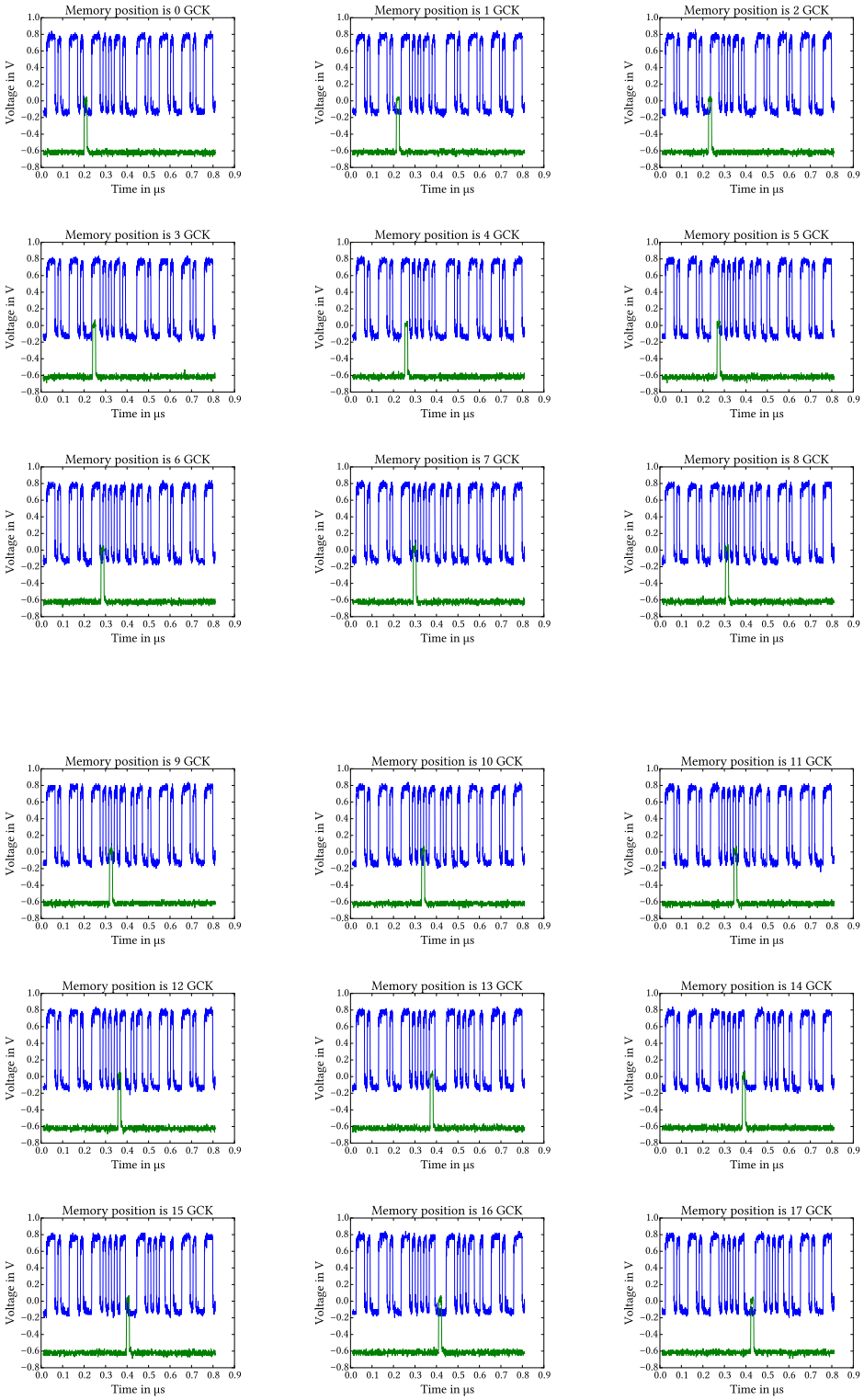


Figure A.2: Starting from memory positions 5 and 13 the DHP trigger information is transmitted one gate later.

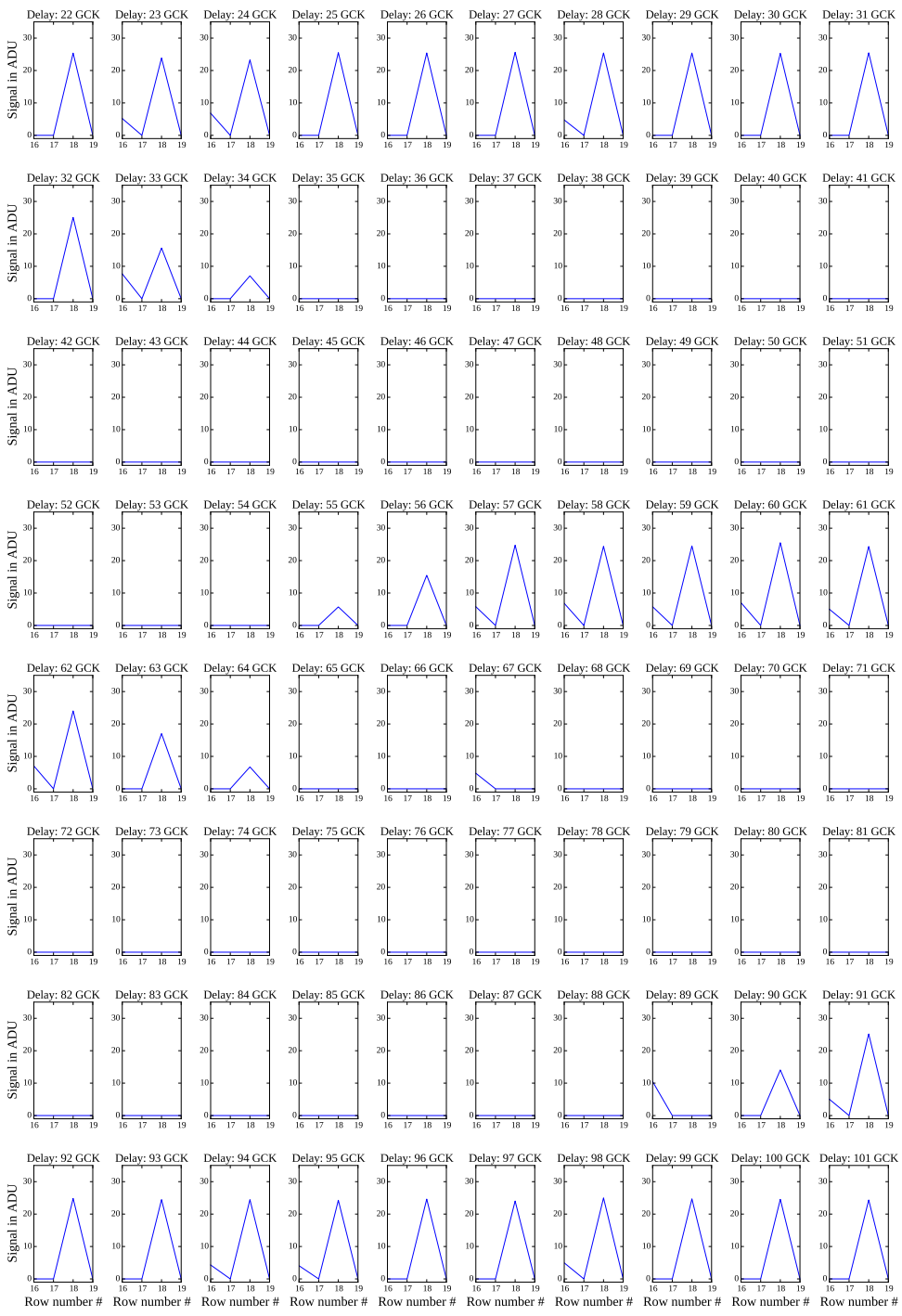


Figure A.3: A pixel which is read out during gated mode is observed. The laser is delayed against the veto signal. The fourth frame is used to check when gated mode was active.

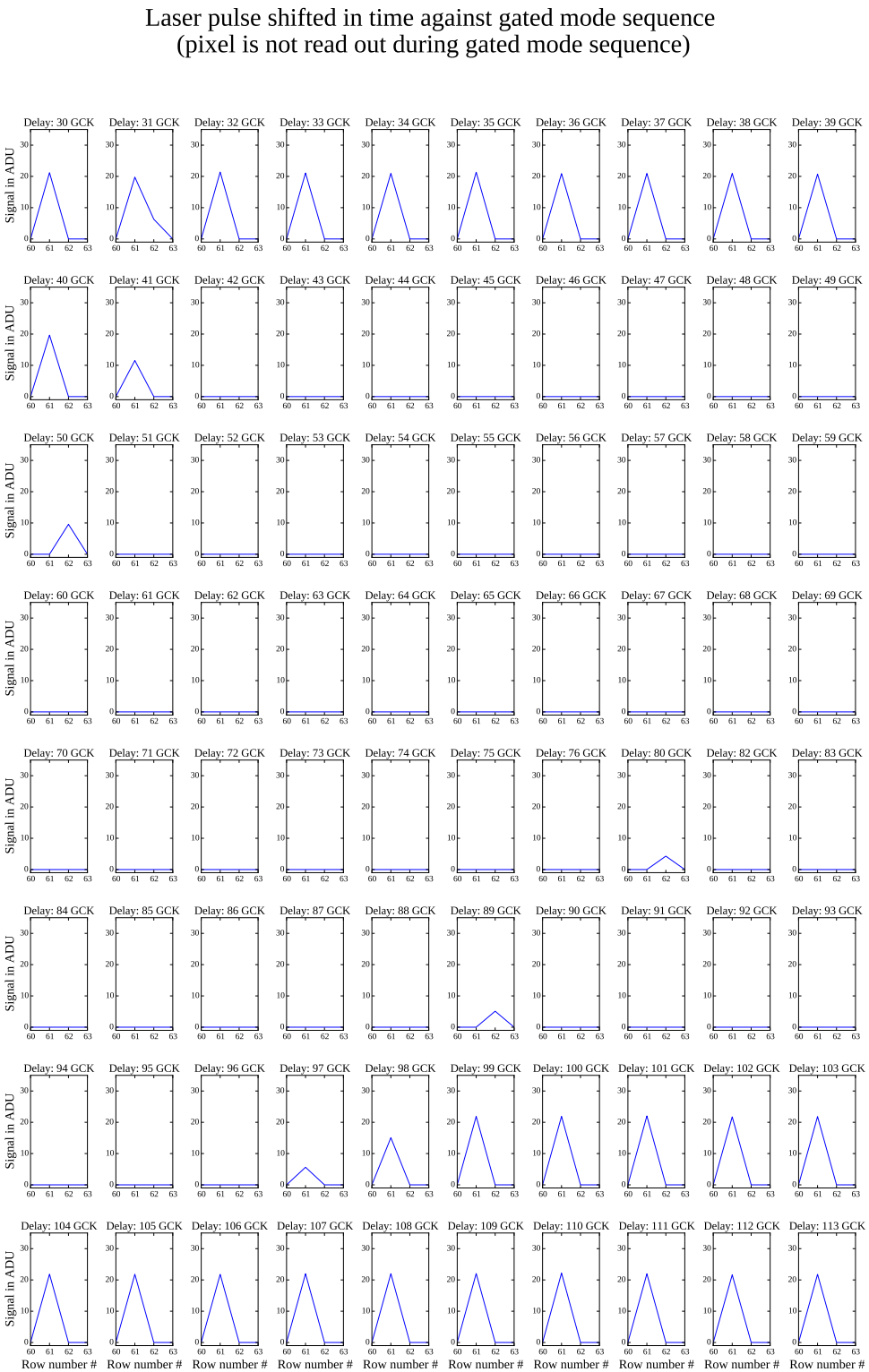


Figure A.4: A pixel which is not read out during gated mode is observed. The laser is delayed against the veto signal. The fourth frame is used to check when gated mode was active.

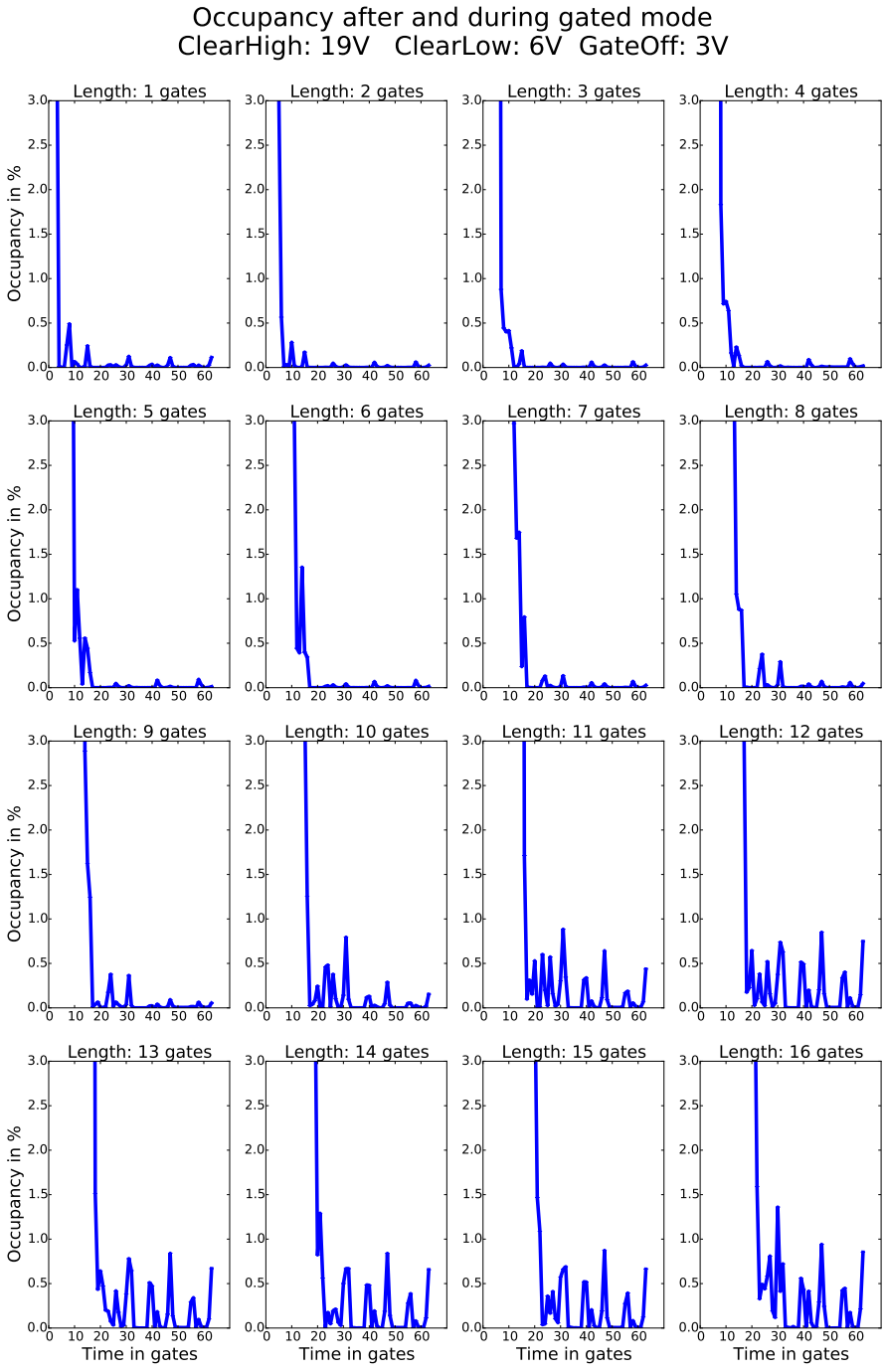


Figure A.5: The figure shows the occupancy of each gate during and after gated mode for different lengths of the gated mode sequence.

APPENDIX B

Configuration

Table B.1: Standard configuration used in the thesis unless specified otherwise. The Hybrid 5 used in this thesis had the serial number H5.007. All DEPFET voltages except for Source are given relative to Source.

DEPFET	
Parameter	Value of the voltage in V
Source	7
GateOff	3
GateOn	-2.5
Bulk	10
ClearLow	6
ClearHigh	19
ClearGate	-1
HighVoltage	-70
Drift	-5
Guard	-5
ASICS	
Parameter	Value of the voltage in mV
SW-dvdd	1800
AmpLow	400
RefIn	875
DCD-avdd	1900
DCD-dvdd	2100
DHP-core	1540
DHP-io	2000
DCD	
Parameter	Value of the parameter in DAC units
IFBPBias	90
IPSource	105
IPSource2	95
Laser (mode set to Ext-Width)	
EXT-IN threshold	−0.2 V
LeadE	3 ns
Voltage	1.75 V

Table B.2: Test criteria used in the DCD optimisation. Measured values were required to be smaller/larger than the provided limit.

DEPFET	
Parameter	Limit
ADC range	> 200 ADU
Linearity (χ^2_{reduced})	< 5
Noise	< 1.2 ADU
Missing codes	< 2 consecutive missing codes
Missing codes (test 2)	< 3 consecutive missing codes

References

[1] J. H. Christenson et al., *Evidence for the 2π Decay of the K_2^0 Meson*, Phys. Rev. Lett. **13** (4 1964) 138, URL: http://link.aps.org/doi/10.1103/PhysRevLett.13.138 (cit. on p. 1).

[2] M. Kobayashi and T. Maskawa, *CP-Violation in the Renormalizable Theory of Weak Interaction*, vol. 49, Progress of Theoretical Physics, 1973 652 (cit. on p. 1).

[3] S. W. Herb et al., *Observation of a Dimuon Resonance at 9.5 GeV in 400-GeV Proton-Nucleus Collisions*, Phys. Rev. Lett. **39** (5 1977) 252, URL: http://link.aps.org/doi/10.1103/PhysRevLett.39.252 (cit. on p. 1).

[4] A. J. Bevan et al., *The Physics of the B Factories*, Eur. Phys. J. **C74** (2014) 3026, arXiv: 1406.6311 [hep-ex] (cit. on p. 2).

[5] K. A. Olive et al., *Review of Particle Physics*, Chin. Phys. **C38** (2014) 090001 (cit. on p. 2).

[6] S. Kurokawa and E. Kikutani, *Overview of the KEKB accelerators*, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment **499**.1 (2003) 1, KEK-B: The {KEK} B-factory, ISSN: 0168-9002 (cit. on p. 2).

[7] T. Abe et al., *Achievements of KEKB*, PTEP **2013** (2013) 03A001 (cit. on p. 2).

[8] Z. Doležal and S. Uno, *Belle II Technical Design Report*, High Energy Accelerator Research Organization, 2010 20 (cit. on pp. 2, 4).

[9] F. Dydak, *Results from LEP and the SLC*, CERN-PPE-91-14. CERN-ALEPH-PUB-91-046, 1991 44 p (cit. on p. 2).

[10] J. Kemmer and G. Lutz, *New detector concepts*, vol. 253, Nuclear Instruments & Methods in Physics Research, Section A, 1987 356 (cit. on p. 2).

[11] M. Koch, *Development of a Test Environment for the Characterization of the Current Digitizer Chip DCD2 and the DEPFET Pixel System for the Belle II Experiment at SuperKEKB*, Presented 05 Sep 2011, PhD thesis: Universität Bonn, 2011 (cit. on pp. 3, 6, 7, 10, 20).

[12] H. Kolanoski and N. Wermes, *Teilchendetektoren*, Springer Spektrum, 2016 (cit. on p. 4).

[13] T. Osamu, "15th International Workshop on Vertex Detectors", *Belle SVD status & upgrade plans*, 2006 19, URL: https://indico.cern.ch/event/1151/contributions/63338/attachments/49505/71156/Tajima.pdf (cit. on p. 4).

[14] A. Abashian et al., *The Belle detector*, vol. 479, 1, Detectors for Asymmetric B-factories, 2002 117, URL: http://www.sciencedirect.com/science/article/pii/S0168900201020137 (cit. on p. 4).

[15] M. Lemarenko, L. Germic and T. Hemperek, *Data Handling Processor Manual*, 2016 (cit. on pp. 4, 14).

[16] P. Ruiz-Valls and C. Marinas,
The ultra low mass cooling system of the Belle {II} {DEPFET} detector,
Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment **731** (2013) 280, {PIXEL} 2012, ISSN: 0168-9002,
URL: http://www.sciencedirect.com/science/article/pii/S0168900213003641
(cit. on p. 6).

[17] H.-G. Moser, *The Belle {II} {DEPFET} pixel detector*, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment **831** (2016) 85, Proceedings of the 10th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors, ISSN: 0168-9002,
URL: http://www.sciencedirect.com/science/article/pii/S0168900216002540
(cit. on pp. 8, 9).

[18] J. C. Hönig, *Charakterisierung eines DEPFET-Detektors*,
MA thesis: Physikalisches Institut Universität Bonn, 2013 (cit. on p. 9).

[19] E. Prinker, *Testing of the Gated Mode for the Belle II Pixel Detector*,
MA thesis: Ludwig-Maximilians-University Munich, 2015 (cit. on p. 10).

[20] A. Ritter et al.,
Investigations on radiation hardness of {DEPFET} sensors for the Belle {II} detector,
Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment **730** (2013) 79, ISSN: 0168-9002,
URL: http://www.sciencedirect.com/science/article/pii/S0168900213004956
(cit. on pp. 11, 31, 32).

[21] F. Berends, P. Daverveldt and R. Kleiss, *Monte Carlo simulation of two-photon processes*,
Computer Physics Communications **40**.2 (1986) 285, ISSN: 0010-4655,
URL: http://www.sciencedirect.com/science/article/pii/0010465586901153
(cit. on p. 11).

[22] T. R. Oldham and F. B. McLean, *Total ionizing dose effects in MOS oxides and devices*,
IEEE Transactions on Nuclear Science **50** (2003) 483 (cit. on pp. 11, 34).

[23] J. Haidl,
Readout Optimization for the Belle II Pixel Detector – Characterization by ADC Transfer Curve,
MA thesis: Ludwig-Maximilians-University Munich, 2016 (cit. on pp. 15, 19).

[24] K. Schmieden, *Charakterisierung einerneuen Generation von DEPFET-Sensoren mit Hilfe eines Lasermesssystems*, MA thesis: Universität Bonn, 2008 (cit. on p. 17).

[25] P. F. Ivan Perić Christian Kreidl, *DCD-Bv4-Pipeline Reference Manual*, 2015 (cit. on pp. 20, 21).

[26] C. M. Botho Paschen Leonard Germic, *Irradiation campaign at KIT*, private communication (cit. on p. 31).

[27] *MSO4000B, DPO4000B Series Data Sheet*, 2016,
URL: http://www.farnell.com/datasheets/866462.pdf (cit. on p. 39).

[28] D. Levit, personal communication, 2016 (cit. on p. 40).

[29] C. Marinas, personal communication, 2013 (cit. on p. 52).

[30] M. Boronat Arevalo, *BELLE II pixel detector*, PoS **VERTEX2015** (2015) 014 (cit. on p. 56).

[31] A. Moll, *Comprehensive study of the background for the Pixel Vertex Detector at Belle II*, PhD thesis: Ludwig-Maximilians-University Munich, 2015 (cit. on p. 56).

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