Belle II Pixel Detector Commissioning and Operational Experience

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The Belle II experiment at the Super Flavour Factory SuperKEKB in Tsukuba, Japan, has started regular operation with its final detector setup in spring 2019. The Belle II vertexing system consists of four layers of double sided silicon strips (SVD) and two layers of DEPFET pixel sensors (PXD). These inner most pixel layers are arranged at radii of 14 mm and 22 mm around the beam pipe. The sensors with pixel sizes down to 50 $\mu m \times$ 55 μm are thinned down to 75 μm thickness to minimize multiple scattering. They are most crucial for reconstructing the secondary decay vertices of short lived B and D mesons with a precision of better than 15 microns. The high luminosity and harsh background conditions impose challenges on the operation of the detector close to the interaction point.

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1. Introduction

The Belle II experiment at the SuperKEKB facility in Japan started taking data in regular operation with a complete detector setup in spring 2019. SuperKEKB is an electron-positron collider with beam energies of $4\,\text{GeV}$ (e^+) and $7\,\text{GeV}$ (e^-) and a design instant luminosity of $8 \times 10^{35}\,\text{cm}^{-2}\,\text{s}^{-1}$, exceeding that of its predecessor KEKB by a factor of 40. The increased luminosity is achieved by a modest increase in beam currents, but mainly by squeezing the beam sizes to the sub-micrometer scale ($\delta y < 50\,\text{nm}$) in the interaction region, using the so-called nano-beam scheme [1].
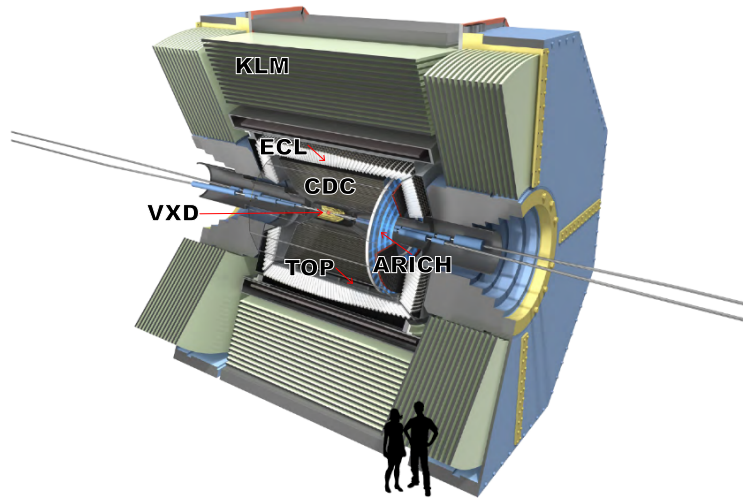
2. Belle II Detector Setup
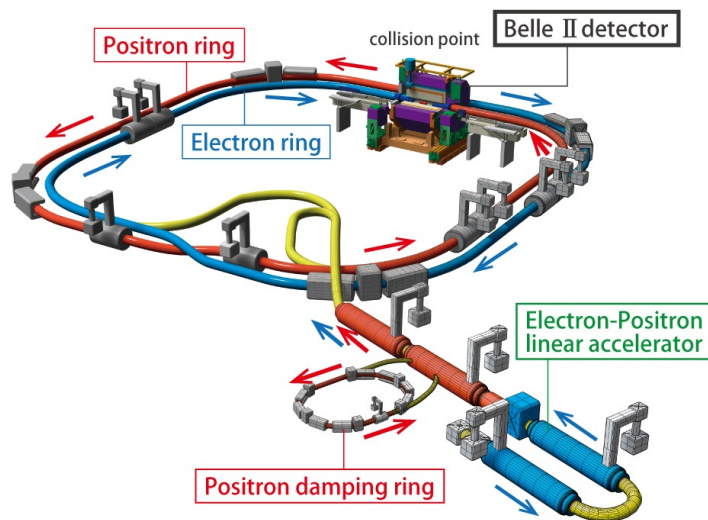
Figure 1: Sketch of the SuperKEKB electron-positron collider.

The Belle II detector consists of several specialized sub-detectors [2]. From the interaction point outwards they start with the vertex detectors, consisting of a silicon pixel and a strip detector (PXD and SVD), surrounded by the main tracking device, the central drift chamber (CDC), followed by the particle identification detectors consisting of a time-of-propagation device in the barrel (TOP) and the aerogel RICH in the forward region. The setup is completed by an electromagnetic calorimeter (ECL) and a K_{long}/muon counter (KLM) embedded in the solenoid's return yoke (Fig. 2).

The physics program of Belle II covers a wide range of topics. An excellent secondary decay vertex resolution is mandatory for, but not only limited to, studies of CP-violation in decays of short lived B and D mesons. This requires vertex detectors close to the interaction point which can provide sufficient position resolution even with the large background and radiation levels expected at design luminosity. The DEPFET-based pixel detector for the inner two layers is fulfilling this requirement [3, 4].

Figure 2: Sketch of the Belle II detector. See the text for a detailed description.

3. The DEPFET-based Pixel Detector

The pixel detector provides the two inner layers for the vertex detector. It is based on a mono-lithic and self-supporting silicon module. The working principle is based on a fully depleted p-channel FET (DEPFET) where the charges generated by traversing particles are collected within an internal gate. The first (second) layer is situated directly outside of the 20 mm diameter beam pipe at a radius of $r_1 = 14$ mm ($r_2 = 22$ mm) and consists of 8 (12) ladders. Due to a delay in the last step of production, the gluing of two modules together to one ladder, only two ladders of the outer layer have been installed together with the complete inner layer in the current setup (Fig. 3). The installation of the fully populated PXD is foreseen during the next long shutdown.

To minimize multiple scattering, the sensor region of the module is thinned down to 75 μm. The readout ASICs are placed outside of the acceptance of the detector. Altogether the material budget inside the detector acceptance is smaller than 0.21 % of X_0 per layer. The active area of each module is segmented into 250×768 pixels with sizes ranging from (50×55) μm^2 in the center of the inner layer to (50×85) μm^2 in the outer layer. Altogether the full PXD consists of nearly 8 million pixels. The detector is read out in a rolling shutter mode with a 50 kHz frame rate. This is controlled by the Switcher ASICs at the side of the module, which successively activate the read-out of four rows of pixels at a time and afterwards clear the stored pixel charges. During read-out the charge collected in the internal gate of each pixel is modulating the drain current which is measured by the DCD (Drain Current Digitizers) located at the end of the module. The DCD features an analog common mode correction and has switchable currents at the input to compress the spread of drain currents. After digitization the data is zero suppressed and formatted in the DHP (Data Handling Processor). The position of the ASICs on the outer ladders can be clearly seen in Fig. 4. The PXD modules are designed to withstand the expected 20 Mrad radiation dose during 10 year operation of the experiment.

SuperKEKB is now operating in top-up continuous injection mode for electron and positron
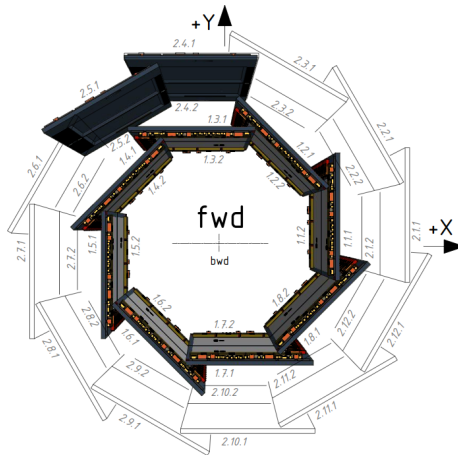
Figure 3: Schematic view of the 40 PXD modules (20 ladders) in beam direction. Only the colored modules are installed up to now.
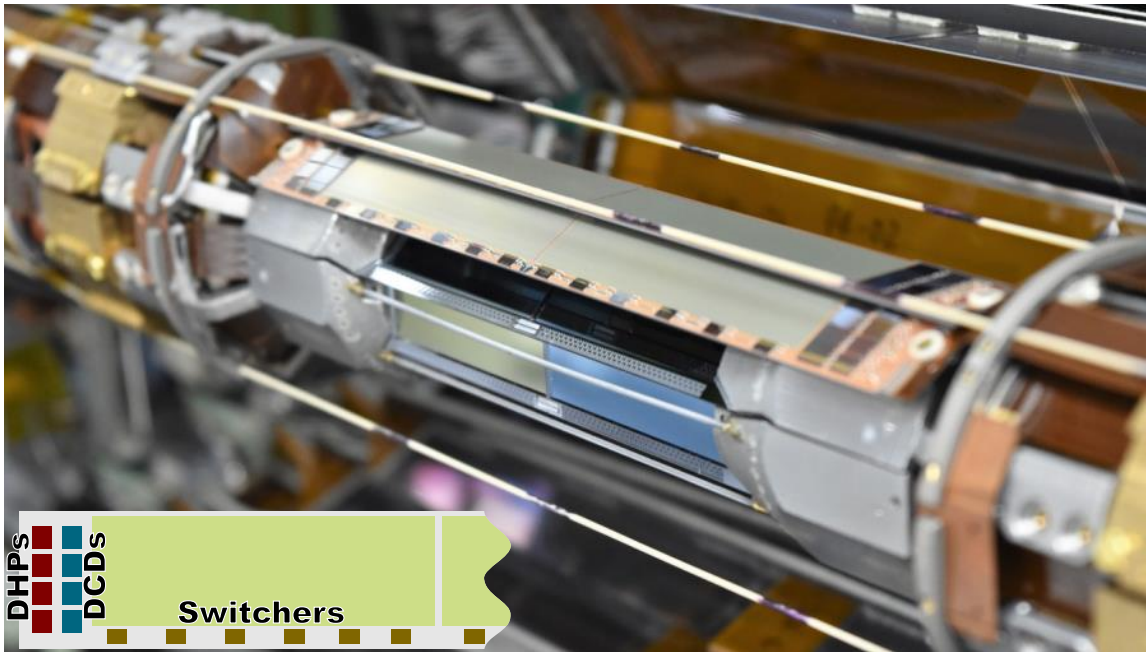
Figure 4: The pixel vertex detector after mounting on the central beam pipe. The inset indicates the position of ASICs on the visible outer layer modules. The DCD and DHP ASICs are located on the cooling block outside of the acceptance, the Switcher ASICs along the side of the modules. The ASICs of the inner layer modules are facing to the inside, thus they are not visible. Carbon cooling tubes for N_2 flow are located between the two layers. Around the second layer fibre optical sensors (FOS) are placed for temperature measurement in the vertex detectors volume.

beams at rates of up to 12.5 Hz per beam. In the first milliseconds after injection the affected bunches can cause large particle background rates each time they pass by the Belle II interaction point. While the trigger logic can veto during these times and therefore prevent data readout of other sub-detectors, this is not true for the PXD because of its large integration time of 20 μs, which corresponds to two bunch revolution cycles of the storage ring. To prevent the PXD from collecting signal charges during the passages of the bunch, the so called "gated mode" can be used. By changing the potentials in the sensor we can prevent newly created charges to enter the internal gate, while still preserving the already stored charges [7].

4. Read-out and Services

The position near the interaction point results in large background contributions to the overall occupancy of the pixel detector. Together with the long integration times, the data rate from the PXD alone amounts up to $10\,\mathrm{GB\,s^{-1}}$ which is 10 times the rate of the other Belle II sub-detectors combined. The mandatory data reduction is achieved in two ways: the High Level Trigger (HLT) will reject uninteresting events, thus reducing the event rate to less than one third. For the remaining events so called Regions of Interest (ROI) will be defined by extrapolating tracks reconstructed from CDC and SVD information back to the PXD planes. Only data within these rectangular areas is then sent to storage, hence reducing the event size by a factor of 10. Technically, this is done in the following way: Upon reception of a trigger, the data stored within the DHP memory is sent to the data handling hub system (DHH) [6] residing outside of the detector, which assigns the data to the correct event number and does sub-event building. If several triggers within one integration cycle are received, the fraction of data belonging to both events has to be duplicated. The output of each DHH unit is distributed by an event-based round-robin scheme to the selector nodes of the ONSEN [5] system. Here the data is buffered until the High Level Trigger has made a decision on the event and calculated the ROIs. The HLT decisions are received out of order, therefore the ONSEN system has to match the buffered data and select pixels within the ROIs. Afterwards the reduced output data is sent to the second event builder and storage. The whole readout path is designed to cope with a maximum mean pixel hit occupancy of 3 %, three times of what is expected in normal operation.

Each PXD module needs 23 independent supply voltages for its matrix and ASICs. These voltages are delivered by power supplies outside of the detector and vary for different modules. To make a PXD module operational, a specific sequence of power supply activation and ASIC configuration is required. This is implemented within the EPICS-based slow control system [8] that is used to interface with the read-out hardware, the cooling system, and the Belle II slow control. Configuration data for the modules, power supplies, and readout system is stored in a configuration database [9]. Control System Studio (CSS) is used for the monitoring of the system variables, log messages, and alarm system by the operators.

The pixel and silicon-strip vertex detectors share the same two-phase CO_2 cooling system as well as the temperature and humidity monitoring. For the PXD, most of the power is dissipated in the read-out ASICs at the end-of-stave, thus CO_2 cooling is limited to the area where the PXD ladders are fixed to the support and cooling blocks (Fig. 4). The active pixel matrix and the Switchers are sufficiently cooled by the forced nitrogen flow through holes along the carbon cooling tubes.

5. Operation

The PXD was operated during the spring 2019 run for several months without major problems. The working points for some modules had to be re-adjusted several times to improve the performance. New pedestals were taken to correct for small variations of the pixel operating point due to temperature or other environmental changes. Even without any radiation damage, new pedestals are needed as baseline for the signal calculation.

As a particle might generate charge in several pixels, hits from adjacent pixels are merged into a cluster. Fig. 5 compares the cluster charge for one inner and one outer layer module. Several peaks can be identified in the cluster charge distribution: The lower peak is mainly caused by low energy photons of ≈ 8 keV as it is dominated by single pixel clusters. Among the possible sources are diffuse reflected synchrotron photons and secondary x-ray photons. Low energy photons are mainly visible in the inner detector as they get absorbed in the detector material.

The main peak is dominated by multi-pixel clusters as most particles traverse the module at some incident angle. The signal in the main peak follows roughly a Landau distribution. For physics analysis, mostly clusters assigned to a particle track are relevant. Their distribution is scaled up by factor of 100 in the plots, which gives some indication of how much the signals in the pixel detector are dominated by background.
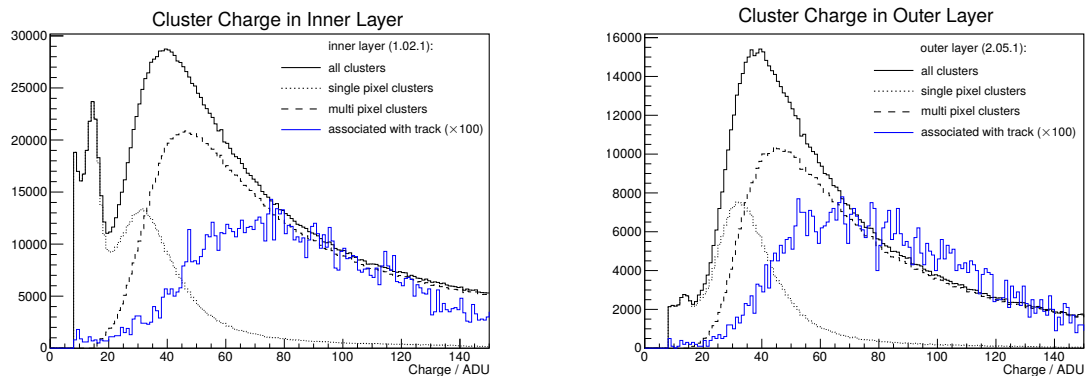
Figure 5: Cluster charge in inner and outer layers. The low energy peak is mostly gone in the outer layer. The distributions originating from single- and multi-pixel clusters (dotted and dashed) and the scaled distribution from clusters associated with a track (blue) are overlaid.

Radiation damage in the sensor mainly affects the readout FET structure of the DEPFET pixel. As a consequence the threshold voltage is increasing and the drain currents are getting smaller. The signal peak position is therefore shifted to lower values. This effect can be directly monitored in the supply line of the common source contact. The gate-on voltages were adjusted when the currents were getting too small.

The hit-efficiency of the modules has been determined by using particle tracking with information from the CDC and SVD. These tracks have been extrapolated to the pixel detector planes and checked for pixel clusters at the interception point. For most of the modules efficiencies above 98 % have been reached (fig. 6). The modules with significantly lower efficiency were not at an optimized working point at that time.

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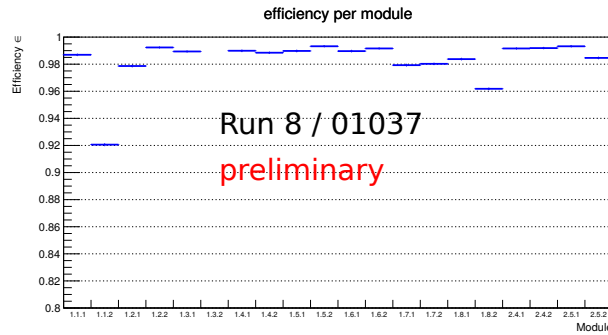
Figure 6: Efficiencies for all modules during spring run. The modules with significantly lower efficiency were not at the optimal working point. This was measured before the radiation bursts described in the text.

At two occasions, large radiation bursts hit the pixel detector just before the beam was aborted. One was estimated to deposit $\approx 300\,\mathrm{rad}$ within $40\,\mu s$ into the PXD. These resulted in two temporarily inoperational modules and several inefficient areas in nearly all modules. The two modules were finally recovered by increasing the current limits for the clear voltages. As the inefficient areas correspond to one gate/clear Switcher channel each, single event effects in the Switcher ASICs due to the short instantaneous radiation are the most probable reason.
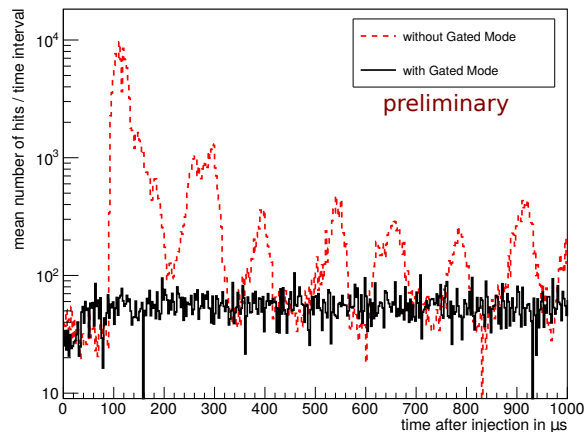
Figure 7: Comparison of the mean hit occupancies in one PXD module after injections in the positron ring with and without gated mode. The injected bunch passes the detector the first time at $t=100\,\mu s$. The gated mode can suppress the charge collection during the time the bunch is passing by.

First tests of the gated-mode operation have been performed and show that the background from continuous injections can be suppressed (Fig. 7). The blinding of the detector comes at the disadvantage of losing a fraction of the data during readout. Careful optimization of the parameters is needed to maximize the overall efficiency during gated-mode operation.

After calibration and alignment, the vertex resolution including data from PXD has been measured to $14.2\,\mu m$ [10]. Together with the first re-measurements of the life time of the D^0 meson this proves the quality of the recorded data as well as the calibration and alignment of the vertex detector.

6. Summary

Belle II is the first particle physics experiment to operate a DEPFET-based pixel detector. Physics data taking including the PXD started in 2019. We could demonstrate a good performance of the detector with efficiencies $> 98\%$ for most modules. Even with only the inner layer installed, the vertex resolution has been measured to $14.2\,\mu m$ and is close to Monte Carlo expectations. In two incidents large radiation bursts have hit the pixel detector just before a beam abort. This instantaneous radiation has most probably caused some single event effects in the Switcher ASICs, leading to inefficient areas on the sensor. The detailed reasons for this ASIC failure are under study. Meanwhile mitigation strategies like improvements of the SuperKEKB collimator system, faster beam abort, and a faster emergency power off for the pixel detector are being implemented.

The readout concept with Region of Interest feedback from the High Level Trigger has been proven to work, even so it is needed only when higher luminosity and backgrounds require significant data reduction.

Background especially from the continuous injection will be an issue when going to higher luminosities and beam currents. In a recent test we could show that the background from top-up injections can be sufficiently suppressed by employing the gated-mode operation of the PXD modules. The detector will be completed with the second layer during the next long shutdown, scheduled for 2021.

Acknowledgments

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