Upgrade to the Belle II Vertex Detector with CMOS pixel sensors

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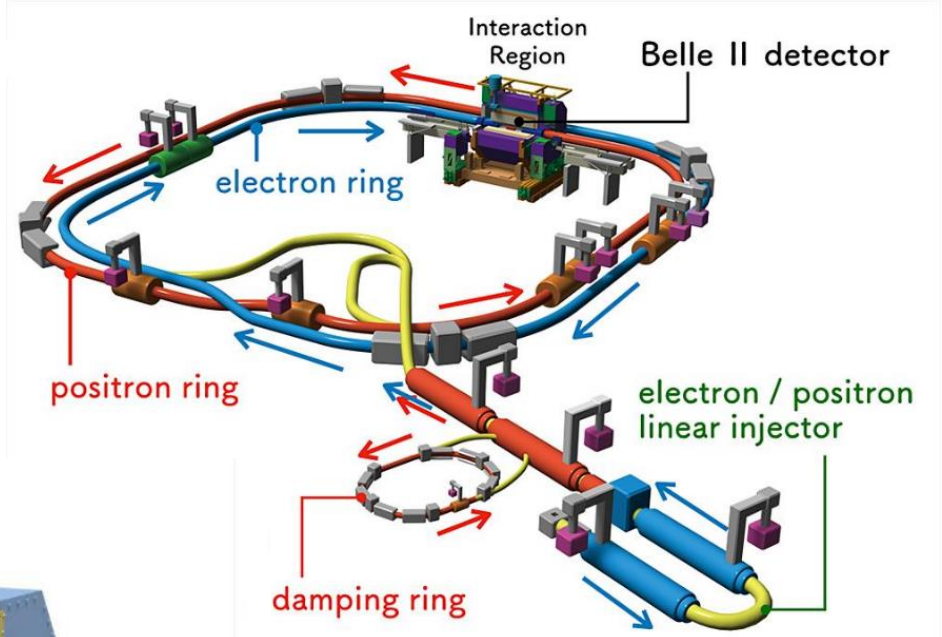
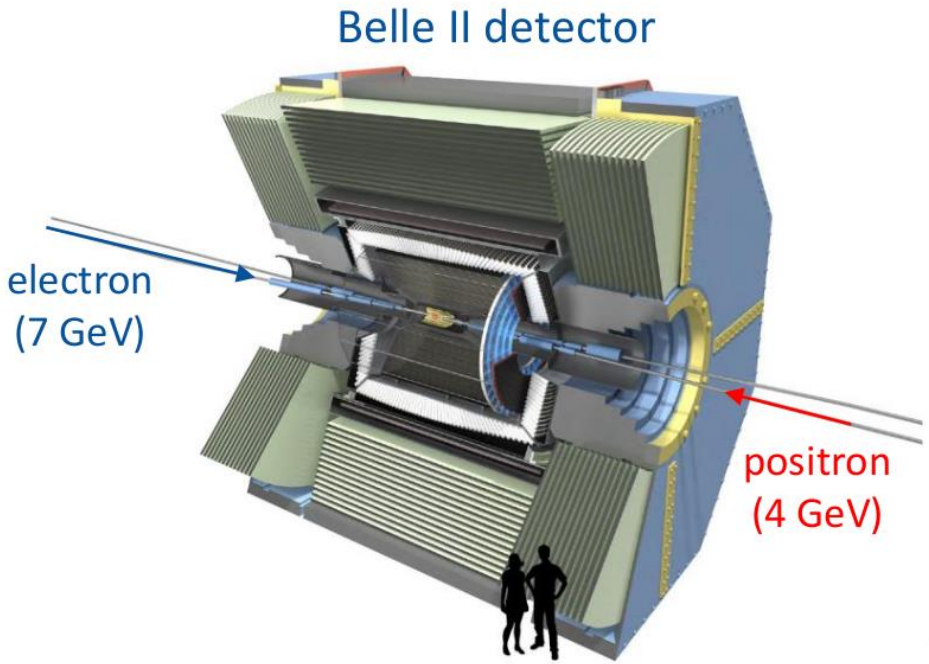
on behalf of the Belle II VXD upgrade collaboration

Belle II and SuperKEKB

Belle II experiment at the SuperKEKB collider

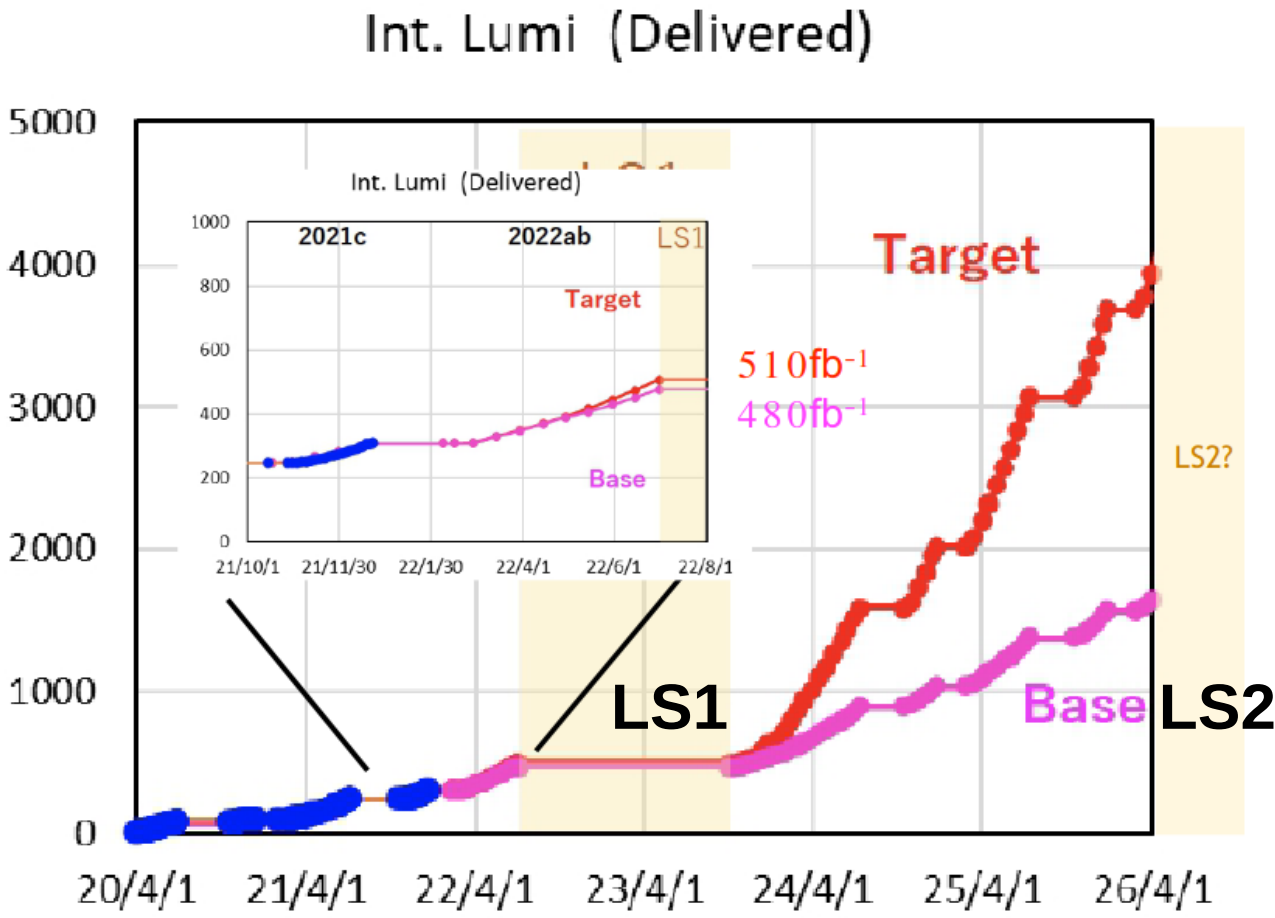
- Asymmetric $e^+ - e^-$ collisions at $\sqrt{s} = 10.58\,GeV$
- Luminosity-frontier experiment, exploring new physics
- Record peak luminosity $3.81 * 10^{34}\ cm^{-2}s^{-1}$
- Path to reach $2 * 10^{35}\ cm^{-2}s^{-1}$ identified
- Target of $6 * 10^{35}\ cm^{-2}s^{-1}$





Overview and Upgrade Timeline

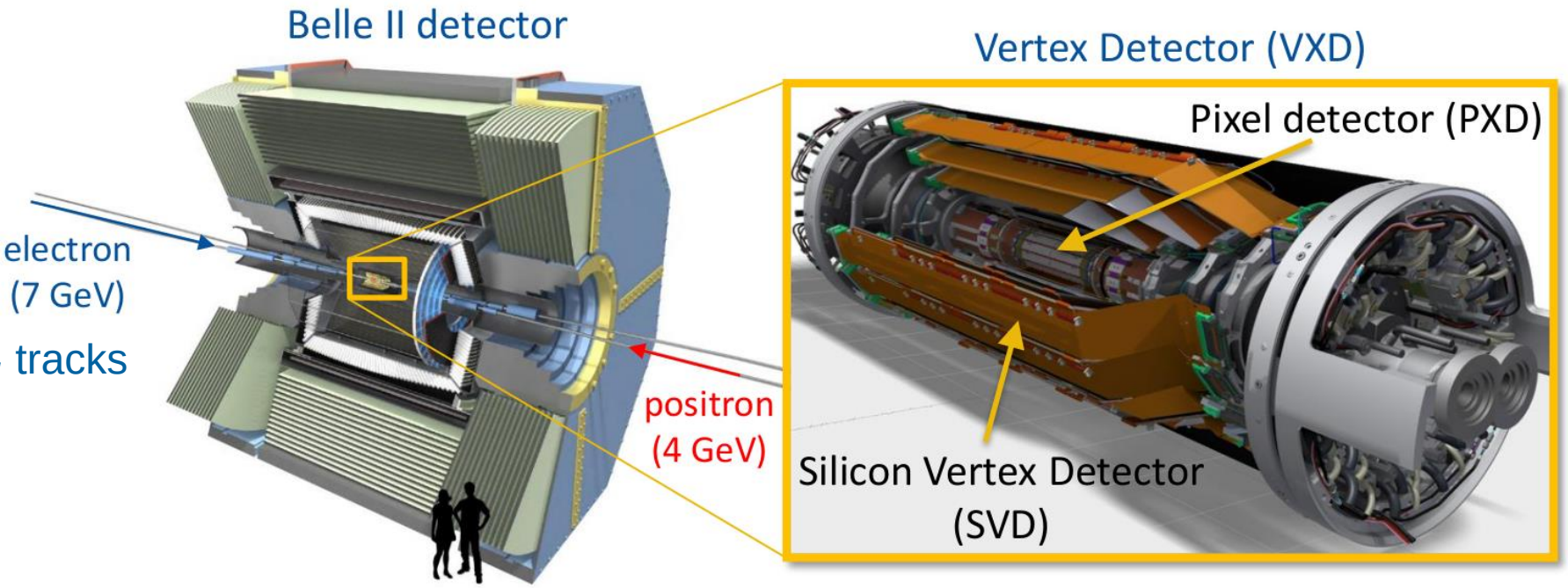
- Long Shutdown 1 (2022/23)
  - Exchange of pixel detector (PXD)
  - TOP-PMT replacement
- Long Shutdown 2 (2026/27)
  - SuperKEKB upgrade foreseen
  - Vertex detector upgrade
- Only few years till then
  - Need to utilize currently available technologies
- Several different options/technologies for a major upgrade of the vertex detector under discussion



Current Belle II Vertex Detector

- 2 inner layers of Pixel Detector (PXD):
  - DEPFET sensor, 50 µm x 55-85 µm pixels
  - ~15 µm spatial resolution
  - 20 µs integration time
  - 0.2%X_0 per layer
  - Layer 2 currently only partially installed
  - Completion of PXD planned for LS1 (2022/23)
- 4 outer layers of Silicon Vertex Detector (SVD):
  - Double-side silicon strip (DSSD) detector
  - ~12/25 µm spatial resolution
  - ~3 ns timing resolution
  - 0.7%X_0 per layer

- Roles of Vertex detector
  - Determine vertex position
  - Standalone tracking
  - PID using dE/dx for low p_T tracks



Vertex Detector Upgrade Motivation

- Limitations of current VXD
  - Tolerance for beam-induced background (BG)
    - Predicted occupancy in L3 will be about 3%, which is basically the limit for efficient tracking
    - Limit can be relaxed to 6% occupancy by hit-time reconstruction and BG rejection
    - Difficult to perform accurate BG prediction
    - Margin is small
  - Level 1 trigger latency
    - Belle II trigger latency is limited to 5 µs by SVD
    - Limited depth of APV25 trigger buffer
  - Tracking and vertexing performance
    - Tracking performance in low-pt limited by material budget
    - Room to improve vertex resolution with better hit position resolution
    - PXD is not used for track-finding

Requirements for an Upgrade

Radius range: R	14 – 135 mm (**)
Tracking & Vertexing performance at least as good as current VXD	
Single point resolution(*)	< 15 um
Total material budget	< (2*0.2% + 4*0.7%) X_0
Robustness against radiation environment	
Hit rate(*)	~ 120 MHz/cm^2
Total Ionizing Dose(*)	~ 10 Mrad/year
NIEL fluence(*)	~ 5.0 × 10^{13} n_{eq}/cm^2/year

K. Nakamura, Vertex 2021

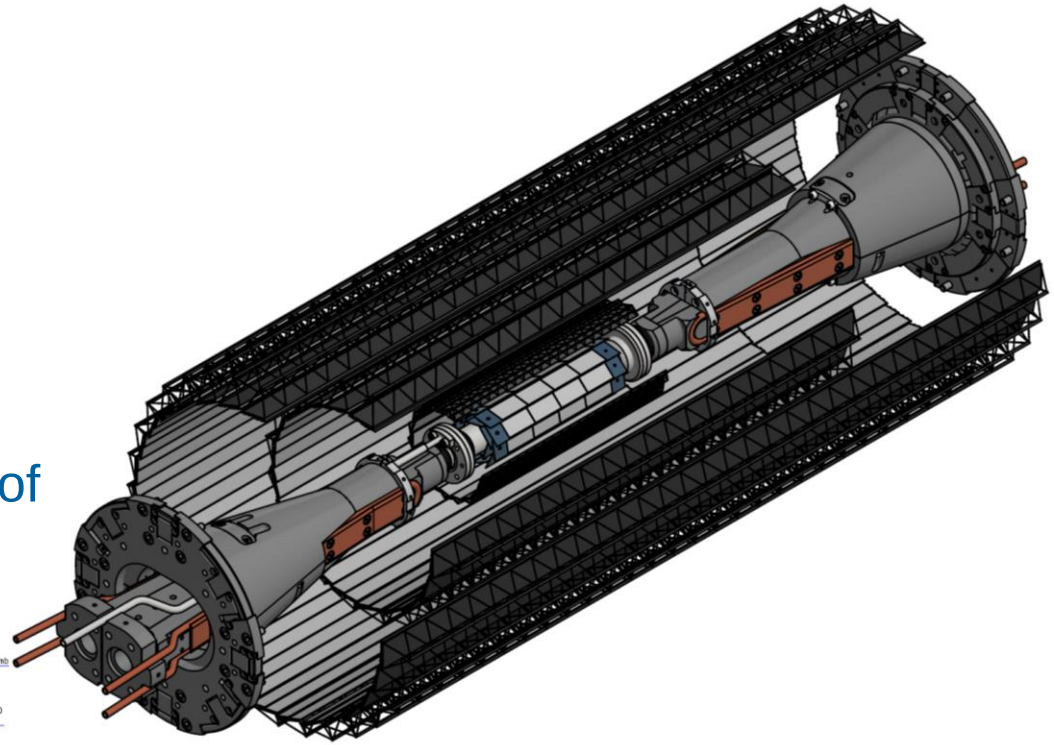
(*) requirement for the innermost layer (R=14mm)
(**) Optionally, we may include also the CDC inner region (135<R<240mm)

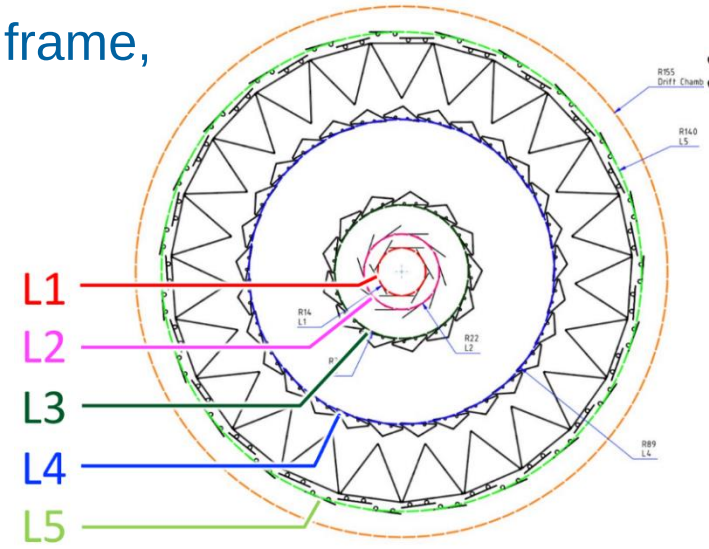
Vertex Detector Upgrade Options

- Several sensor technologies and concepts under discussion, R&D ongoing
  - **Thin DSSD sensor**
    - DSSDs with 140µm thickness and fine pitch (~85µm) on both sides
    - Dedicated front-end ASIC (SNAP128A) with lower noise, binary readout and long buffer for larger trigger latency
    - Target: outer layers (L3-L5)
  - **DEPFET pixel sensor**
    - Improvement of currently used pixel detectors, higher gain, faster ASICs
    - Target: inner layers (L1,L2)
  - **Silicon-on-isolator pixel (SOIPIX) sensor**
    - CMOS circuit produced on silicon wafer isolated by a buried oxide (BOX) layer
    - Fully depleted sensor, fast signal, good SNR
    - Dual Timer Pixel (DuTiP) concept: alternate operation of two timers allows detect next particle hit before the previous one is red out.
  - **Depleted monolithic active pixels sensors** (DMAPS)
    - Pixel sensor in CMOS technology
    - Based on TJ-Monopix2 R&D
    - Target: fully pixelated CMOS Vertex Detector (Belle II VTX)

CMOS VTX Concept

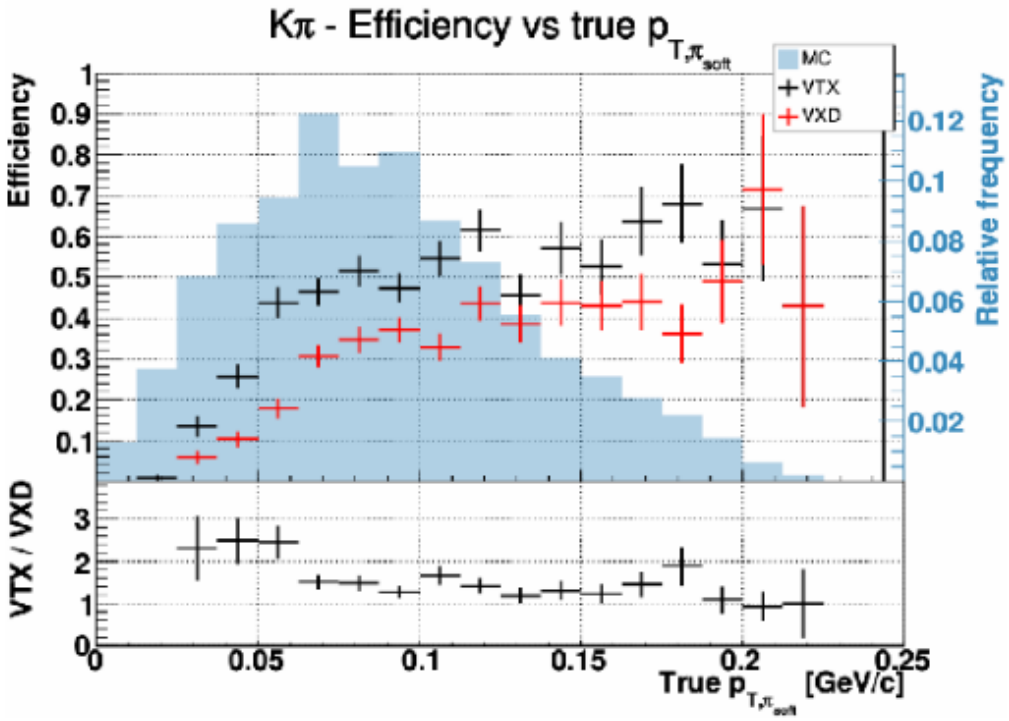
- 5 straight layers with DMAPS
  - Radii: ~14, 22, 39, 90, 140 mm
- Ladder / stave design
  - Chips are identical in all layers, but the ladder / stave concept is different depending on the layer (L1 is 14 cm long, L5 is 70 cm long)
  - **L1+L2 (iVTX):** All silicon ladders, air cooling, services out of the acceptance.
  - **L3+L4+L5 (oVTX)**: Support frame, cold plate, sensors, flex, power bus, water cooling

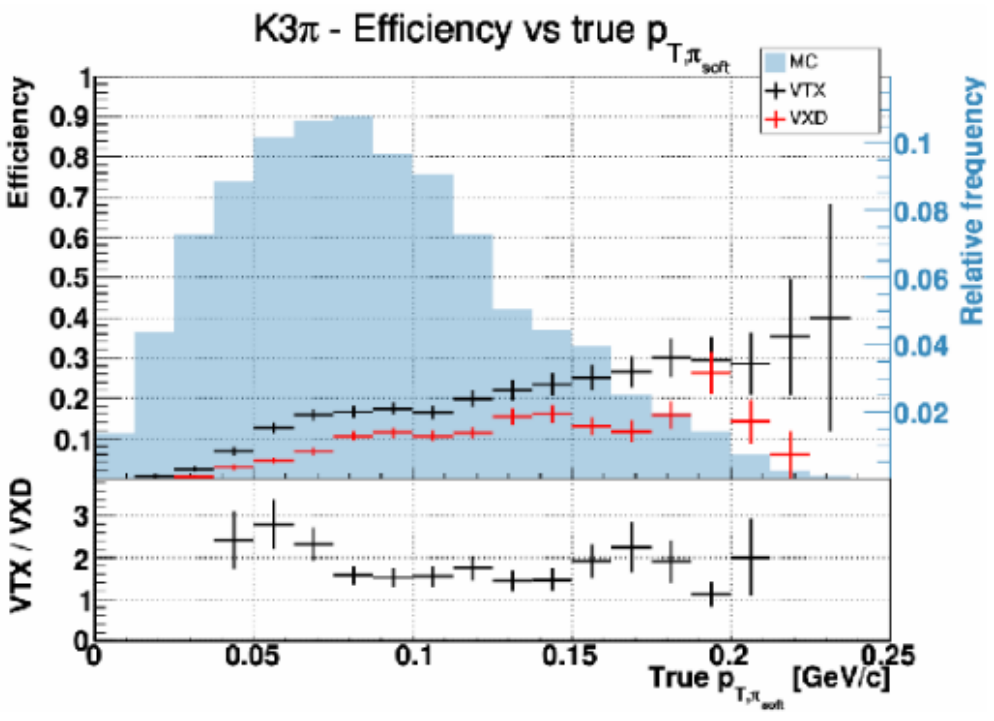




VTX Performance Simulation

- Expected performance of TJ-Monopix2 used for simulation
- Decay channel used: $B^0 \rightarrow D^* \mu\nu \rightarrow (D^0\pi)\mu\nu$ with $D^0 \rightarrow K\pi(\mu\mu)$
- Reconstruction efficiency increases x1.5 – x1.8
- Lower reconstruction limit from 75 MeV to 50 MeV for p_T





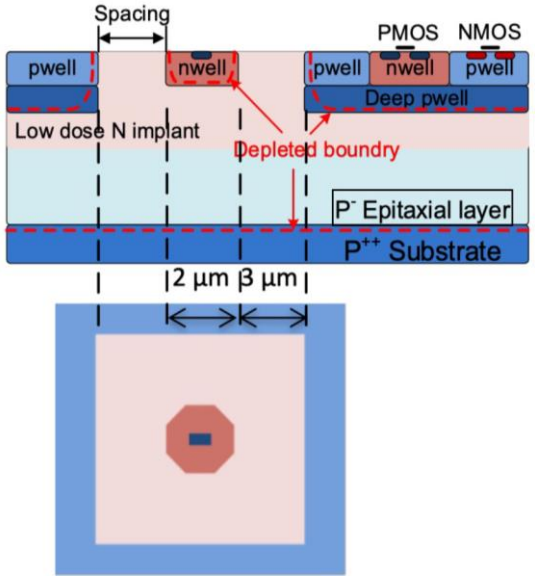
Existing CMOS MAPS options

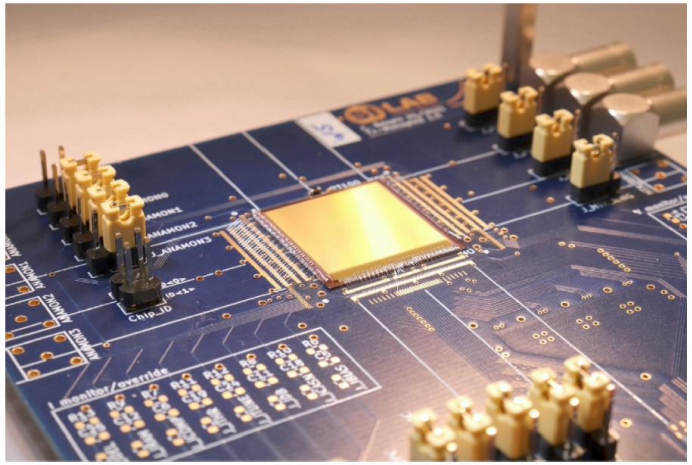
Non-exhaustive table built in late 2020

Starting point

Sensor available 2020	ALPIDE	MIMOSIS-1	TJMonopix-2	LFMonopix-2	ATLASPix-3	Belle II
Techno	TJ-180 nm	TJ-180 nm	TJ-180 nm	LF-150 nm	TSI 180 nm	
Pixel pitch [µm2]	29x27	30x27	33x33	150x50	150x50	**30 to 40**
#Columns x #Rows	1024x512	1024x504	512x512	56x340	132x372	
Sensitive area [cm^2]	27.5x15.0	31.0x13.6	16.9x16.9	8.4x17	19.8x18.6	**~30x20**
Time Stamp [ns]	5000	5000	25	25	25	**<100**
Readout scheme	Contin./Trig.	Continuous	Global shutter	Continuous	Trigger: 25 µs latency	**5 → 10**
Output charge (bits)	1	1	7	6	7	**1-7**
Bandwidth (Mbit/s)	1200	3200	320		1300	**O(320)**
Power (mW/cm^2)	18-35	~50	O(200)		~140	**~100**
Hit rate (MHz/cm^2)	<10	15-70	>100	>100	>100	**≤120**
TID kGy	27	100	1000		1000	**1000**
Fluence (x $10^{13} n_{eq}.cm^{-2}$)	1.7	7	100	100	100	**10**

TJ-Monopix2



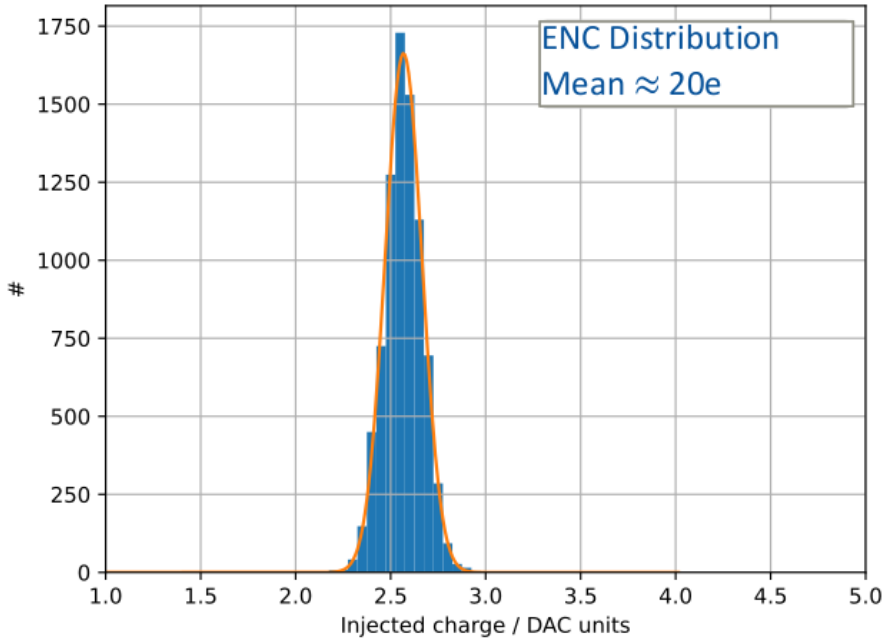


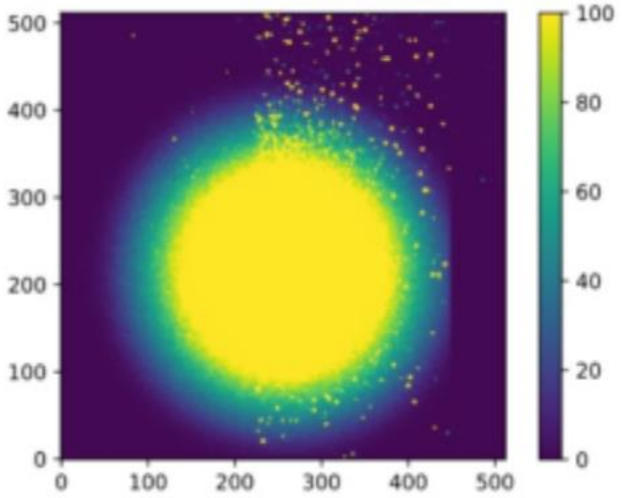
- TJ-Monopix2
  - Chosen as basis for Belle II VTX
  - DMAPS in TowerJazz (TJ) 180 nm process
  - Small collection electrode
    - small capacitance
    - low power and noise
  - High-resistivity epi layer: ~1-2 kΩ cm
  - Chip size: 2 × 2 cm^2
  - Pixel pitch: 33 × 33 μm^2
  - 512 × 512 pixels
  - Power: ~ 1 µW/pixel (100 to 200 mW/cm^2)
  - Column drain readout
  - Triggerless

First Results from TJ-Monopix2

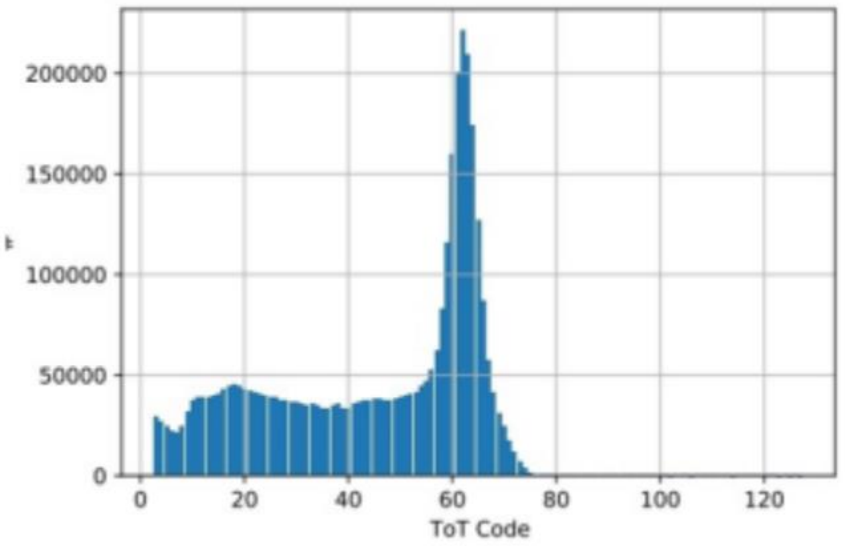
- First lab tests checking ENC and threshold (still room for tuning)
- Chip detects radiation
- Further tests necessary

➔ See previous talk by Lars Schall



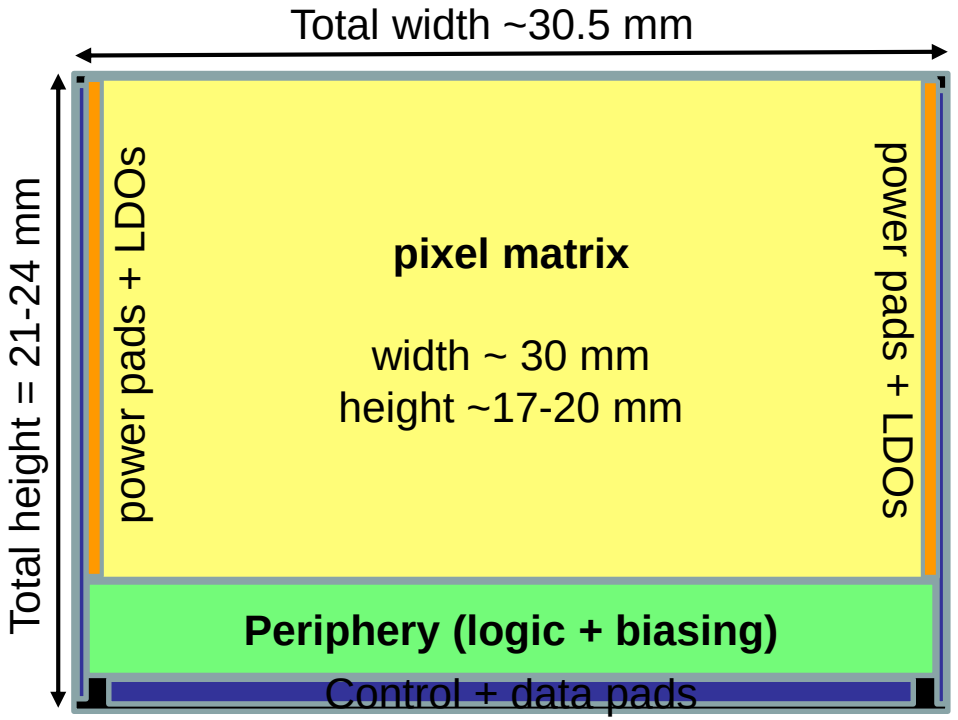


Fe^{55} Spectrum



OBELIX

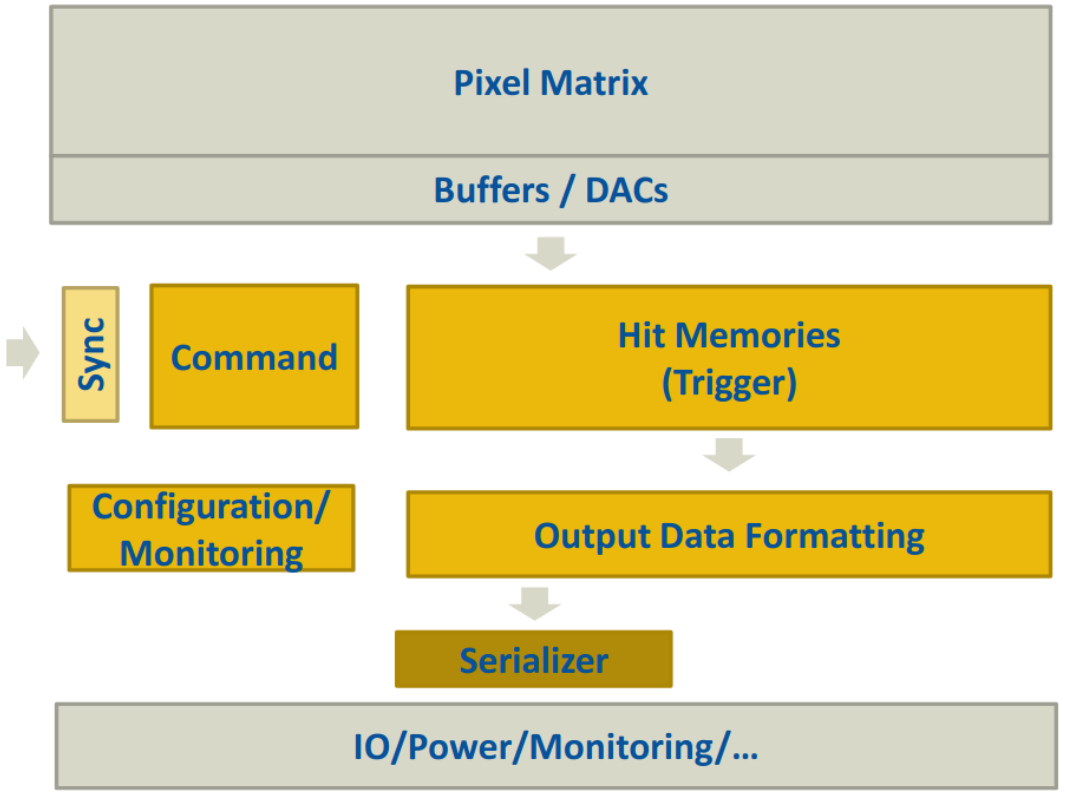
- OBELIX: **O**ptimized **BEL**le II p**IX**el sensor
  - Based on the TJ-Monopix2
  - Benefits from the whole Monopix1/2 family
  - Optional tuning of analog circuit when results are available
  - Inherits high radiation tolerance and small integration time
- Slowed down
  - TJ-Monopix2 clock: 40 MHz (LHC bunch-crossing)
  - OBELIX: ~ 20 MHz (derived from accelerator RF)
  - Reduced power consumption
- Relaxed pixel size: ~ 40 µm pitch
  - Sufficient for VTX
- Narrow LDOs on both sides of the chip
  - Newly developed for this chip
  - Analog power distribution from Monopix2



OBELIX

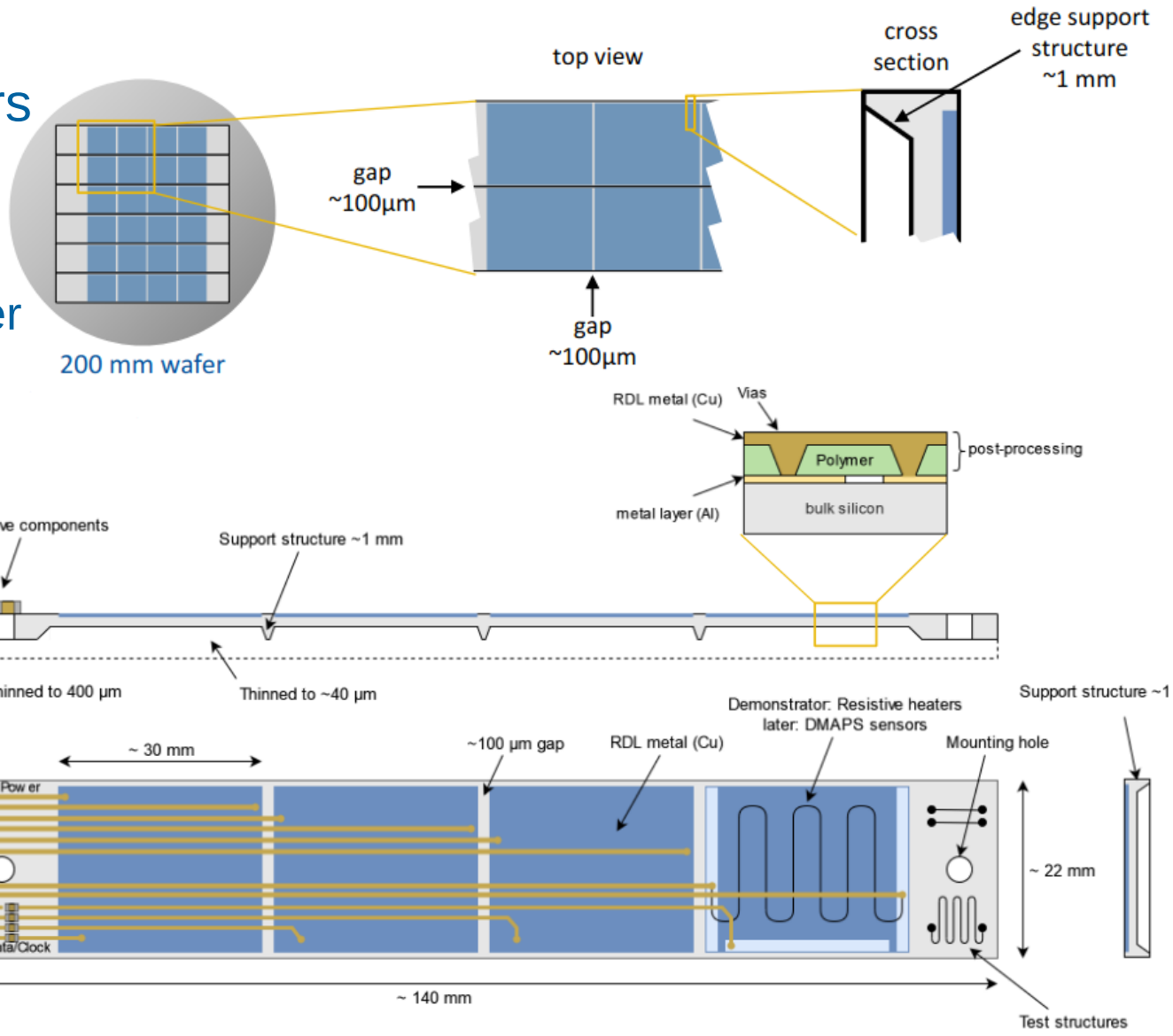
- OBELIX implements Belle II specific adaptions
  - Hit memory
  - Large trigger latency is required (>5 µs)
  - Trigger synchronisation
  - On-chip clustering (optional)

- Powerful digital processing required
- High granularity
  - Can operate at high hit-rates from high luminosity
- Expected trigger rate: 30 kHz (poisson)



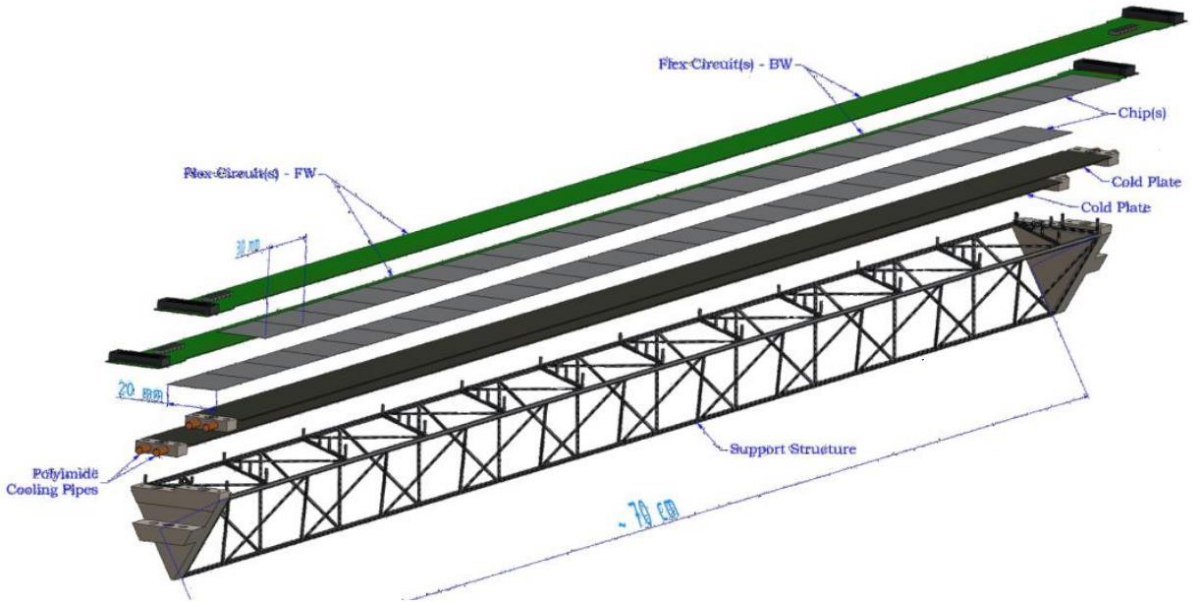
iVTX Design

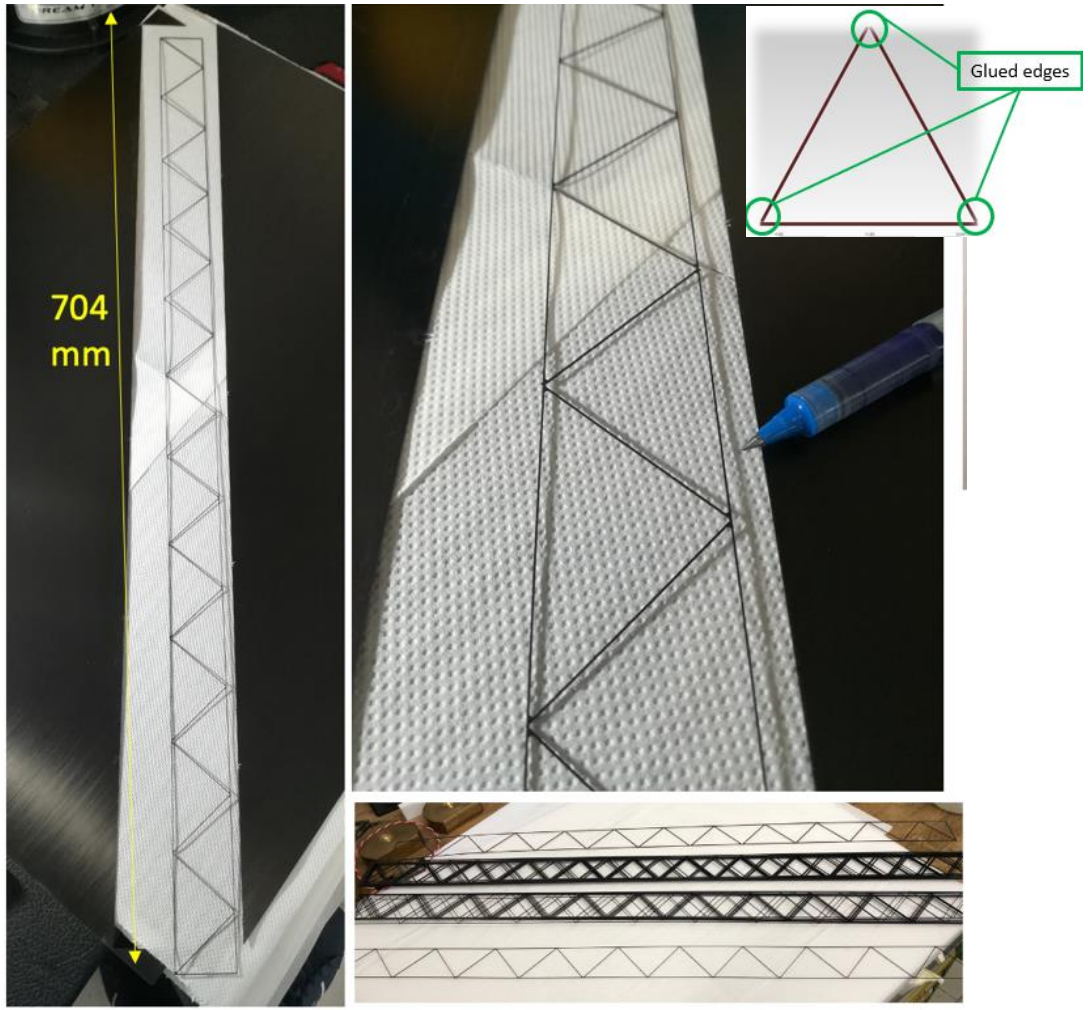
- L1+L2: full silicon design
- Single piece of silicon with multiple sensors per ladder
- Connected via redistribution layer (RDL)
  - All connections routed to one end of the ladder
  - Simpler cable routing
- Thicker frame for mechanical support with thinned sensing area
- Thinning-steps planned for evaluation:
  - 400 µm, 200 µm, 100 µm, 50 µm
- expected material budget: 0.1%X_0 per Layer



oVTX Design

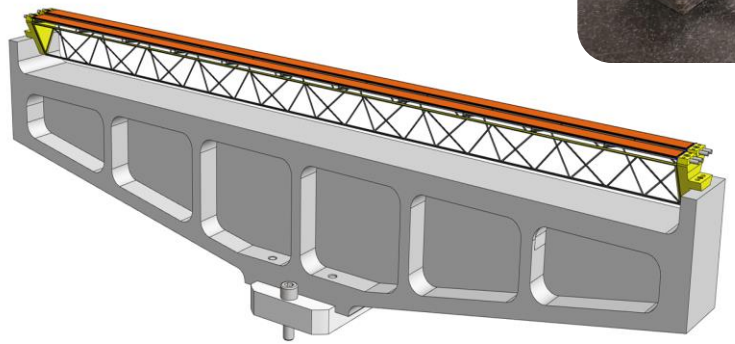
- Based on ALICE ITS2 space frame design
- Three flat carbon-fiber structures glued together
- Up to 704 mm long (L5) but only 5.8 g
- Up to 60 g payload: very stiff design needed
- expected material budget: (2*0.3% + 1*0.8%) X_0



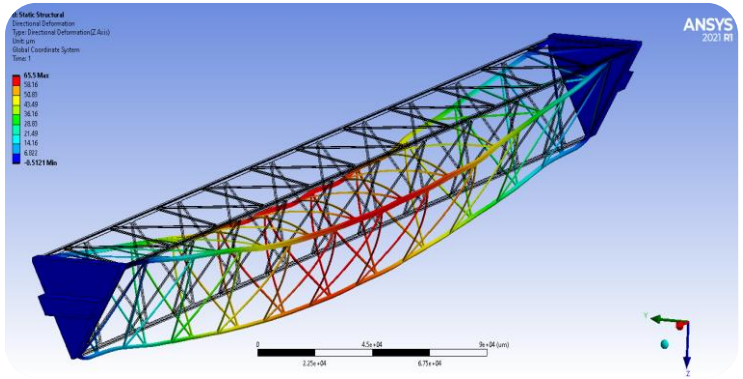


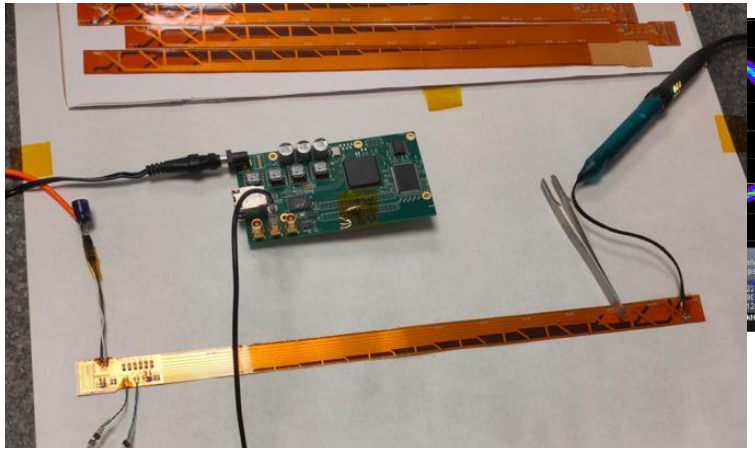
oVTX R&D and Tests

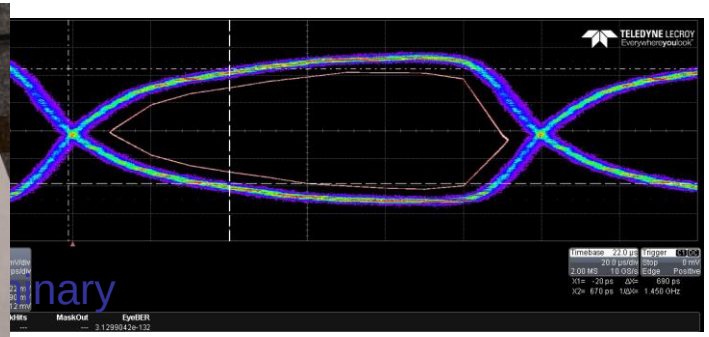
- Cu Flex: first prototype for power and data
  - Plans to switch to Al (material budget)
  - Tests of signal integrity and bit error rate
- Vibrational Tests: mandatory to stay above the typical earthquake frequencies (<20 Hz)
- Thermal characterization ongoing



Vibration Test Setup







eye diagram @250 MHz (500 Mbit/s)

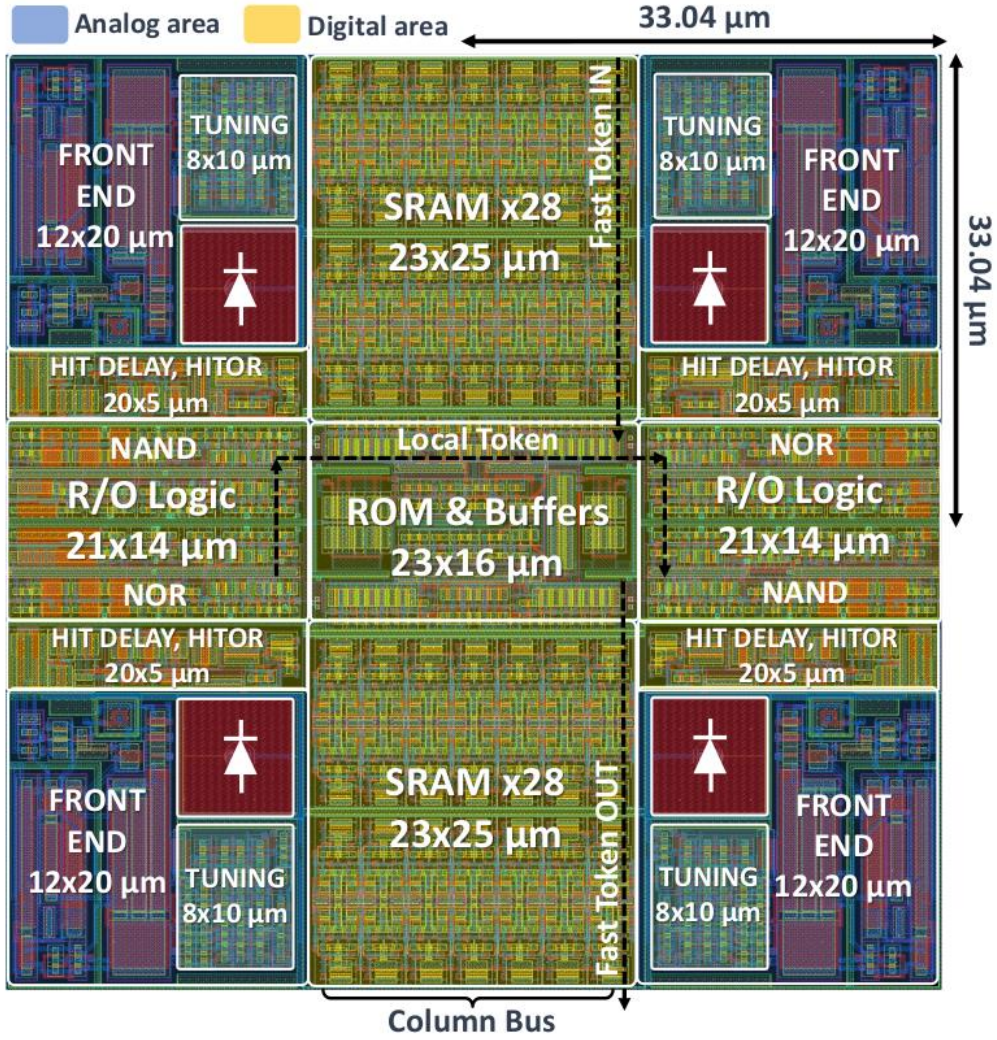
Summary and Outlook

- All pixel detector design improves tracking performance
- DMAPS promising technology for the Belle II upgrade at LS2
- Testing of **TJ-Monopix2** ongoing, first results available
- Deveopment of next version **OBELIX** started recently
  - Powerful one-chip solution
  - Dedicated for Belle II VTX
  - Additional digital processing for Trigger
  - Improvements of analog circuitry when tests are completed
- VTX design currently prototyped
  - low material budget can be achieved

Backup Slides

TJ-Monopix2

- 33 x 33 μm^2 per pixel
- 4 pixels form pixel-cores ➔ area saving
- Pixel cores form double-columns
- 7-bit Timestamp for LE/TE
- Per pixel threshold tuning
- Timestamp delay compensation



TJ-Monopix readout scheme