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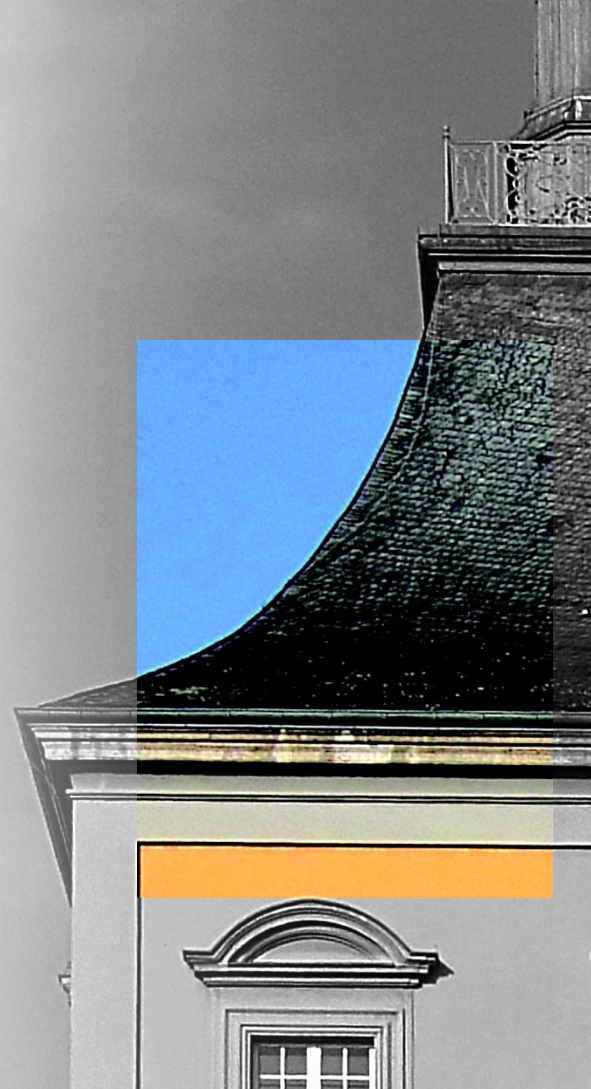
On behalf of the Belle II VTX collaboration

CMOS MAPS UPGRADE FOR THE BELLE II VERTEX DETECTOR

Pisa Meeting on Advanced Detectors

24.05.2022



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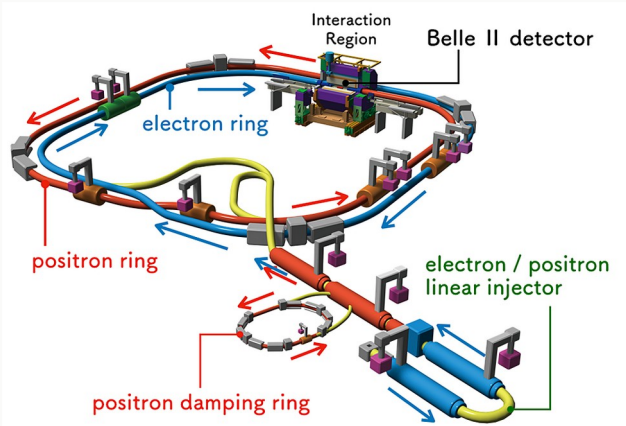
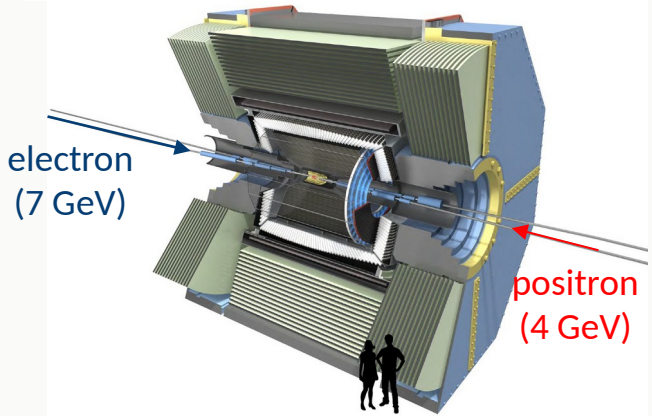
BELLE II

Belle II experiment at the SuperKEKB collider in Tsukuba, Japan

- Luminosity frontier experiment
- Asymmetric e^+e^- collider at 4 / 7 GeV and $\sqrt{s}$ = 10.58 GeV
- Target integrated luminosity of 50 ab^{-1}
- Target instantaneous luminosity of $6x10^{35}$ cm^{-2} s^{-1}
- Nano beam scheme:
  - Small beam spot size
  - High collision rates
  - Occupancy due to beam background dominates on innermost layers





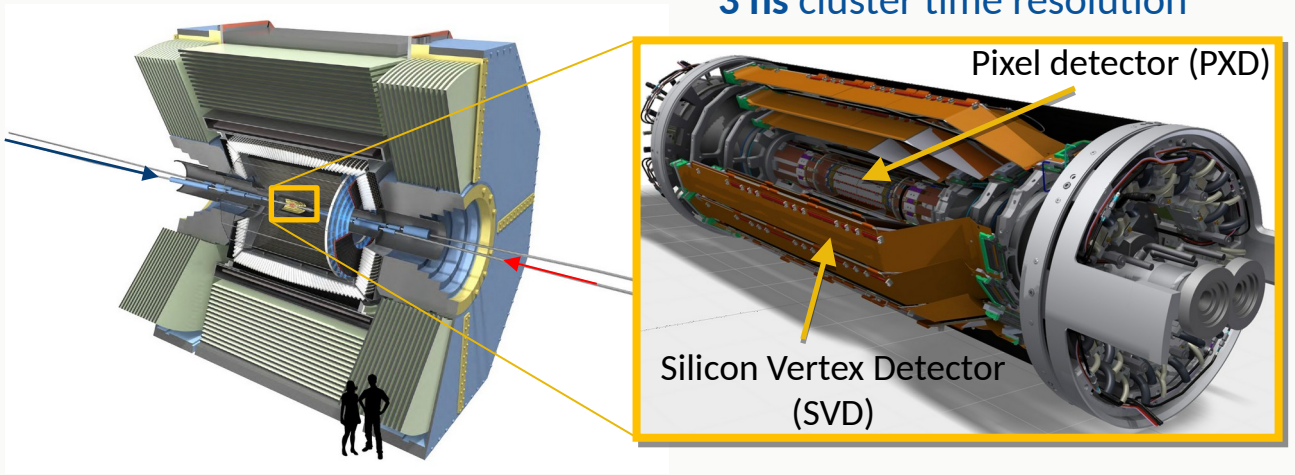
BELLE II VERTEX DETECTOR (VXD)

2 layers of PiXel Detector (**PXD**)

- **DEPFET** sensor @ 14 and 22 mm
- 50 x 55-85 µm² pixel size
- **20 µs** integration time,
  10 µm impact parameter resolution

4 layers of Silicon Vertex Detector (**SVD**)

- Double-sided silicon strip detector (**DSSD**)
- Radii of 39, 80, 104, 135 mm
- Strip pitch of 50/75 µm (r-φ) and 160/240 µm (z)
- **8 µm** spatial resolution on innermost layer,
  3 ns cluster time resolution

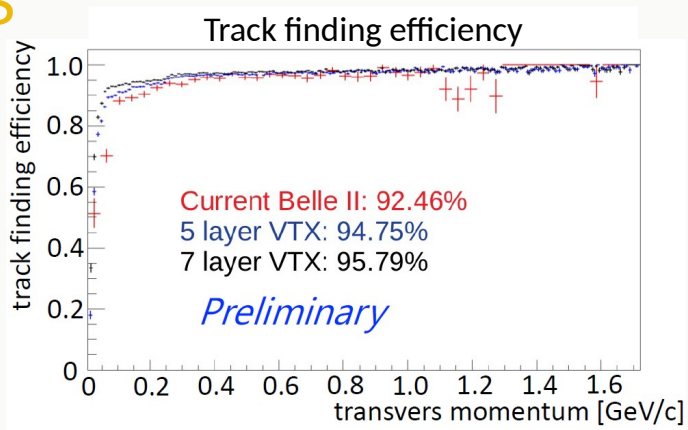


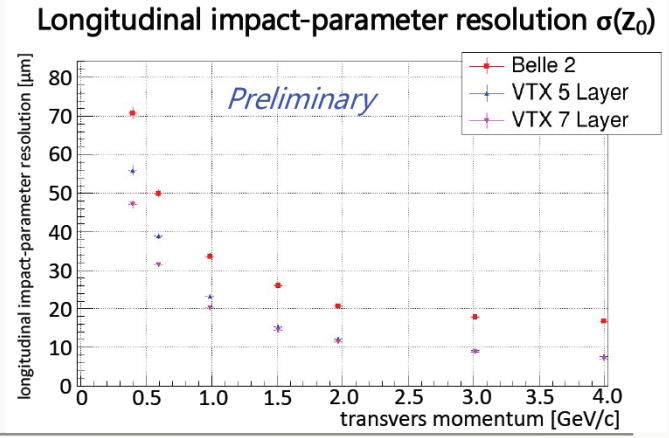
Poster on SVD by C. Irmler

BELLE II UPGRADE PLANS

SuperKEKB upgrade during **LS2 in 2026/2027**
- Redesign of interaction region
- Opportunity to install new vertex detector
- Belle II Upgrade Program presented by J. Baudot on Monday

Motivation for a new vertex detector
- **Occupancy** of up to 3% due to high backgrounds
- **PXD is not included in track finding**
  → potentially missing very low p_T tracks
- Smaller pixel pitch + faster integration time
  → **reduction in occupancy**
- Fully pixelated tracking detector enables pattern recognition



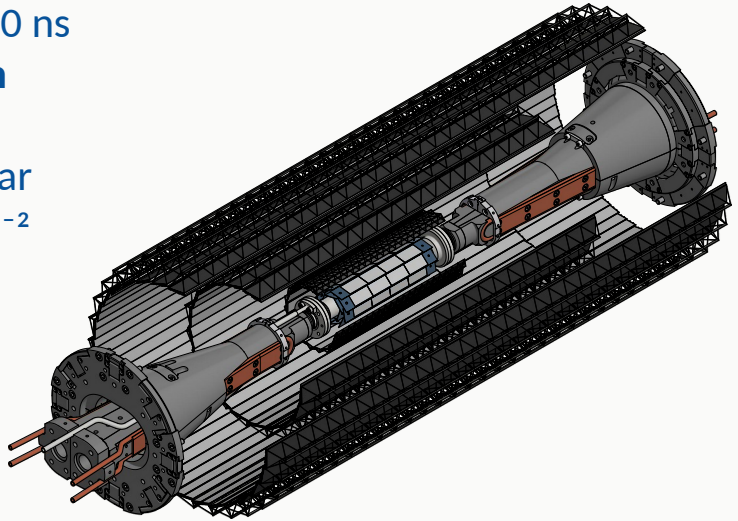


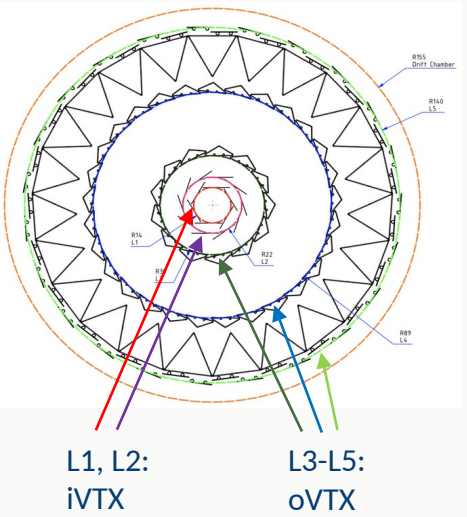
VTX CONCEPT

VTX: successor to VXD

- Low material budget:
  0.1% X_0 (L1+L2), 0.5% X_0 (L3), 1% X_0 (L4+L5)
- **Depleted Monolithic Active CMOS** pixel sensors
  - 2 x 3 cm^2, pixel pitch of 30-40 μm^2
  - Fast integration time of 25-100 ns
- **Radiation levels for L1 at 14 mm**
  - TID: about 10 Mrad / year
  - NIEL: about $5x10^{13}$ n_{eq}/cm^2/year
  - Hit rate of about 120 MHz cm^{-2}

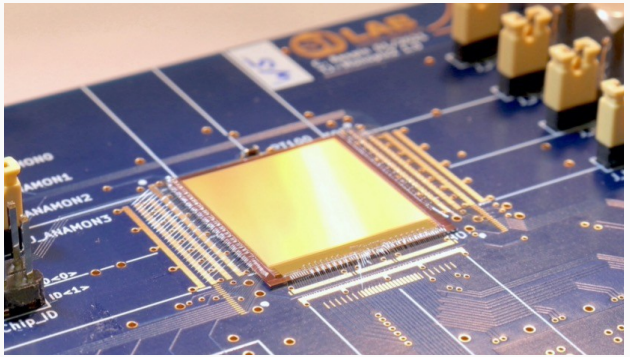
- 5 straight **fully pixelated** barrel layers
- **Same sensor type** for all layers
- **iVTX**: innermost 2 layers, self-supported, air cooled
- **oVTX**: 3 outer layers, CF structure, water cooled
- **Power dissipation** of about 200 mW / cm^2



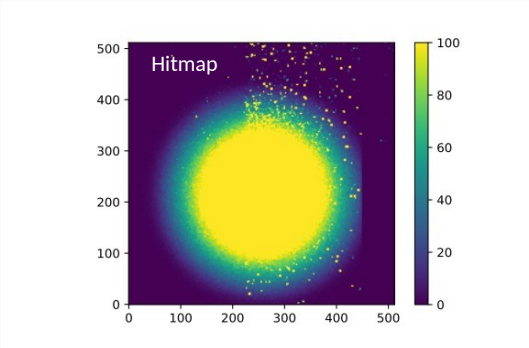


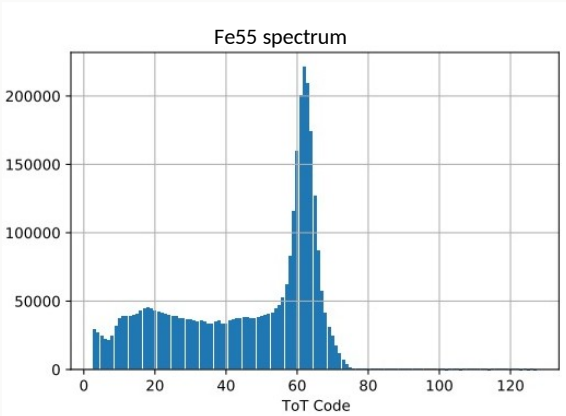
TJ-MONOPIX2 FEATURES

- TJ-Monopix developed for ATLAS, meets Belle II requirements
  - Small fill factor, fast integration time of 25 ns
- TJ-Monopix2 is next iteration
- 2x2 cm² chip with 33 x 33 µm² pixels
- Large matrix of 512 x 512 pixels
- Testing in Bonn: Chip is alive and working
- Testbeam at DESY in June 2022



TJ-Monopix2: Proof-of-principle prototype of Belle II VTX





TJ-Monopix2	
Chip size	$2x2\ cm^2$(512x512 px)
Pixel size	$33.04\ x\ 33.04\ \mu m^2$
Total matrix power	$170\ mW/cm^2$
Noise	$< 8\ e^-$ (improved FE)
LE/TE time stamp	7-bit
Threshold dispersion	$< 10\ e^-$ rms (improved FE + tuning)
Minimum dispersion	$< 200\ e^-$
In-time threshold	$< 250 - 300\ e^-$
Efficiency at $10^{15} n_{eq}/cm^2$, 30 µm epi	> 97 %
Efficiency at $10^{15} n_{eq}/cm^2$, Cz	> 99 %

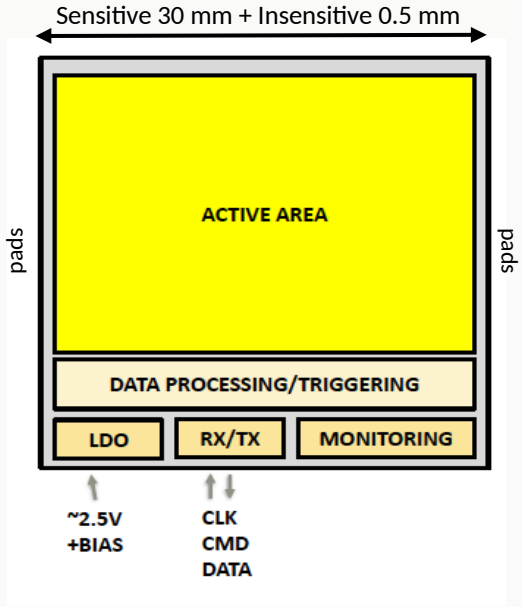
Expectations

TOWARDS BELLE II: OBELIX

Target: first complete prototype **OBELIX-1 fabricated in 2022**
- Digital design starting
- Analog design still under organisation

Reminder of guidelines:
- Keep pixel matrix core from TJ-Monopix2 but
  - Enlarged for **sensitive width of ~3 cm along z**
  - Possible pitch **increase to 40 µm** if beneficial for robustness against electrical noise
  - Adapt digital logic to Belle II triggering
  - **Short integration time < 100 ns** and trigger rate of 30 kHz
    → limit the data throughput to ~ 320 Mbps

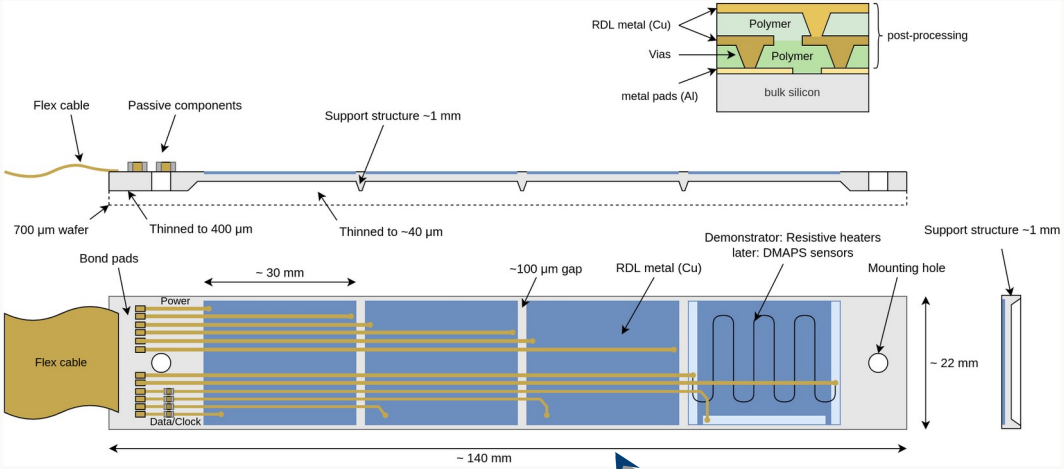
Sensor layout and powering
- Baseline matrix powering sticks to TJ-Monopix2 with **additional on-sensor regulators**
  → ~ 500 µm insensitive gaps on the side



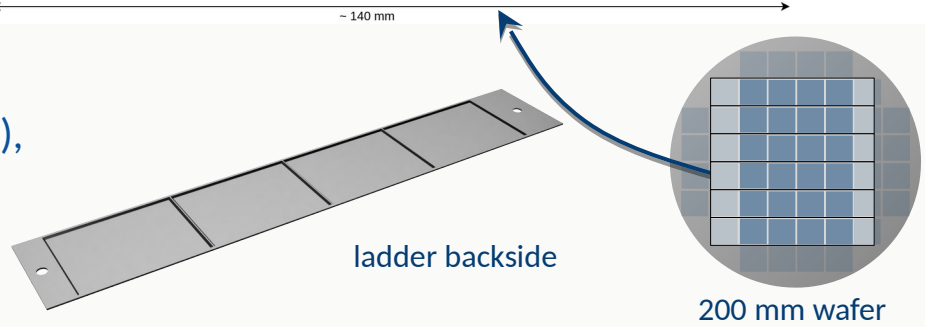
Power dissipation
- Decreasing timing resolution from 25 ns to 100 ns to mitigate power dissipation from clock propagation within matrix
  → Dissipation closer to ~ **200 mW/cm²** expected

IVTX DEMONSTRATOR

All-silicon ladder
- Single piece of silicon
- 4 sensors per ladder
- RDL for data and power
- Selective thinning of active areas to ~40 µm

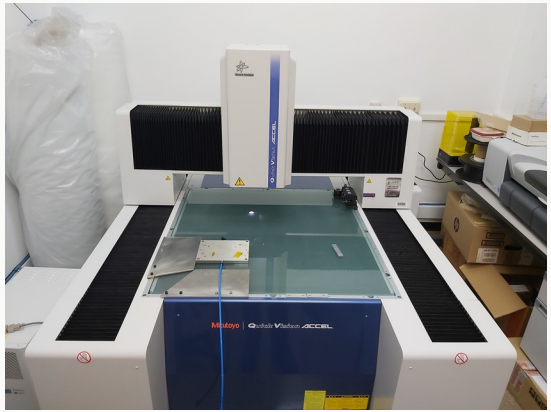


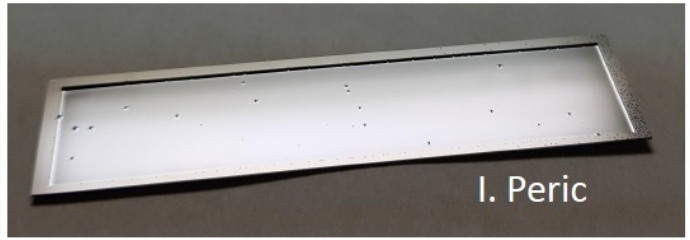
Goals for the demonstrator:
- Process evaluation (RDL and thinning)
- Thermal studies (resistive heaters instead of sensors), mechanical stability
- Signal quality, power delivery, component assembly



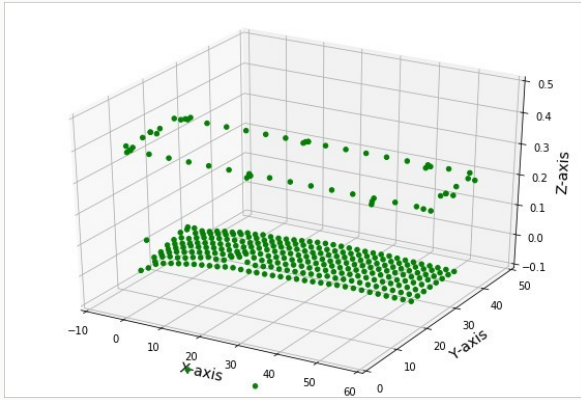
IVTX THERMOMECHANICS

- Multichip CMOS thinned ladders produced with different thickness and geometries
- First ladders characterised: homogeneous thickness over 10 cm² area (with some outliers)





Thinned Ladder (units in mm)		
Frame	Nominal thickness	0.428 ± 0.008
	Planarity	0.01647
Center	Nominal thickness	0.09 ± 0.04
	Planarity	0.0176
	Length/Width	71.0638 ± 0.0009 15.9730 ± 0.0016

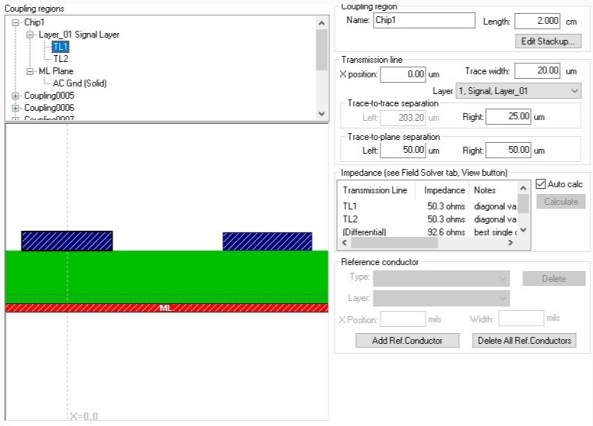


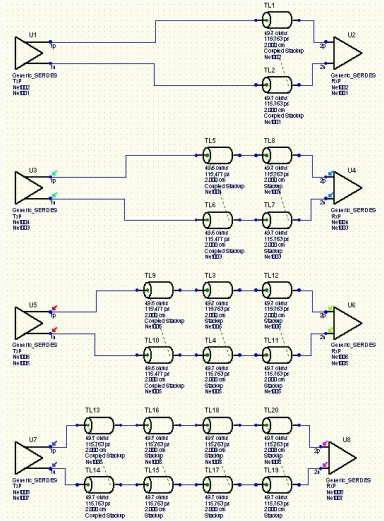
IVTX TRANSMISSION LINES

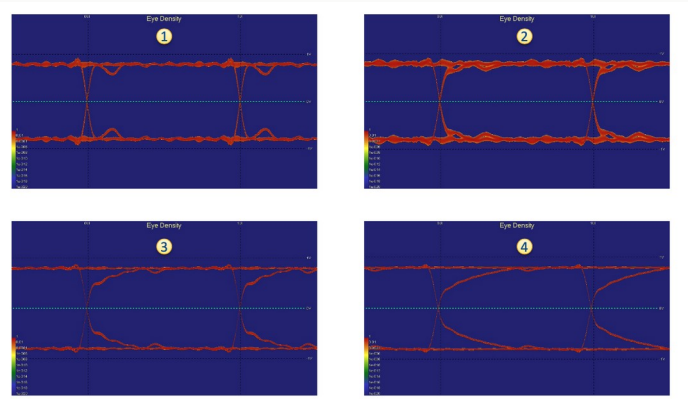
First studies based on IZM post-processing options
Simple models of the geometry:

- Layer stack, transmission lines, schematic
- Atennuation, eye opening

→ Output driver model of OBELIX







Eye diagrams for 1...4*3 cm trace length. PRBS-15 @640 Mbps

OVTX THERMOMECHANICS

oVTX concept: sensors glued to a support structure ("truss“)

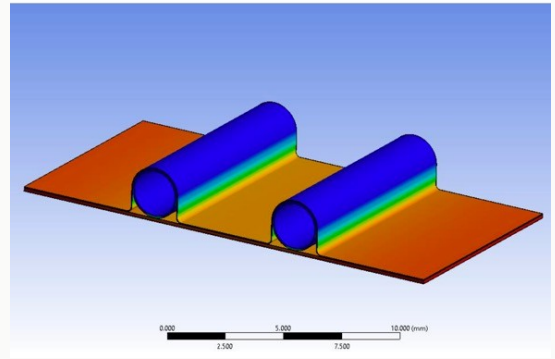
Cold place concept for L3-L5, evolving from **ALICE frame**, in production

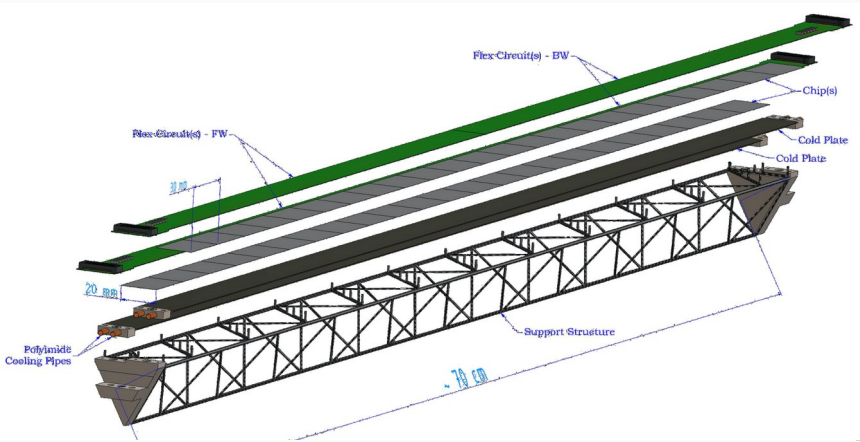
Material budget for L3-L5: 0.5 – 1.0 % X_0 (preliminary)

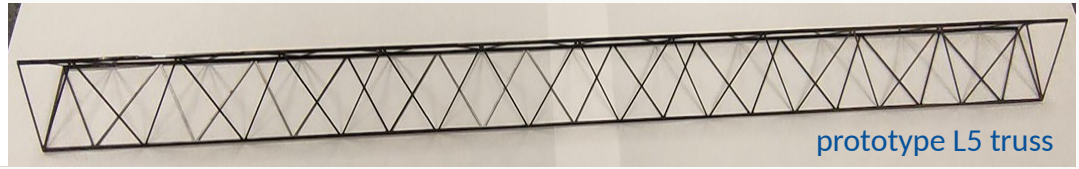
First **prototype L5 truss** assembled (70 cm long, 5.8 g)

→Thermomechanical characterisation about to start

Modified Cold Plate – M55J+Carbon Paper





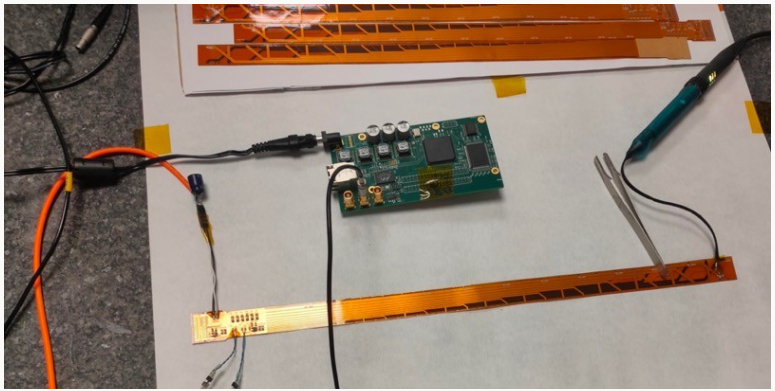


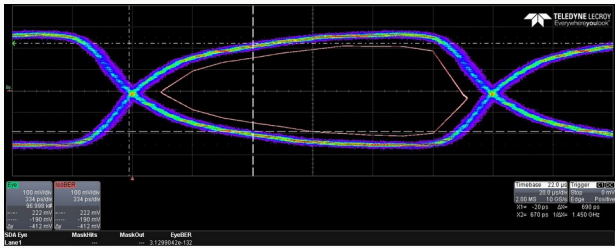
OVTX TRANSMISSION LINES

First prototype of the low power and signal bus available

Testing ongoing:

- Verification of signal integrity at the far end
- Estimation of BER at 160 Mhz





eye diagram @250 MHz (500 Mbit/s)

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SUMMARY

- Belle II experiment considers a **vertex detector upgrade in 2026/2027**
- **All-layer monolithic** vertex detector upgrade (**VTX**): more performant and resilient against higher machine backgrounds
- Target specs in terms of material budget, spatial resolution, and integration time window seem reachable
- Baseline technology: **small collection node monolithic sensor**, evolving from TJ-Monopix2
  - Chip alive and looks healthy
- **OBELIX**: first steps towards a Belle II CMOS sensor **submission in 2022**
- Thermomechanical and electrical mockups of inner and outer layers in the making
- Preparing for **CDR submission end of 2022**
- Also check the poster on simulation results using the VTX by L. Massacesi

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Belle II

SI LAB
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THANK YOU FOR YOUR ATTENTION!